SWEJAL LANJEWAR

SOFTWARE ENGINEER

Passionate & Self-Motivated Engineer. Eager to contribute technical skills effectively & implement innovative ideas for the development of the organization & society, while keeping honesty & punctuality at the highest priority.

CONTACT

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Nagpur, Maharashtra

SOFT SKILLS

- Good Communication
- Teamwork
- Adaptability
- Problem Solving
- Creativity

LANGUAGES

- English
- Hindi
- Marathi

INTERESTS

- Photography
- Travelling

PROFESSIONAL EXPERIENCE

AVANCED VLSI DESIGN AND VERIFICATION
Maven Silicon VLSI Training Institute, Banglore
Jan 2023 - Nov 2023

C, C++ PROGRAMMING LANGUAGE
Great Learning approved Certificate

SOFTWARE ANALYSIS & TESTING
Udacity approved Certificate

JAVA PROGRAMMING
Udemy approved Certificate

EDUCATION

Priyadarshini College of Engineering, Nagpur | 2022
RASHTRASANT TUKDOJI MAHARAJ NAGPUR UNIVERSITY
Electronics and Communication - 8.91 CGPA

Lokmanya Tilak Rashtriya Vidyalaya, Tumsar | 2016
MAHARASHTRA STATE BOARD
Science - 6.7 CGPA

Maharishi Vidya Mandir,Tumsar | 2014
CBSE BOARD - 7.0 CGPA

FOUNDATION SKILLS

- Programming Language
  - C [Datatype | Array | Pointers | Functions|Memory Allocation | List | Queues & stacks | Data structure]
  - C++(OOPs concept, Class, Inheritance, Polymorphism)
  - Java
- HDL - Verilog
- HVL - System Verilog
- TB Methodology - UVM
- EDA Tool - ModelSim, Synopsys Design Compiler, Mentor Graphics - Questasim
- Operating System - Linux

DESIGN SKILLS

Digital Electronics, Verilog Programming, Code Coverage

VERIFICATION SKILLS

System Verilog , Basic object-oriented programming, Functional coverage, Basic System Verilog Assertions, Universal Verification Methodology

PROJECTS

1] SPI Controller Core – Verification

The SPI IP core provides serial communication capabilities with external device of variable length of transfer word. This core can be configured to connect with 32 slaves.

- ➢ Architected the class-based verification environment in UVM.
- ➢ Defined Verification Plan.
- ➢ Verified the RTL module using System Verilog.

2] Router 1x3 - RTL Design and Verification

HDL : Verilog
HVL : System Verilog
TB Methodology : UVM
EDA Tools : Questasim and ISE

A router accepts data packets on a single 8-bit port and route them to one of the three output channel, channel0, channel1, channel2.

- ➢ Architected the block level structure for the bridge.
- ➢ Developed Verilog RTL for each block.
- ➢ Verified each block with different transfers like single READ, WRITE & Burst READ,WRITE
- ➢ Synthesized the design and generated code coverage report for RTL Design signoff

3] Smart Health Care kit for patient monitoring based on Arduino & Android platform (Final year project)

I have worked in this project as a group leader in a team of 4 members. This project is an IOT based patient health tracking system effectively uses internet to monitor patients health.

- ➢ **Journal Publication** - IJARCCE published a paper entitled Smart health care kit for patient monitoring based on arduino and android platform. Thomson Reuters ID I-8645-2017 DOI: 10.17148/IJARCCE.2022.11320

ACHIEVEMENTS

- ➢ Ministry of Electronics & Information Technology Certificate in UX Design by Adobe
- ➢ Elearnmarket's Certificate in Advanced Excel
- ➢ AICTE approved Certificate in Robotics & Automation Certificate of Graphic Design