CS-232: Digital Logic Design and Computer Architecture Lab.

Assignment 1

Design the following complex gates (operators) using the basic gates. It must be described in structural description in VHDL

(a) 2 – input NOR
(b) 2 – input NAND
(c) 2 – input XOR
(d) 2 – input XNOR
(e) 2 – input Implication operator

Submission Document: VHDL file(s) of the description which can be simulated.

Submission Deadline: 20 Jan 2022 (Thursday) 23:59 pm.