

Sequential Circuits

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CS-230: Digital Logic Design & Computer Architecture



Lecture 14 (07 February 2022)

CADSL

Arithmetic

C_1 ✓
 C_2
 $C_3 = g_3 + p_1 \cdot C_2$
 C_4

~~Multiplexers~~

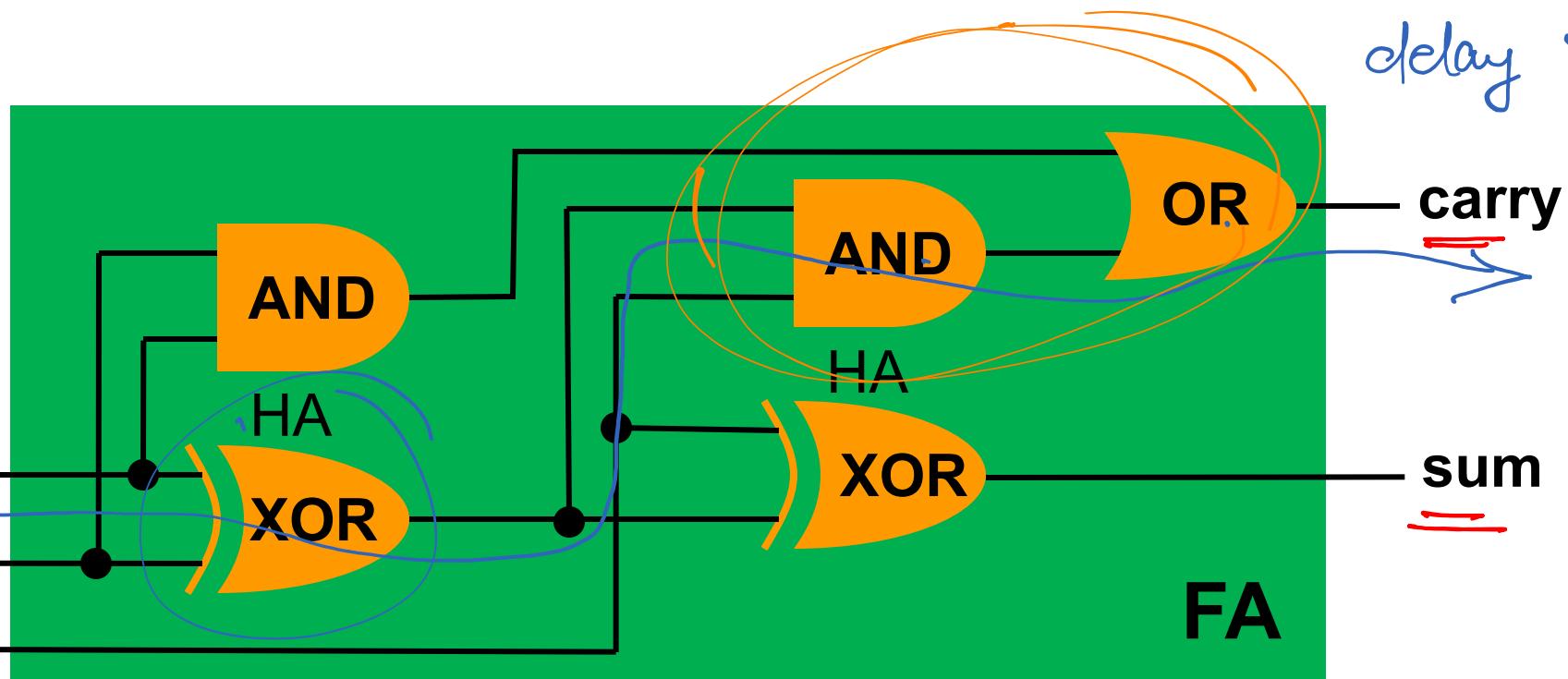
Circuits:

Adders

Adders
✓ Area / Power
RCA
Performance
CLA → αn
CSA - carry select
 $\alpha k \log n$ ← Prefix - Adder



Full-Adder Adds Three Bits



$$\begin{array}{c} 2 \times \text{XOR} + 2 \times \text{AND} + 1 \times \text{OR} \\ \hline \text{PA} - \oplus \quad \text{A} \quad \text{= } \end{array}$$

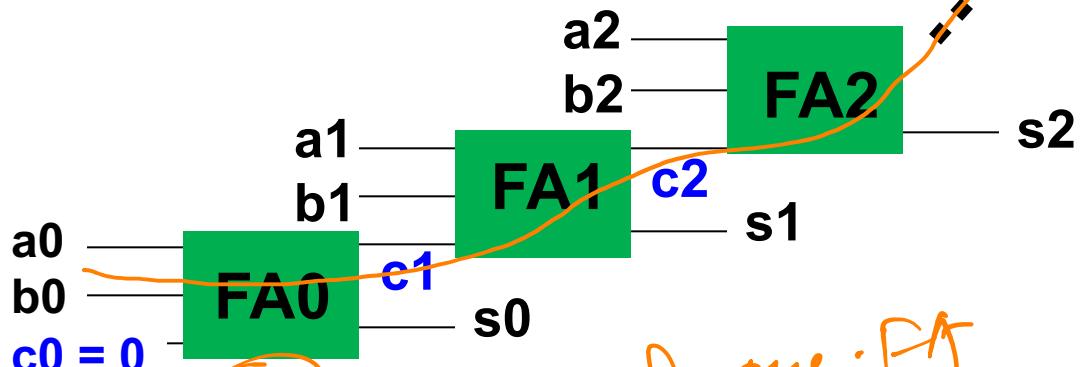


32-bit Ripple-Carry Adder

c₃₂ cell

s₃₂

$$\begin{array}{r}
 c_{32} \ c_{31} \dots \ c_2 \ c_1 \ 0 \\
 a_{31} \dots \ a_2 \ a_1 \ a_0 \\
 + b_{31} \dots \ b_2 \ b_1 \ b_0 \\
 \hline
 s_{31} \dots \ s_2 \ s_1 \ s_0
 \end{array}$$



① \leftarrow delay \Rightarrow one FA

$$\textcircled{2} = 10 \text{ ps}$$

$$42 = 40 \text{ ps}$$

$$32 \times 40 = 1280 \text{ ps}$$

CADSL

$$\begin{aligned}
 & 42 + 42 + 42(n-1) \\
 & = 82 + 42 + 42n2 \\
 & = 62 + 42n2
 \end{aligned}$$

$$\begin{aligned}
 & \frac{62 + 42n2}{n} \\
 & = 1.25
 \end{aligned}$$

$$42 + 42 + 42(n-1)$$

$$= 82 + 42 + 42n2$$

$$= 62 + 42n2$$

$$\begin{aligned}
 & \frac{62 + 42n2}{n} \\
 & = 1.25
 \end{aligned}$$

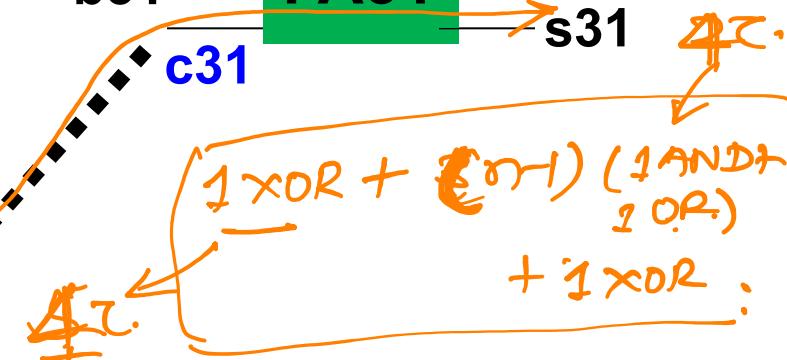
$$\frac{62 + 42n2}{n} = .$$

$$42 + 42 + 42(n-1)$$

$$= 82 + 42 + 42n2$$

$$= 62 + 42n2$$

$$\begin{aligned}
 & \frac{62 + 42n2}{n} \\
 & = 1.25
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$$42 + 42 + 42(n-1)$$

$$= 82 + 42 + 42n2$$

$$= 62 + 42n2$$

$$\begin{aligned}
 & \frac{62 + 42n2}{n} \\
 & = 1.25
 \end{aligned}$$

$$42 = 40 \text{ ps}$$

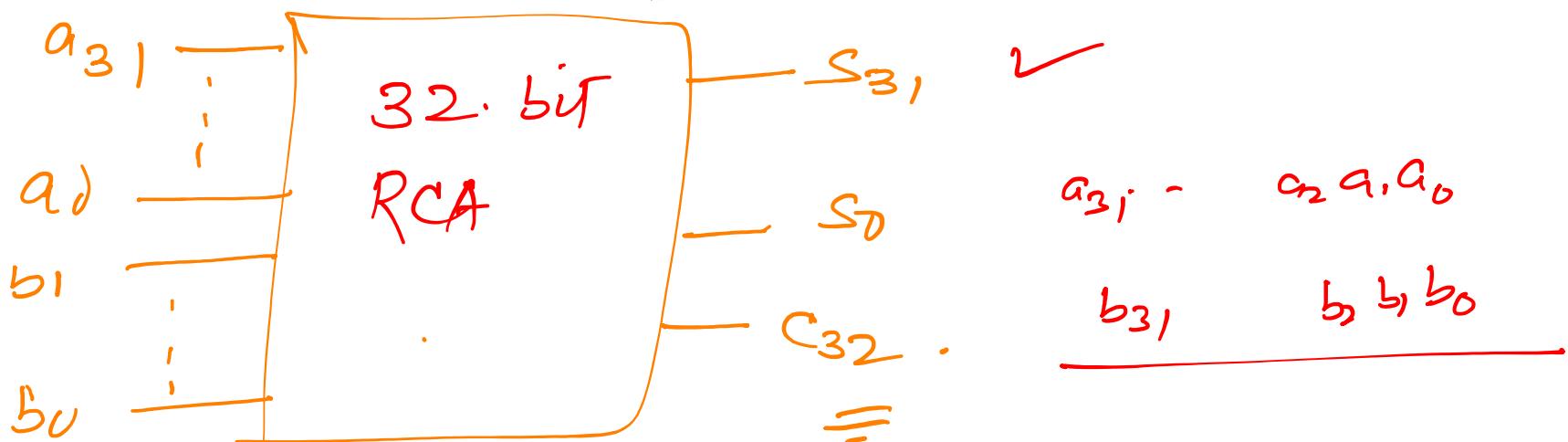
$$32 \times 40 = 1280 \text{ ps}$$



needs $32 \cdot FA$
 delay $\underline{32} \times \underline{\text{delay of one } FA}$
 \uparrow $\uparrow 1 \text{ ns}$

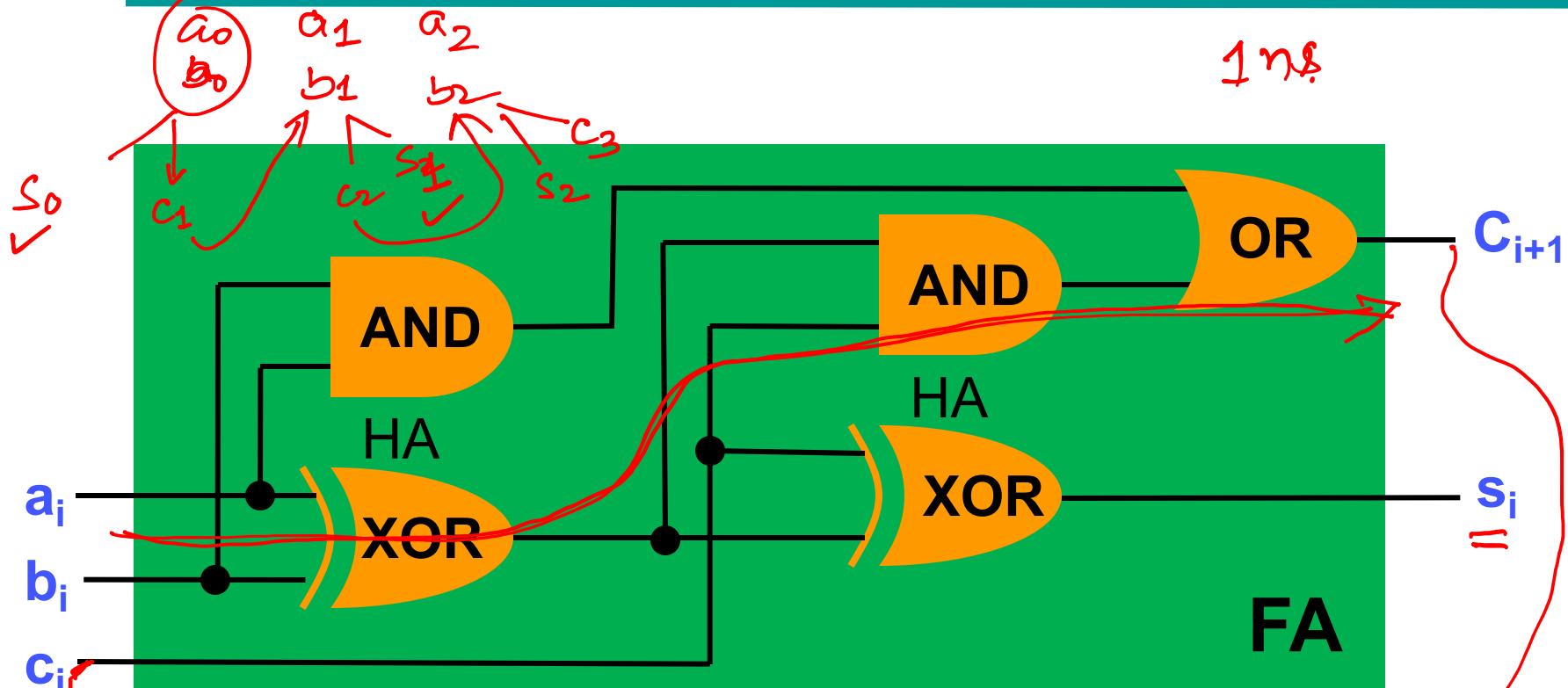
$32A =$

$\checkmark \underline{32 \text{ } \overset{\circ}{\text{ns}}}$ result



Full-Adder Circuit

Serial addition



feed. exactly after 1 ns

1 ns.

1 ns 2 ns 3 ns ... 32 ns

s_0

s_1

s_2

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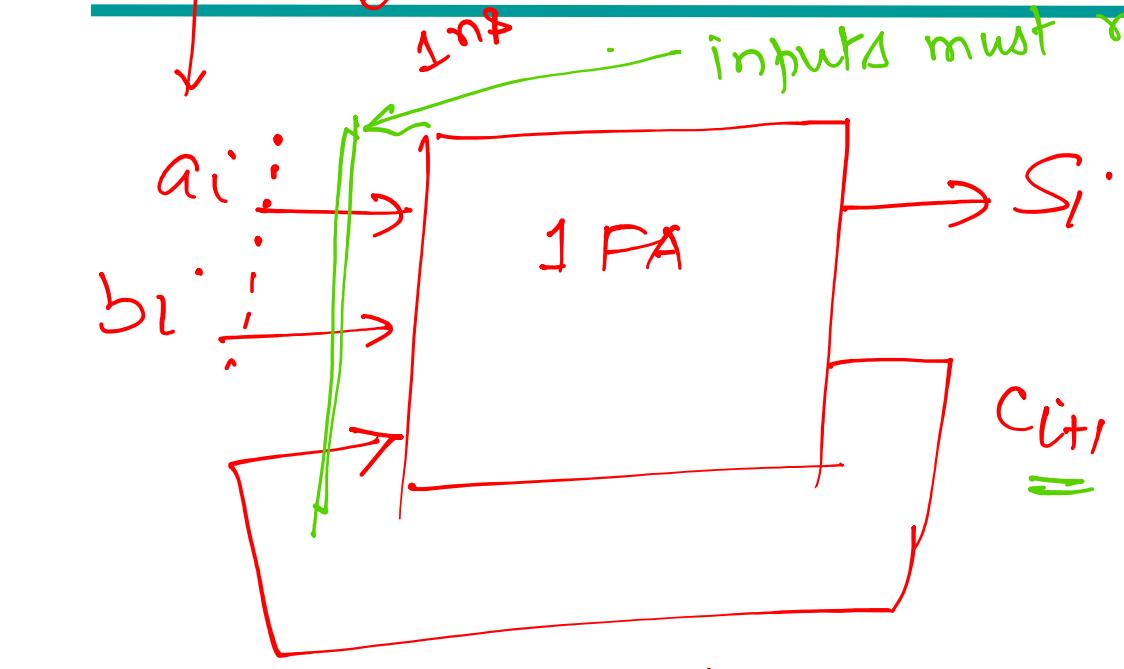
$\underline{s_{31}}$

CADSL



Serial Adder

inputs must be supplied every 1 ns

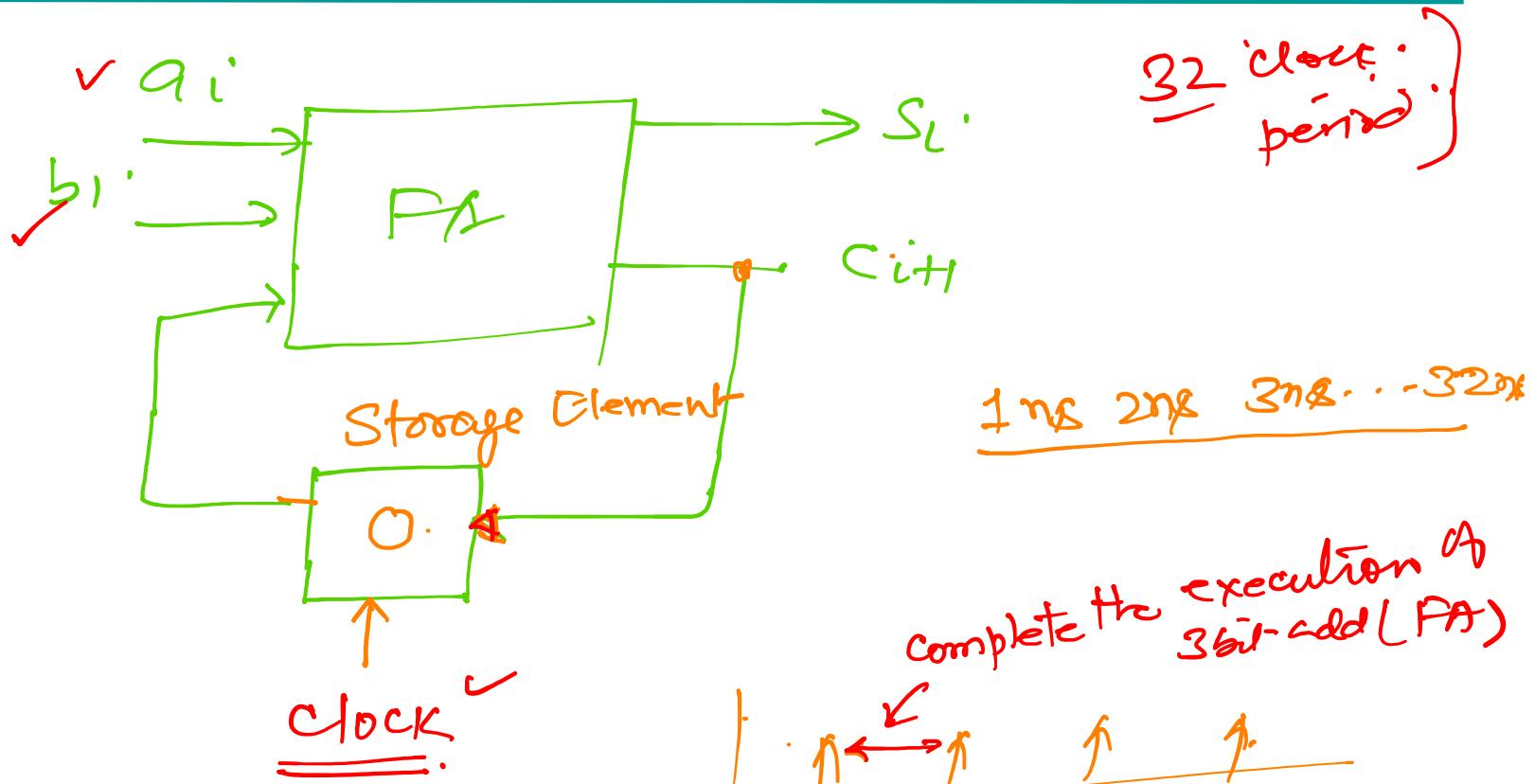


delay. ✓

32 ns.

Cost
1 FA
Very cheap.

Serial Adder

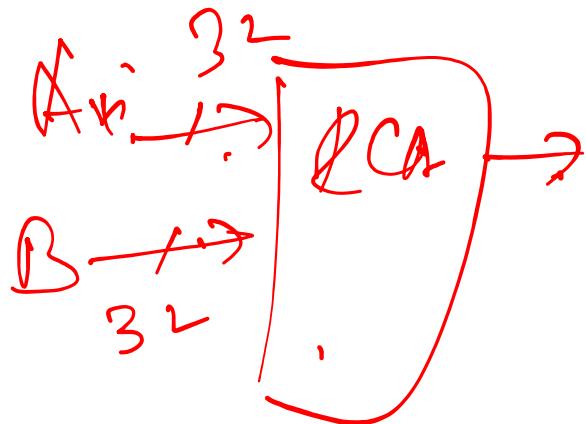


$$\text{freq} = \frac{1}{1 \times 11} \text{ ns} = \frac{10^9}{11} \text{ Hz} = 1 \text{ GHz}$$

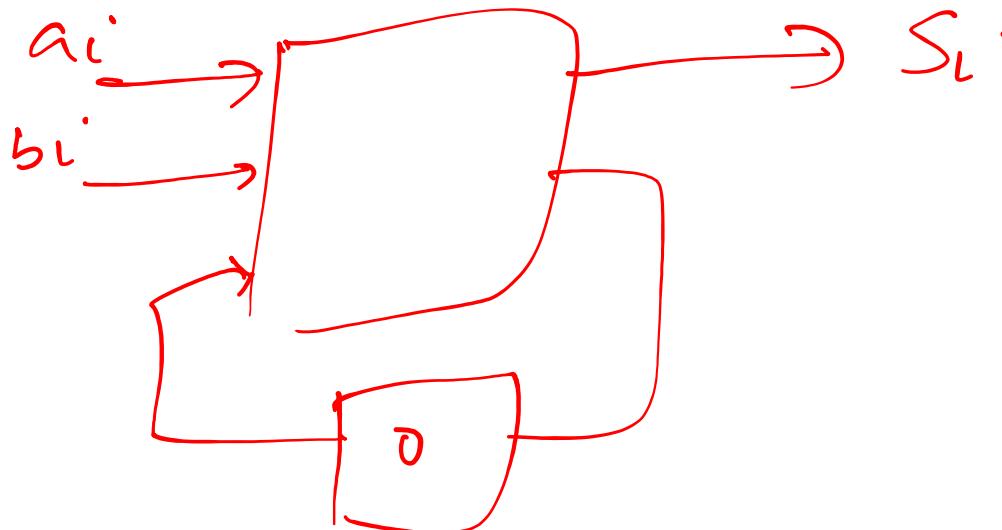


Serial Adder

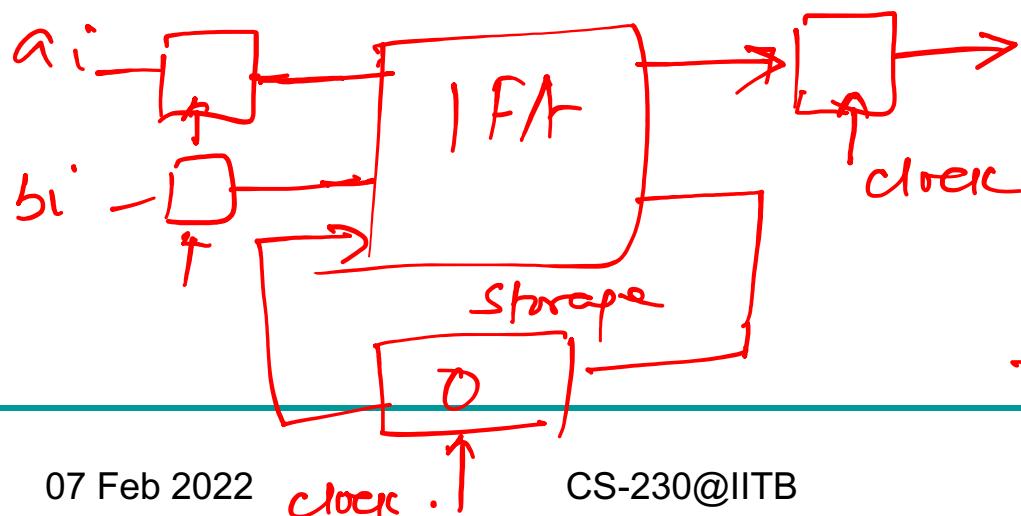
32 bit no → 32 ns)
16 bit → 16 ns
8 bit → 8 ns



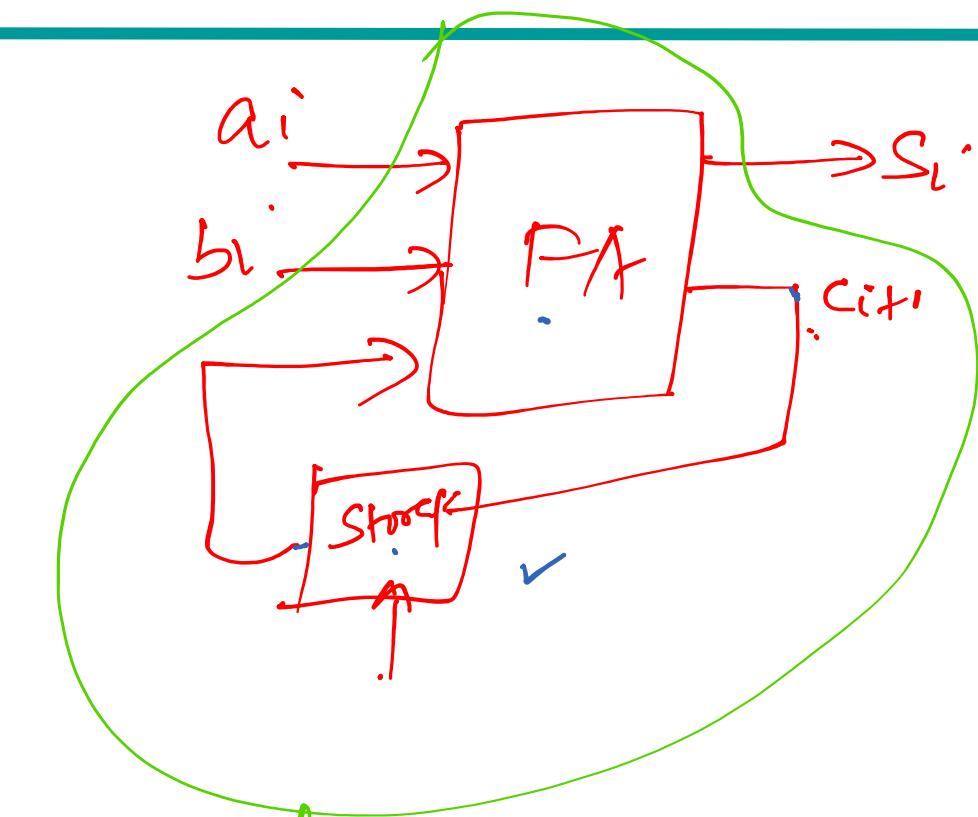
Serial Adder



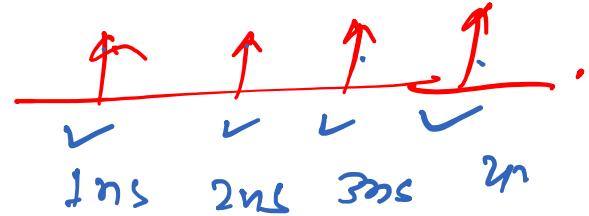
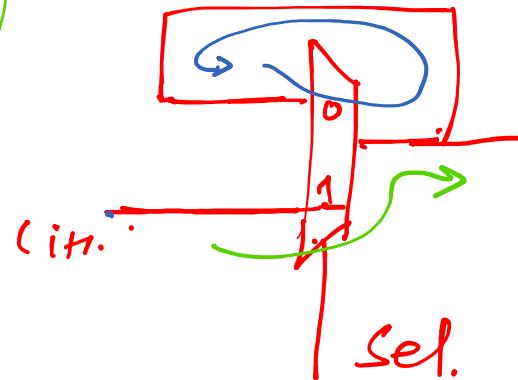
$\underbrace{1 \text{ FA}}_{\begin{array}{l} 1. \text{ Storage} \\ \text{element} \end{array}} = \checkmark$



Serial Adder



external
interface.



Serial Adder

<i>Input</i> $a_i \ b_i$	c_i	S_i - Output
0 0	0	0
0 1	0	1
0 1	1	0
1 0	0	1
1 0	1	0
1 1	0	0
1 1	1	1

Output is not only dependent on the current inputs but also dependent on previous inputs
=

Sequential behaviour

Synchronous Sequential Circuits



Serial Adder

Temporal Behaviour \rightarrow sequential logic

(MEMORY)

STATE OF THE SYSTEM

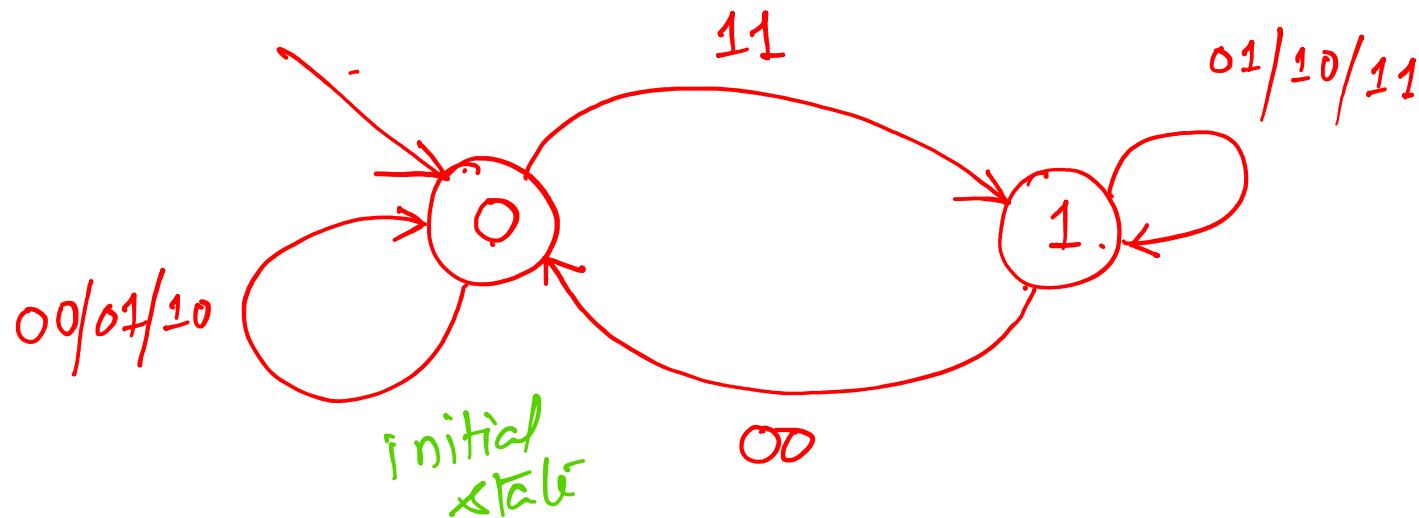
c_3, c_2, c_1
 $a_3, -a_1, a_0$
 b_3, b_1, b_0

Memorize the carry.

Carry = 0]
Carry = 1]



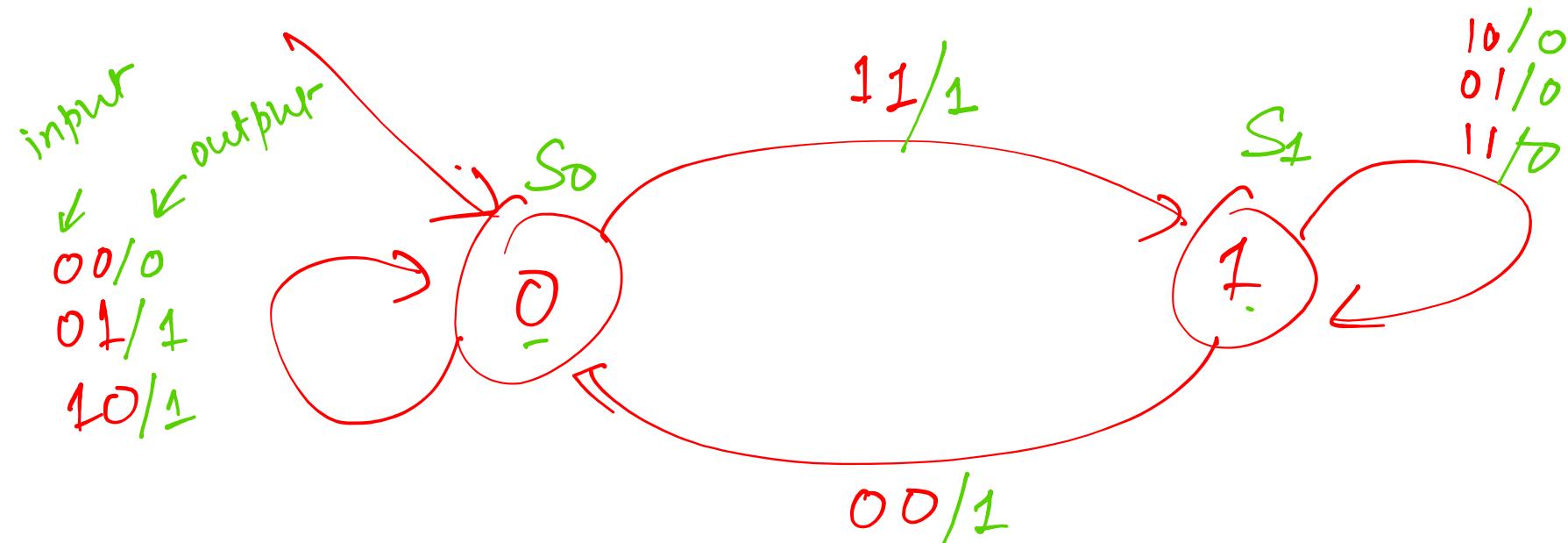
Adder



State Transition Graph. (STG)



Serial Adder



Thank You

