Sequential Circuits

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CS-230: Digital Logic Design & Computer Architecture

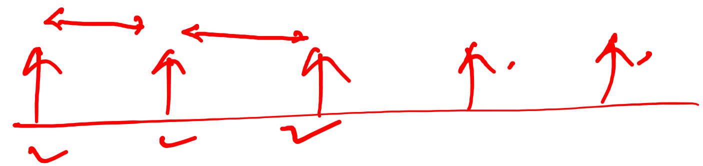
Lecture 17 (14 February 2022)

CADSL

Sequential Circuit

- temporal behaviour

clock



Synchronous Sequential Circuit

⇒ Asynchronous Sequential Circuits.

(no clock).

Order the event. (handshaking)

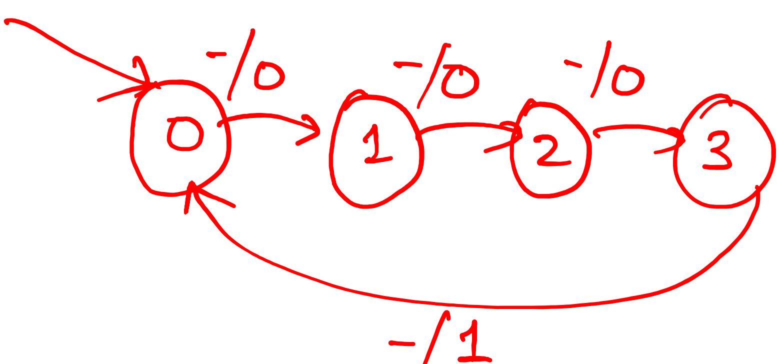
State Machine

$M(\underbrace{I, O, S, S_0, \delta, \lambda})$

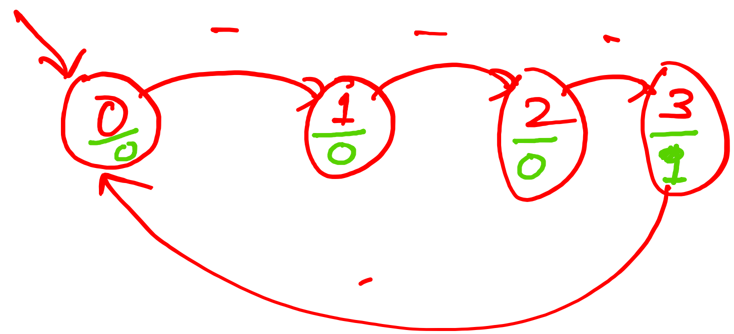
$\lambda : S \rightarrow O$ ~~MEALY~~ MOORE

$\lambda : S \times I \rightarrow O$ MEALY

0, 0, 0, 1, 0, 0, 0, 1 ·



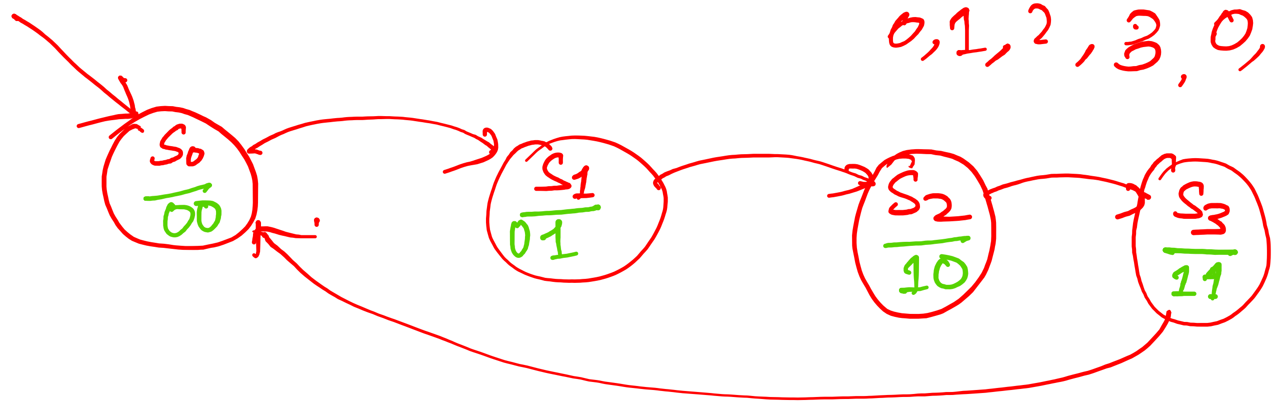
MEALY MACHINE



MOORE MACHINE

State Machine

0, 1, 2, 3, 0, 1, 2, 3, 0, 1, ...



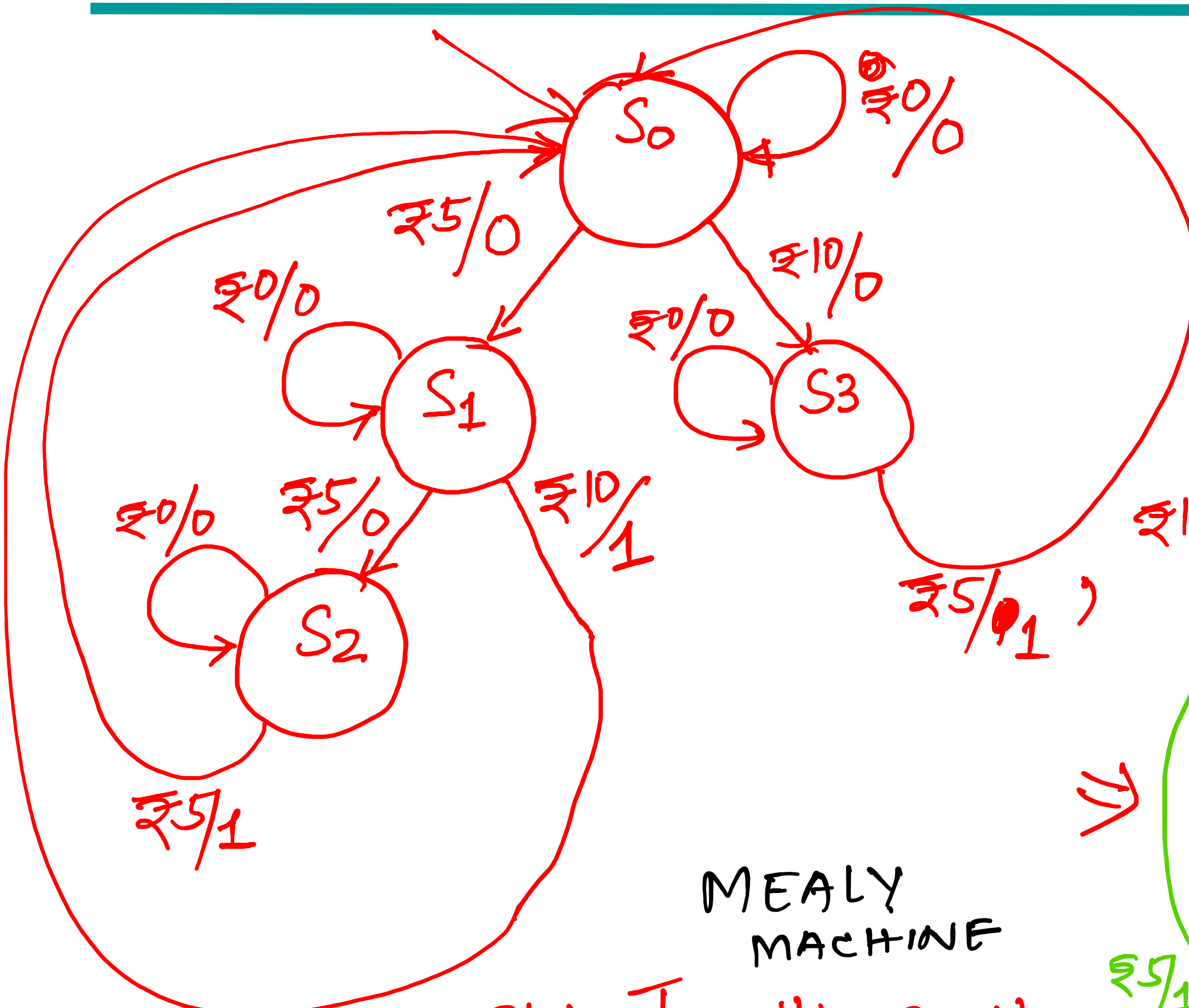
Free running counter.

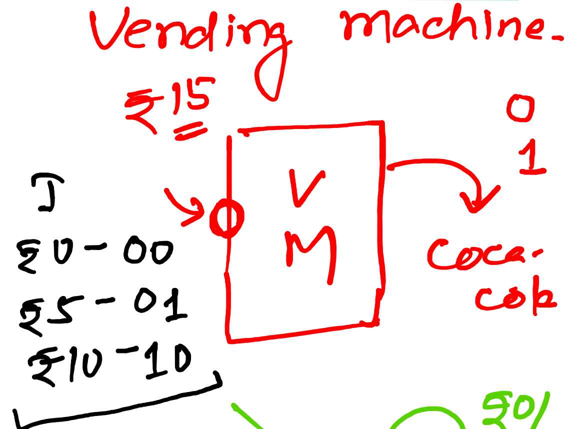
0, 1, 2, 3, 0, 1, 2, 3, . . .

0: {0, 1, 2, 3}

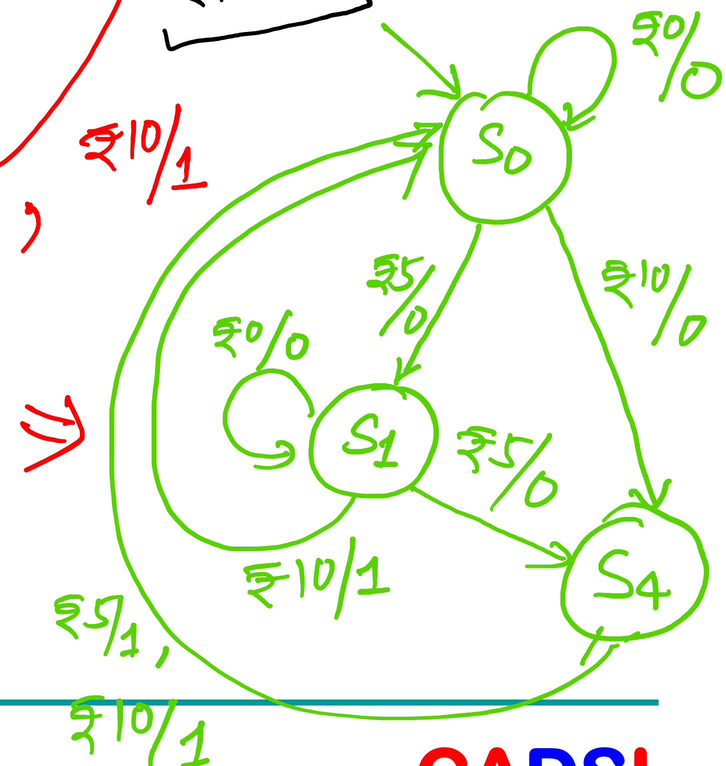
00 01 10 11

Finite State Machine



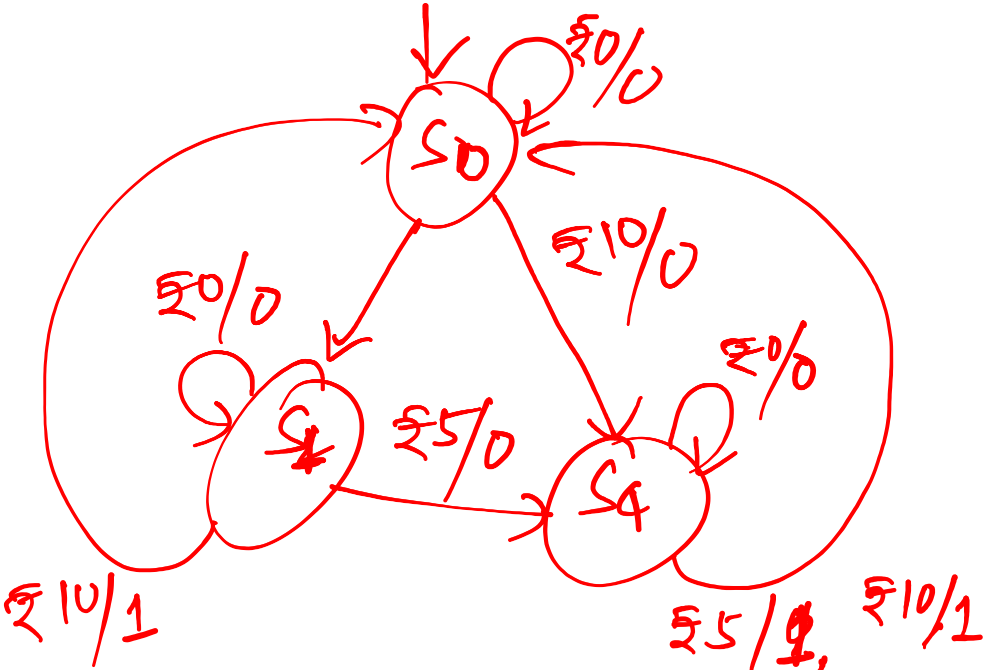


MEALY MACHINE



State transition graph

Finite State Machine



PS	NS, Output		
	00 ₹0	01 (₹5)	10 (₹10)
S_0 00	S0, 0	S1, 0	S4, 0
S_1 01	S1, 0	S4, 0	S0, 1
S_4 10	S4, 0	S0, 1	S0, 1

3 States

	t_1	t_0
S0 -	0	0
S1 -	0	1
S4 -	1	0

I	a_1	a_0
₹0	0	0
₹5	0	1
₹10	1	0

$M(I, O, S, S_0, \delta, \lambda)$

$I = \{00, 01, 10\}$ $O = \{0, 1\}$

$S = \{S0, S1, S4\}$ $S_0 = \{S_0\}$

δ' δ, λ

Finite State Machine

$\delta^{t_1}(t_1, t_0, a_1, a_0)$

$\delta^{0}(t_1, t_0, a_1, a_0)$

$\lambda(t_1, t_0, a_1, a_0)$

λ

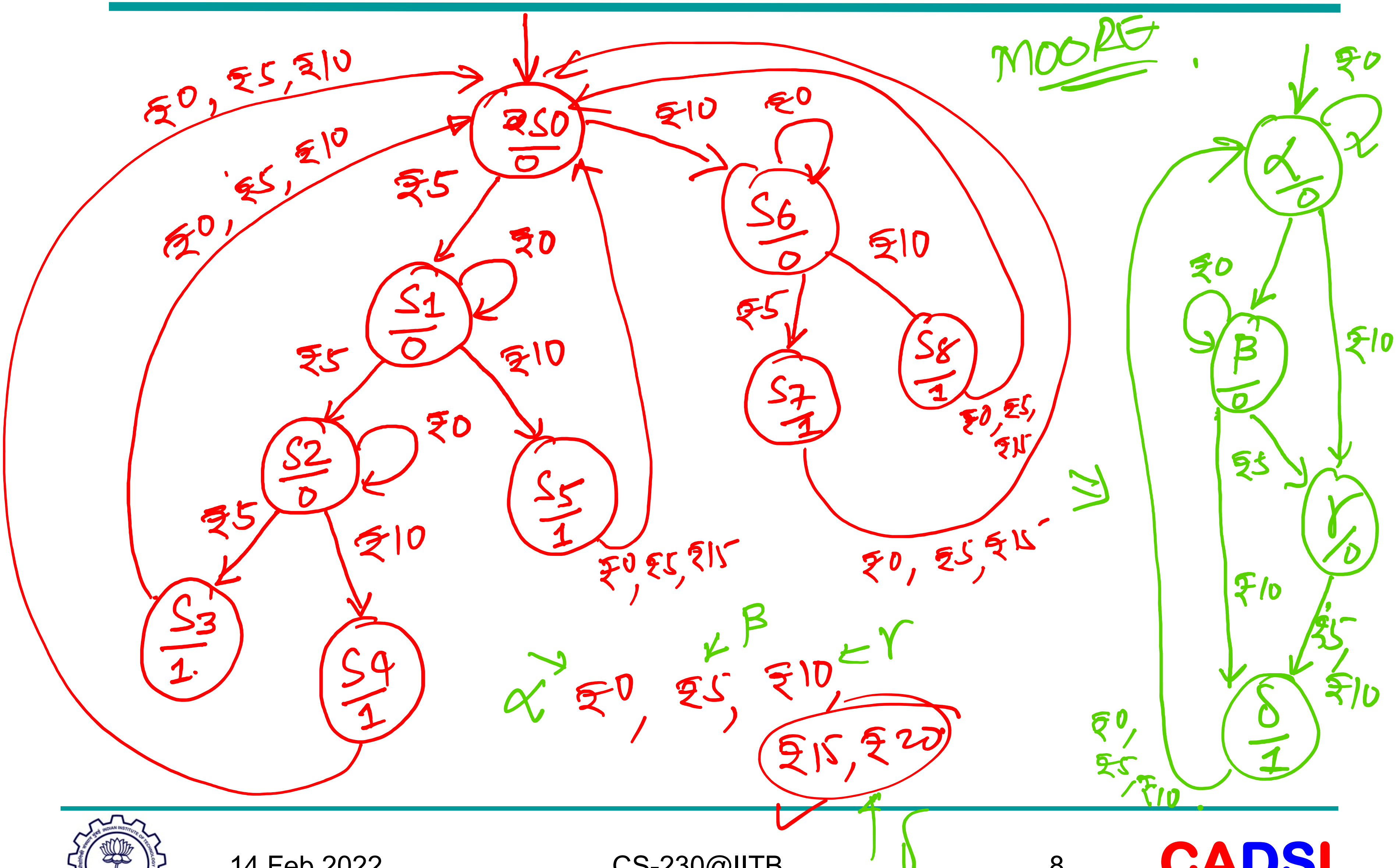
$t_1t_0 \backslash a_1a_0$	00	01	11	10
00	0	0	X	0
01	0	0	X	1
11	X	X	X	X
10	0	1	X	1

$\lambda = t_0 a_1 + t_1 a_1 + t_1 a_0$

$\delta^{t_1} =$

$\delta^{t_0}:$

Finite State Machine



Finite State machine

MOORE MACHINE

a_1, a_0

$I = \{$ ₹50 00, ₹25 01, ₹10 10

→ $\alpha, \beta, \gamma, \delta$

00 01 10 11

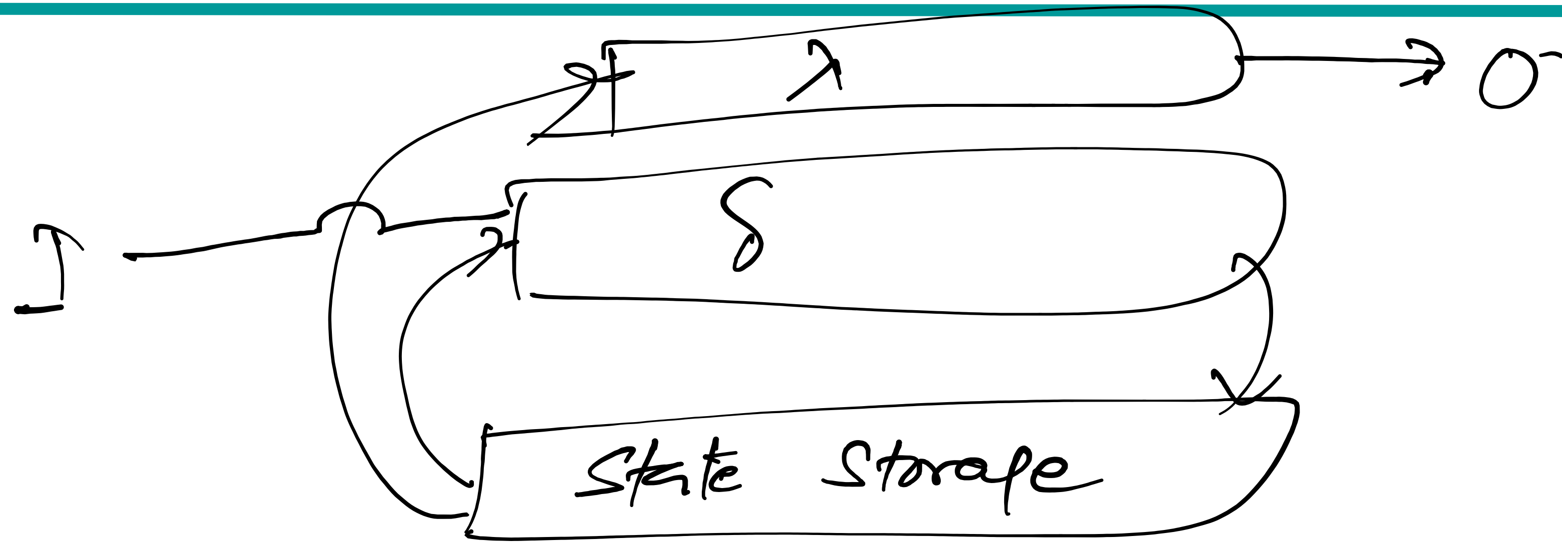
t_1, t_0

$\delta^{t_1}(t_1, t_0, a_1, a_0)$

$\delta^{t}(t_1, t_0, a_1, a_0)$

$\lambda(t_1, t_0)$

Finite State machine



Thank You