Logic Optimization

Virendra Singh
Professor
Computer Architecture and Dependable Systems Lab
Department of Computer Science & Engineering, and
Department of Electrical Engineering
Indian Institute of Technology Bombay
http://www.cse.iitb.ac.in/~viren/
E-mail: viren@{cse, ee}.iitb.ac.in

CS-230: Digital Logic Design & Computer Architecture

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CADSL

Representation

(1) Truth Table (2) Sum of min terms
(3) Product of Maxterms

UNIQUE

Canonical.

Graphical.

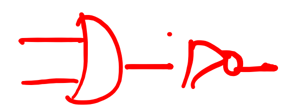
Canonical

(4) Binary Decision Diagram (ROBDD)

(5) Reed Muller Representation - canonical.
(AND and XOR)

not canonical

(6) And Inverter Graph (AIG)



ABC (7) SOP (8) POS

non-canonical

(8) Hybrid

Function Minimization

SOP → 2 level.
POS → 2 level

AND → OR ≡ NAND-NAND
OR → AND ≡ NOR-NOR.

minimize → Boolean Algebra ⇐

⇒ Not scalable approach

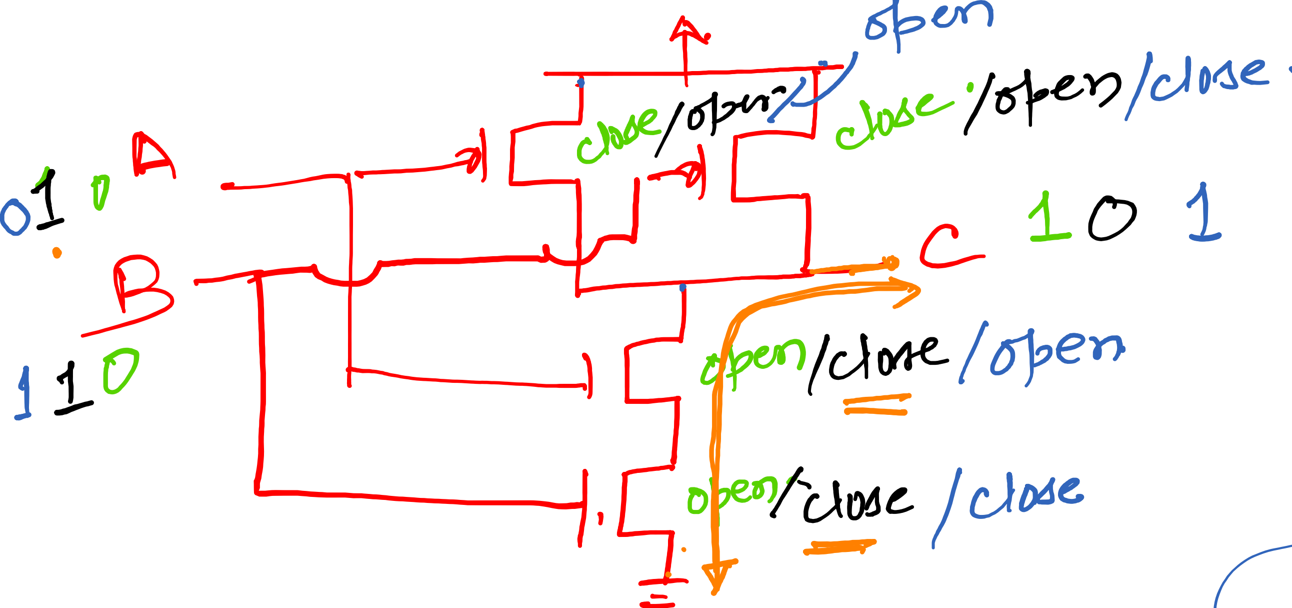
Automatic

Algorithmic approach.

① Graphical Method. (K-Map)

② Tabular Method. (QM.)

NAND



0 0 – 1
0 1 – 1
1 0 – 1
1 1 – 0

NAND

4 switches

N input = 2N switches/transistors

Delay.

delay of one switch is τ

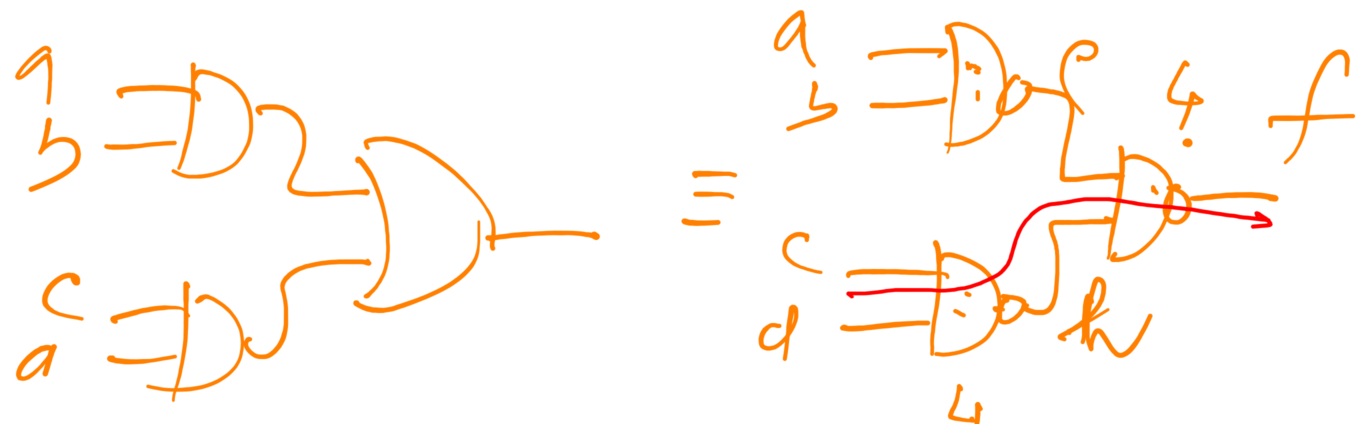
Delay of 2 input NAND is 2τ

for N input NAND = $N\tau$

COST of N input NAND : 2N.

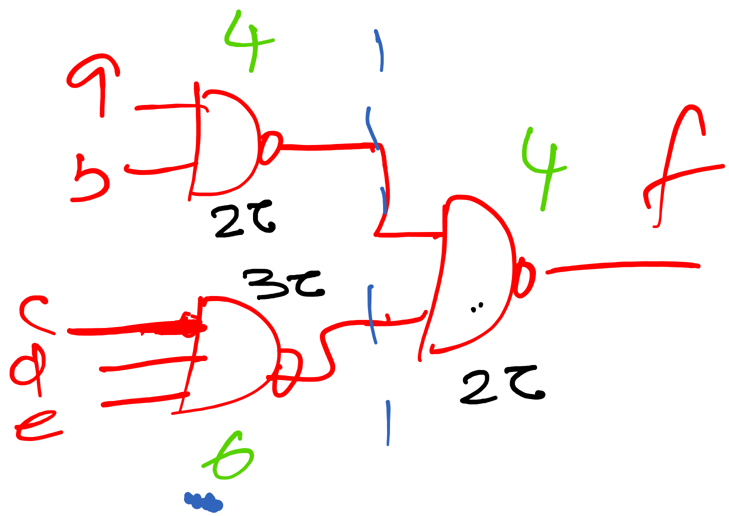
delay of N input NAND : $N\tau$.

$f(a,b,c,d) = ab + cd$



COST = 2× # literals + 2× # product terms.

$f(a,b,c,d,e) = \underbrace{ab} + \underbrace{cde}$



<u>delay</u> = Max delay of first level + delay of second level.

$= \cancel{\{(2,3)\}} + \max\{2\tau, 3\tau\} + 2\tau. = 5\tau$

(Max literals in any prod. term + # prod. term)

9 5 2 3 3 3

AREA:

Minimize

COST

Min (# literals + # prod. terms)

Delay

Min ((max # literal in any prod. term) + # prod. terms)

min # product terms

minimize cost

minimize delay

~~POS~~,

SOP

Logic Minimization

- Generally means
  - In SOP form:
    - Minimize number of products (reduce gates) and
    - Minimize literals (reduce gate inputs)
  - In POS form:
    - Minimize number of sums (reduce gates) and
    - Minimize literals (reduce gate inputs)

$a=1$ & $b=1 \Rightarrow f=1$ $\quad f(a,b)$

$a \cdot b \rightarrow f$

implicants

a	b	f
0	0	0
0	1	0
1	0	0
1	1	1

Product or Implicant or Cube

- Any set of literals ANDed together.
- Minterm is a special case where all variables are present. It is the largest product.
- A minterm is also called a 0-implicant of 0-cube.
- A 1-implicant or 1-cube is a product with one variable eliminated:
  - Obtained by combining two adjacent 0-cubes
  - $ABCD + ABC\bar{D} = ABC(D + \bar{D}) = ABC$

$\underbrace{D+\bar{D}}_{1}$

ABC → f

Function Minimization

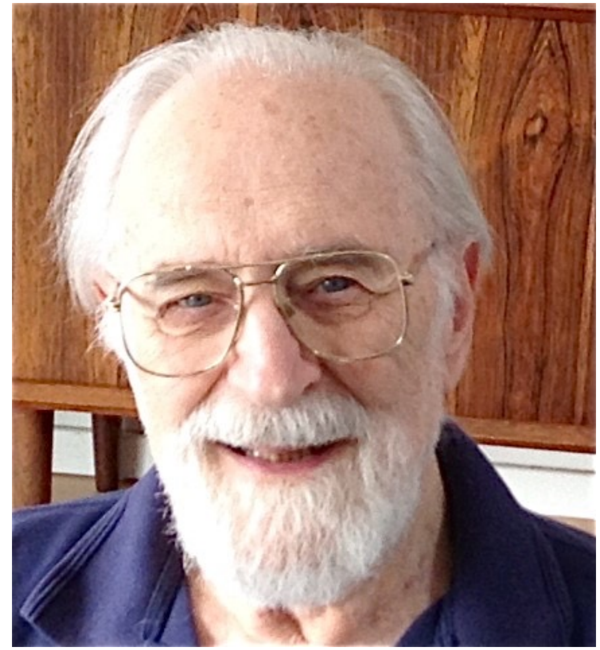
$$f(a,b) = ab + a\bar{b}$$

$$= a\cdot\underbrace{(b+\bar{b})}_{1} = a$$

Graphical Method: Karnaugh Map

Maurice Karnaugh

- American Physicist
- Bell Lab (1952 – 66)
- Developed K-Map in 1954



Maurice Karnaugh
Born: 4 October 1924

Karnaugh, Maurice (November 1953), "The Map Method for Synthesis of Combinational Logic Circuits" . *Transactions of the American Institute of Electrical Engineers, Part I: Communication and Electronics*. **72**(5): 593–599

Function Minimization: K-Map

$f(a,b) = \underline{ab + a\bar{b}} = a\cdot(b+\bar{b}) = a \qquad a \to f$

$abc + a\bar{b}c \Rightarrow ac$

a	0	1
f	0	1

$f(a) = a$

a	0	1
f	1	0

$f(a) = \bar{a}$

a	0	1
f	1	1

$f = 1$

a	b	c
0	0	1
0	1	0
1	0	1
1	1	0

$\bar{a}\bar{b} + a\bar{b} = \bar{b}$

a \ b	0	1
0	1	0
1	1	0

$f(a,b) = \bar{b}$

ab	00	01	11	10
f	1	0	0	1

$f(a,b) = \bar{b}$

Function Minimization: K-Map

a \ bc	00	01	11	10
0	1 (m_0)	0 (m_1)	0 (m_3)	1 (m_2)
1	0 (m_4)	1 (m_5)	1 (m_7)	0 (m_6)

$f(a,b,c)$

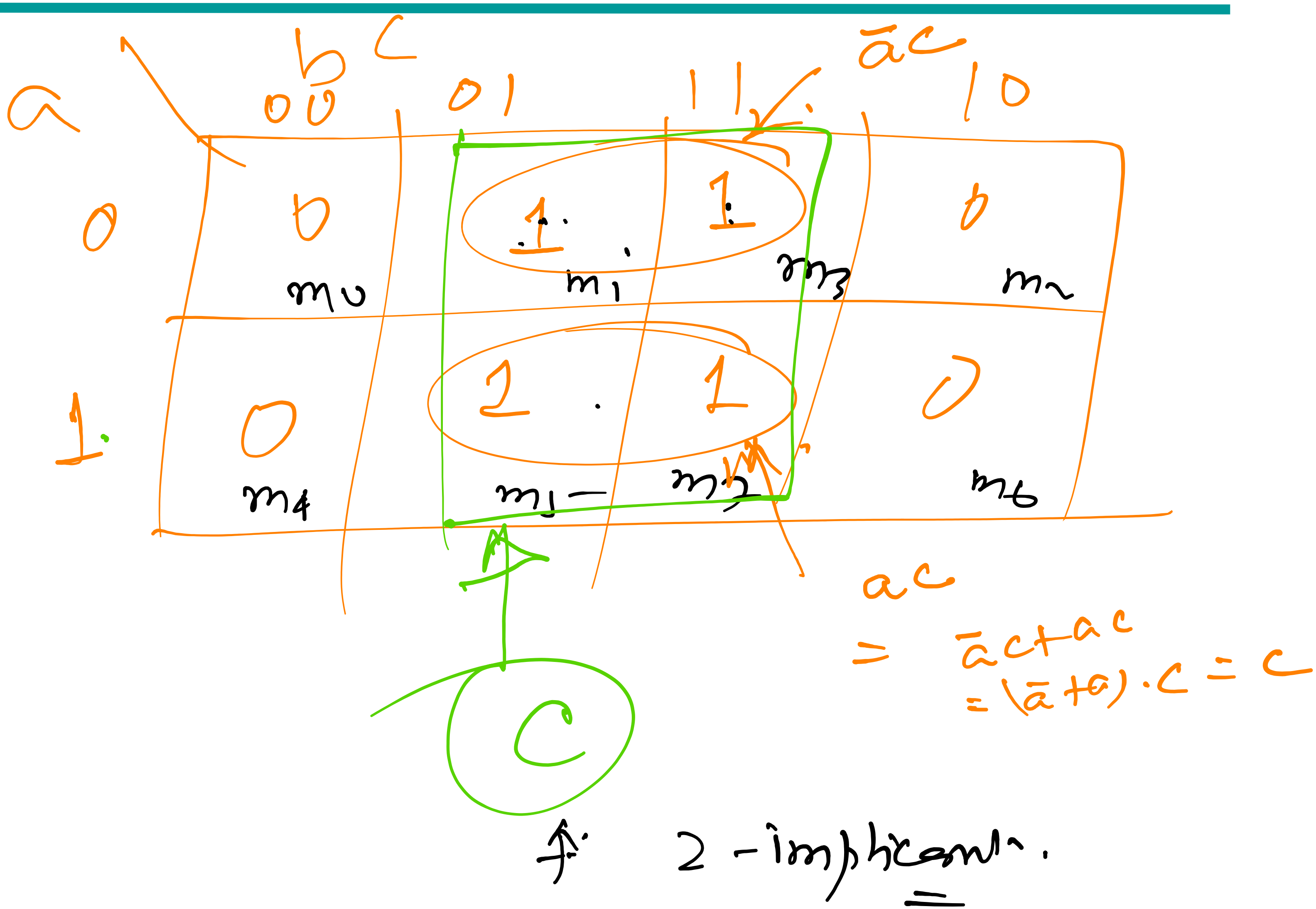
$\bar{a}\bar{c}$

1-Implicant

$a.c$

$\Rightarrow \bar{a}\bar{c}+ac$

Function Minimization: K-Map



Prime.

Function Minimization: K-Map

ab \ cd	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

PRIME IMPLIC.

a \ b	0	1
0	1	0
1	0	1

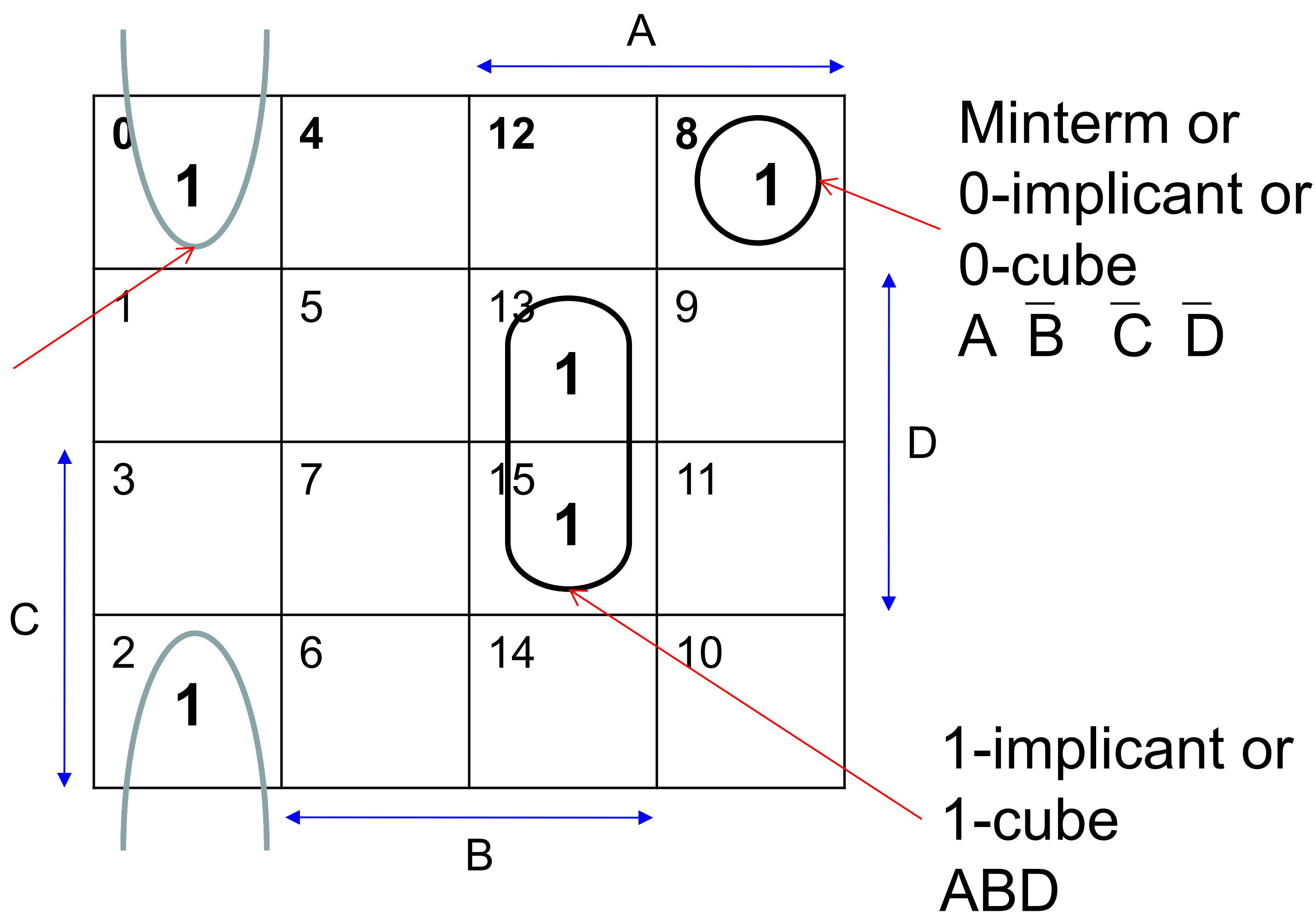
$\bar{a}\bar{b} + ab$

a \ b	0	1
0	1	1
1	0	1

$\boxed{\bar{a} + b}$

PI $\Leftarrow$ # prod. terms.

Cubes (Implicants) of 4 Variables



Thank You