



CS305: Computer Architecture

World of Instructions-V (The MIPS language)

https://www.cse.iitb.ac.in/~biswa/courses/CS305/main.html

Quick recap

Usage of j, jr, jal, and \$ra

We stopped at: Protocol between caller and callee

MIPS provides

Upto four arguments can be passed from the caller to the callee while using jal. It uses registers \$a0 to \$a3

A callee can return upto two values to the caller. It uses registers \$v0 and \$v1

What if?

```
main(){
a = a + f1(a);
                                 f1:
f1(a) {
                                      f2's argument in $a0 to $a3
                                               jal f2
        a = a - f2(a); return a;
f2(a) {
        a = a + f3(a); return a;
f3(a) {
        a = a + 1; return a;
```

What if?

. . .

```
f1:
  f2's argument in $a0 to $a3
  jal f2
f2:
  f3's argument in $a0 to $a3
  jal f3
```

Computer Architecture

What is the big deal?

```
f1:
   f2's argument in $a0 to $a3
   jal f2
f2:
   f3's argument in $a0 to $a3
   jal f3
```

. . .

What is the big deal? Oh no!

```
f1:
 PC: f2's argument in $a0 to $a3
                     // $ra = PC+8
 PC+4: jal f2
f2:
 PC+100: f3's argument in $a0 to $a3
 PC+104: jal f3 // $ra = PC+108
                                        f3: ...
                                           jr $ra
```

What is the big deal? Oh no!

```
f1:
 PC: f2's argument in $a0 to $a3
 PC+4: jal f2 // $ra = PC+8
f2:
 PC+100: f3's argument in $a0 to $a3
 PC+104: jal f3 // $ra = PC+108
jr $ra ⊗ Oh no!!
                                        f3: ...
                                          jr $ra
```

Saving and Restoring Registers (limited)

caller registers callee registers

Why?

Callee does not know, registers used by callers, can be many callers too

Caller does not know the callee's plan ©

MIPS 32 registers

• Registers	Total Regs
• \$Zero	1
(Return) Value registers (\$v0,\$v1)	3
 Argument registers (\$a0-\$a3) 	7
 Return Address (\$ra) 	8
 Saved registers (\$s0-\$s7) 	16
 Temporary registers (\$t0-\$t9) 	26
 Global Pointer (\$gp) 	27
Stack Pointer (\$sp)	28
 Frame Pointer (\$fp), or \$t10 	29

• 2 for OS (\$k0, \$k1), 1 for assembler (\$at)



Do not forget 32 MIPS registers only Register spilling 😂

Gracias