Sequential Circuits

Virendra Singh

Professor

Computer Architecture and Dependable Systems Lab

Department of Computer Science & Engineering, and

Department of Electrical Engineering

Indian Institute of Technology Bombay

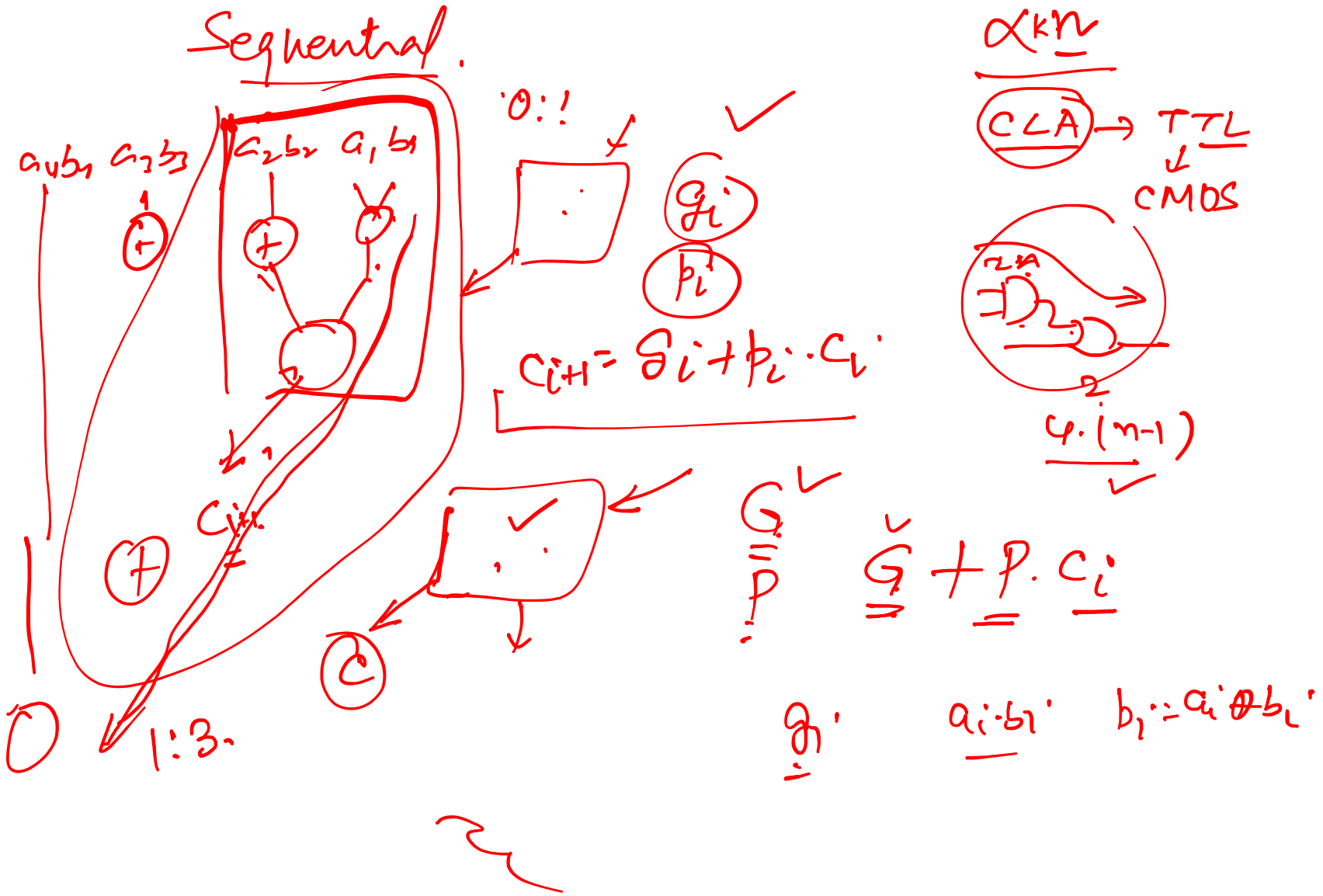
http://www.cse.iitb.ac.in/~viren/

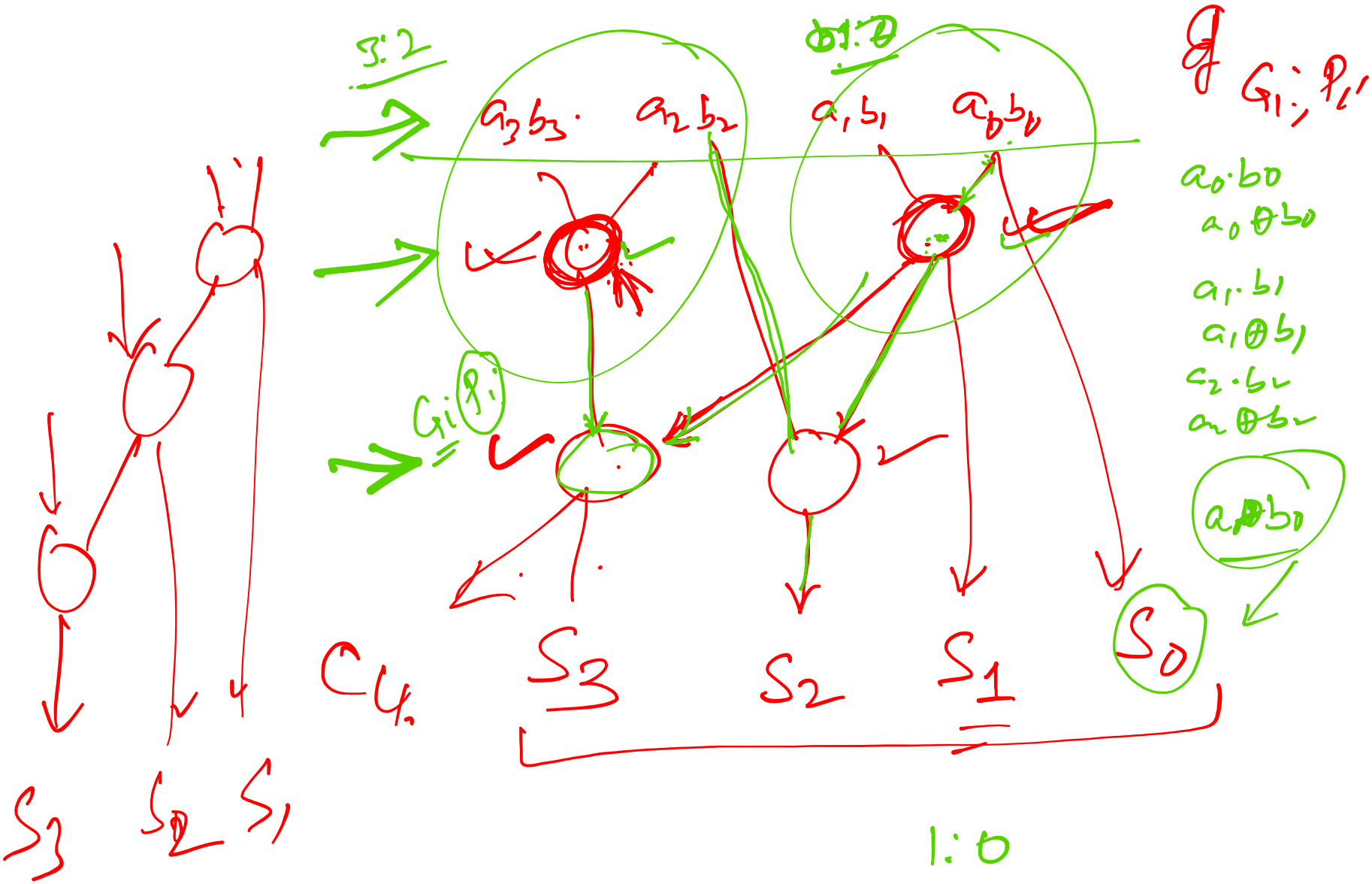
E-mail: viren@{cse, ee}.iitb.ac.in

CS-230: Digital Logic Design & Computer Architecture

Lecture 15 (08 February 2022)

CADSL


Sequential.
a0b0 a1b1 a2b2 a3b3
0:1
1:3
gi
pi
ci+1 = gi + pi · ci
ci
G
P
G + P · ci
gi
ai·bi
bi = ai ⊕ bi
CLA → TTL
CMOS
4-bit CLA
c4 (n-1)


3:2
1:0
G_i P_i
$a_3 b_3$
$a_2 b_2$
$a_1 b_1$
$a_0 b_0$
$a_0 \cdot b_0$
$a_0 \oplus b_0$
$a_1 \cdot b_1$
$a_1 \oplus b_1$
$c_2 \cdot b_2$
$a_2 \oplus b_2$
$a_3 \oplus b_3$
C_4
S_3
S_2
S_1
S_0
S_3 S_2 S_1
1:0

3:2

$g_3 \cdot a_3 \cdot b_3$

$g_4 \cdot a_2 \cdot b_2$

$a_3 \oplus b_3 = p_3$

$a_3 \oplus b_3 = p_4$

$G_{3:2} = g_3 + g_2 \cdot p_3$ generated from left 3:2

$\rightarrow P_{3:2} = p_3 \cdot p_2$

$G_{3:2} = g_3 + g_2 p_3$

$P_{3:2} = p_3 \cdot p_2$

$a_1\ b_1$ $\quad$ $a_0\ b_0$

$g_1 = a_1 \cdot b_1$ $\quad$ $g_0 = a_0 \cdot b_0$

$p_1 = a_1 \oplus b_1$ $\quad$ $p_0 = a_0 \oplus b_0$

$G_{3:2} = g_3 + p_3 g_2$

$P_{3:2} = p_3 \cdot p_2$

$G_{1:0} = g_1 + g_0 \cdot p_1$

$P_{1:0} = p_1 \cdot p_0$

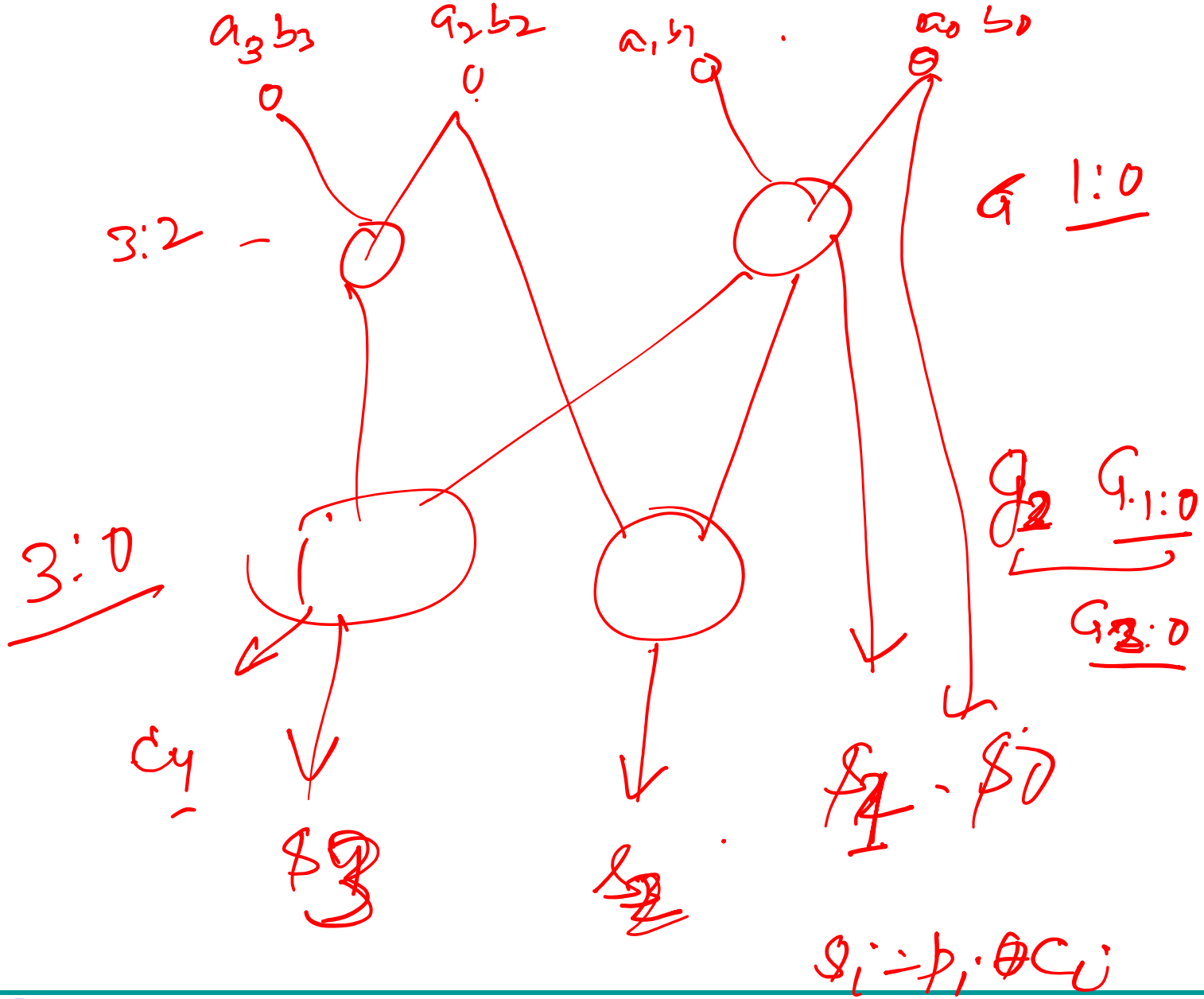
$G_{3:0} = G_{3:2} + P_{3:2} \cdot G_{1:0}$

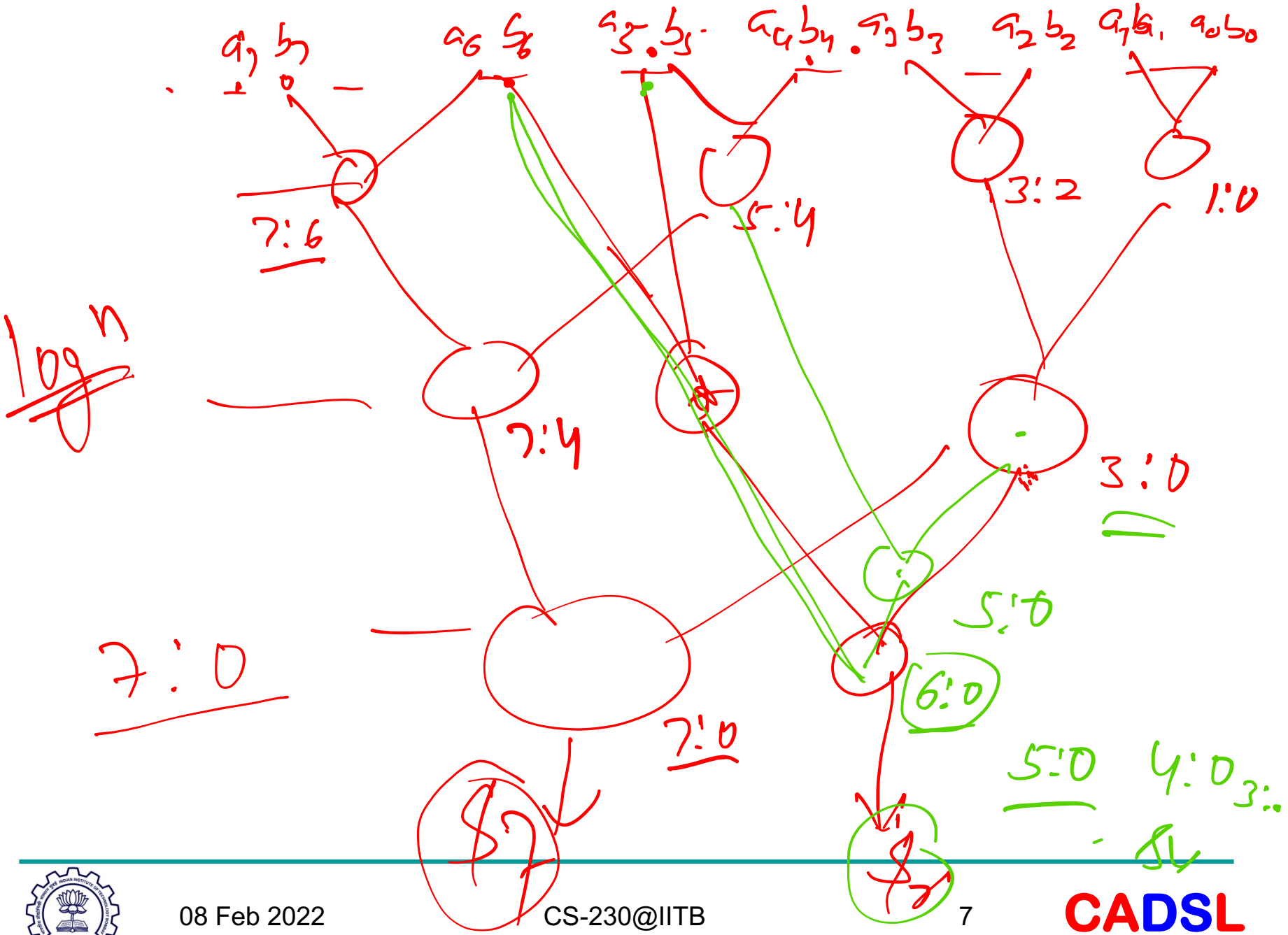
$P_{3:0} = P_{3:2} \cdot P_{1:0}$

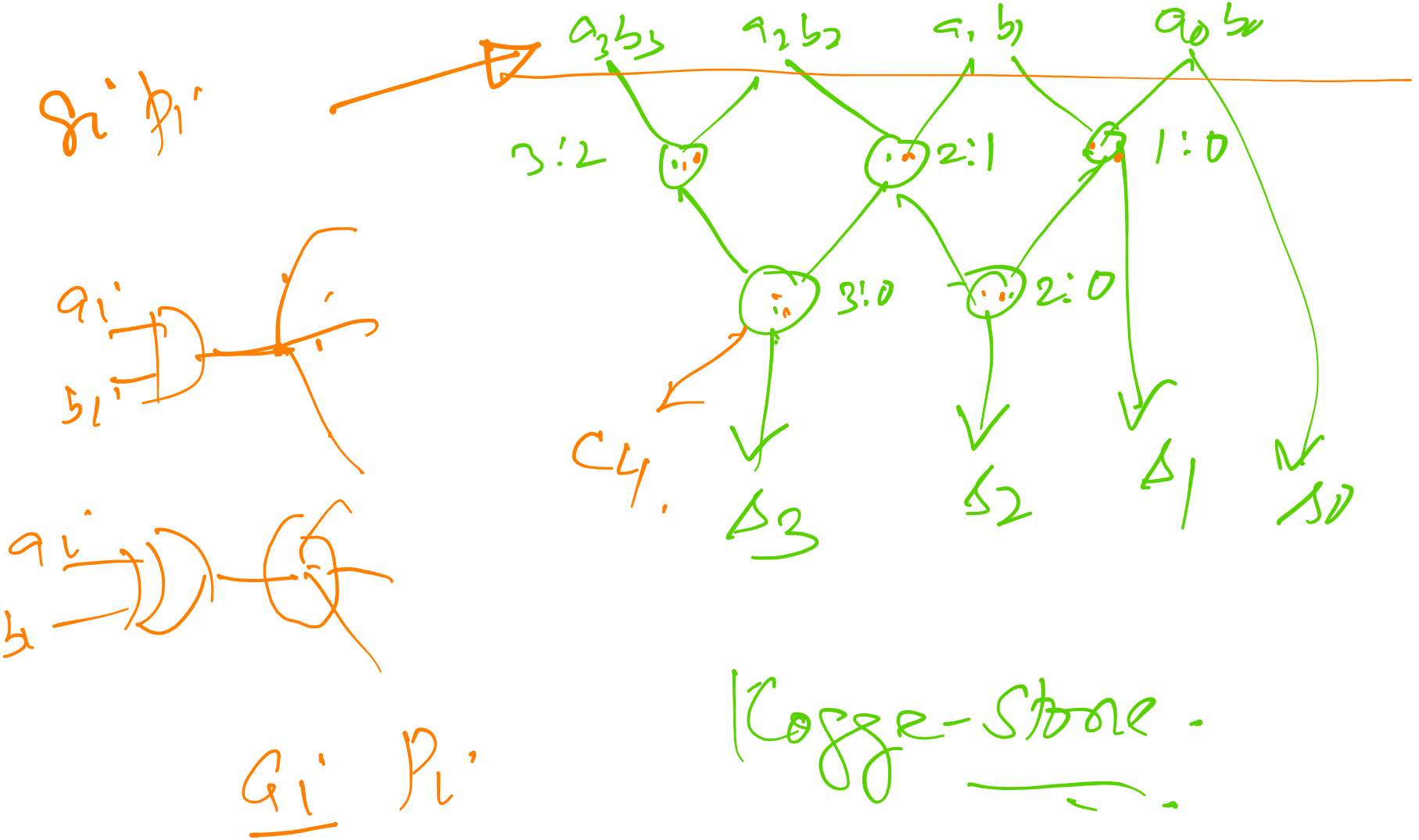
3 − 0

$s_1 = p_1 \oplus$ $\quad$ $s_0 = p_0$

$c_{i+1} = G_{3:0} + P_{3:0} \cdot c_0$ $\quad$ $s_i = p_i \oplus c_i$

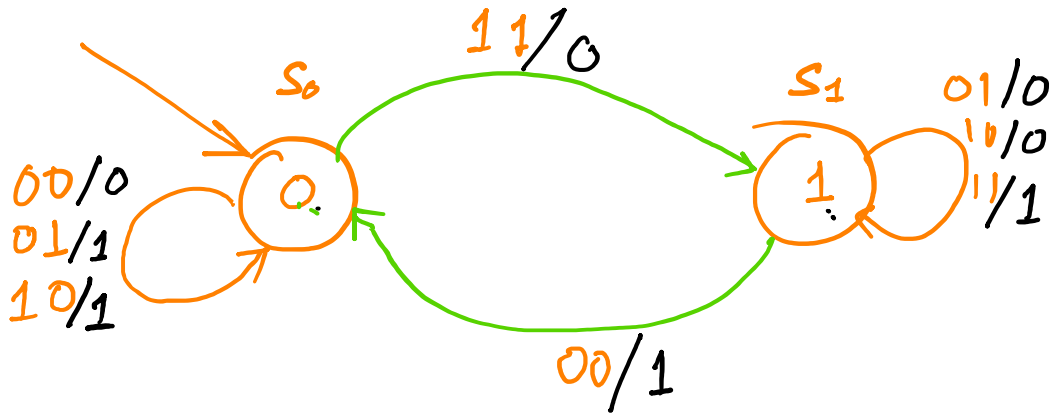

$a_3 b_3$
$a_2 b_2$
$a_1 b_1$
$a_0 b_0$
3:2
G 1:0
3:0
G_2 G.1:0
G3:0
C_4
S_3
S_2
$S_1 - S_0$
$S_i = p_i \oplus C_i$

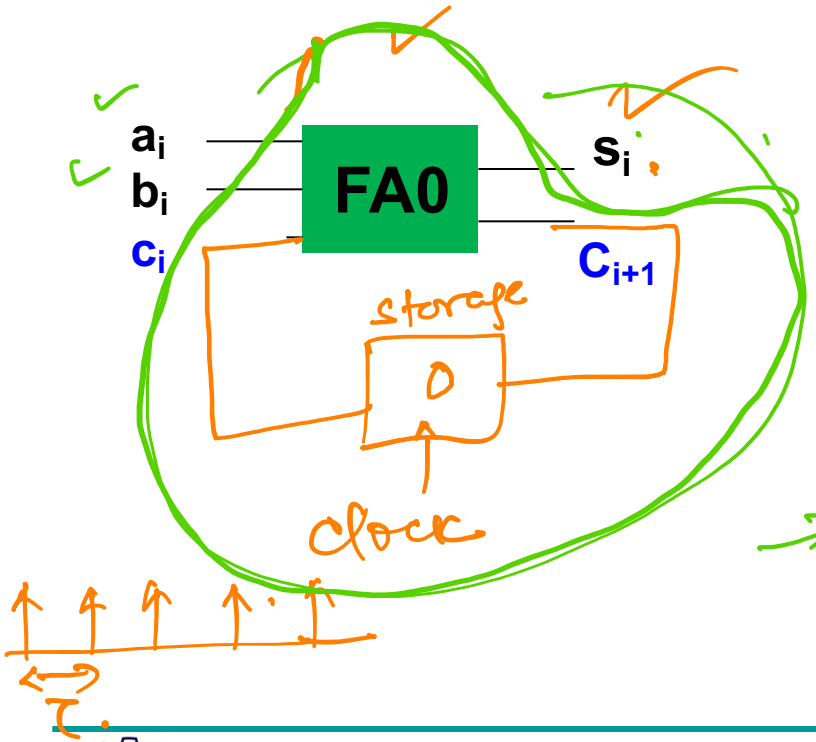

7:6
5:4
3:2
1:0
7:4
3:0
7:0
5:0
6:0
7:0
5:0
4:0


gi pi
a3b3
a2b2
a1 b1
a0 b0
3:2
2:1
1:0
3:0
2:0
c4
s3
s2
s1
s0
gi
pi
gi
pi
Gi Pi
Kogge-Stone

Serial Adder

```
c32  c31 . . .  c2  c1   0
      a31 . . . a2  a1  a0
    + b31 . . . b2  b1  b0
-------------------------
      s31 . . .  s2  s1  s0
```





STG

State	inputs 00	01	10	11
0	0/0	0/1	0/1	1/0
1	0/1	1/0	1/0	1/1

SIT

State Machine

$M(I, O, S, S_0, \delta, \lambda)$

I: Input symbols $\{00, 01, 10, 11\}$

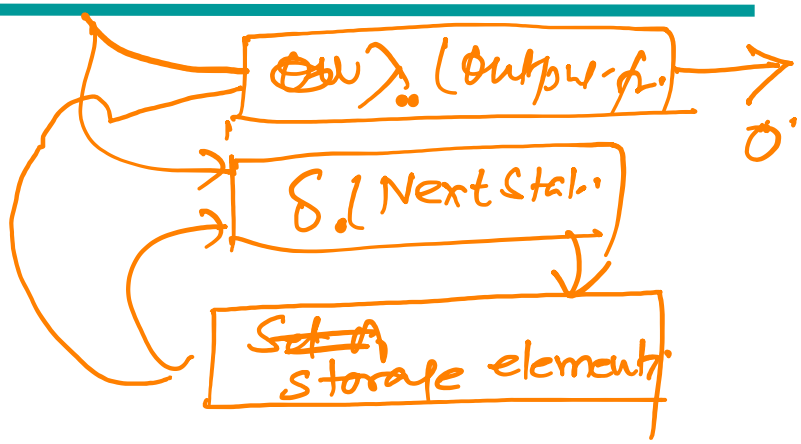
O: Output symbol $\{0, 1\}$

S: Set of States $\{0, 1\}$

S_0: Initial State $\{0\}$

δ: $S \times I \rightarrow S$ Transition function

λ: $S \times I \rightarrow O$ Output function



δ λ → Combinational logic

Storage $= \log_2 |S|$

Thank You