Low-Power, High-Speed, and Area-Efficient Multiplier Based on the PTL Logic Style

DCMOS PROJECT REPORT

submitted by

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ABSTRACT

With the development of Very Large-Scale Integration (VLSI) technology, circuit designers are increasingly focused on achieving low power, high speed, and small area. Among various circuit components, multiplier circuits play an important role in improving the overall system performance due to their significant power consumption and impact on circuit speed. In this brief, we propose a novel 8-bit signed multiplier based on the Pass Transistor Logic (PTL) that outperforms existing designs. Relative to CMOS logic, PTL logic provides a 3.21 % decrease in power consumption, a 35.78 % reduction in delay, and a 37.84% improvement in PDP.

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Chapter 1

INTRODUCTION

Multipliers are essential components in modern digital systems such as DSPs, machine-learning accelerators, and processors. Their efficiency directly impacts overall system speed, power consumption, and area. While CMOS logic remains reliable, its growing transistor count and switching capacitance limit performance in scaled technologies.

Pass Transistor Logic (PTL) offers a promising alternative due to its lower transistor count, reduced node capacitance, and potentially higher speed. However, PTL circuits suffer from threshold-voltage loss and weak drive strength when cascaded, making careful usage necessary.

This project leverages the advantages of PTL while avoiding its limitations by developing a hybrid PTL–CMOS Radix-4 Booth Multiplier. A fully CMOS multiplier is also implemented as a reference, enabling detailed comparison in terms of delay, power, area, and power-delay product (PDP).

1.1 Radix-4 Booth Multiplier Overview

Radix-4 Booth encoding reduces the number of partial products by grouping the multiplier bits in triplets and generating values from the set 0, ± 1, ± 2. For 8-bit signed multiplication: The multiplier is segmented into four overlapping 3-bit groups. Hence, only four partial products are generated, instead of eight.

Advantages:

50% fewer partial products than conventional array multipliers.

Reduced adder tree depth → potential for lower delay.

Efficient for signed multiplication due to two's-complement handling.

Chapter 2

METHODOLOGY

2.1 Modified Booth Encoder (MBE)

The MBE circuit selectively computes ±Y, ±2Y, or 0 depending on three multiplier bits X2i+1, X2i, X2i−1. The MBE circuit gives the 1's complement of the multiplicand in the case of selecting -Y and -2Y. A one is generated externally using separate control logic and is added to the 1's complement generated by the MBE in the adder tree to get the 2's complement of the multiplicand. The structure of the MBE, which shows a remarkable use of PTL XOR gates.

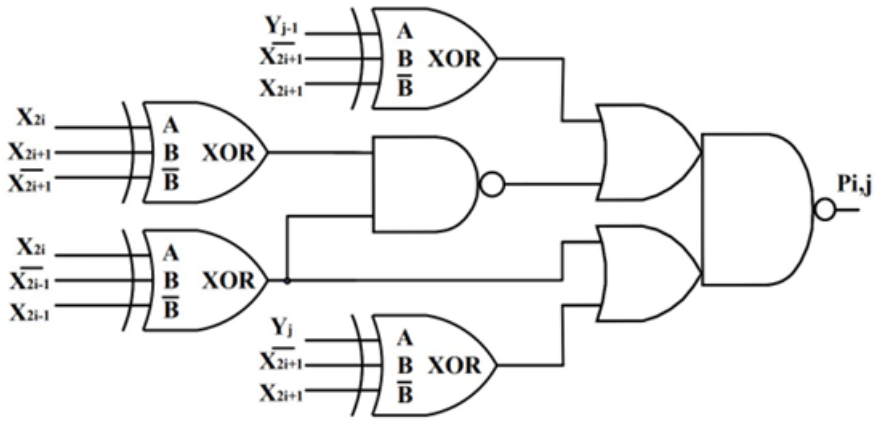

Figure 2.1: Structure of Modified Booth Encoder.

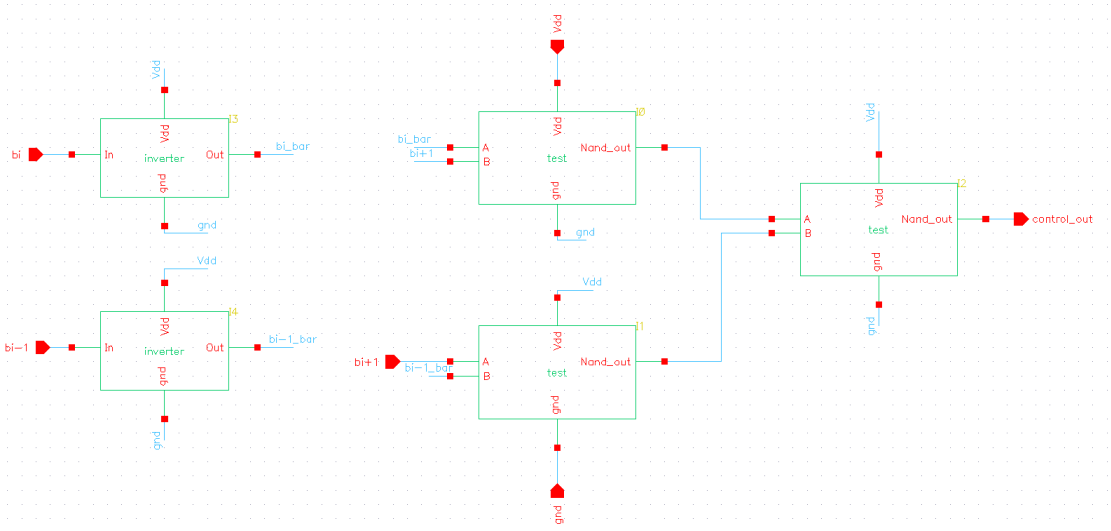

Figure 2.2: Control Logic.

2.2 Adder Tree Architecture

The utilization of PTL HA can effectively reduce the power consumption and delay of the multiplier. To further minimize circuit power consumption, the integration of PTL FA is plausible, but this leads to an increase in the critical path delay. While the maximum delay of the PTL FA surpasses that of the CMOS FA, its carry propagation delay is significantly smaller. Therefore, the low carry propagation delay of the PTL FA can be used to improve the critical path delay in the RCA circuit of a multiplier. However, one problem with this RCA circuit is that when n transmission gates are connected in series, the propagation delay increases in proportion to n2, leading to a rapid increase in delay as the number of gates grows. In the proposed architecture, an inverter is inserted after every two FAs. In order to ensure proper circuit functionality, we use a PTL FAINV. The main difference between the PTL FA and the FAINV lies in their carry inputs and carry outputs. Specifically,

the FAINV uses an inverted carry input Cin and an inverted carry output Co. In contrast, the PTL FA uses regular inputs and outputs.

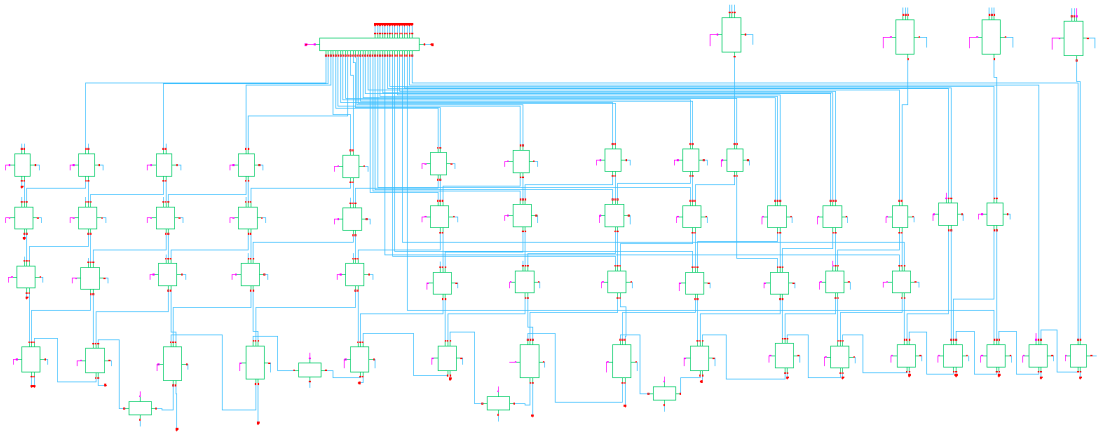

Figure 2.3: Entire Multiplier Architecture showing the Adder Tree

2.3 Circuit Diagrams

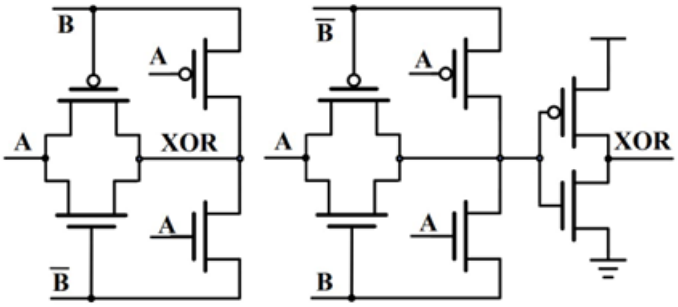

Figure 2.4: Cells designed by PTL logic style 4/6-T XOR.

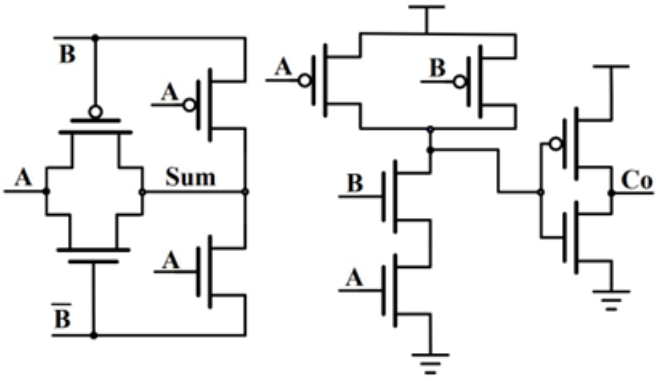

Figure 2.5: Cells designed by PTL logic style 12-T Half Adder.

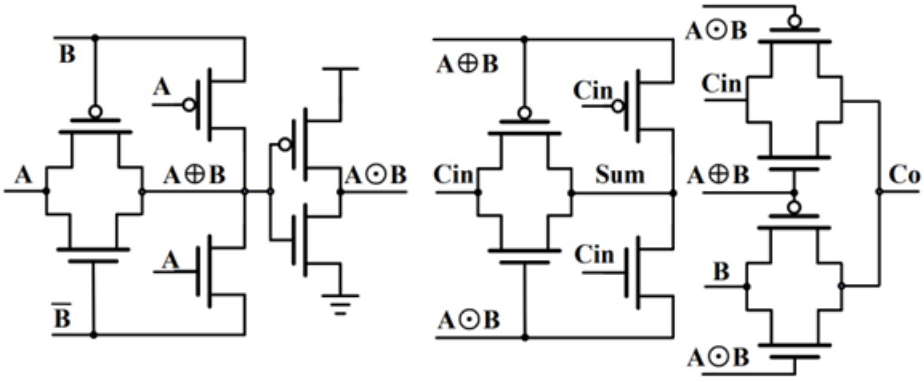

Figure 2.6: Cells designed by PTL logic style 16-T Full Adder.

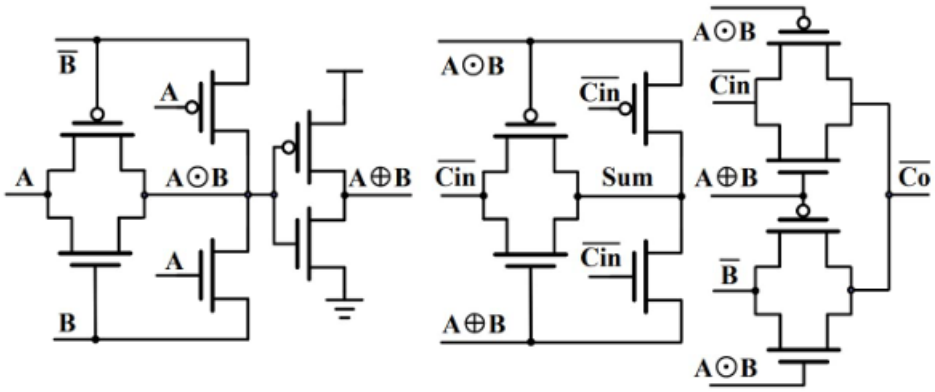

Figure 2.7: Proposed PTL 16-T FAINV circuit with inverted input Cin and inverted output Co.

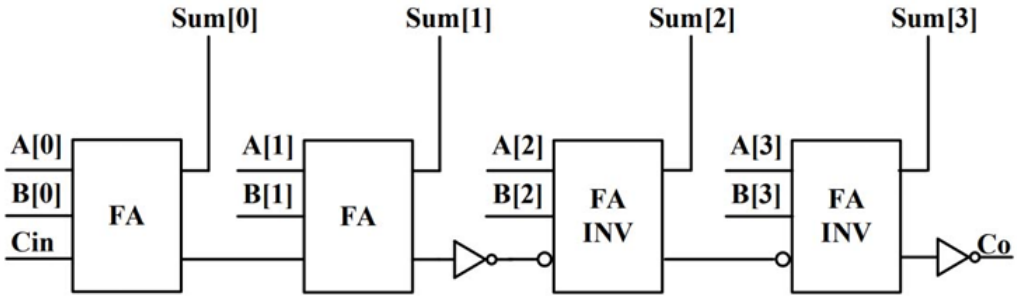

Figure 2.8: Proposed RCA circuit.

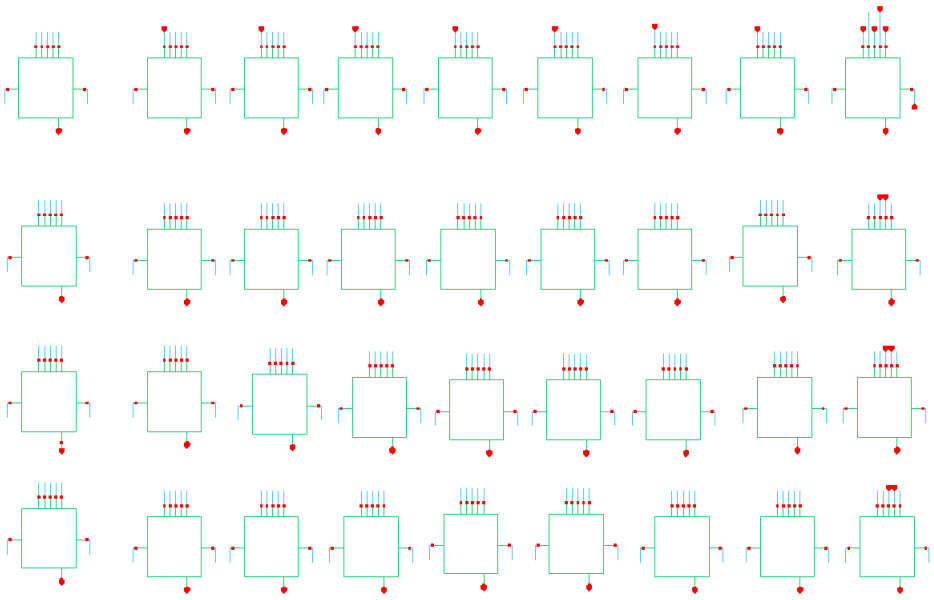

Figure 2.9: Modified Booth Encoder Block

Chapter 3

RESULTS

The input we gave is 01110101 and 11011000. The output we got is 1110110110111000.

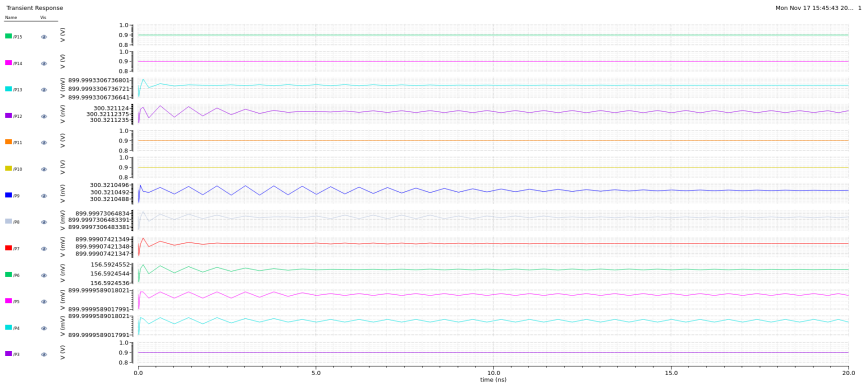

Figure 3.1: Output

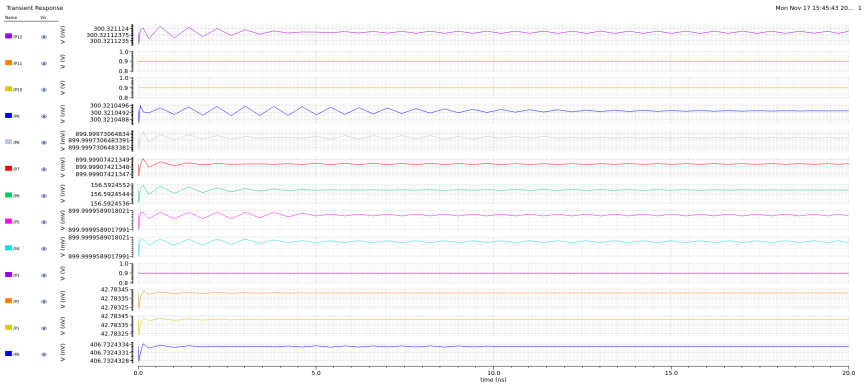

Figure 3.2: Output

Designs	**Transistor Count**	**Delay(ps)**	**Power(uW)**
CMOS FA	28	39.92	220.8
PTL FA	16	40.39	79.30
CMOS XOR	12	36.46	172.5
PTL XOR	4	20.68	35.52
CMOS HA	20	36.45	226.4
PTL HA	12	21.08	88.7

Table 3.1: Performance Comparison of CMOS and PTL Designs

PTL cells require fewer transistors and consume less power compared to CMOS cells. However, the delay of a PTL-based full adder is higher than that of a CMOS full adder. Therefore, PTL FA cells are not used in the higher rows of the adder tree.

Delay(ps)	**CMOS FA**	**PTL FA**	ΔT
A=0, B=1, Cin $\uparrow$	61.32	18.68	42.64
A=0, B=1, Cin $\downarrow$	55.08	19.77	35.31
A=1, B=0, Cin $\uparrow$	56.50	18.68	37.82
A=1, B=0, Cin $\downarrow$	58.19	19.77	38.42
Average	56.7725	19.2075	38.5475

Table 3.2: Comparison of Carry Propagation Delay

Compared to the CMOS full adder, the PTL full adder exhibits a lower carry propagation delay, which makes it suitable for use in the final RCA in the Adder Tree

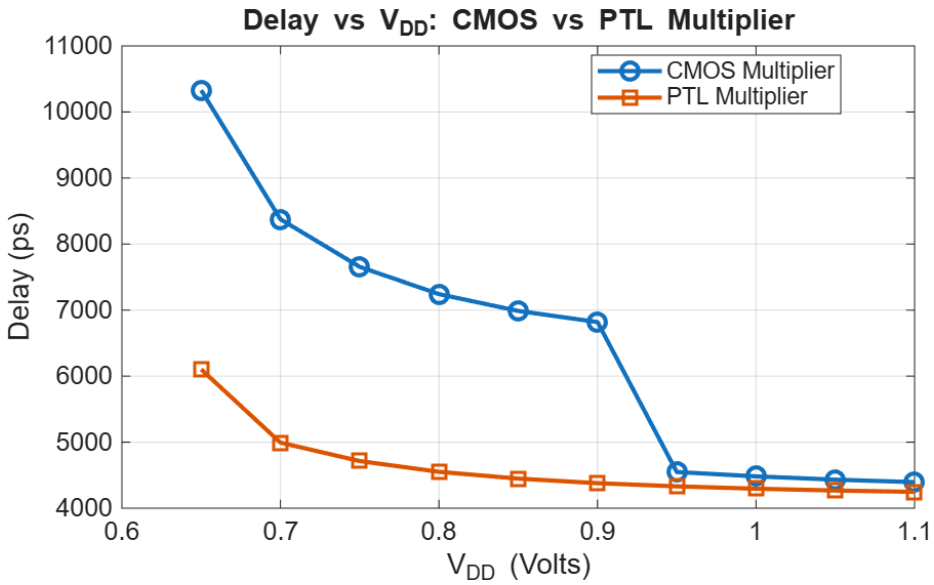

Figure 3.3: Delay vs VDD

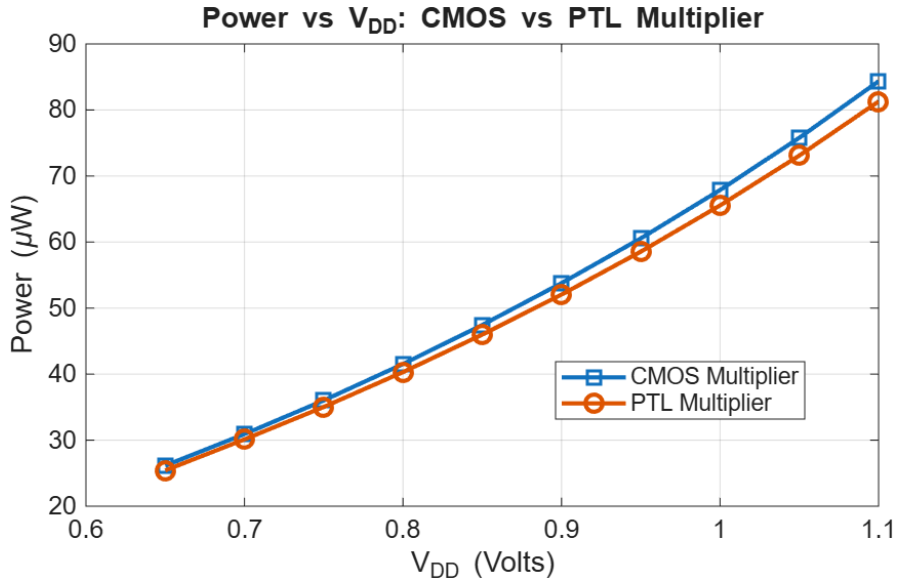

Figure 3.4: Power vs VDD

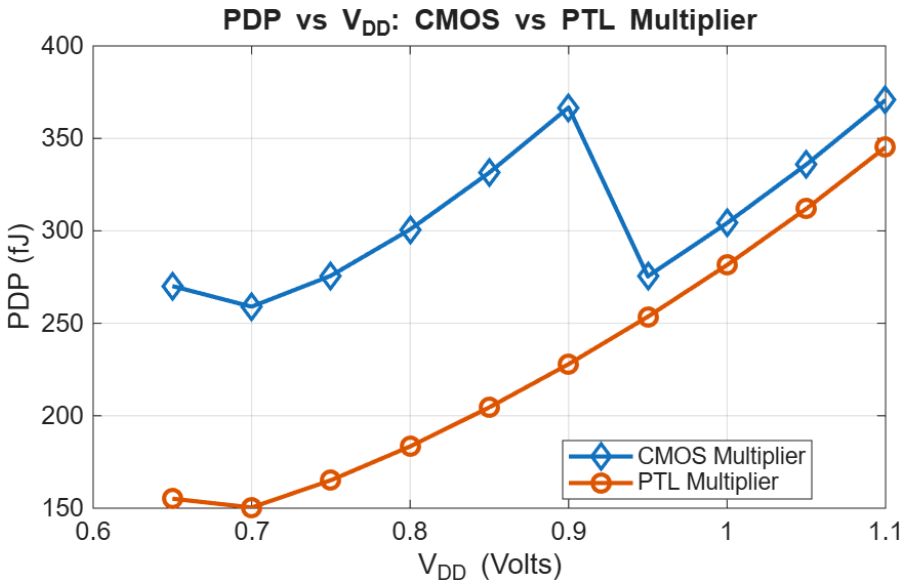

Figure 3.5: PDP vs VDD

Chapter 4

CONCLUSIONS

This project successfully demonstrates a hybrid PTL–CMOS Radix-4 Booth Multiplier that achieves:

Significant delay reduction (35.78%)

Lower power consumption (3.21%)

Substantial PDP improvement (37.84%)

Reduced transistor count (6.7%)

Multiplier	Technology (nm)	Frequency (MHz)	Supply Voltage (V)	Delay (ns)	Power (μW)	PDP (fJ)	Transistors
PTL	45	500	0.9	4.379	52.05	227.9269	2640
CMOS	45	500	0.9	6.819	53.78	366.7258	2830

Table 4.1: Comparison of PTL and CMOS Multipliers