Low-Power, High-Speed, and Area-Efficient Multiplier Based on the PTL Logic Style

Team Members:

V Thathrathrayan – MS2025018

Lekkala Shravan Kumar – MT2025511

Shivaranjini T P – MT2025523

Annapureddy Venkata Harsha Vardhan Reddy – MT2025506

Madineni Bhavya Sree – MT2025512

Radix 4 Booth Multiplier for 8 Bit Signed Multiplication

- Uses Booth encoding to speed up multiplication.
- Groups the multiplier bits in sets of 3.
- Each group generates one partial product -> 4 partial products in total.
- Partial products reduced by half compared to conventional multipliers.

Radix-4 Booth Encoding Table

3-bit Group (Xi+1 Xi Xi−1)	Operation
000	0 × M
001	+1 × M
010	+1 × M
011	+2 × M
100	−2 × M
101	−1 × M
110	−1 × M
111	0 × M

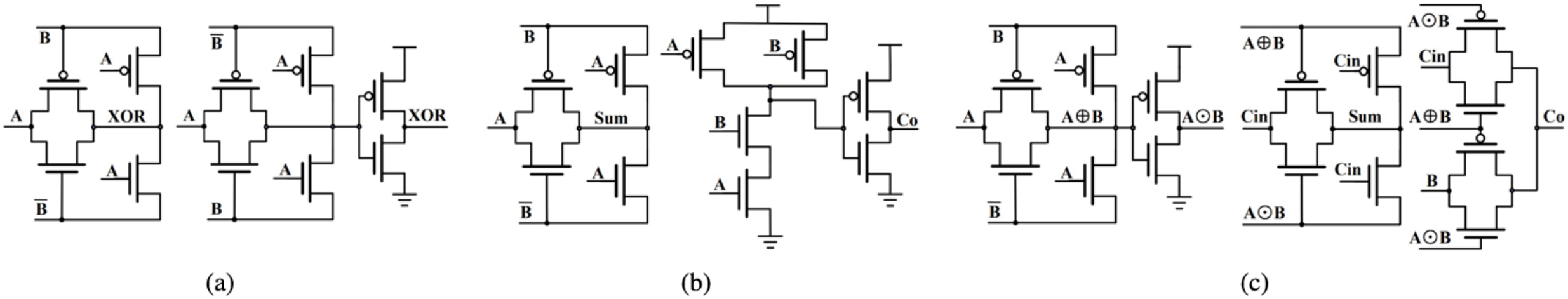
Advantages of Pass Transistor Logic (PTL) Over CMOS Logic

- **Reduced Transistor Count:**
PTL implements logic functions using fewer transistors than CMOS, resulting in smaller area and higher integration density.

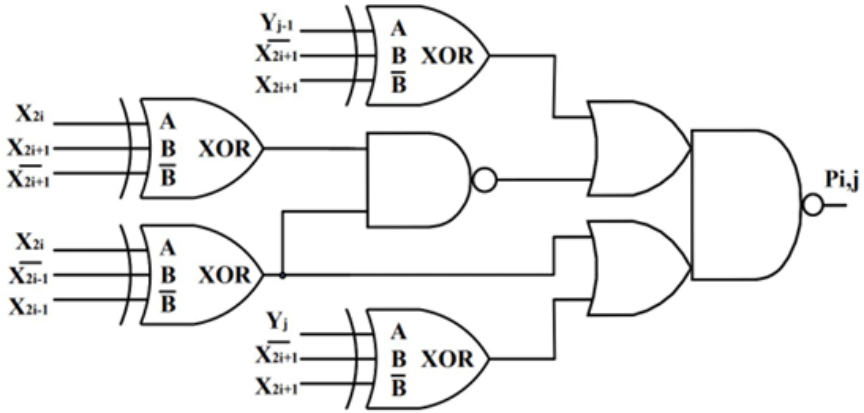
- **Lower Power Consumption:**
With fewer switching devices and reduced loading, PTL circuits dissipate less dynamic power compared to CMOS.

- **Higher Speed:**
PTL offers faster operation due to smaller capacitances, fewer stages, and reduced propagation delay.

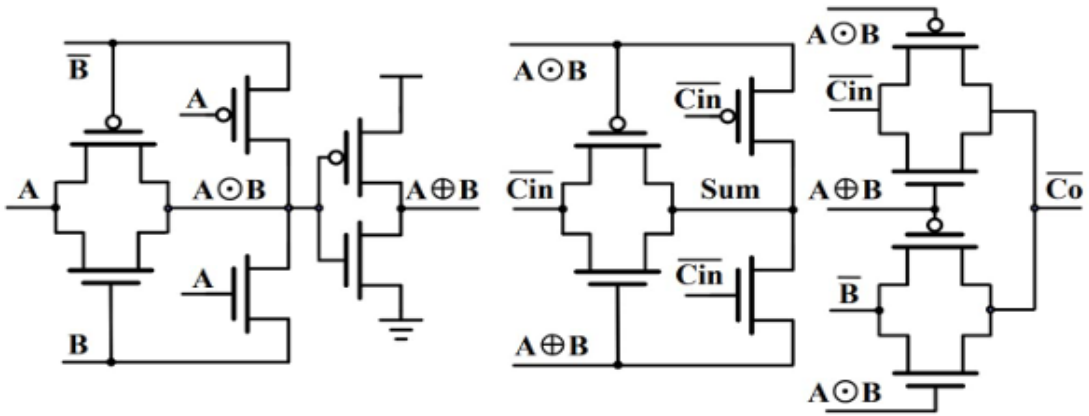
Schematics



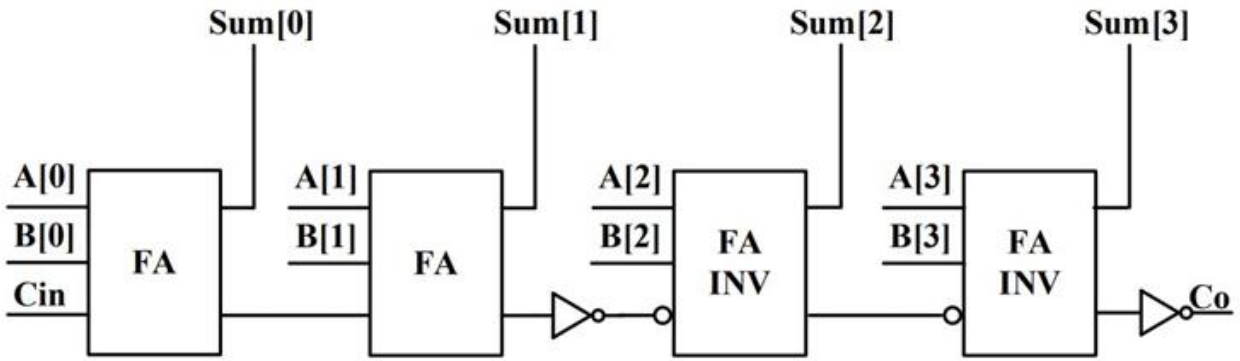
Cells designed by PTL logic style (a) 4/6-T XOR. (b) 12-T HA. (c) 16-T FA.



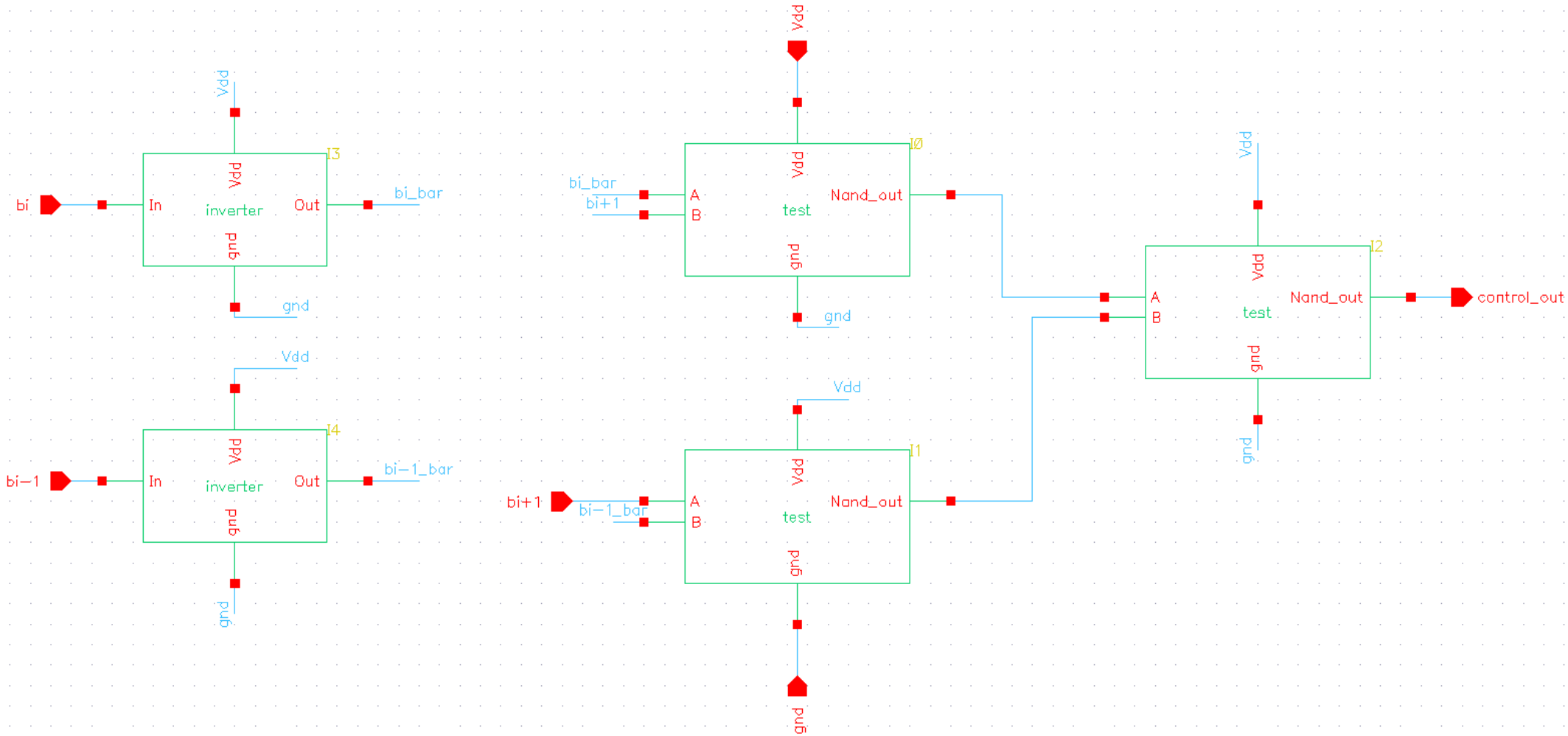
The structure of the Modified Booth Encoder



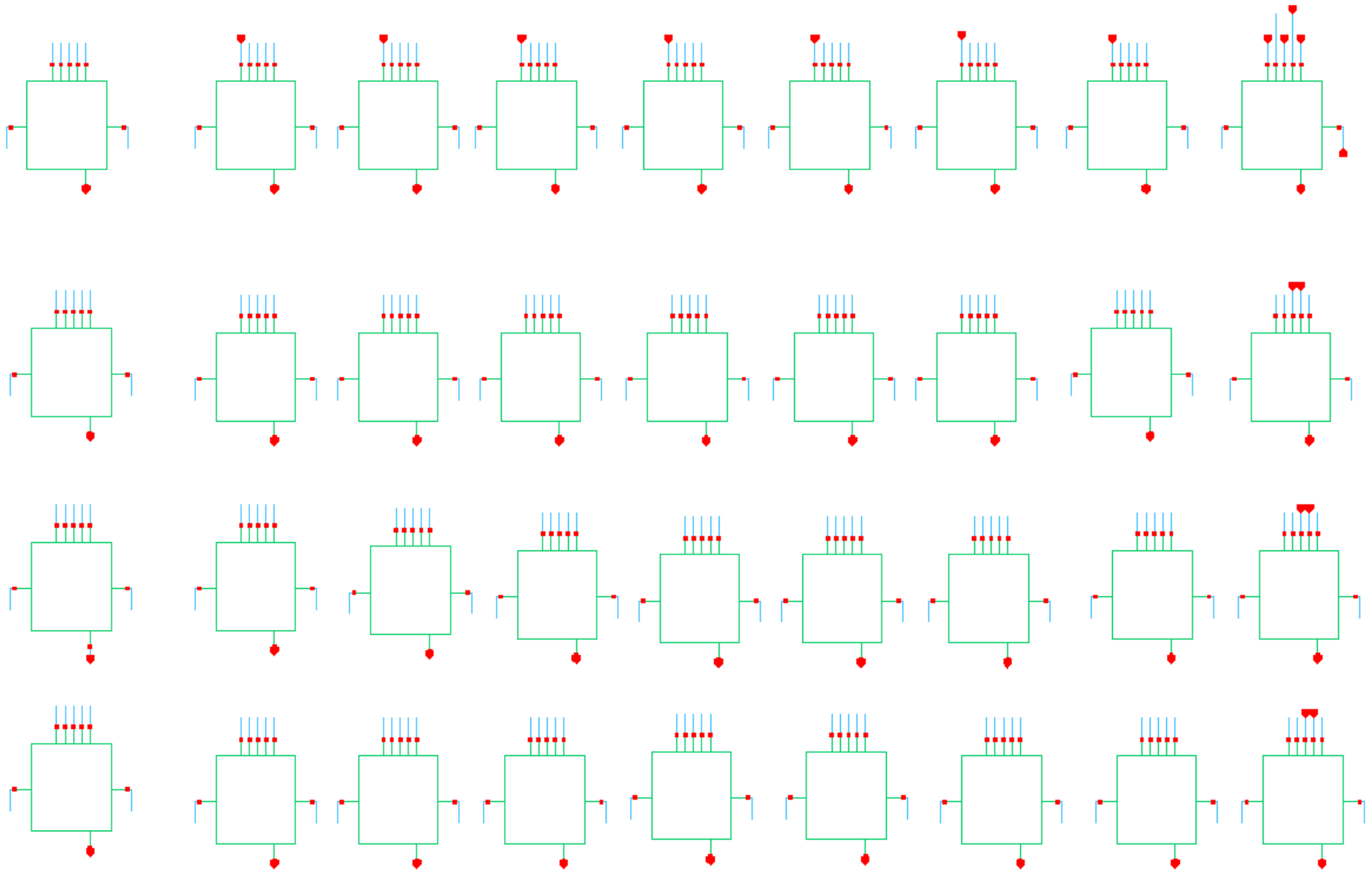
Proposed PTL 16-T FAINV circuit with inverted input Cin and inverted output Co.



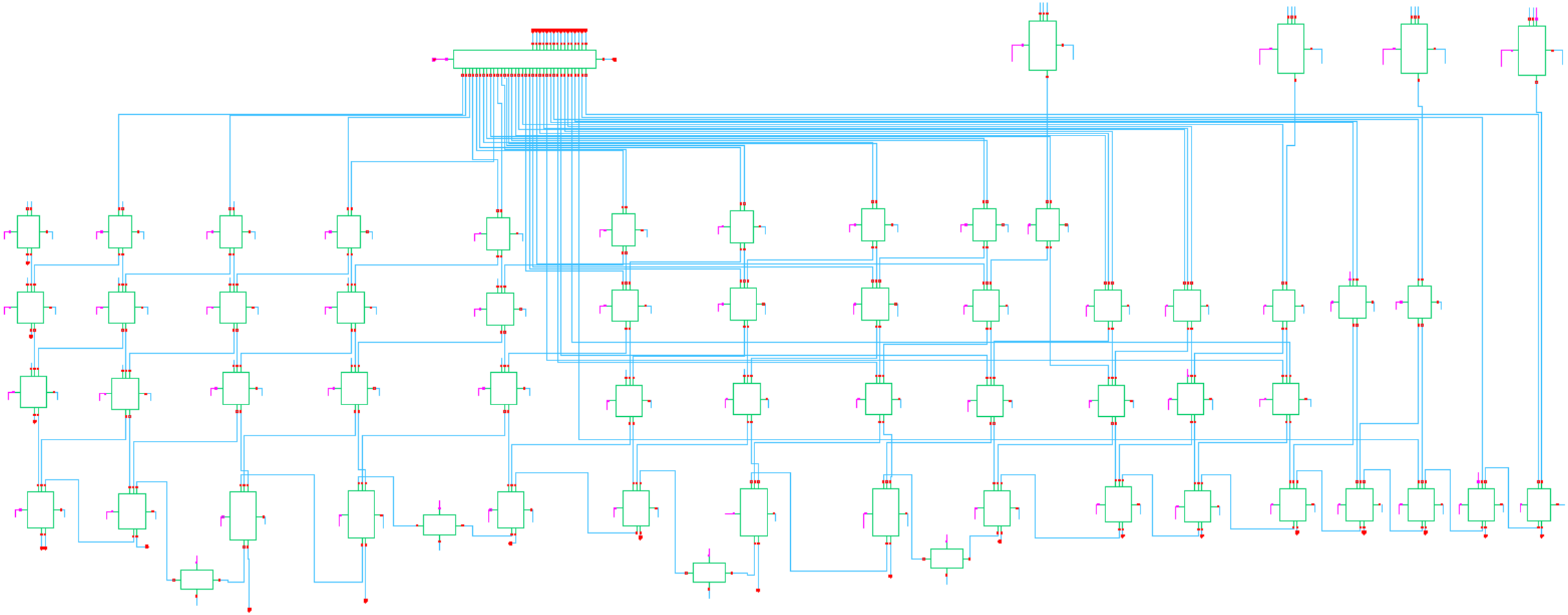
Proposed RCA circuit.



Control Logic



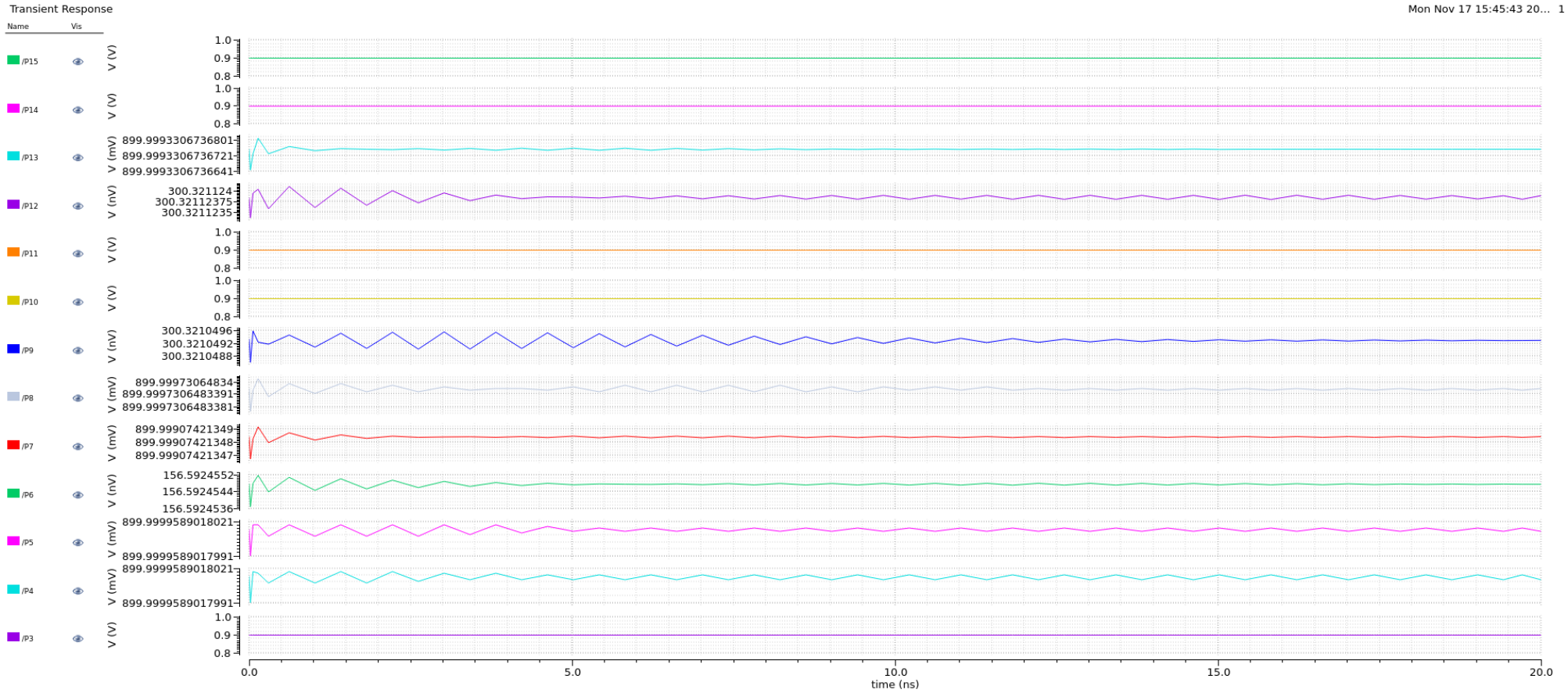
MBE Block

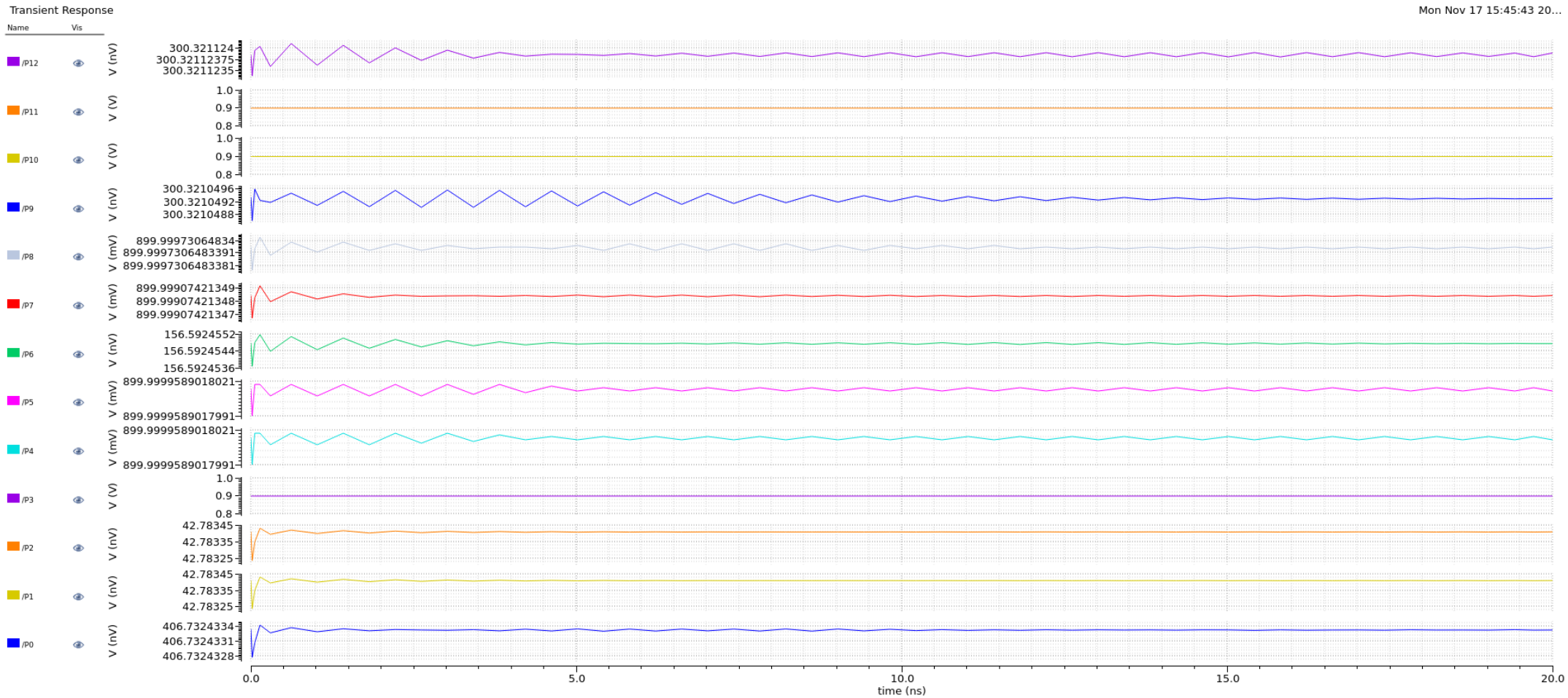


PTL Architecture

Simulation Results

Input we gave is 01110101 and 11011000.
The output we got is 1110110110111000.




Transient Response
Mon Nov 17 15:45:43 20... 1
Name
Vis
/P12
/P11
/P10
/P9
/P8
/P7
/P6
/P5
/P4
/P3
/P2
/P1
/P0
V (nV)
V (V)
V (mV)
300.321124
300.32112375
300.3211235
1.0
0.9
0.8
300.3210496
300.3210492
300.3210488
899.99973064834
899.9997306483391
899.9997306483381
899.99907421349
899.99907421348
899.99907421347
156.5924552
156.5924544
156.5924536
899.9999589018021
899.9999589017991
42.78345
42.78335
42.78325
406.7324334
406.7324331
406.7324328
0.0
5.0
10.0
15.0
20.0
time (ns)

Performance Comparison of CMOS and PTL Designs

Designs	Transistor Count	Delay(ps)	Power(uW)
CMOS FA	28	39.92	220.8
PTL FA	16	40.39	79.30
CMOS XOR	12	36.46	172.5
PTL XOR	4	20.68	35.52
CMOS HA	20	36.45	226.4
PTL HA	12	21.08	88.7

PTL cells require fewer transistors and consume less power compared to CMOS cells. However, the delay of a PTL-based full adder is higher than that of a CMOS full adder.

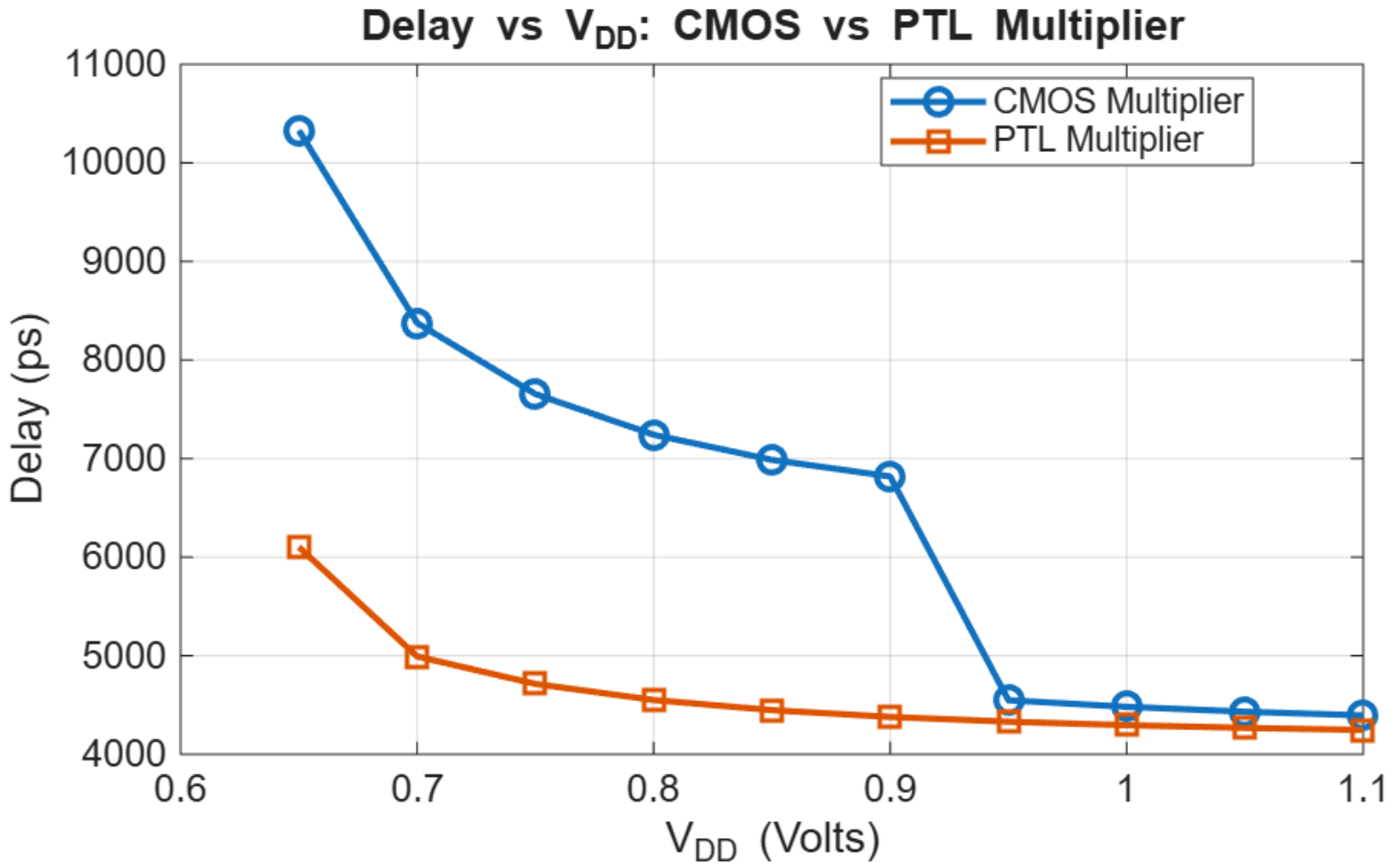
Comparison of Carry Propagation Delay

Delay(ps)	CMOS FA	PTL FA	Δ T
A=0, B=1, Cin ↑	61.32	18.68	42.64
A=0, B=1, Cin ↓	55.08	19.77	35.31
A=1, B=0, Cin ↑	56.50	18.68	37.82
A=1, B=0, Cin ↓	58.19	19.77	38.42
Average	56.7725	19.2075	38.5475

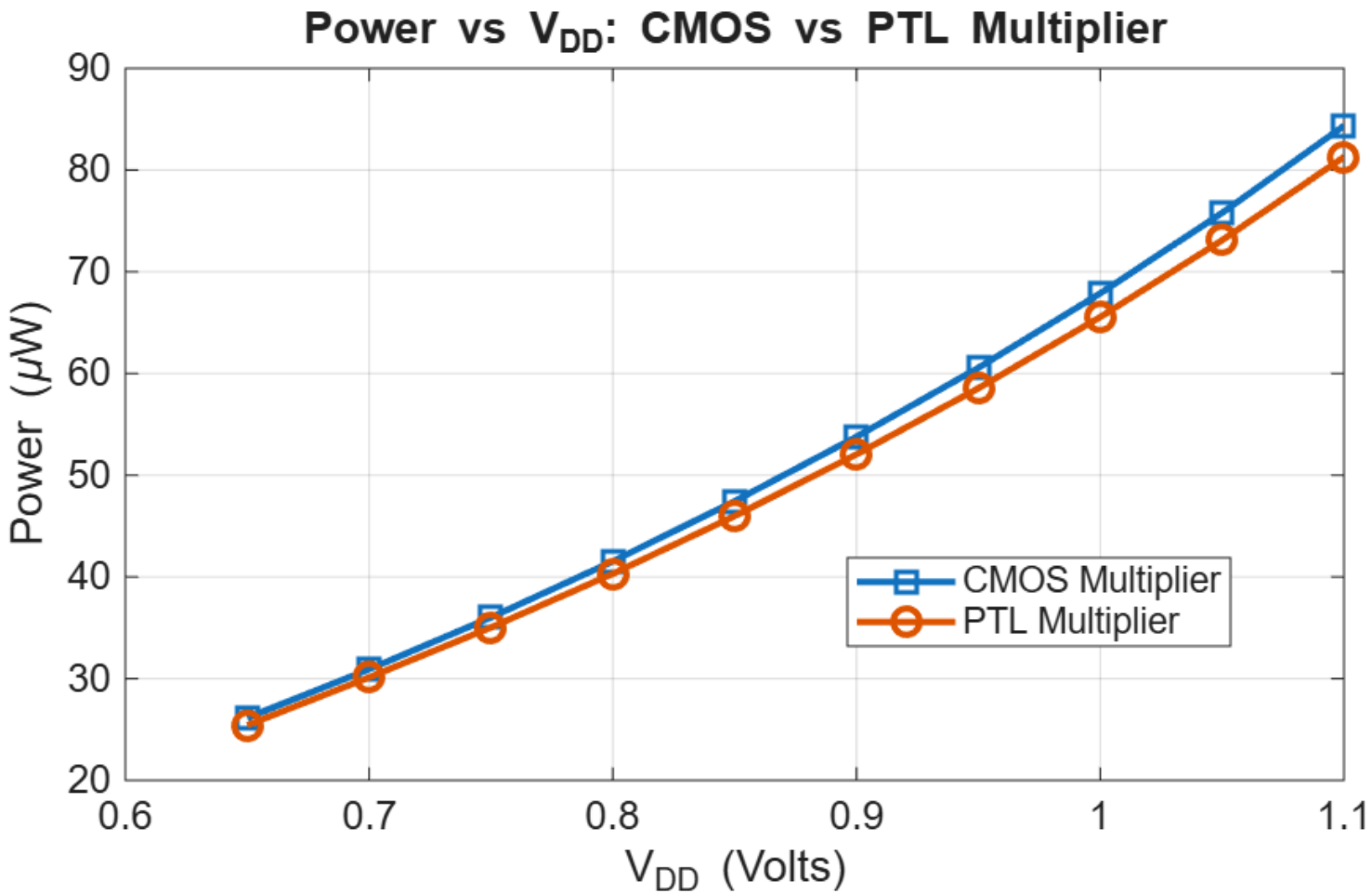
Compared to the CMOS full adder, the PTL full adder exhibits a lower carry propagation delay, which makes it suitable for use in our architecture.

Simulation Result of Multipliers

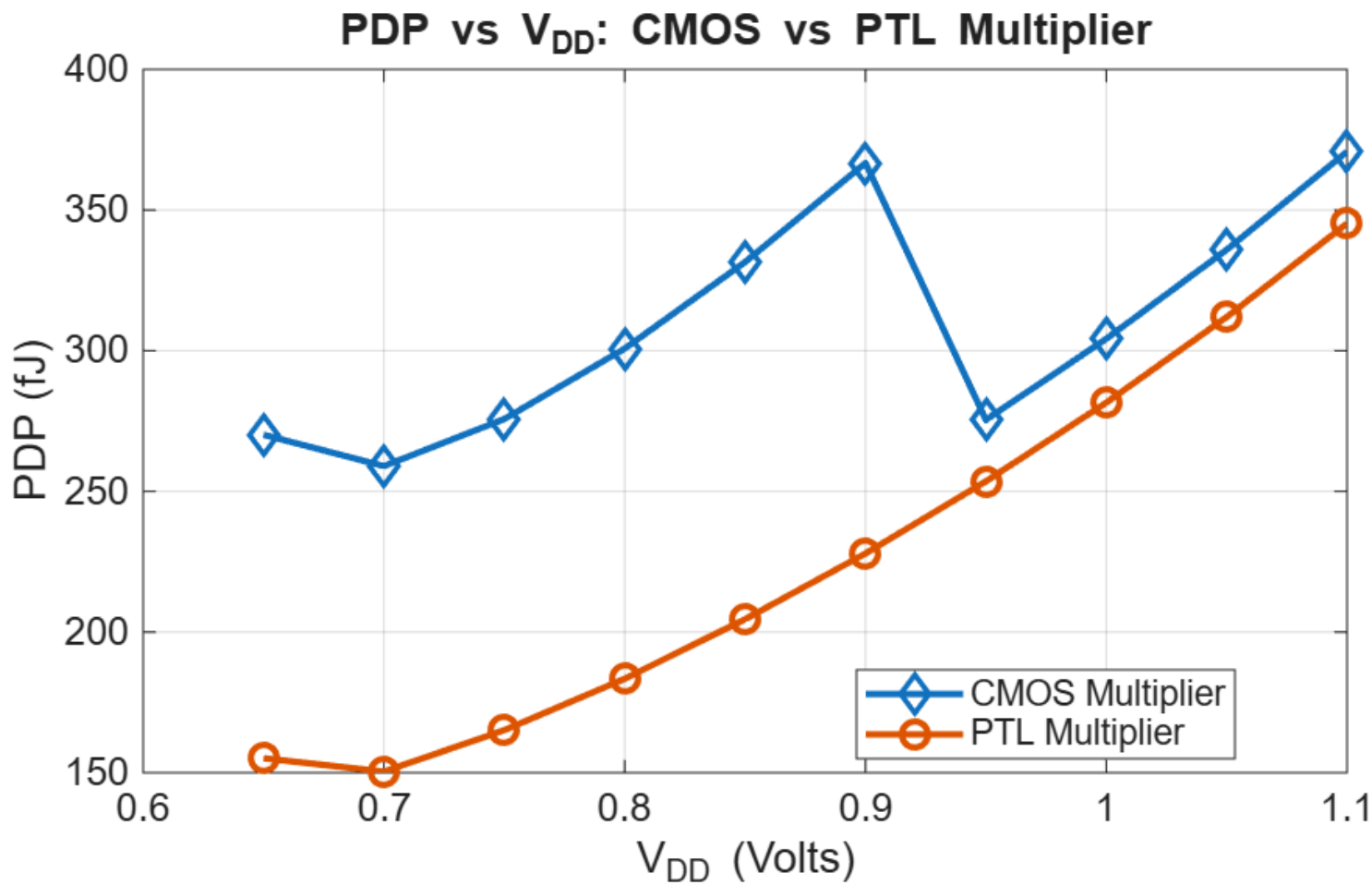
a) Delay Vs Vdd



b) Power Vs Vdd



c) PDP Vs Vdd


PDP vs V_{DD}: CMOS vs PTL Multiplier
PDP (fJ)
400
350
300
250
200
150
0.6
0.7
0.8
0.9
1
1.1
V_{DD} (Volts)
CMOS Multiplier
PTL Multiplier

Conclusion

Multiplier	Technology (nm)	Frequency (MHz)	Supply Voltage (V)	Delay (ns)	Power (uW)	PDP (fJ)	Number of Transistors
PTL	45	500	0.9	4.379	52.05	227.92695	2640
CMOS	45	500	0.9	6.819	53.78	366.72582	2830

Relative to CMOS logic, PTL logic provides a 3.21% decrease in power consumption, a 35.78% reduction in delay, and a 37.84% improvement in PDP.

THANK YOU