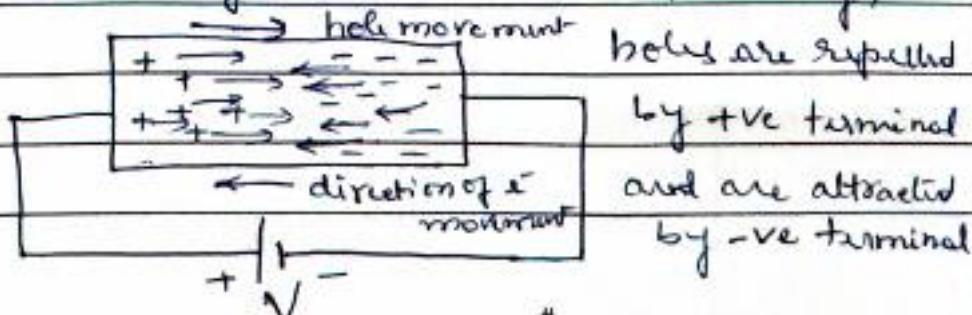


Physics of materials.

Materials can be classified into 3 types.

- * Conductors : are very good carriers of electricity.
- * They have large number of free electrons since there is no energy gap b/w conduction & valence band. Eg: copper, aluminium.
- * Insulators : Do not conduct electricity. There is a large energy gap b/w CB & VB. Hence it is impossible for electrons to move from VB to CB. eg: wood, glass. But it may conduct at very high temperature or when subjected to high external voltage.
- * Semiconductors: are neither insulators, nor conductors. Band gap b/w CB & VB is very narrow. It is 1 eV. Eg: Ge, Si. Conductivity lies b/w conductors & insulators. There are 2 types of semiconductors.
- * Intrinsic Semiconductors: Semiconductor in its purest form is intrinsic semiconductor. It behaves as an insulator at zero temperature. At room temperature, e^- -hole pairs are created due to the drift of e^- s to the conduction band. This creates a vacancy called as a hole. Holes are positively charged while e^- s are negatively charged.
- * When a battery is connected a/c intrinsic semiconductor, the e^- s are repelled by -ve terminal and are attracted by +ve terminal. Similarly,



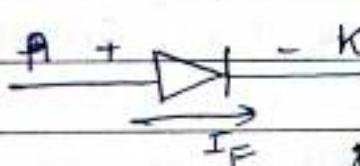
Thus, the movement of e^- in conduction band yields electron current and the movement of holes in valence band gives rise to a hole current.

- * Extrinsic semiconductors: are created by adding impurities (or other materials) to intrinsic semiconductors to improve conductivity or conduction nature of the materials.
 - used in diodes, transistors etc.
- * Depending upon type of impurities added, we have 2 types: p-type semiconductors & n-type.
- * p-type semiconductors are produced by doping intrinsic semiconductor with trivalent impurities also known as acceptor impurities (ions). In this holes are majority charge carriers & e^- are the minority carriers. Eg: Boron, Aluminium.
- * n-type semiconductors: are generated by doping intrinsic semiconductor with pentavalent impurities. Eg: Arsenic, phosphorous. These impurities are known as donor ions. In n-type semiconductors, e^- are majority charge carriers & holes are minority charge carriers.

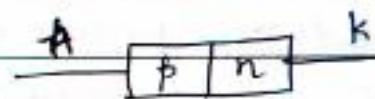
NOTE: Active components: Transform signals to another form & Eg: Transistors, MOSFETs, OPAMP, Gates (delivers E^2 P)

Passive components: Diodes, R, L, C → utilizes P or E from other sources.

- * n-type and p-type semiconductor materials are chemically combined with a special fabrication technique to form a p-n junction.
- * Such a p-n junction forms a popular electronic device called as p-n junction diode.
- * A diode is a basic element of no of electronic circuits.
- * p-n junction diode allows current flow when forward biased and blocks the current flow when reverse biased.
- * It is a uni-directional (one-way) device offering low-resistance when forward biased and behaving almost as open switch when reverse biased.



Device symbol



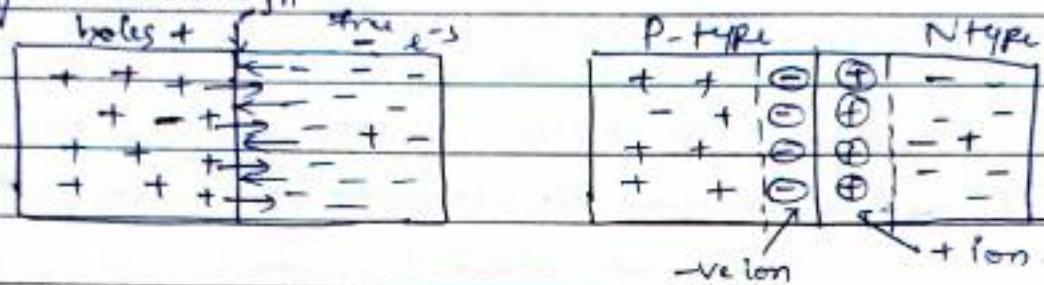
- * Arrow head indicates the conventional direction of current flow when the diode is forward biased.
- * Manufacturers provide datasheets that specifies the max forward current & reverse voltage for various types of diodes.
 - Some diodes are low current diodes (diodes) that are used in switching circuits. High current diodes are often used as rectifiers for ac to dc conversion.
 - Zener diodes are operated in reverse breakdown because they have a very stable breakdown voltage.
- * p-n junction diode can be destroyed if
 - a high forward current overheats the device.
 - if a large reverse voltage causes the junction breakdown.

- * Physically, large diodes pass largest currents & survive largest reverse voltages Date _____
 - * Small diodes are limited to low current levels and low reverse voltages.

Unbiased p-n junction diode (zero bias)

- * Unbiased p-n junction is the one where no external source is connected across the terminals of the device.

consider a zero bias p-n junction as shown in figure below.



- * At n-type semiconductor, large number of free e^- s are present while at p-type, small no. of free e^- s are present. Hence, the concentration of e^- s at n-type semiconductor is high, while the concentration of e^- s at p-type semiconductor is low.
 - * Due to this high concentration of e^- s at n-side, they get supplied from each other and hence try to move towards lower concentration region. Hence, the free e^- s from n-side are attracted towards the holes at p-side. Thus the free e^- s move from n-side (high concentration region) to p-side (low concentration region) (Drifting)
 - * At p-type semiconductor, large no. of holes are present while at n-type semiconductor, small number of holes are present. Hence, the concentration of holes at p-type semiconductor is high, while the concentration of holes at n-type semiconductor is low.

is low.

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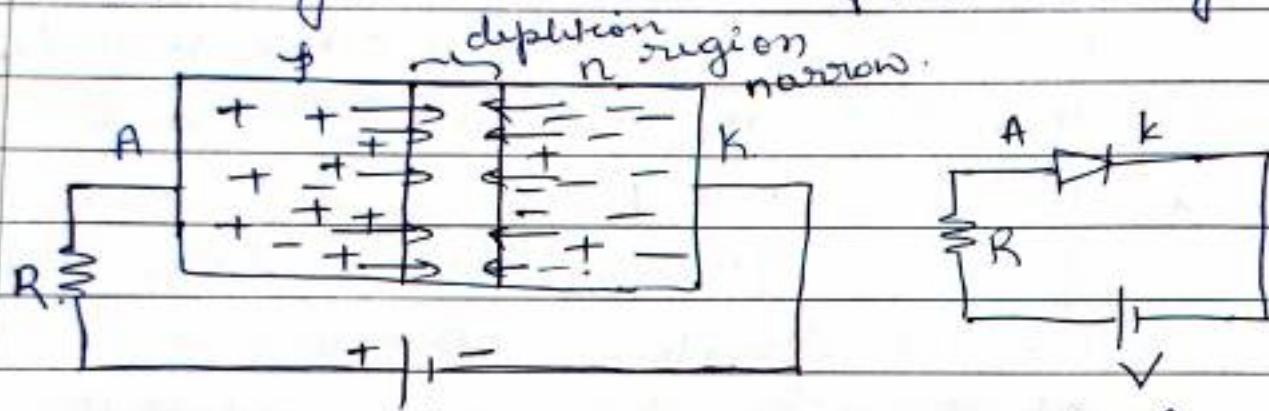
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- * Due to this high concentration of holes at p-side they get repelled and move towards lower concentration n-side. Hence, the holes from p-side are attracted towards the free e^{-s} at n-side. Thus, the holes move from p-side (high concentration) to n-side (low concentration).
- * The charge carriers cross the junction where, e^{-s} leave behind +ve charged donor ions N_D on n-side and holes leave behind -ve charged acceptor ions on p-side N_A. This process is diffusion.
- * Thus, the net positive charge at n-side prevents further flow of holes from p to n side. Similarly, the net negative charge at p-side prevents or repels the free e^{-s}.
- * Hence +ve charge present at n-side & -ve charge present at p-side of p-n junction acts as a barrier b/w p-type and n-type semiconductor.
- * Thus a barrier is built up near the junction which prevents the further movement of e^{-s} & holes. The total charge formed at the p-n junction is called barrier voltage, barrier potential or junction potential.
- * The size of the barrier voltage at the p-n junction depends on the amount of doping, junction temperature & type of material used. The barrier potential for Si diode is 0.7V & for Ge is 0.3V.

Biasing of a p-n junction diode

- * Applying an external voltage acr̄ the terminals of the p-n junction diode is known as biasing.
2 types : Forward biasing, Reverse biasing.
- * Forward biased p-n junction.

A diode is said to be forward biased when its anode is connected to the positive terminal of the battery and cathode is connected to the negative terminal of the battery.



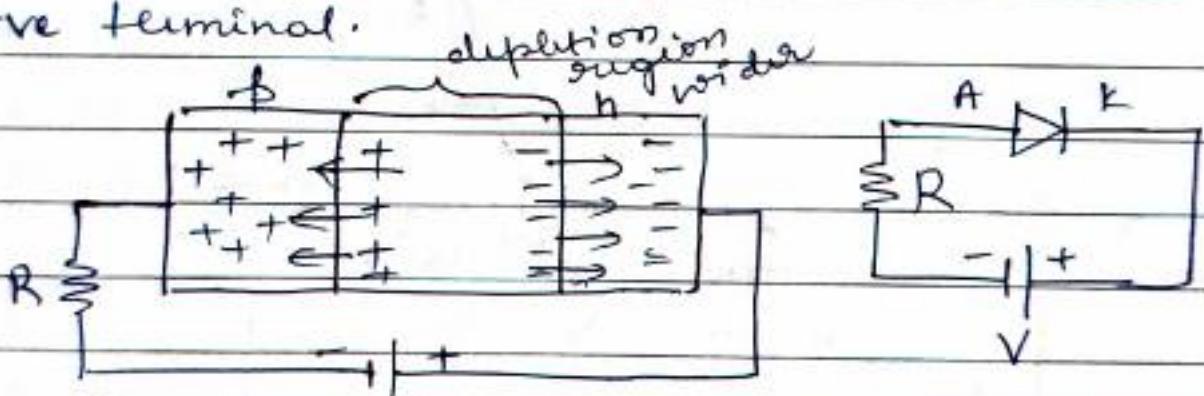
Forward biased p-n junction diode.

- * when the diode is forward biased, as long as the applied voltage V is less than the barrier potential, there cannot be any conduction.
- * when the applied voltage V becomes more than the barrier potential, the diode is forward biased, where holes (+ve) on p-side are repelled from +ve terminal of the battery and are driven towards the junction. Similarly e⁻s on n-side are repelled from -ve terminal of the battery towards the junction.

- * Due to this, the width of the depletion region (barrier potential) decreases.
- * As the biasing voltage is increased further, the depletion layer reduces until it disappears completely and allowing large number of charge carriers to flow across the junction resulting in exponential rise in current.
- * The voltage beyond which the current starts rising exponentially is known as knee voltage V_k or forward Voltage V_F = barrier potential.

* Reverse biased p-n junction.

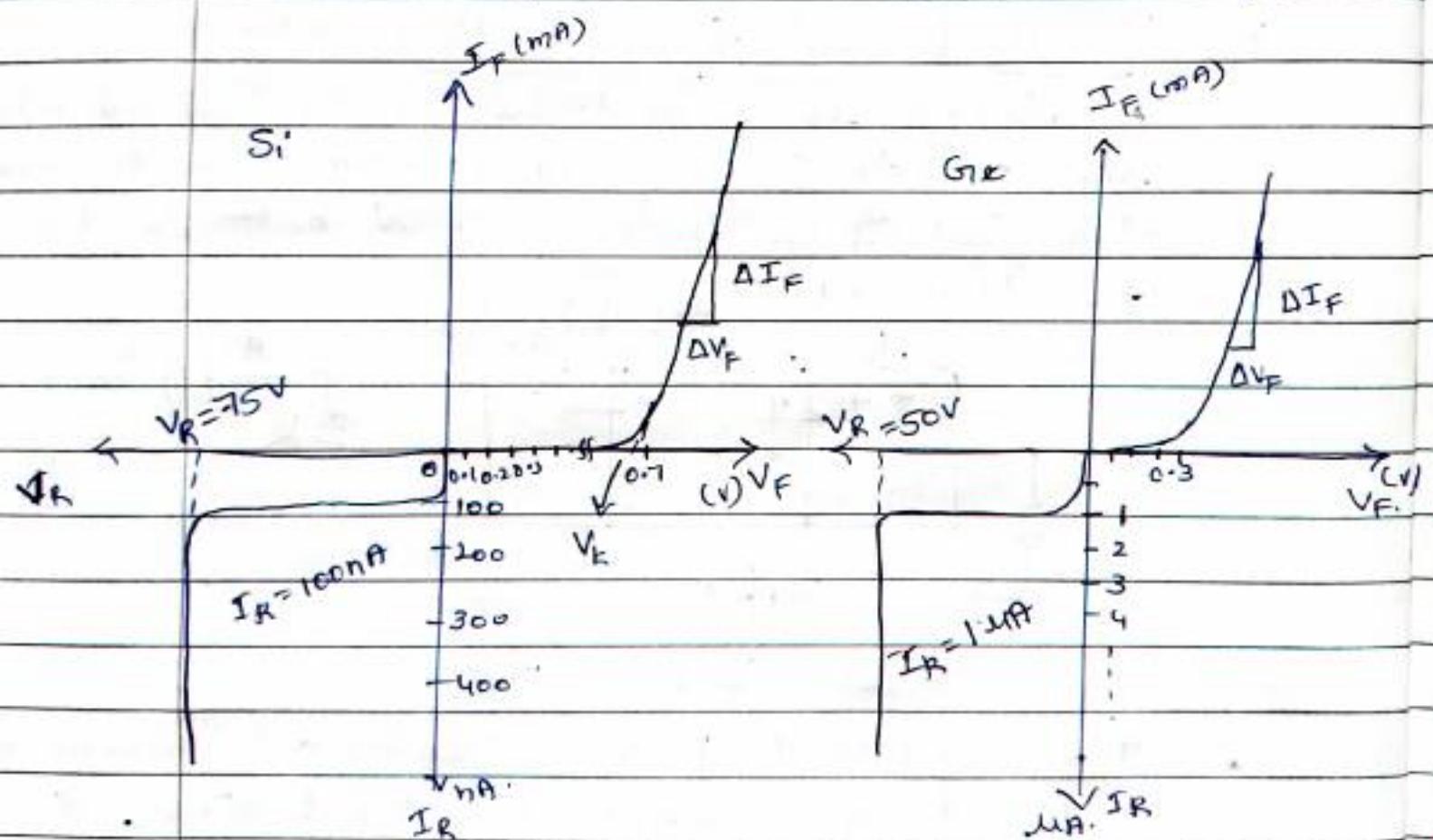
A diode is said to be reverse biased when the anode (p-region) is connected to -ve terminal of the battery and cathode to +ve terminal.



Reverse biased p-n junction.

- * The electrons from n region are attracted by towards +ve terminal of the battery & holes from p-side towards -ve terminal. This causes depletion region to be widened & barrier potential to be increased. Hence, this reduces majority charge carrier current flow across the junction. (zero)

- + Since there is only a very small reverse current, a reverse biased p-n junction can be said to have a high reverse resistance.
- * The minority charge carriers such as e^- on p-side and holes on n-side constitute a drift current flow that ~~stays~~ stays at saturation level I_s . I_s is known as reverse saturation current that is almost negligible. (nA for Si and mA for Ge diodes)
- * For a constant temperature, the reverse current is almost constant though reverse voltage is increased upto a certain limit. ~~If~~



VI characteristics of (Si) & (Ge) diodes.

when the diode reverse voltage (V_R) is sufficiently increased, the diode goes into breakdown. For Si it occurs at $75V + 6\Omega$ or at $50V$. Reverse breakdown can destroy a diode unless the current is limited by a suitable series resistor.

Pb. calculate the forward and reverse resistance offered by a Si diode at $I_F = 100mA + V_R = 75V$, $V_R = 50V + I_R = 100nA$.

Solu: At $I_F = 100mA$, for Si $V_F = 0.7V$

$$\text{forward resistance } R_F = \frac{V_F - 0.7}{I_F} = \frac{0.7}{100mA} = 7\Omega$$

At $V_R = 50V$, $I_R = 100nA$,

$$\text{reverse resistance } R_R = \frac{V_R}{I_R} = \frac{50V}{100nA} = 500M\Omega$$

At $V_R = 75V$, $I_R = 100nA$,

$$R_R = \frac{75V}{100nA} = 750M\Omega$$

Diode Parameters:

1. Forward voltage drop: (V_F or V_k)

The voltage drop across the diode in forward bias condition is known as forward voltage drop.

It is represented as V_F + is generally equal to the knee voltage V_k . ($0.7V$ for Si & $0.3V$ for Ge)

2. Maximum forward current: (I_{Fmax})

It is the maximum current a diode can pass under forward bias condition, without permanent damage to the p-n-j-n due to overheating.

3. Reverse breakdown voltage : (V_{BR})

It is the reverse bias voltage at which the p-n junction breaks down and permanently damages the diode. (V_g beyond which there is a sharp increase in current)

Note: Diodes which can recover after such breakdown are called as zener diodes, which finds application as voltage regulators

4. Reverse saturation current (I_s):

The current that exists when diode is in reverse bias is known as reverse saturation current. ($Ge - 1\text{A}, Si - 1\text{nA}$)

5. Dynamic resistance (r_d):

It is the resistance offered by the diode to changing voltages in forward bias condition.

It is also known as incremental resistance or ac resistance. It is given by

$$r_d = \frac{\Delta V_F}{\Delta I_F} \quad \text{From the graph}$$

$$\text{Slope} = \frac{\Delta I_F}{\Delta V_F}$$

$$\therefore r_d = \frac{1}{\text{Slope}}$$

6. Forward resistance (R_F):

It is the ratio of voltage to current at the diode in forward biased condition. It is known as static resistance. It is a constant dc resistance at a constant forward current.

$$R_F = \frac{V_F}{I_F}$$

7. Reverse resistance (R_R):

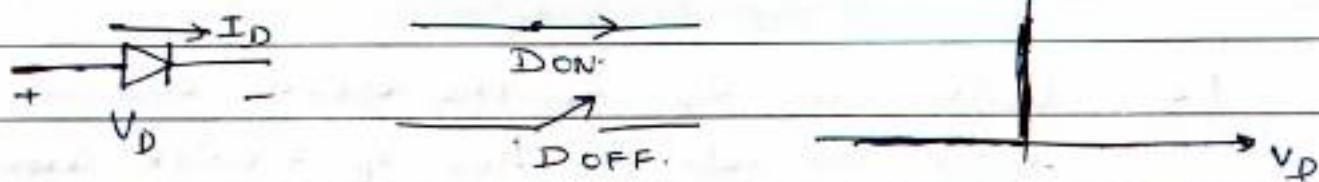
It is the ratio of voltage to current a/c the diode in reverse biased state. It is also known as static reverse resistance.

$$R_R = \frac{V_R}{I_R}$$

Diode Models-

DC equivalent circuits: An equivalent circuit for a device is a circuit that represents the circuit behavior. The circuit is made up of no. of components such as resistors and voltage cells.

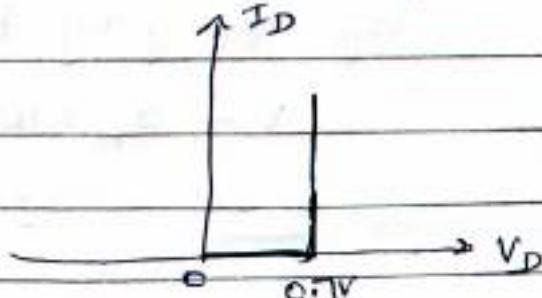
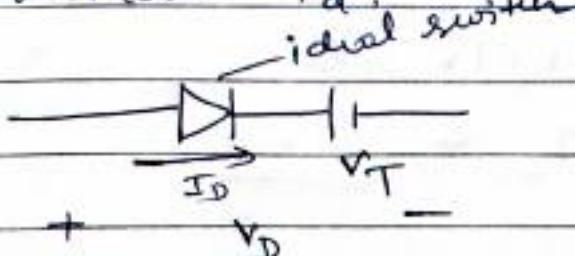
* Ideal diode model



* An ideal diode would have zero forward voltage drop & zero forward resistance. It would also have infinitely high reverse resistance which would result in zero reverse current ie $V_F = 0$, $R_F = 0$, $R_R = \infty$, $I_R = 0$.

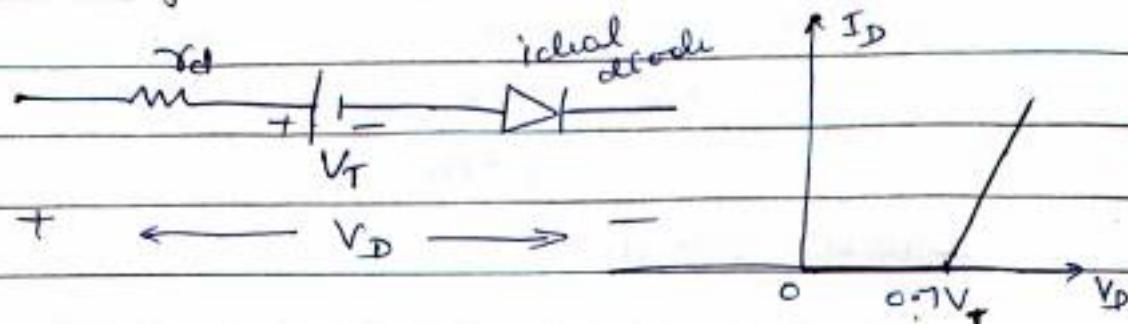
* Approximate model:

An approximate model of a diode consists of an ideal diode switch with a voltage cell V_T without V_d .



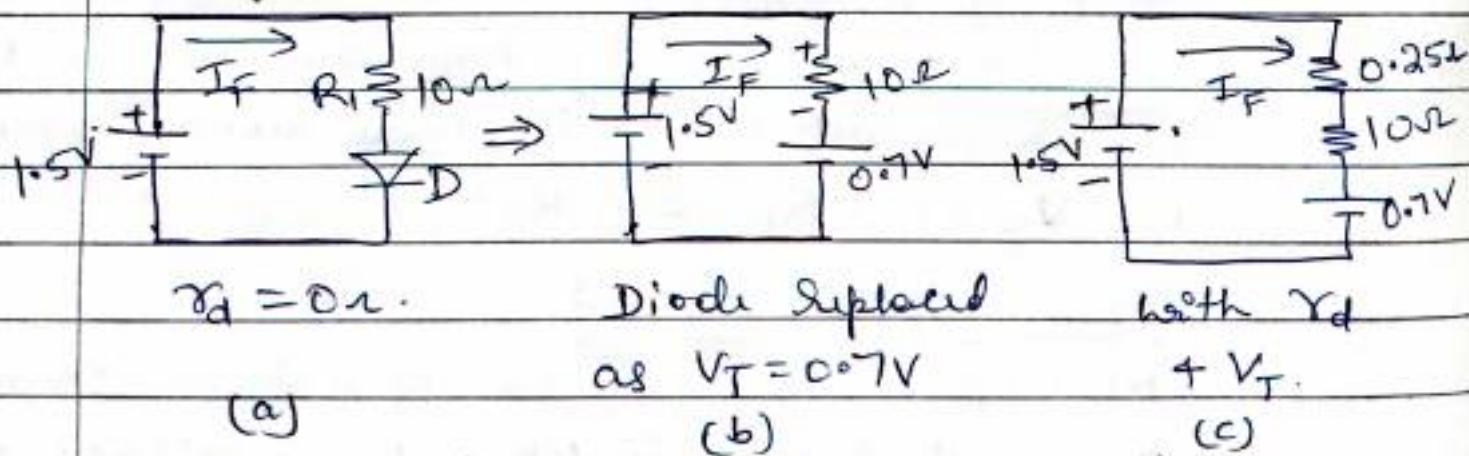
Piecewise linear model:

It consists of an ideal diode, an voltage cell and a dynamic resistance r_d in series.



* When the forward characteristics of the diode is not available, the straight line approximation of the forward characteristics of a diode can be employed and it is called as piecewise linear characteristics.

Pb. Calculate I_F for the diode circuit assuming that the diode has $V_F = 0.7V$ and $r_d = 0$
Reqd. current by taking $r_d = 0.25\Omega$



By applying KVL to (b),

$$V - I_F \times 10\Omega - 0.7V = 0.$$

$$\frac{1.5V - 0.7V}{10\Omega} = I_F = \underline{\underline{80mA}}.$$

Applying KVL to (c)

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$$V - I_F R_1 - I_F \times 0.7 V = 0$$

$$\frac{1.5 - 0.7}{(0.25 + 10)} = I_F = \underline{\underline{78 \text{ mA}}}$$

Reduction in diode current as resistance increases.

Diode Rectifiers

- * One of the most important applications of a p-n junction diode is in rectification.
- * Rectification is a process of converting alternating current into direct current (a.c to d.c)
- * Rectification may be performed by using a half wave or a full wave rectifier circuits (2 diodes, 4 diodes)
- * Depending on the type of alternating current supply (a.c) and the arrangement of the rectifier circuit, the output voltage may require additional smoothing to produce a uniform steady voltage. i.e. the o/p of the rectifier circuit contains a.c ripples along with dc components. (pulsating d.c)
- * Many applications of rectifiers such as power supplies for radio, television and computer equipments require a steady constant DC voltage.
- * In these applications, the o/p of the rectifier is smoothed by an electronic filter circuit. It comprises of capacitor, choke or a combination of capacitors, chokes + a resistor to reduce the a.c ripples and generate a pure dc o/p v.g.

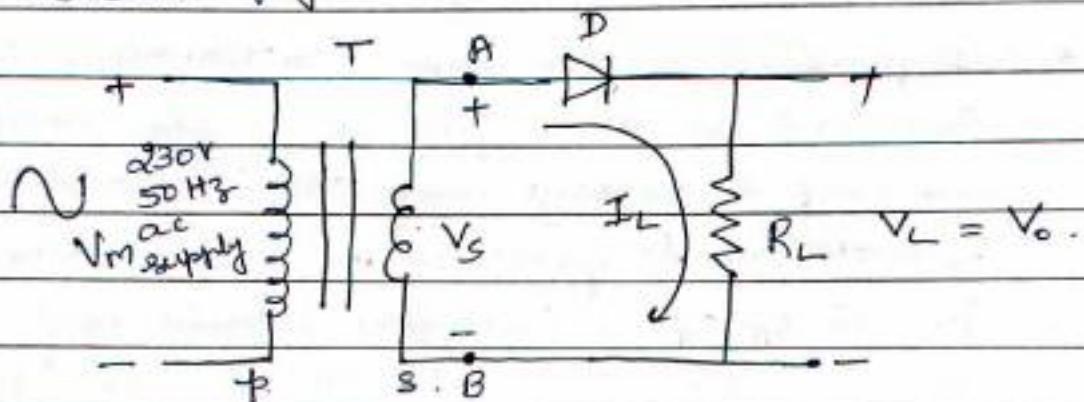
The filtering process involves the use of a large capacitor which charges to the peak i/p voltage level to produce the dc o/p voltage.

It can be RC filters or LC filters

Half wave Rectifier

Half wave rectifier requires only one diode for the construction of the circuit. In HWR, the rectifying element conducts only during +ve half cycle of i/p ac supply. The -ve half cycle of ac i/p supply are eliminated from the o/p.

Circuit fig:



* Working :

During positive half cycle of the i/p ac signal b/w $0 \leq \omega t \leq \pi$, at the secondary of the transformer node A is +ve compared to node B. Hence the diode D is forward biased and acts as a closed switch. The current flows through the load resistor R_L causing a potential to appear across it. Since the load is resistive, current w/f exactly follows the voltage waveform.

* The load current is given by

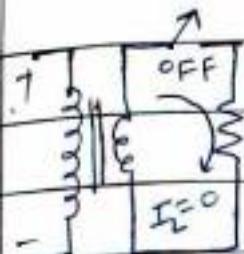
$$I_L = I_m \sin \omega t \quad 0 \leq \omega t \leq \pi$$

where $I_m = \frac{V_m}{R_s + R_f + R_L}$ is the peak value of the current.

* The o/p voltage obtained is a pulsating dc.

It is discontinuous. Hence we take the average or dc value of current or voltage by integrating one full cycle.

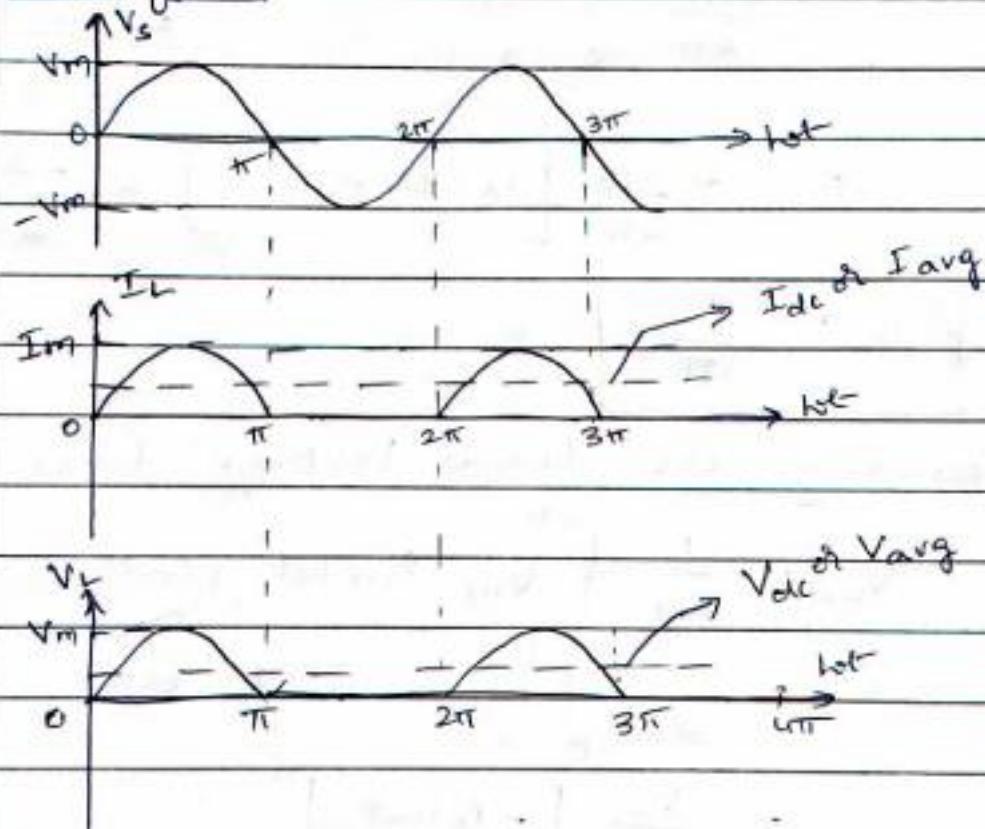
- * During -ve half cycle of the ac i/p signal, ie $\pi \leq wt \leq 2\pi$, A is -ve and mode B is +ve.



Hence diode D is reverse biased and acts as an open switch. There is no current flow through the load and hence o/p voltage is zero.

$$\therefore I_L = 0; \quad \pi \leq wt \leq 2\pi$$

Waveforms.



Parameters.

- i) Average dc load current : (I_{dc} or I_{avg})

The average value of an alternating current is the area under the curve of load current from 0 to 2π and then dividing it by the base ie 2π .

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_L \sin \omega t \, dt.$$

$$= \frac{1}{2\pi} \int_0^{2\pi} I_m \sin \omega t \, dt.$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t \, dt + \int_{\pi}^{2\pi} I_m \sin \omega t \, dt \right].$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t \, dt \right] \quad \because I_L = 0 \\ \text{from } \pi \rightarrow 2\pi$$

$$= \frac{I_m}{2\pi} \int_0^{\pi} \sin \omega t \, dt.$$

$$= \frac{I_m}{2\pi} \left[-\cos \omega t \Big|_0^{\pi} \right]$$

$$= -\frac{I_m}{2\pi} [\cos \pi - \cos 0] = -\frac{I_m}{2\pi} [-1 - 1]$$

$I_{dc} = \frac{I_m}{\pi}$

2. Average dc load voltage: (V_{dc})

$$V_{dc} = \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t \, dt.$$

$$= \frac{1}{2\pi} \int_0^{\pi} V_m \sin \omega t \, dt \quad \because V_L = 0 \\ \text{from } \pi \rightarrow 2\pi$$

$$= \frac{V_m}{2\pi} \left[-\cos \omega t \Big|_0^{\pi} \right]$$

$$= -\frac{V_m}{2\pi} [\cos \pi - \cos 0] = -\frac{V_m}{2\pi} [-1 - 1]$$

$V_{dc} = \frac{V_m}{\pi}$

$$= -\frac{V_m}{2\pi} [-2]$$

OR: It is the product of dc load current I_{dc} and load resistance R_L .

$$V_{dc} = I_{dc} \times R_L$$

$$= \frac{I_m}{\pi} R_L = \frac{V_m}{\pi (R_L + R_s + R_f)} \cdot R_L$$

$$= \frac{V_m}{\pi \left(1 + \frac{R_s + R_f}{R_L} \right)}$$

R_s : transformer secondary resistance
 R_f : diode forward resistance

But $R_s + R_f$ are small compared to R_L , $R_s + R_f \ll R_L$

$$\Rightarrow \frac{R_s + R_f}{R_L} \ll 1$$

$$\therefore V_{dc} = \frac{V_m}{\pi}$$

3. RMS value of load current: (I_{rms})

RMS means squaring, finding mean and then finding square root. RMS value of load current is obtained as

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_L^2 dt} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} I_L^2 dt}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t dt}$$

$$\because I_L = 0$$

$$b) \omega \pi \text{ to } 2\pi$$

$$= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \sin^2 \omega t dt} = \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} [1 - \cos 2\omega t] dt}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \int_0^{\pi} [1 - \cos 2\omega t] dt}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \Big|_0^\pi \right]}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \left[(\pi - 0) - \left(\frac{\sin 2\pi}{2} - 0 \right) \right]}$$

$$= \sqrt{\frac{I_m^2}{4\pi}} (\pi) = \frac{I_m}{2}$$

4.

RMS value of load voltage: V_{rms}

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$$V_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} V_L^2 dt} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} V_m^2 \sin^2 \omega t dt}$$

Ans:
$$V_{rms} = \frac{V_m}{2}$$

↓ simplify

OR

$$V_{rms} = I_{rms} \times R_L$$

$$= \frac{I_m}{2} \times R_L = \frac{V_m}{2(R_L + R_s + R_f)} \cdot R_L$$

$$V_{rms} = \frac{V_m}{2 \left(1 + \frac{R_s + R_f}{R_L} \right)}$$

Since $R_s + R_f \ll R_L$
 $\frac{R_s + R_f}{R_L} \ll 1$.

∴
$$V_{rms} = \frac{V_m}{2}$$

5. Ripple factor (γ):

It is defined as the ratio of RMS value of ac component to dc component present at the o/p.

$$\gamma = \frac{I_{ac}}{I_{dc}} = \frac{\text{RMS value of ac component of o/p}}{\text{dc component of o/p}}$$

here

I_{rms} is the total current of the rectifier.

$$I_{rms}^2 = I_{ac}^2 + I_{dc}^2$$

$$\text{or } I_{ac}^2 = I_{rms}^2 - I_{dc}^2$$

$$\gamma = \frac{I_{ac}}{I_{dc}} = \sqrt{\frac{I_{ac}^2}{I_{dc}^2}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$\gamma = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\frac{I_m^2/4}{I_m^2/\pi} - 1} = \sqrt{\frac{k_1}{1/\pi^2} - 1}$$

$\gamma = 1.21 \text{ or}$
 $\therefore \gamma = 121\%$

* Ripple content in the o/p is 121% of the dc component.

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- * This indicates $I_{ac} > I_{dc}$, hence poor rectification
- * Smaller the ripple factor, closer the o/p to dc.

6. Efficiency (η)

It is defined as the ratio of o/p dc power to the i/p ac power supplied to the rectifier

$$\begin{aligned}\eta &= \frac{o/p \text{ dc power}}{i/p \text{ ac power}} = \frac{P_{dc}}{P_{ac}} \\ &= \frac{I_{dc} R_L}{I_{rms} (R_s + R_f + R_L)} \\ &= \frac{(I_m/\pi)^2}{(I_m/2)^2} \frac{1}{\left(1 + \frac{R_s + R_f}{R_L}\right)}, \quad \frac{R_s + R_f}{R_L} \ll 1 \\ &= \frac{\cancel{\pi^2} \times 4}{\cancel{\pi^2} \cancel{D_o^2}} = \frac{4}{\pi^2} = 0.406\end{aligned}$$

$$\boxed{\% \eta = 40.6 \%}$$

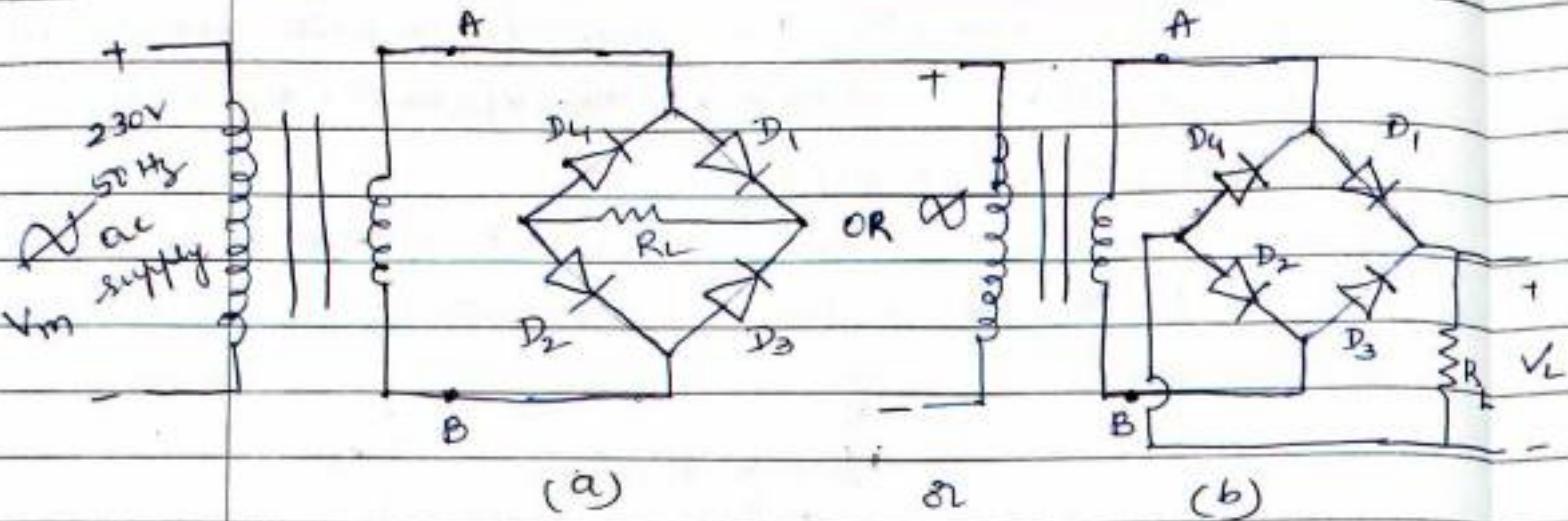
Hence in HWR, ripple contents are more therefore efficiency is less.

Full Wave Bridge Rectifier

- * It is a FWR circuit with 4 diodes - that avoids a centre tapped transformer which is present in FWR with 2 diodes
- * To one diagonal of the bridge a.c voltage applied through transformer and the rectified dc o/p voltage is taken from the other diagonal of the bridge.

circuit diagram (Any one)

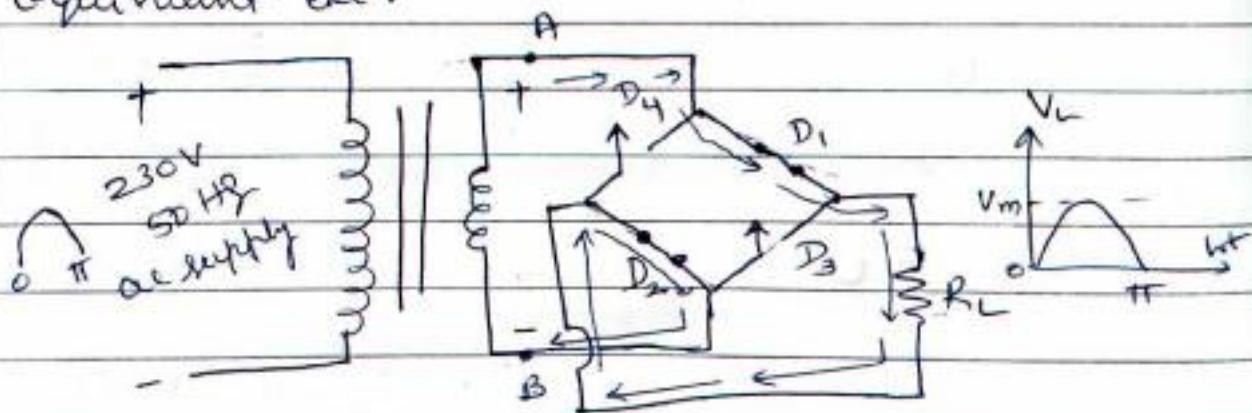
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Working:

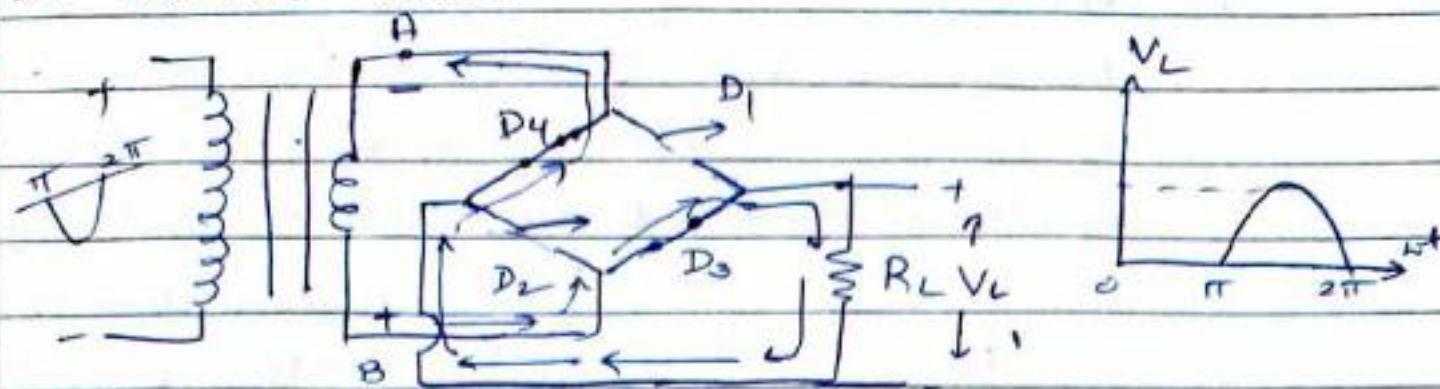
- * During +ve half cycle of ac i/p signal, node A at secondary is +ve while node B is -ve. Hence diodes D₁ and D₂ will be forward biased and D₃ & D₄ will be reverse biased. The diodes D₁ & D₂ are connected in series with the load R_L. The direction of current flow is shown in fig below.

Equivalent ckt:



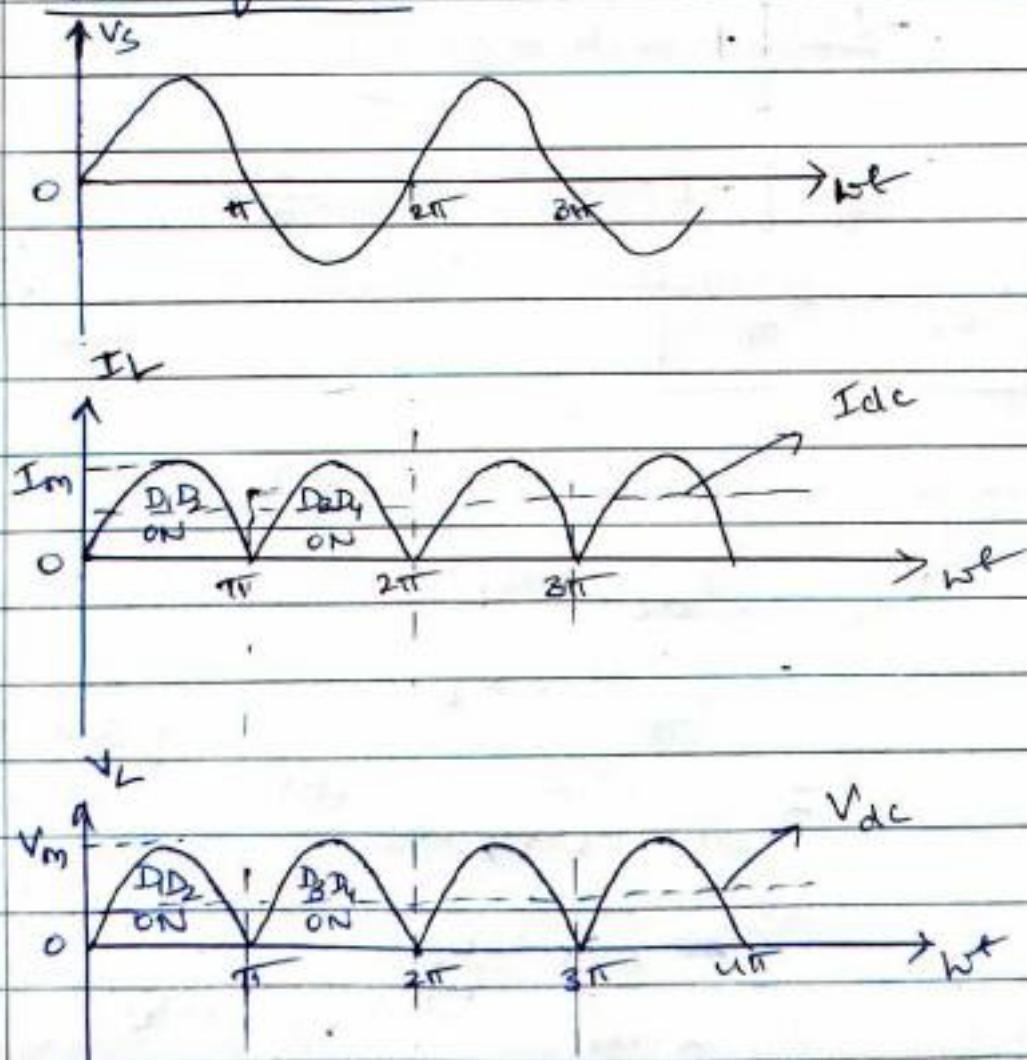
- * During -ve half cycle of ac i/p signal, node A is -ve at secondary, while node B is +ve. Hence Diodes D₃ & D₄ will be forward biased and D₁ & D₂ will be reverse biased.

The diodes D_3 & D_4 are connected in series with the load R_L . The direction of current flow is shown below.



In FWR, load current flows in both half cycles of ac voltage and in the same direction through the load resistance. Hence the negative half cycle of i/p also appears above the axis in the o/p w/f.

Waveforms



Parameters:1. Average value of load current (I_{dc})

The average value of current during one full cycle of ac i/p is given by area under the curve of load current I_L for one full cycle.

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_L dt$$

Since the w/f repeats itself for every π we can rewrite I_{dc} as

$$I_{dc} = \frac{1}{2\pi} \times 2 \int_0^{\pi} I_L dt = \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t dt$$

$$= \frac{I_m}{\pi} \left[\int_0^{\pi} \sin \omega t dt \right] = \frac{I_m}{\pi} \left[-\cos \omega t \Big|_0^{\pi} \right]$$

$$= -\frac{I_m}{\pi} [+\cos \pi - \cos 0]$$

$$= \frac{I_m}{\pi} [-1 - 1] = \frac{2I_m}{\pi}$$

$$\therefore I_{dc} = \boxed{\frac{2I_m}{\pi}}$$

2. Average dc load voltage (V_{dc})

$$V_{dc} = I_{dc} \times R_L$$

$$= \frac{2I_m}{\pi} \times R_L$$

$$= \frac{2}{\pi} \frac{V_m}{R_L + 2R_f + R_s} R_L$$

$$= \frac{2}{\pi} \frac{V_m}{\left(1 + \frac{R_f + R_s}{R_L}\right)}$$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}}$$

(2 diodes conduct at a time for half cycle $\therefore 2R_f$)

$$\therefore \frac{R_f + R_s}{R_L} \ll 1$$

3. RMS value of load current (I_{rms}) PNB

$$\begin{aligned}
 I_{rms} &= \sqrt{\frac{1}{\pi} \int_0^{\pi} I_L^2 dt} \\
 &= \sqrt{\frac{1}{\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t dt} \\
 &= \sqrt{\frac{I_m^2}{\pi} \int_0^{\pi} \left[1 - \frac{\cos 2\omega t}{2} \right] dt} \\
 &= \sqrt{\frac{I_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_0^{\pi}} \\
 &= \sqrt{\frac{I_m^2}{2\pi} \left[(\pi - 0) - \frac{1}{2} (\sin 2\pi - 0) \right]} \\
 &= \sqrt{\frac{I_m^2}{2}} = \frac{I_m}{\sqrt{2}} \\
 \therefore I_{rms} &= \frac{I_m}{\sqrt{2}}
 \end{aligned}$$

4) RMS value of load voltage. V_{rms} .

$$V_{rms} = I_{rms} \times R_L$$

$$= \frac{I_m}{\sqrt{2}} \times R_L = \frac{V_m}{\sqrt{2}(R_s + 2R_f + R_L)} R_L$$

$$= \frac{V_m}{\sqrt{2} \left(1 + \frac{R_s + 2R_f}{R_L} \right)} \quad ; \quad \frac{R_s + 2R_f}{R_L} \ll 1.$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad ; \quad R_s + 2R_f \ll R_L$$

5) Ripple factor. (γ)

$$\begin{aligned}
 \gamma &= \frac{I_{ac}}{I_{dc}} \quad \text{wktb} \quad I_{rms}^2 = I_{ac}^2 - I_{dc}^2 \\
 &\text{or} \quad I_{ac}^2 = I_{rms}^2 - I_{dc}^2
 \end{aligned}$$

$$\therefore \gamma = \frac{I_{ac}}{I_{dc}} = \sqrt{\frac{I_{ac}^2}{I_{dc}^2}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^{2\text{Date}}}{I_{dc}^2}}$$

$$= \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\frac{I_m^2/2}{4 I_m^2/\pi^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1} = 0.483$$

$\therefore \gamma = 48.3\%$ Same as FWR with 2 diodes.

- * The ripple contents in the o/p are 48% of the dc component. $\Rightarrow I_{ac} < I_{dc}$. Hence good rectification.

6. Efficiency (η):

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_s + 2R_f + R_L)}$$

$$\text{but } I_{dc} = \frac{2I_m}{\pi}, \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\therefore \eta = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_s + R_L + 2R_f)}$$

$$= \frac{\frac{4I_m^2}{\pi^2}}{\frac{I_m^2}{2}} \times \frac{1}{\left(1 + \frac{R_s + 2R_f}{R_L}\right)} \quad \because \frac{R_s + 2R_f}{R_L} \ll 1$$

$$= \frac{8}{\pi^2} = 0.812$$

$\therefore \eta = 81.2\%$

Hence in a FWR, ripple contents at the o/p is less and therefore the efficiency is high.

Advantages of FWR.

- 1) DC load voltage and current are more than HWR
- 2) Efficiency is high
- 3) Large dc Power o/p.
- 4) Ripple factor is less.
- 5) used in regulated Power supplies.

Bridge Rectifier with Capacitor filter

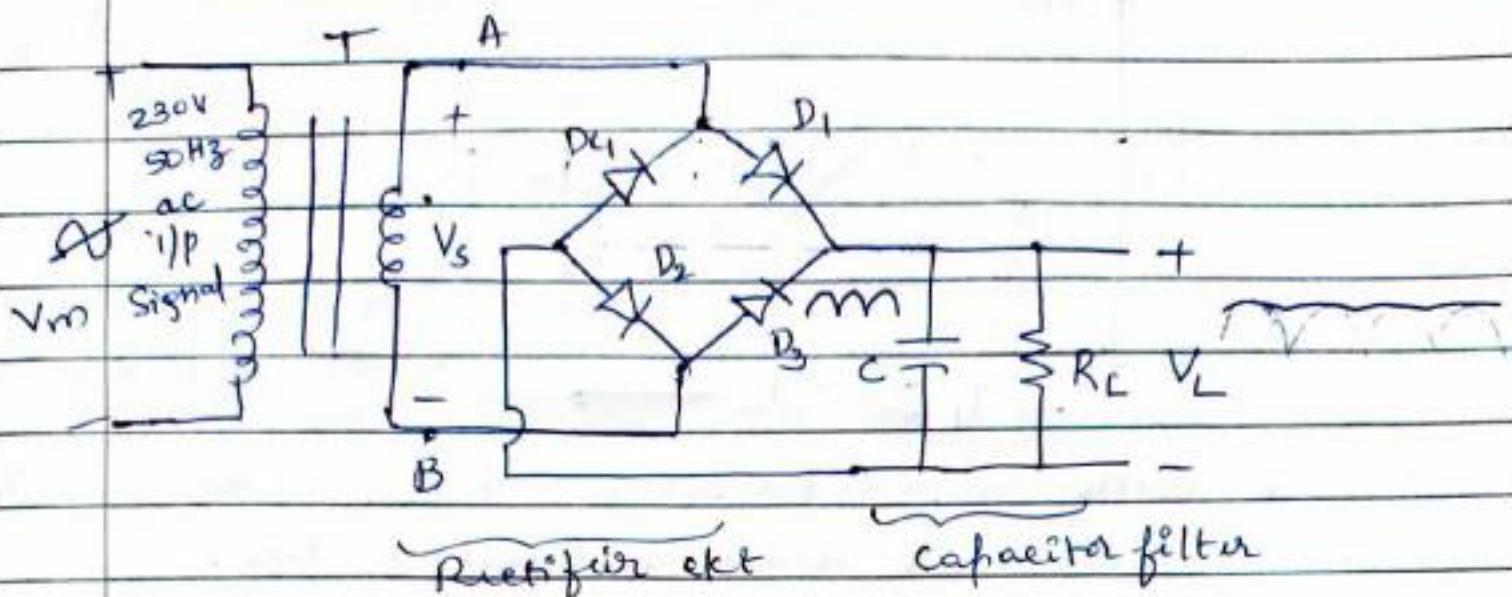
Filter circuits.

- * Filter circuits are used at the o/p of the rectifiers to obtain ripple free dc voltage.
Filter circuits try to minimize the ripples at the o/p as far as possible.
- * Two components used by the filter circuits are
Inductor: Blocks ac and allows dc components to pass through. Hence it is connected in series with load
Capacitor: Blocks dc and allows ac components to pass through. Hence it is connected in parallel with the load.

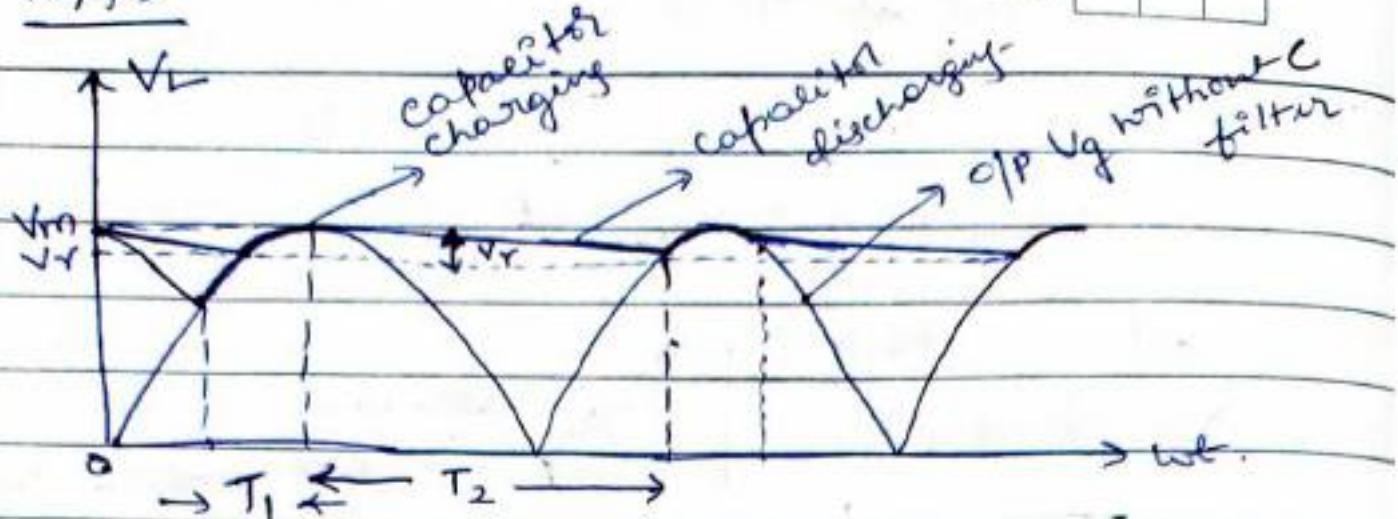
Capacitor filter:



- * capacitor charges to the peak value V_m during diode conduction period and delivers this energy during non conduction period to the load R_L .
- * Charging time of the capacitor must be small so that it charges faster to reach the peak value. The discharging time must be large so that it slowly discharges to reach the next peak.

Circuit diagram.

- * During +ve half cycle of ac supply, diodes D_1 & D_2 conduct and charge the capacitor to the peak value V_m . Diodes D_3 & D_4 stop conducting when the transformer secondary voltage falls below V_m .
- * Now the capacitor starts discharging through R_L and the voltage across capacitor begins to fall. The discharging continues until the diodes D_3 & D_4 start conducting and charge the capacitor in the next half cycle of the ac supply.
- * The capacitor charges faster to reach the peak value with small time and discharges slowly due to large time. Hence ripples in the o/p gets considerably reduced.
- * charging time is $T_1 = 2R_f C$.
- * Discharging time is $T_2 = R_L C$.

ω/f_8 

- * With capacitor filter, the variation in V_o is smaller than without filter.
- * without filter ($0 \rightarrow V_m$)
- * with filter ($[V_m - V_r] \rightarrow V_m$)
- * This indicates that parallel combination of R_L & C considerably reduces the ripple contents of the o/p voltage.

For HWR ripple factor with C filter is given as

$$\boxed{\gamma = \frac{1}{2\sqrt{3} f C R_L}}$$

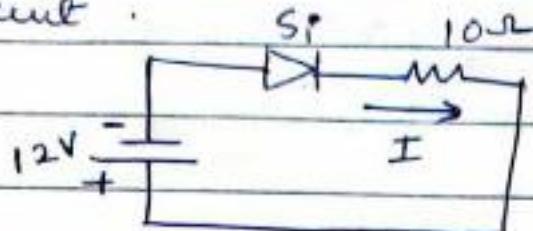
For FWR, ripple factor with C filter is given as

$$\boxed{\gamma = \frac{1}{4\sqrt{3} f C R_L}}$$

Hence, by selecting large value of C , o/p can be made more smoother thereby reducing the ripple contents.

Diode circuits numericals.

1. Find the value of current I in the following circuit.

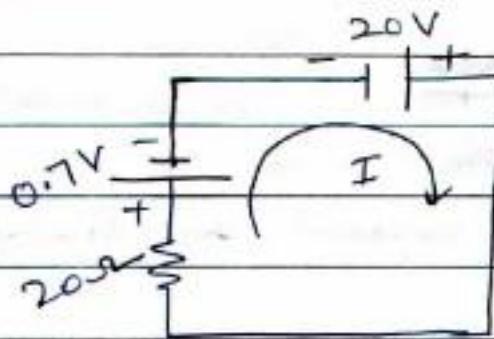


Soln. The Si diode is reverse biased by -12V.
So it does not conduct. $\therefore I = 0$.

2. calculate the current I in the circuit.



Soln. Here 10Ω is independent of 20V. Hence the equivalent circuit is



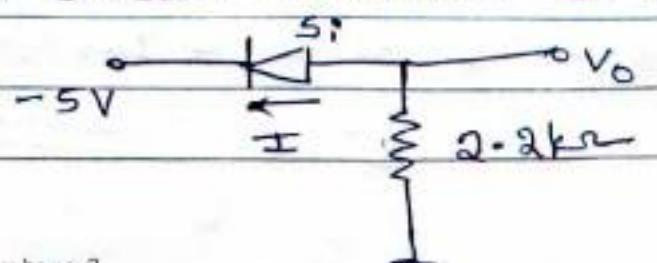
Applying KVL to the loop,

$$-0.7V + 20V - I \times 20\Omega = 0$$

$$\therefore I = \frac{20 - 0.7}{20} = 0.965A$$

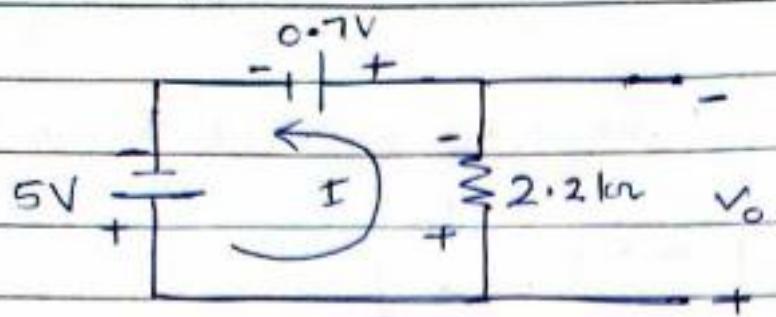
965mA

3. For the circuit calculate I & V_o .



Ques

The equivalent circuit is

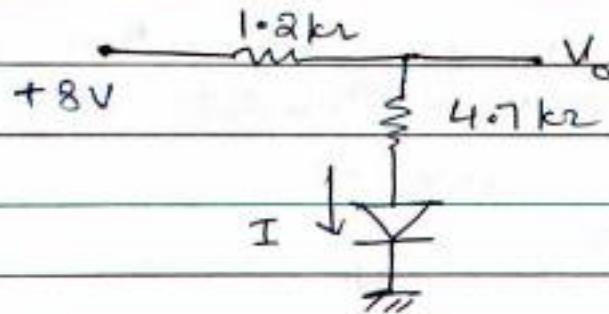


Applying KVL, we have

$$+5V - 2.2k\Omega \times I - 0.7V = 0$$

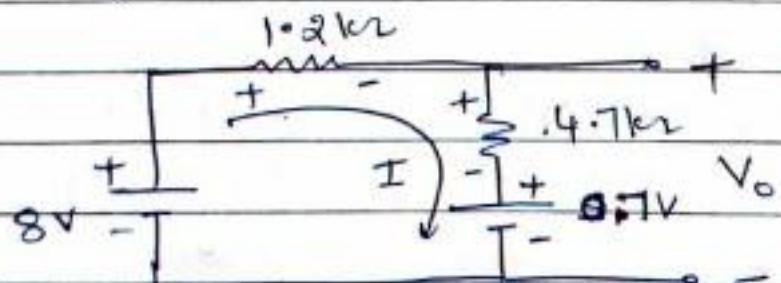
$$\therefore I = \frac{5 - 0.7}{2.2k\Omega} = 1.95mA$$

$$\therefore V_o = 1.95mA \times 2.2k\Omega \\ = 4.3V$$

4. Calculate I & V_o for the given circuit

Ques

The equivalent circuit is shown as



Applying KVL, we get

$$8V - I \times 1.2k\Omega - I \times 4.7k\Omega - 0.7V = 0$$

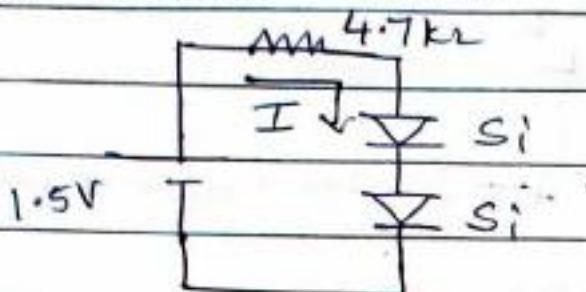
$$I = \frac{8 - 0.7}{(4.7 + 1.2)k\Omega} = 1.237mA$$

$$V_o = I \times 4.7 \times 10^3 + 0.7$$

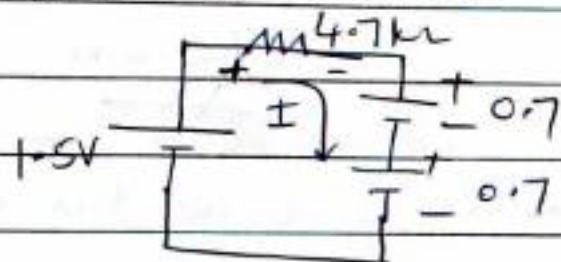
$$= 1.237 \times 10^{-3} \times 4.7 \times 10^3 + 0.7$$

$$= \underline{6.51V}$$

5. Calculate the value of diode current I in the circuit below.



Ans The equivalent circuit is

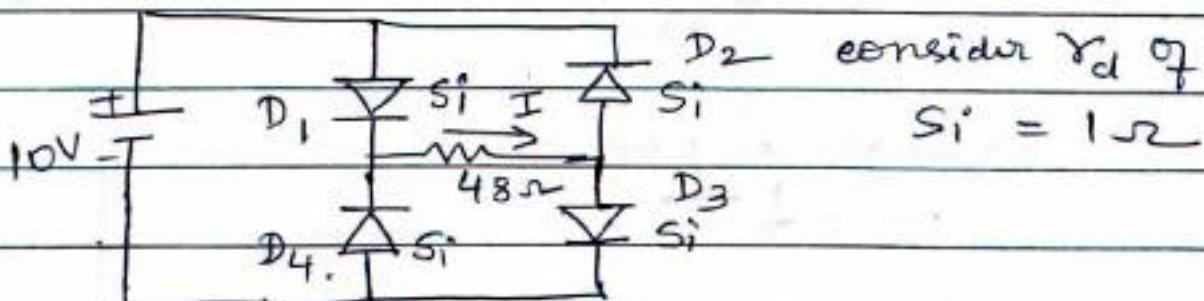


Applying KVL,

$$1.5V - 0.7V - 0.7V - I \times 4.7k\Omega = 0$$

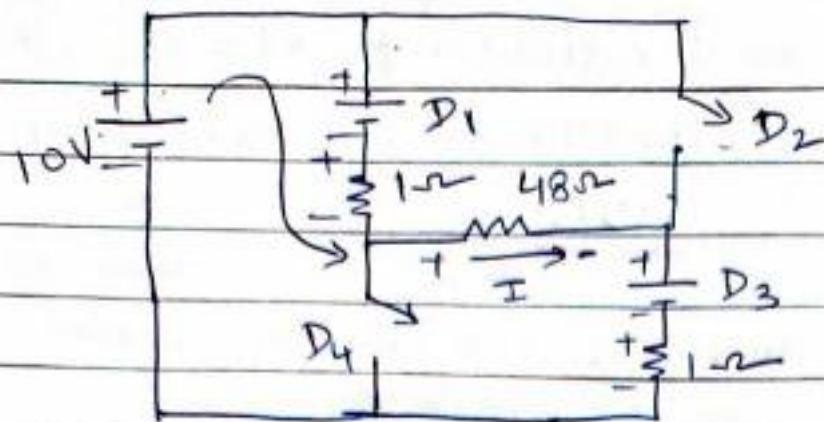
$$I = \frac{1.5 - 1.4}{4.7k\Omega} = \underline{0.021mA}$$

6. Calculate I in the circuit.



Ans In the circuit, for a supply of 10V, only diodes D_1 & D_3 gets forward biased.
 D_2 & D_4 are open switches.

Equivalent-circuit is as below.



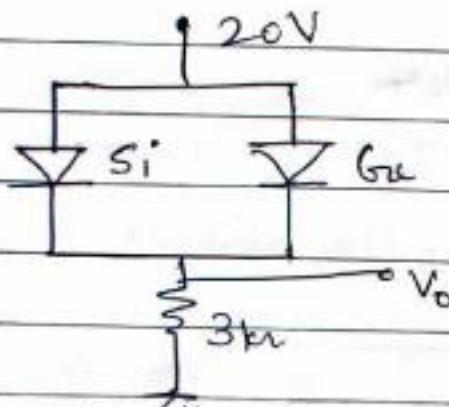
Applying KVL:

$$10V - 0.7V - I(1\Omega + 48\Omega + 1\Omega) - 0.7V = 0$$

$$I = \frac{10V - 1.4V}{50\Omega} = 0.172A$$

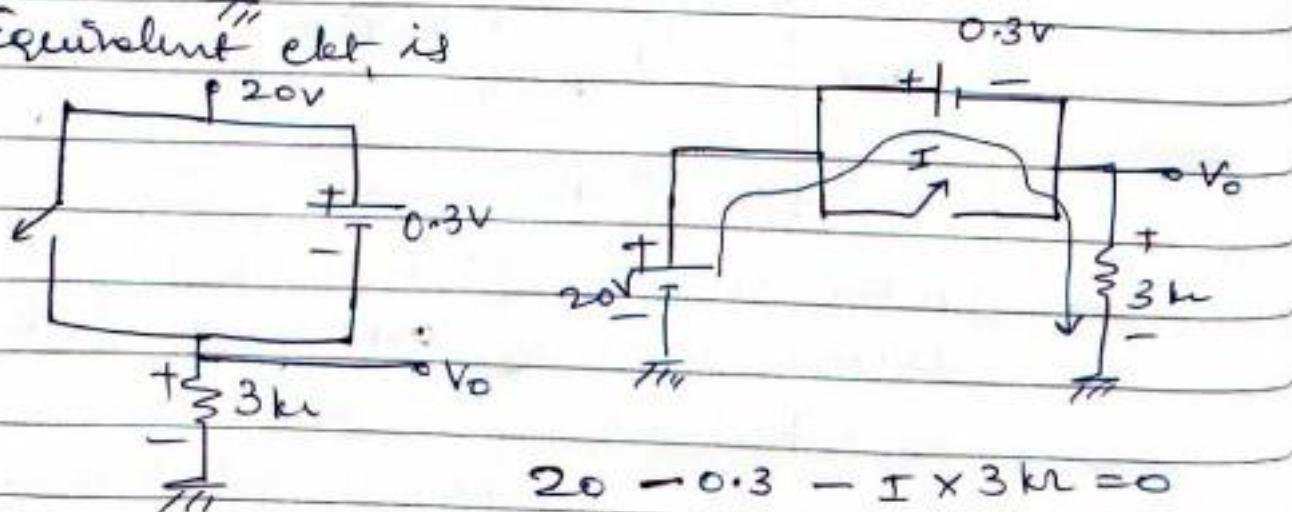
$$= 17.2mA$$

8. calculate the current in the circuit & V_o .



Here Ge gets forward biased first once 20V is switched ON.
Si never gets to switch ON.

Equivalent circuit is



$$20 - 0.3 - I \times 3k\Omega = 0$$

$$\therefore I = \frac{20 - 0.3}{3k\Omega} = 6.56mA$$

$$V_o = I \times 3k\Omega = 19.7V$$

Rectifier circuits : Numericals.

1. A sinusoidal voltage of peak value 40V & frequency 50Hz is applied to a HWR without filter. It has a load $R_L = 800\Omega$ with $R_f = 8\Omega$. Calculate a) peak, dc and rms value of load current
 b) DC o/p power
 c) AC i/p power &
 d) Rectifier efficiency.

Solu. Given: $V_m = 40V$, $f = 50\text{Hz}$.

$$R_L = 800\Omega, R_f = 8\Omega$$

a) Peak value of the load current I_{mL} is

$$I_m = \frac{V_m}{R_L + R_f} = \frac{40}{800 + 8} = 49.5\text{mA}$$

$$I_{dc} = \frac{I_m}{\pi} = \frac{49.5\text{mA}}{\pi} = 15.757\text{mA}$$

$$I_{rms} = \frac{I_m}{2} = \frac{49.5\text{mA}}{2} = 24.75\text{mA}$$

b) DC power to load, $P_{dc} = I_{dc}^2 R_L$

$$= (15.757 \times 10^{-3})^2 \times 800$$

$$= 198.45\text{mW}$$

c) AC i/p Power. $P_{ac} = I_{rms}^2 (R_L + R_f)$

$$= (24.75\text{mA})^2 (800 + 8)$$

$$= 494.95\text{mW}$$

d) Efficiency $\eta = \frac{P_{dc}}{P_{ac}} = \frac{198.45\text{mW}}{494.95\text{mW}}$

$$= 0.4009$$

2. An input to a HWR is $23 \sin 314t$. If $R_f = 50\Omega$ and $R_L = 500\Omega$ determine,

- i) DC load voltage ii) RMS load voltage
 iii) Rectification efficiency iv) dc power delivered to the load.

Solu. Given $V_{\text{avg}} = V_m \sin \omega t$
 $= 23 \sin 314t$.

$$R_f = 50\Omega \quad R_L = 500\Omega$$

i) $V_{dc} = I_{dc} \times R_L$

$$I_{dc} = \frac{I_m}{\pi}, \quad I_m = \frac{V_m}{R_f + R_L} = \frac{23}{50 + 500}$$

$$= 41.81 \text{ mA}$$

$$\therefore I_{dc} = \frac{41.81 \text{ mA}}{\pi} = 13.31 \text{ mA}$$

$$\therefore V_{dc} = 13.31 \text{ mA} \times 500\Omega = 6.65 \text{ V}$$

ii) $V_{Rms} = I_{Rms} \times R_L$

$$I_{Rms} = \frac{I_m}{2}, \quad I_m = \frac{V_m}{R_f + R_L}$$

$$= \frac{23}{550} = 41.81 \text{ mA}$$

$$I_{Rms} = \frac{41.81 \text{ mA}}{2}$$

$$= 20.90 \text{ mA}$$

$$\therefore V_{Rms} = 20.90 \text{ mA} \times 500\Omega$$

$$= 10.45 \text{ V}$$

iii) $P_{dc} = I_{dc}^2 \times R_L$

$$= (13.31 \text{ mA})^2 \times 500$$

$$= 88.57 \text{ mW}$$

iv) $\eta = \frac{0.406}{1 + R_f/R_L} = \underline{\underline{36.91\%}}$

3. In a Full wave bridge rectifier, the transformer secondary voltage is $100 \sin \omega t$. The forward resistance of each diode is $25\Omega + \text{load}$ resistance is 950Ω . Calculate
 a) dc op V_d , b) Ripple factor c) Efficiency.

Solu. $V_s = V_m \sin \omega t = 100 \sin \omega t$

$$V_m = 100, R_f = 25\Omega, R_L = 950\Omega$$

a) $V_{dc} = I_{dc} R_L$

$$I_{dc} = \frac{2I_m}{\pi}, I_m = \frac{V_m}{2R_f + R_L} = \frac{100}{2 \times 25 + 950}$$

$$I_m = \frac{100}{1000} = 100mA$$

$$\therefore I_{dc} = \frac{100mA \times 2}{\pi} = 63.66mA$$

$$V_{dc} = I_{dc} R_L = 63.66mA \times 950$$

$$= 60.478V$$

b) Ripple factor (γ)

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \frac{100mA}{\sqrt{2}}$$

$$\gamma = \sqrt{\left(\frac{100mA}{63.66mA}\right)^2 - 1} = \sqrt{1.233 - 1}$$

$$= \sqrt{0.2337} = 0.4834$$

$$\therefore \underline{\underline{\gamma = 48.34\%}}$$

$$\eta = \frac{P_{dc}}{P_{ac.}} = \frac{I_{dc}^2 R_L}{I_{rms}^2 (2R_f + R_L)} = \frac{3.85}{5 \times 10^3 (1000)}$$

$$= 0.77$$

$$\underline{\underline{n = 77 \%}}$$

4. A bridge rectifier uses 4 diodes with rms voltage of 110V. Forward resistance of each diode is 25Ω with load R_L of $1\text{ k}\Omega$. Find i) max value of current ii) DC value of current through the load iii) DC load voltage.

Solu: given $V_{rms} = 110\text{V}$, $R_f = 25\Omega$, $R_L = 1\text{k}\Omega$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \therefore V_m = V_{rms} \times \sqrt{2} \\ = 155.56\text{V.}$$

$$\text{i) } I_m = \frac{V_m}{2R_f + R_L} = \frac{155.56}{50 + 1 \times 1000} = \underline{\underline{148.15\text{mA}}}$$

$$\text{ii) } I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 148.15\text{mA}}{\pi} = \underline{\underline{94.36\text{mA}}}$$

$$\text{iii) } V_{dc} = I_{dc} \times R_L = 94.36\text{mA} \times 1\text{k}\Omega \\ = \underline{\underline{94.36\text{V}}}$$

with capacitor filter

PNB
Date _____

1. Determine the ripple factor of a bridge rectifier using a capacitor filter. The load used is $2\text{ k}\Omega$ while dc o/p V_d is 12V. Assume supply frequency of 50Hz and ideal diodes. The capacitor of $100\text{ }\mu\text{F}$ is used in the filter circuit.

Solu. given: $R_L = 2\text{ k}\Omega$, $V_{dc} = 12\text{ V}$, $f = 50\text{ Hz}$
ideal diodes, $C = 100\text{ }\mu\text{F}$.

$$\gamma = \frac{1}{4\sqrt{3} f C R_L} = \frac{1}{4\sqrt{3} \times 50 \times 2 \times 10^3 \times 100 \times 10^{-6}}$$
$$= \frac{1}{69.28} = 0.0144$$

$$\therefore \gamma = \underline{1.44\%}$$

2. Calculate the value of capacitor C that has to be used for filter of a Bridge rectifier to get a ripple factor of 0.01. The rectifier supplies current to a load of $2\text{ k}\Omega$ while the supply frequency is 50Hz.

Solu.

given $\gamma = 0.01$ (1.1), $R_L = 2\text{ k}\Omega$, $f = 50\text{ Hz}$.

$$\gamma = \frac{1}{4\sqrt{3} f C R_L} \therefore C = \frac{1}{4\sqrt{3} f R_L \times \gamma}$$

$$C = \frac{1}{4\sqrt{3} \times 50 \times 2 \times 10^3 \times 0.01} = \frac{1}{6928.203}$$
$$= 0.0001443$$

$$= \underline{\underline{144.34\text{ }\mu\text{F}}}$$

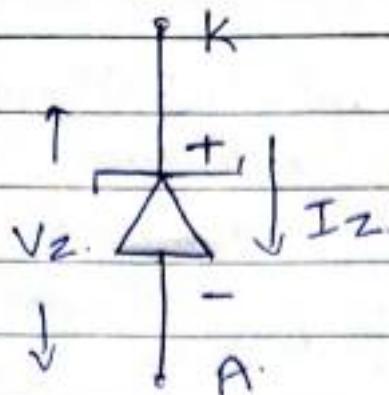
Zener diode.

- * Zener diodes are designed for the operation in reverse breakdown.
- * When a junction diode is reverse biased, there is normally a small amount of reverse saturation current (I_S),
- * When the reverse voltage is sufficiently increased, the junction breaks down and a large reverse current flows.
- * If the reverse current is limited by means of a suitable series connected resistor (R) the power dissipation in the diode can be kept to a level that will not destroy the device.
- * Under this condition, diode may be continuously operated in reverse breakdown.

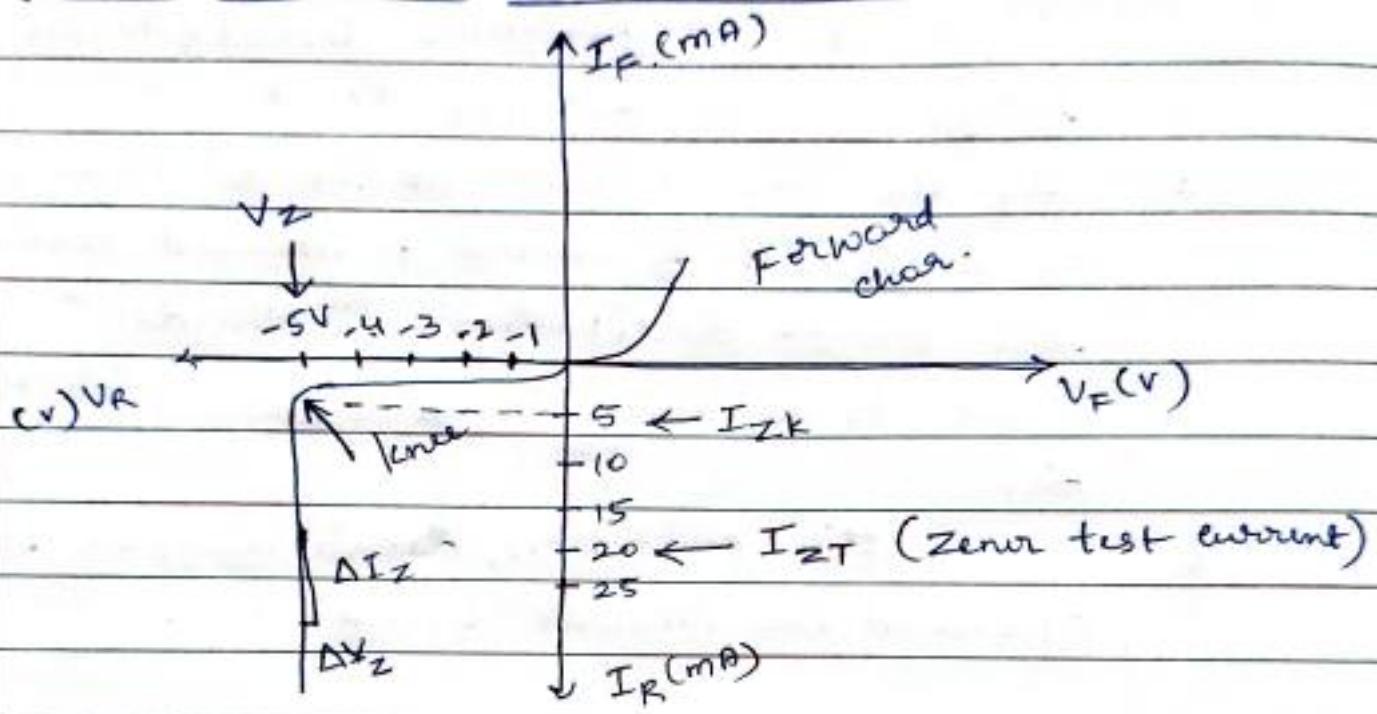
Zener breakdown:

- * When a narrow junction with a narrow depletion region is applied with a high reverse voltage, due to high electric field, electrons breakaway from the atoms thus converting the depletion region from an insulating material into a conducting material. This ionization by electric field is known as Zener breakdown.
- * This property of breakdown may be useful as applications as a voltage reference source.

Symbol.



Zener diode V-I characteristics



Zener parameters.

1. Zener breakdown voltage (V_z):

It is a voltage beyond which there is a sharp increase in current for a small change in reverse voltage. It is the voltage across the Zener in breakdown.

2. Reverse knee current (I_{ZK}):

It is the zener current corresponding to the knee region of characteristics.

3. Maximum zener current (I_{Zm}):

It is the maximum Zener current through the zener that would not destroy the device.

4. Zener test current: (I_{ZT})

It is the test current used for measuring the working condition of the zener diode.

5 Dynamic resistance (r_z):

It is the ratio of change in reverse voltage to change in reverse current beyond knee.

$$r_z = \frac{\Delta V_z}{\Delta I_z}$$

Max power dissipation is

$$P_{z\max} = V_z \times I_{z\max}$$

NOTE:

Many low power zener diodes have a test current specified as $I_{ZT} = 20\text{mA}$.

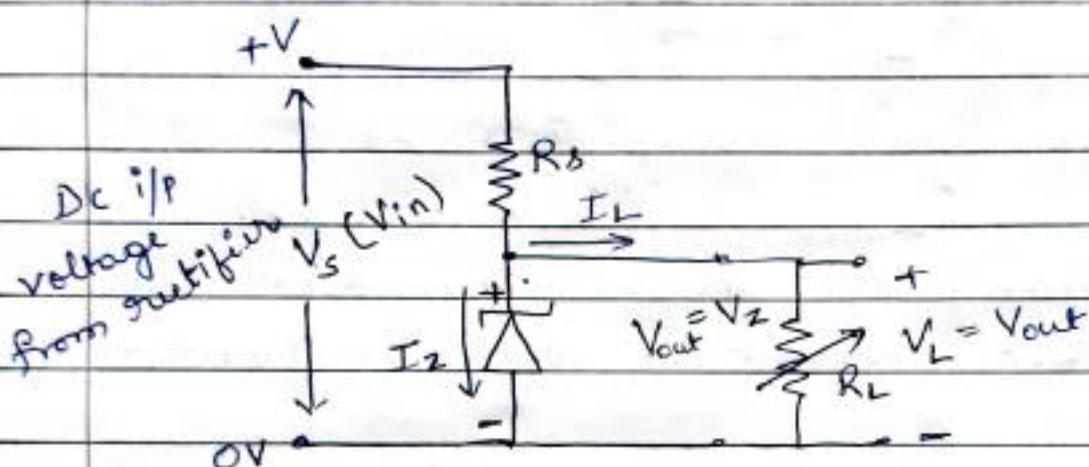
Zener as a voltage regulator

- * Voltage regulators are devices used to maintain constant voltages across a load irrespective of fluctuations in the input voltage and load currents.
- * Zener diodes are widely used as voltage regulators to regulate the voltage across small loads. Zener diodes have a sharp reverse breakdown voltage and this voltage will be constant for a wide range of currents.
- * Zener diodes can be used to produce a stabilized

Output voltages with low ripple under varying load current conditions.

- * By passing a small current through the diode from a voltage source, via a suitable current limiting resistor R_s , the zener diode will conduct sufficient current to maintain a voltage drop of V_{out} .

A simple zener voltage regulator circuit is shown below.



Working:

Zener diode is connected with its cathode terminal connected to the positive of the DC supply.

Hence it is reverse biased and will be operating in breakdown condition.

Resistor R_s is connected in series with the zener diode. Its value is selected so as to limit the maximum current flowing in the circuit.

Case 1: When no load is connected ($I_L = 0$) to the circuit, the load current will be zero. The entire circuit current passes through

the zener diode - the diode hence dissipates maximum power. Therefore R_s should be so chosen that it can maintain the power dissipation within the range.

Case 2: when load R_L is connected ($I_L \neq 0$)

In the circuit, load is connected in parallel to zener diode. Here, the voltage across R_L is same as zener voltage. ($V_{out} = V_z = V_{RL}$)

- * There is a minimum zener current (I_{zmin}) for which the zener maintains stabilization of voltage. The zener current must always be above I_{zmin} with load, within its breakdown region. I_{zmax} depends upon the power rating of the device.

Voltage regulation can be done through 2 techniques.

1. Line regulation :

In this case, series resistance R_s and load resistance R_L are kept constant. It is assumed that all the variations in o/p voltage arise due to fluctuations in input power supply.

The regulated o/p voltage is achieved for input voltage above certain minimum level.

∴ regulation is

$$\frac{\Delta V_{out}}{\Delta V_{in}} \times 100.$$

$\Delta V_{out} \rightarrow$ change in output voltage for a particular change in input voltage ΔV_{in} .

--	--	--

2. Load regulation: In this case,

the input voltage is fixed, while the load resistance is varied. The constant o/p voltage is obtained as long as the load resistance R_L is maintained above a minimum value.

i. regulation is

$$\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

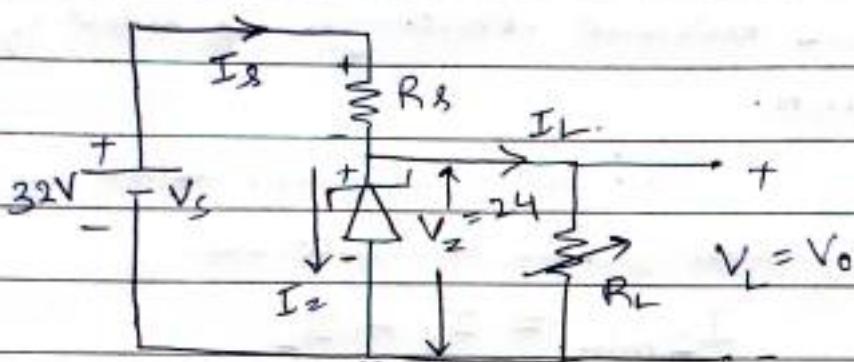
V_{NL} → is the voltage across zener diode when no load is applied (R_L)

V_{FL} → is the full load applied or voltage across the zener in the presence of R_L .

Numericals.

1. A 24V, 600mW zener diode is used for providing a 24V stabilized supply to a variable load from a 32V supply. Calculate
 i) Value of series resistance required
 ii) Zener current when the load is 1200Ω .

Solve circuit diagram:



Given: $V_z = 24V$, $P_z = 600mW$, $V_s = 32V$.

(i) without load R_L ie $I_L = 0$ & $R_L = 0$.

We know that $I_s = I_z + I_L$. (from the ekt)

since $I_L = 0$, $I_s = I_{z \text{ max}}$.

$$P_z = I_z V_z.$$

$$\therefore I_z = \frac{P_z}{V_z} = \frac{600mW}{24V} = 25mA = I_{z \text{ max}}$$

Applying KVL,

$$I_s = I_{z \text{ max}} \\ = 25mA$$

$$V_s - I_s R_s - V_z = 0.$$

$$32 - 25mA \times R_s - 24 = 0$$

$$\therefore R_s = \frac{32V - 24V}{25mA} = \underline{\underline{320\Omega}}$$

The value of series resistance to be connected in the circuit is $R_s = \underline{\underline{320\Omega}}$

ii) with load R_L :

$$\text{wkt } I_S = I_L + I_Z.$$

$$\text{also } V_S = V_o = V_L = I_L R_L$$

$$\Rightarrow V_Z = I_L R_L.$$

$$\text{Given } V_Z = 24V \text{ & } R_L = 1200\Omega.$$

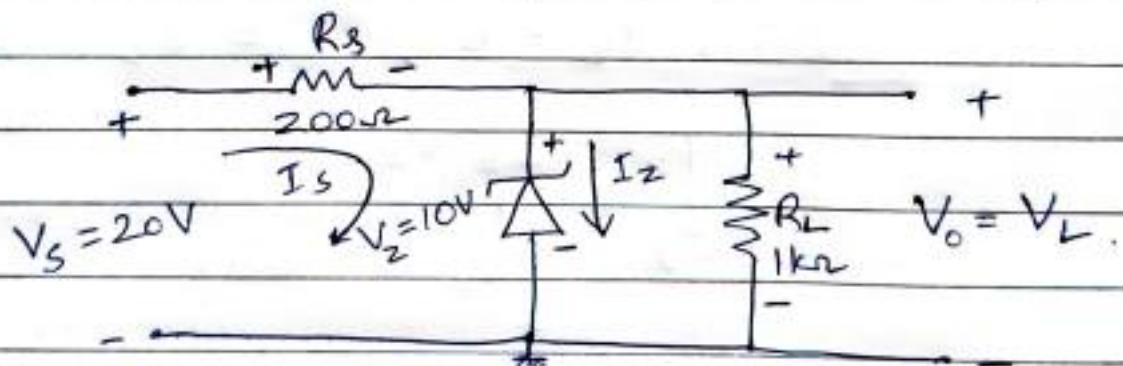
$$\therefore I_L = \frac{V_Z}{R_L} = \frac{24V}{1200\Omega} = \underline{\underline{20mA}}$$

Load current through a load of 1200Ω is 20mA.

\therefore At maximum load of 1200Ω , minimum zener current is

$$\begin{aligned} I_{Z\min} &= I_S - I_L \\ &= 25mA - 20mA = \underline{\underline{5mA}} \end{aligned}$$

2. A circuit has a zener diode connected ac/c the load with following details. Find I_S , I_L & P_Z .



Sol:

Given, $V_S = 20V$, $R_S = 200\Omega$, $V_Z = 10V$, $R_L = 1k\Omega$.

To find I_S , I_L and Power P_Z .

Applying KVL to the i/p loop, we get

$$V_S - I_S R_S - V_Z = 0.$$

$$20V - I_S \times 200\Omega - 10V = 0.$$

$$\therefore I_S = \frac{20V - 10V}{200\Omega} = \underline{\underline{50mA}}$$

Wkt $V_L = V_o = I_D R_L = V_Z$

$$\Rightarrow V_Z = I_L R_L.$$

$$\therefore I_L = \frac{V_Z}{R_L} = \frac{10V}{1 \times 10^3} = \underline{\underline{10mA}}$$

The load current through a load of $1\text{k}\Omega$ is 10mA

To find the current through zener &
hence the power dissipation.

Wkt $I_S = I_Z + I_L$

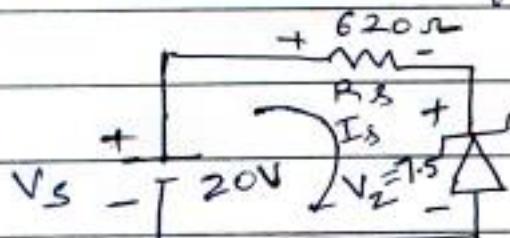
$$\therefore I_Z = I_S - I_L \\ = 50mA - 10mA = \underline{\underline{40mA}}$$

\therefore The power dissipated is

$$P_Z = V_Z I_Z.$$

$$= 10V \times 40mA = \underline{\underline{400mW}}$$

3. A circuit uses a zener with $V_Z = 7.5V$. Find the diode current and max power dissipation in the absence of load.



$$\text{Given: } V_S = 20V$$

$$V_Z = 7.5V$$

$$R_g = 620\Omega.$$

to find P_Z with $R_L = 0$.

Soln. Wkt $I_S = I_L + I_Z$.

Since $R_L = 0$, $I_S = I_Z$ max.

Applying KVL,

$$V_S - I_S R_g - V_Z = 0.$$

$$20 - I_S \times 620 - 7.5 = 0.$$

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$$\therefore I_S = I_Z = \frac{20V - 7.5V}{6\Omega \text{ or } 6k\Omega} = 20.16 \text{ mA}$$

\therefore Max zener current $I_{Z\max} = 20.16 \text{ mA}$

Power dissipation in zener is

$$\begin{aligned}
 P_Z &= I_Z V_Z \\
 &= 20.16 \text{ mA} \times 7.5 \text{ V} \\
 &= \underline{\underline{151.2 \text{ mW}}}
 \end{aligned}$$

Transistors and Applications.

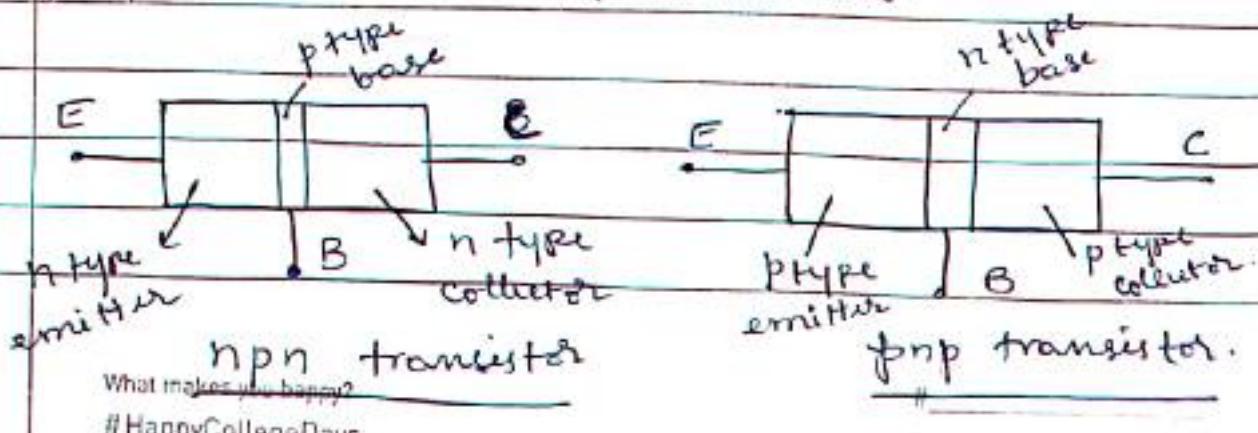
Bipolar junction transistor:

- BJT is a 3 terminal device constructed using doped semiconductor materials.
- It is mainly used in amplifying and switching applications.
- Bipolar because both holes and electrons take part in conduction of current.
- The three terminals of a BJT are E: emitter, B: Base & C: collector.
- 2 junctions present in a BJT are:
 - B-E junction (Base-Emitter)
 - C-B junction (Collector-Base).

Two types of transistors are

- 1) npn transistor: p type semiconductor material is sandwiched b/w 2 n type materials.
- 2) pnp transistor: n type semiconductor material is sandwiched b/w 2 p type materials

Junction representations of ~~n type~~ npn & pnp transistors with terminals.



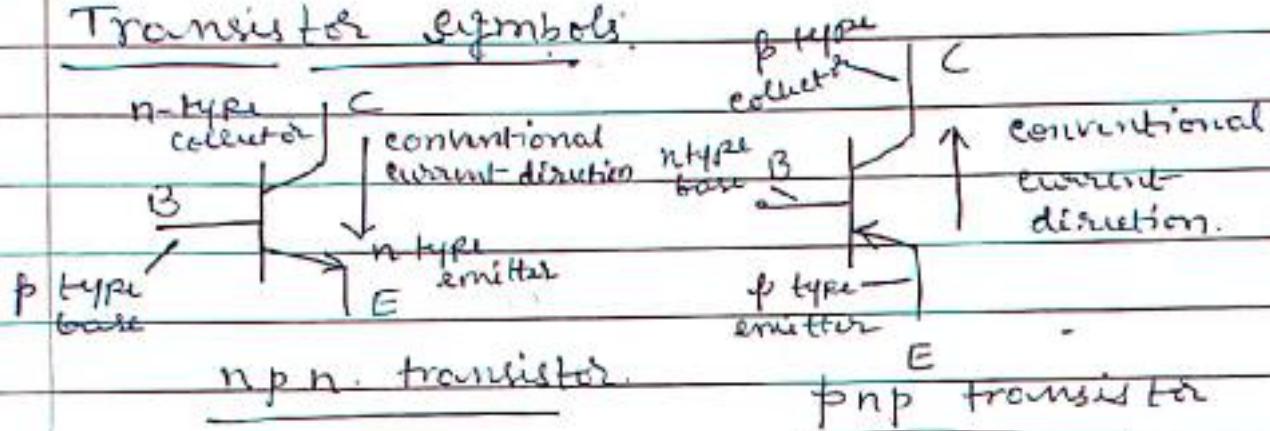
The three terminals of transistor are

Emitter : It is highly doped and is the supplier of electrons.

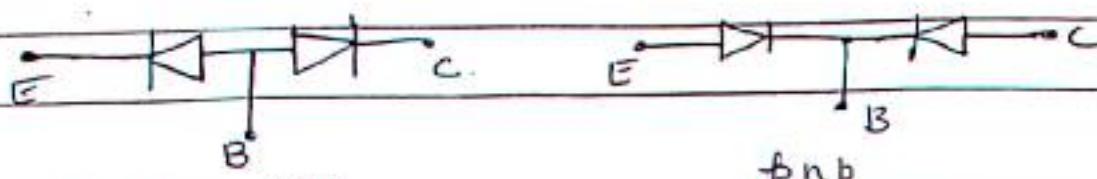
Base : It is thin and lightly doped.

Collector : It is moderately doped and large in size. It collects the electrons emitted by the emitter (npn).

Transistor symbols:

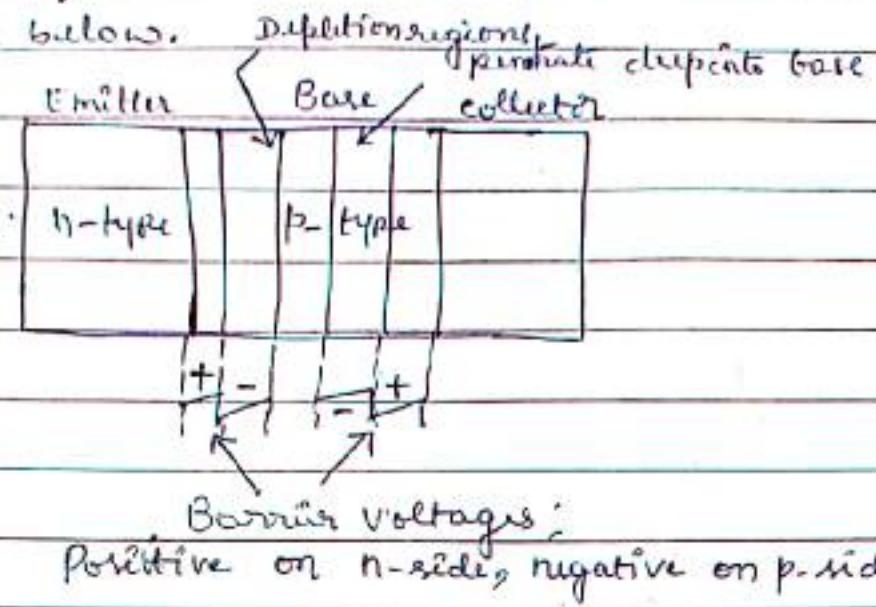


- * The arrow indicates the emitter terminal of the transistor. It also indicates the conventional direction for the current flow.
- * In n-p-n transistor the arrow head points outwards, from base to emitter.
- * In p-n-p transistor the arrow head points inwards for emitter towards the base.
- * n-p-n transistor can be considered to be made up of 2 diodes with common anode. Similarly p-n-p using 2 diodes with common cathode.

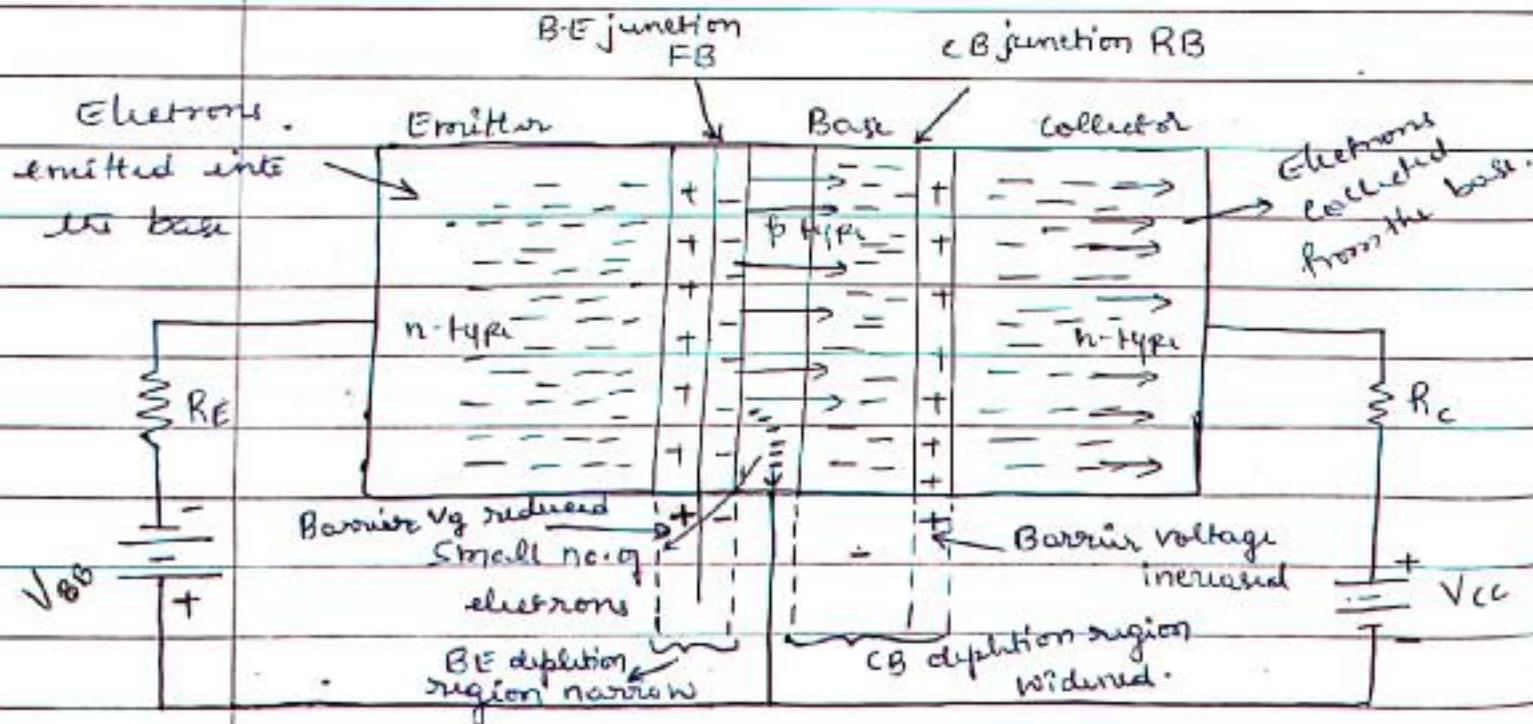


npn transistor operation

The depletion regions and barrier voltages at the junctions of an unbiased npn transistor is as shown below.



Connection diagrams of npn transistor with biasing



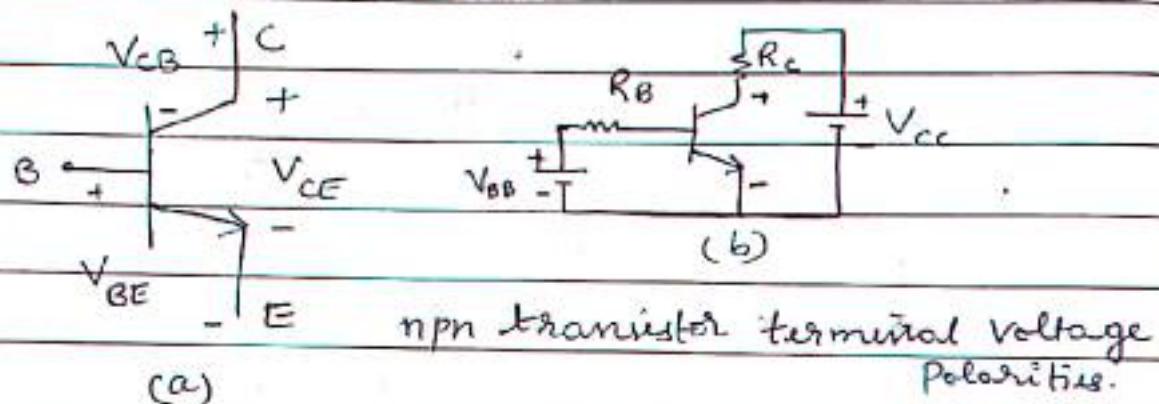
- * Emitter and collector are heavily doped whereas Base is lightly doped.
- * Figure shows an npn transistor applied with external bias voltages.
- * Here EB junction is forward biased by the external dc source. This reduces the barrier voltage and causes the electrons in the n-type emitter to flow towards the p-type base. Thus the depletion region at EB junction is reduced and becomes narrow. (Electrons are emitted into the base region, hence the name emitter and emitter current) I_E
- * CB junction is reverse biased by the external dc source. This increases the barrier voltage and causes the CB depletion region to be widened.
- * The electrons flow from the emitter through the p-type base to combine with the holes in the base. Base region is thin & lightly doped, and hence only few electrons injected by n-type emitter to base recombine with holes to form base current I_B .
- * Remaining electrons from the base arrive at CB depletion region and are drawn across the CB junction by the external dc bias supply. These electrons are said to be collected in collector region. This gives rise to a current known as collector current I_C .
- * Thus the electron current is dominant in an npn transistor

Since around 98% of the electrons from the emitter flow in the collector circuit & very few electrons combine with holes in the base, base current is very small and collector current is a large one.

BJT voltages and currents (npn)

Terminal voltages:

The terminal voltage polarities for an npn transistor is as below:



- * The direction of the arrow head indicates the conventional current direction. For an npn transistor, the base is biased with positive voltage with respect to emitter. The collector is biased with a higher positive voltage than base.
- * In fig b) the voltage V_{BB} is the base bias voltage connected via R_B . The collector supply V_{cc} is connected via R_c . The negative terminals of the two sources are connected to the emitter terminal.
- * $V_{cc} > V_{BB}$ to ensure that CB junction is reverse biased. (+ve on C & -ve on B)

NOTE: Typical transistor B-E voltages are 0.3V for Germanium + 0.7V for a silicon transistor. Typical collector voltages might vary from 3V to 20V for most transistors. Low power transistors generally pass currents of 1mA to 20mA. Current levels for high power transistors range from 100mA to several amperes.

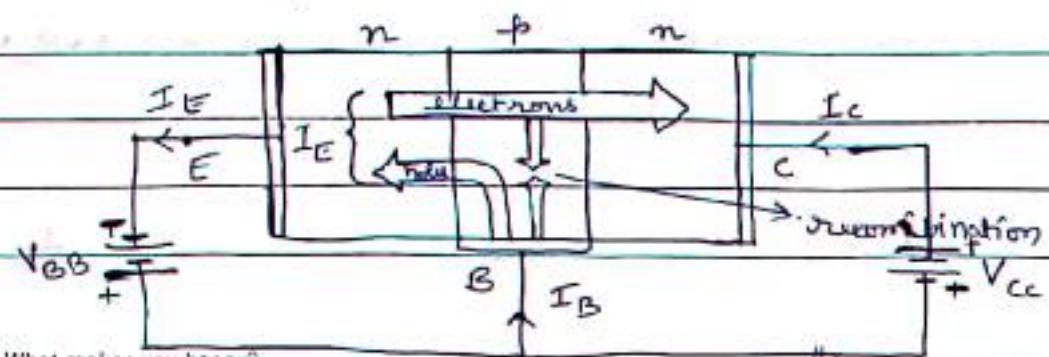
Transistor currents : (npn)

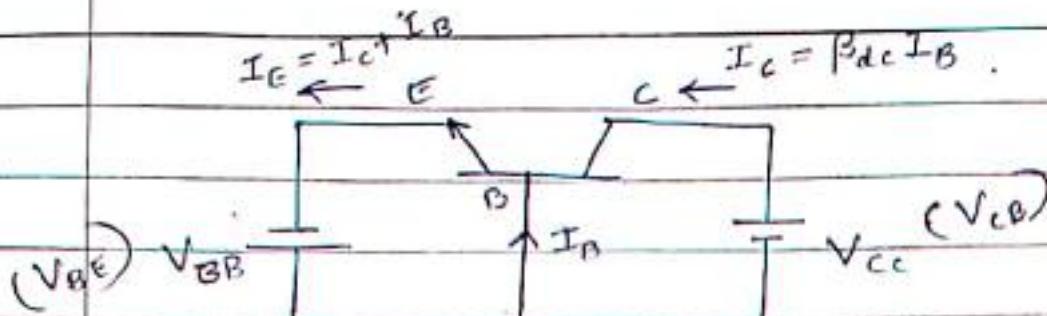
- * For an npn transistor, I_B and I_C are assumed to flow into the device (conventional current direction) and I_E is considered to be flowing out.
- * In an npn transistor, electrons are the majority charge carriers. They move in a direction opposite to conventional current direction.

$$I_E = I_B + I_C$$

For low power transistors, $I_C = 1\text{mA}$, $I_E = 25\text{mA}$ & I_B is $< 100\mu\text{A}$.

- * Almost all of I_E flows to the collector and only a small portion of current flows out of base terminal.





Terminal currents in npn transistor:

Nearly 96% to 99% of I_E flows across CB junction to become the collector current I_C .

$$I_C = \alpha_{dc} I_E \quad \text{--- (2)}$$

where, α_{dc} is the emitter to collector current gain. It is also referred to as common base dc current gain. It is the ratio of collector current to emitter current.

$$\alpha_{dc} = \frac{I_C}{I_E} \quad \text{--- (3)}$$

Normally α_{dc} varies from 0.96 to 0.99.

Hence, the collector current is almost equal to emitter current. In many circuits, it is assumed that $I_C \approx I_E$.

Since CB junction is reverse biased, very small reverse saturation current I_{CBO} flows across the junction. It is known as collector to base leakage current.

Substituting eq ① in ② for I_E we get

$$I_c = \alpha_{dc} (I_c + I_B)$$

$$I_c - \alpha_{dc} I_c = \alpha_{dc} I_B$$

$$\therefore I_c = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} \quad (4)$$

Eq (4) can be rewritten as

$$I_c = \beta_{dc} I_B \quad (5)$$

where

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \quad (6)$$

where β_{dc} is the base to collector current gain
It is the ratio of collector to base current.

$$\beta_{dc} = \frac{I_c}{I_B} \quad (7)$$

Normally β_{dc} ranges from 25 to 300.

It is also referred to as common emitter current gain.

Relation between α & β .

$$\text{Wkt } I_E = I_c + I_B \quad (1)$$

$$\therefore \alpha = \frac{I_c}{I_E}, \quad \beta = \frac{I_c}{I_B} \quad \text{or}$$

$$I_E = \frac{I_c}{\alpha}, \quad I_B = \frac{I_c}{\beta}.$$

Substituting for $I_E + I_B$ in (1)

$$\frac{I_c}{\alpha} = I_c + \frac{I_c}{\beta} \Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta}.$$

$$\therefore \alpha = \frac{\beta}{1+\beta}$$

$$\text{and } \beta = \frac{\alpha}{1-\alpha}$$

Numericals.

1. Calculate I_c & I_E for a transistor that has $\alpha = 0.98$ and $I_B = 100\mu A$. Determine the value of β for the transistor.

Solu:

$$\text{Given } \alpha = 0.98, I_B = 100\mu A.$$

$$I_E = I_C + I_B.$$

$$I_C = \beta I_B.$$

$$\therefore \beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49.$$

$$I_C = \beta I_B \Rightarrow 49 \times 100 \times 10^{-6} A = 49 \times 10^{-3} A \\ = 4.9 \text{ mA}$$

$$+ I_E = 4.9 \times 10^{-3} + 100 \times 10^{-6} \\ = 5 \text{ mA}$$

2. Calculate α and β for $I_c = 1\text{mA}$ and $I_B = 25\mu A$. Determine the new base current to give $I_c = 5\text{mA}$.

Solu:

$$\beta = \frac{I_C}{I_B} = \frac{1\text{mA}}{25\mu A} = 40$$

$$I_E = I_C + I_B = 1\text{mA} + 25\mu A = 1.025\text{mA}$$

$$\alpha = \frac{I_C}{I_E} = \frac{1\text{mA}}{1.025\text{mA}} = 0.976$$

$$I_{B\text{new}} = \frac{I_C}{\beta} = \frac{5\text{mA}}{40} = 125\mu A$$

3. Determine β and I_E for transistor where

$I_B = 50 \mu A$ and $I_C = 3.65 \text{ mA}$.

Solu: $I_B = 50 \mu A$, $I_C = 3.65 \text{ mA}$ - given

$$I_E = I_B + I_C \Rightarrow 50 \mu A + 3.65 \text{ mA} \\ = \underline{\underline{3.70 \text{ mA}}}$$

$$\beta = \frac{I_C}{I_B} = \frac{3.65 \text{ mA}}{50 \mu A} = \underline{\underline{73}}$$

4. A transistor has $I_C = 3 \text{ mA}$ and $I_E = 3.03 \text{ mA}$.

Find β of the transistor used. Assuming no change in the base current, find the new collector current when transistor is replaced with a new one with β of 70.

Solu: given, $I_E = 3 \text{ mA}$, $I_E = 3.03 \text{ mA}$

$$I_B = I_E - I_C \\ = 0.03 \text{ mA} = \underline{\underline{30 \mu A}}$$

$$\beta = \frac{I_C}{I_B} = \frac{3 \text{ mA}}{30 \mu A} = \underline{\underline{100}}$$

New collector current when transistor is replaced with $\beta = 70$ is

$$I_C = \beta I_B \Rightarrow 70 \times 30 \times 10^{-6} \\ I_C = \underline{\underline{2.1 \text{ mA}}}$$

5. Find I_C & I_E for a transistor with $\alpha = 0.99$ & $I_B = 20 \mu A$.

Solu: Given $\alpha = 0.99$ $I_B = 20 \mu A$.

Wkt $I_C = \beta I_B$

$$= \frac{\alpha}{1-\alpha} \cdot I_B$$

PNB

Date

$$I_c = \frac{0.99}{1 - 0.99} (20 \times 10^{-6})$$

$$= \underline{\underline{1.98 \text{ mA}}}$$

$$I_E = I_c + I_B = (1.98 + 0.02) \text{ mA}$$

$$I_E = \underline{\underline{2 \text{ mA}}}$$

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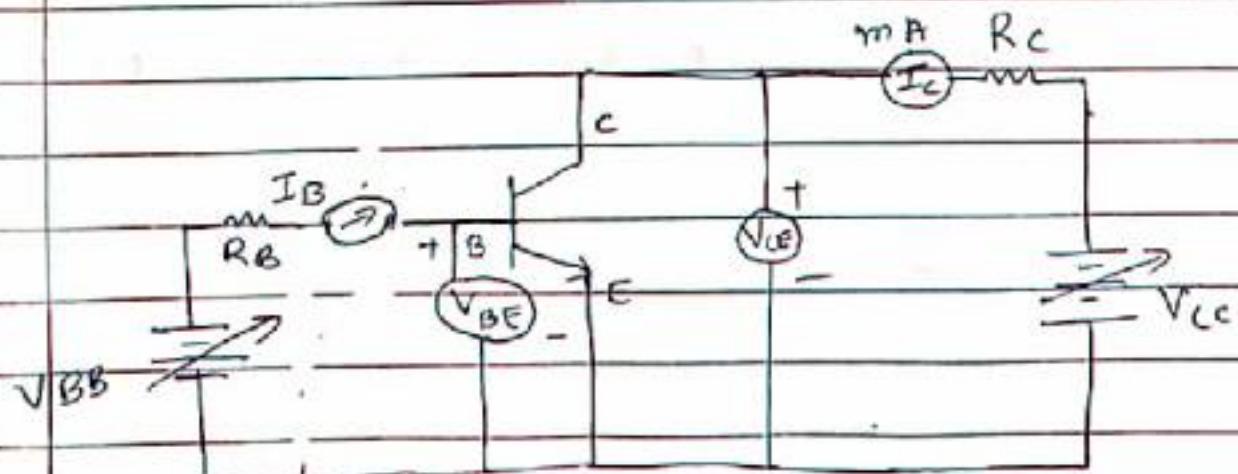
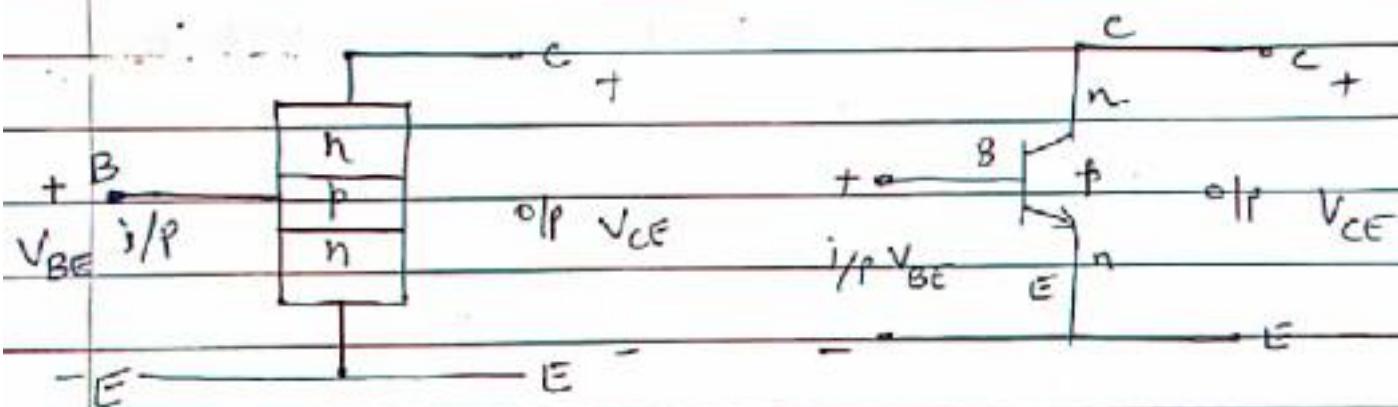
Transistor characteristics

- * The graphs showing the relationship between different currents and voltages of a transistor are known as the characteristics of the transistor.
2 types are:
 1. Input characteristics and
 2. Output characteristics.
- * Any transistor circuit can be designed using three types of configurations. Based on the connection of transistor terminals there are three configurations. They are:
 - Common Emitter configuration
 - Common Base "
 - Common collector "
- * Each of these circuit configurations has its own characteristics curve.

Study of Common Emitter configuration is as below

Common Emitter configuration (n-p-n)

- In this configuration its emitter terminal is taken as common b/w its input and o/p terminals as shown below.



Connection diagrams.

- * Input is applied between B-E terminals and output is taken between collector and emitter terminals.
- * This configuration is most widely used as an inverting amplifier. It generates a phase shift of 180° at the output.

Consider npn transistor connected in common emitter configuration. Similar to CB configuration, B-E junction is forward biased and C-B junction is reverse biased by the supplies V_{BB} & V_{CC} . The negative terminal of V_{BB} repel the electrons in the emitter and hence current flows through the emitter and base to the collector to contribute collector current.

- * In CE configuration, input current is I_B and output current is I_C . The emitter current I_E is equal to the sum of small base current I_B and large collector current I_C .

Input characteristics:

It is a graph obtained between input current I_B and input voltage V_{BE} with constant output voltage V_{CE} .

→ This configuration provides good current gain and voltage gain.

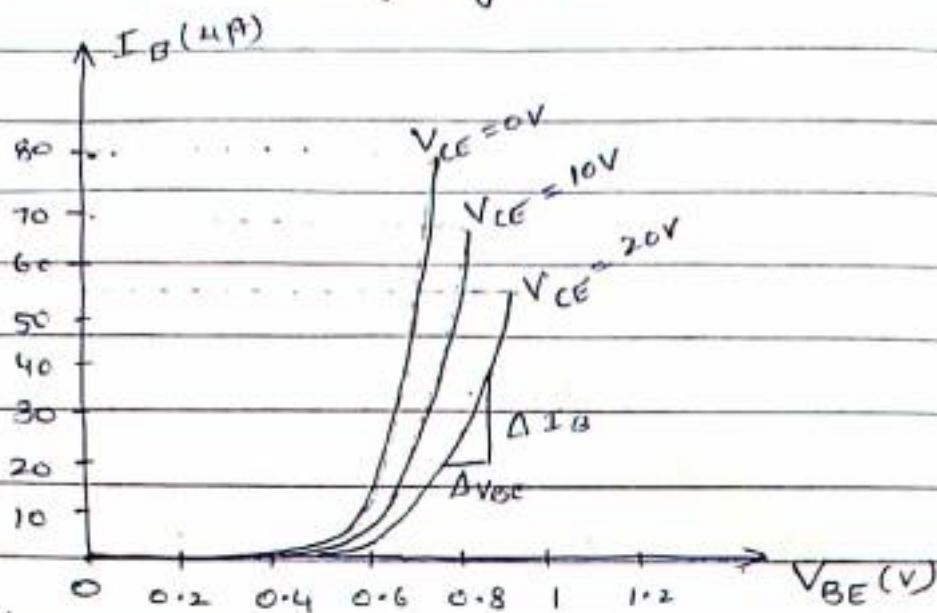


Fig: Input characteristics of CE configuration.

- * When V_{CE} is set constant, for a small increase in V_{BE} , the base current I_B increases rapidly as shown in the graph.
- * When the o/p voltage V_{CE} is set as 1V, B-E junction is forward biased by the supply V_{BB} . The B-E junction acts like a normal p-n junction. Hence, i/p characteristic curves are same as forward biased characteristics of a pn junction diode. ($S_i = 0.7V$) .
- * I_B is only a small portion of the total current I_C that flows across the BE junction.
- * When the output voltage V_{CE} is set to higher levels, for the applied input voltage V_{BE} I_B reduces continuously as shown in the graph.

This is because, the higher V_{CE} produces greater depletion region penetration of CB junction into the base, hence reducing the distance between C-B and E-B depletion regions. Therefore more charge carriers flow across the CB junction and few flow out through the base terminal.

- Hence in the graph, it can be observed that for a small change in V_{BE} , with large V_{CE} , I_B reduces and the curves are shifted towards right side.

Current amplification factor β

The ratio of change in collector current ΔI_C to the change in base current ΔI_B is known as common emitter current gain β .

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Input resistance

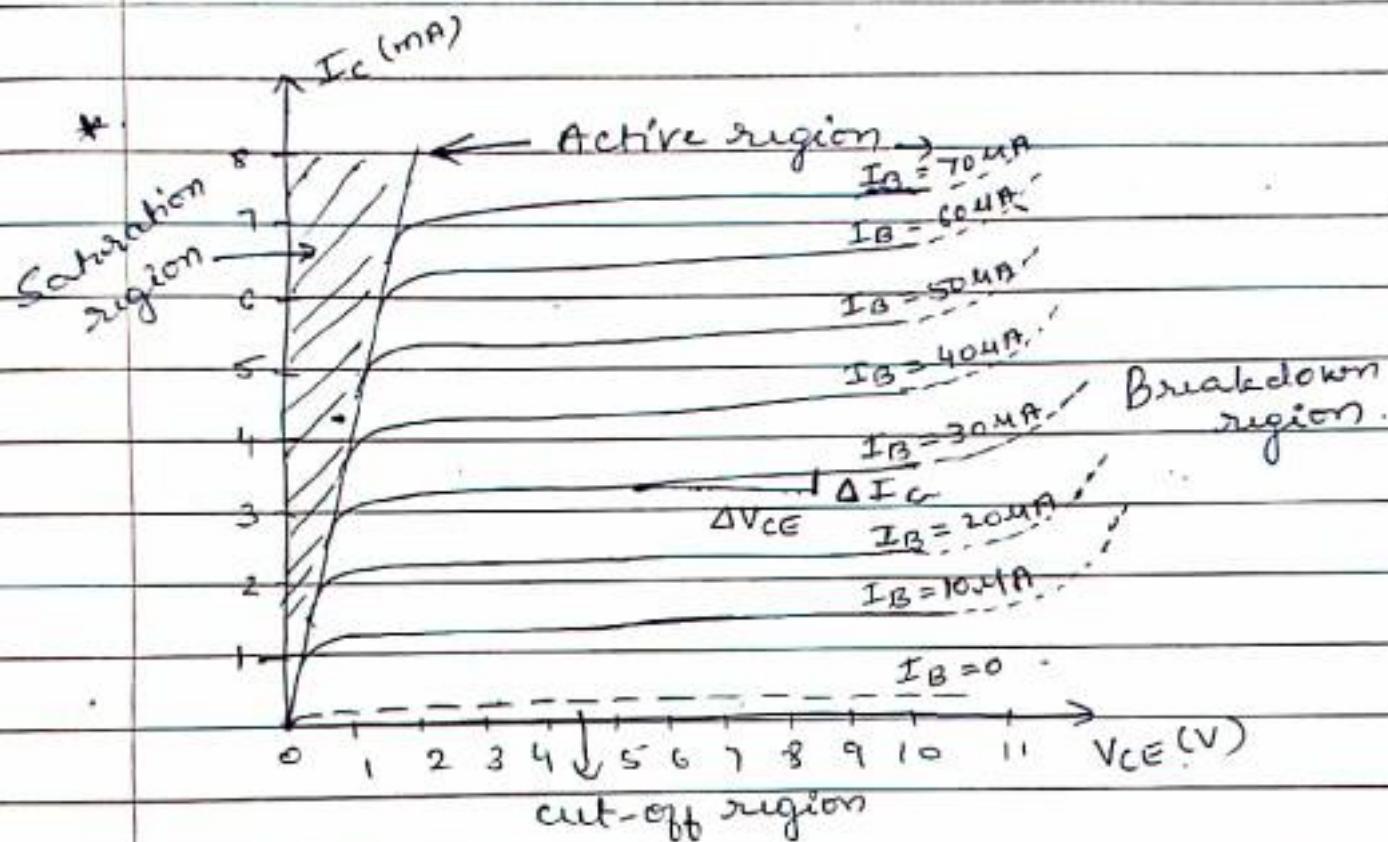
The ratio of change in base-emitter voltage ΔV_{BE} to change in base current ΔI_B at constant collector-emitter voltage V_{CE} is known as input resistance.

$$i_c \quad r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad | V_{CE} \text{ constant.}$$

Output characteristics

It is obtained between output current and output voltage with constant i/p current.

The output characteristics of CE configuration is drawn as a graph of variation in I_C with V_{CE} when the base current I_B is held constant.



- * Even though I_B is constant, I_C increases to some extent with increase in V_{CE} causing the slopes in CE characteristics to be more pronounced than that of CB characteristics (observable).
- * When V_{CE} is increased to a higher value beyond a limit, the CB junction breaks down and normal transistor action is lost. This causes I_C to increase rapidly damaging the device. It is called as breakdown region.

Three regions of operation in the o/p characteristics are

1. When E-B junction is forward biased and C-B junction is reverse biased, the transistor is said to be in active region. In this region the transistor acts as an amplifier. The collector current I_c increases slightly as collector-emitter voltage V_{CE} increases thereby generating a slope.
2. The region that lies to the left of the curve is called as saturation region. In this region, both E-B junction and C-B junction are forward biased and the device acts as a closed switch. When V_{CE} falls, I_c also decreases rapidly.
3. In cut-off region, both E-B junction and C-B junction are reverse biased and hence no current flows through the transistor. Now the transistor acts as an open switch.

Output resistance:

- * The ratio of change in C-E voltage to that of the change in collector current I_c at a constant base current I_B is known as output resistance r_o .

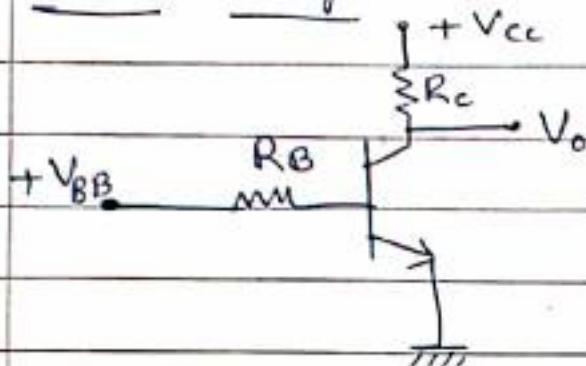
$$r_o = \frac{\Delta V_{CE}}{\Delta I_c} \quad | \text{ with } I_B \text{ constant.}$$

Applications .

1. Transistor as a switch.

Transistor can be made to operate as ON/OFF switch.

Circuit diagram.



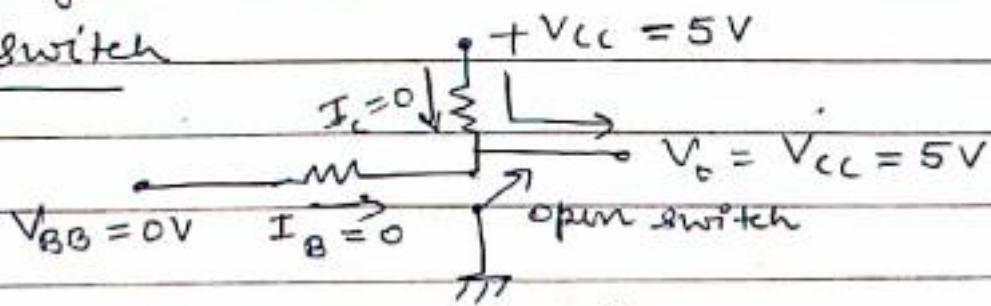
case 1: when base voltage $V_{BB} = 0V$. Both BE and CB junctions are reverse biased.

No base current I_B flows. Hence $I_C = 0$.

\therefore C and E terminals are open circuited.

Transistor acts as an open switch and the output V_o is $V_o = V_{CC}$.

open switch



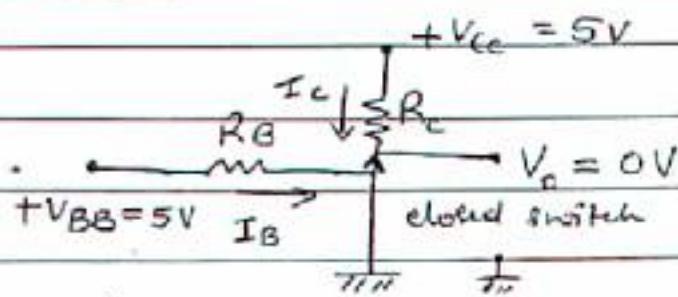
\therefore Transistor is in cut-off state.

Case 2: when a higher level of base voltage V_{BB} is applied, Both BF and CB junctions are forward biased. A large base current I_B flows due to $+V_{BB}$ that makes collector current to reach saturation level.

C & E
Hence collector and emitter terminals are short circuited and the output voltage is $V_o = 0V$. with a saturation collector current being a maximum value of

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

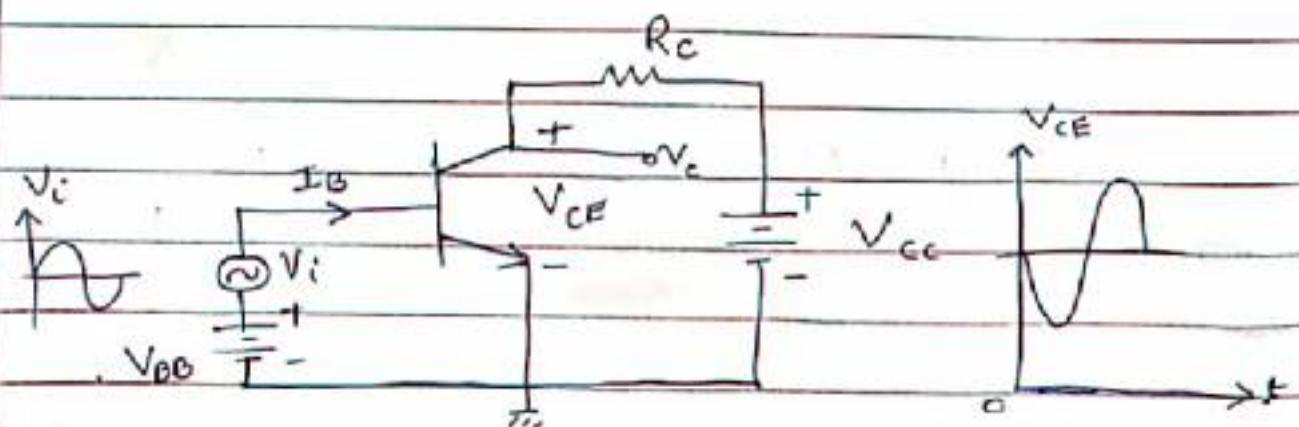
closed switch



\therefore Transistor is in saturation.

Basic amplifier operation (CE)

A transistor in CE configuration is shown below that operates as an amplifier.



A battery V_{BB} is connected along with a ac signal voltage V_i . The dc voltage V_{BB}

is known as bias voltage and its magnitude is such that it always keeps the E-B junction forward biased.

Working:

During +ve half cycle of the ac signal, ac and dc voltages will get added together that increases the forward bias on B-E junction. Hence more electrons flow from emitter to the collector through the base. This increases the collector current, i.e. $I_c = \beta I_B$. This increase in I_c produces voltage drop across R_c that will increase.

Since $V_c = V_{cc} - I_c R_c$, increase in I_c increases $I_c R_c$ voltage drop for a fixed V_{cc} . Hence the collector terminal voltage V_c reduces (moves in -ve direction).

During negative half cycle of ac signal, a-c and d.c voltages oppose each other and hence forward bias voltage across B-E junction decreases. There is a decrease in base current which in turn decreases collector current.

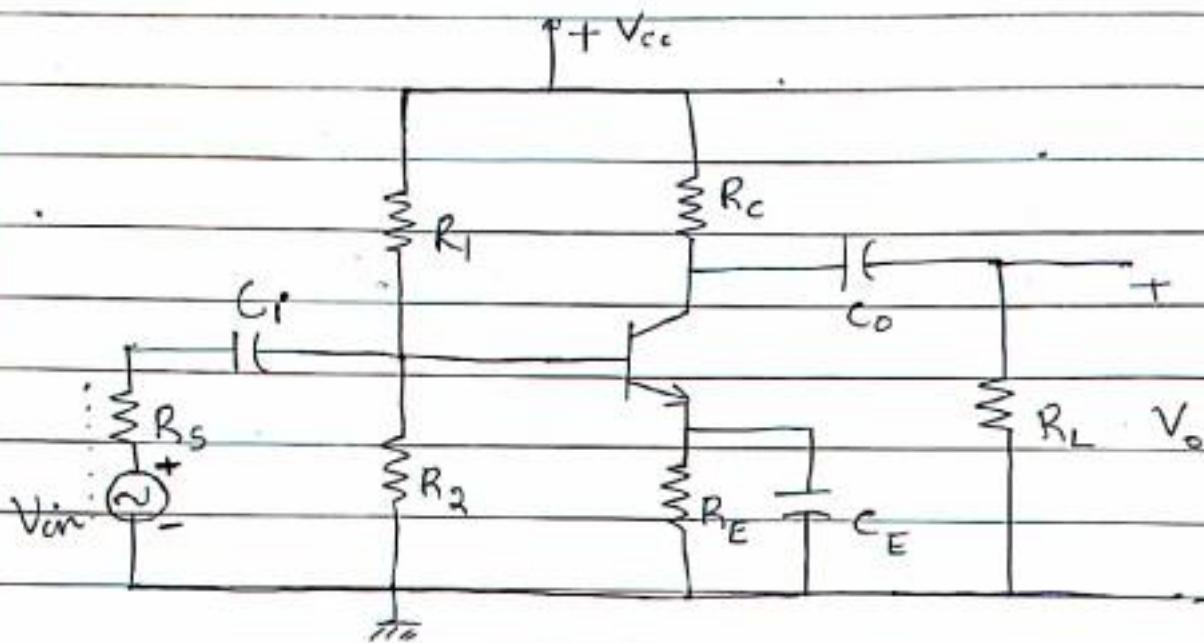
This reduces the $I_c R_c$ voltage drop with fixed V_{cc} .

Since $V_c = V_{cc} - I_c R_c$, the collector terminal voltage (o/p) increases (moves in +ve direction). Hence an amplified o/p signal can be obtained.

CE - RC Coupled amplifier (Single Stage)

Single stage RC coupled amplifiers are designed to improve the strength of the weak signals for the further amplification process.

Circuit diagram.



CE - RC coupled amplifier.

Circuit description and working:

Significance of the components.

The source V_{in} is a small signal ac connected in series with source resistance R_s & coupling capacitor C_i .

- * The i/p coupling capacitor C_i couples the small signal ac V_{in} to the base of the transistor. It acts as a filter and blocks the dc components and allows only ac voltage to the base of the transistor for amplification.

If any external dc voltage reaches the base of the transistor, it alters the dc biasing conditions and hence affects the performance of the amplifier.

- * Biasing circuit: Resistors R_1 and R_2 provide the necessary biasing to the transistor base. $R_1 + R_2$ form an voltage divider biasing n/w. It generates a necessary base voltage to drive the transistor in active region.
- * Resistor R_E provides stabilization & R_C is a current-limiting resistance. The values of R_C and R_E are selected in such a way that both should drop V_{CC} by 50%.
- * Emitter bypass capacitor C_E is connected in parallel to R_E . This capacitor provides a low impedance path to the amplified ac signal. (low voltage drop a/c R_E to increase the gain)

NOTE: If C_E is not connected, the amplified ac signal passes through R_E and causes a large voltage drop across it, thereby output voltage will reduce hence reducing the gain of the amplifier.

- * Output coupling capacitor C_O is connected at the collector to block dc and allows only ac signal components to pass. It is coupled to the load or next stage amplifier.

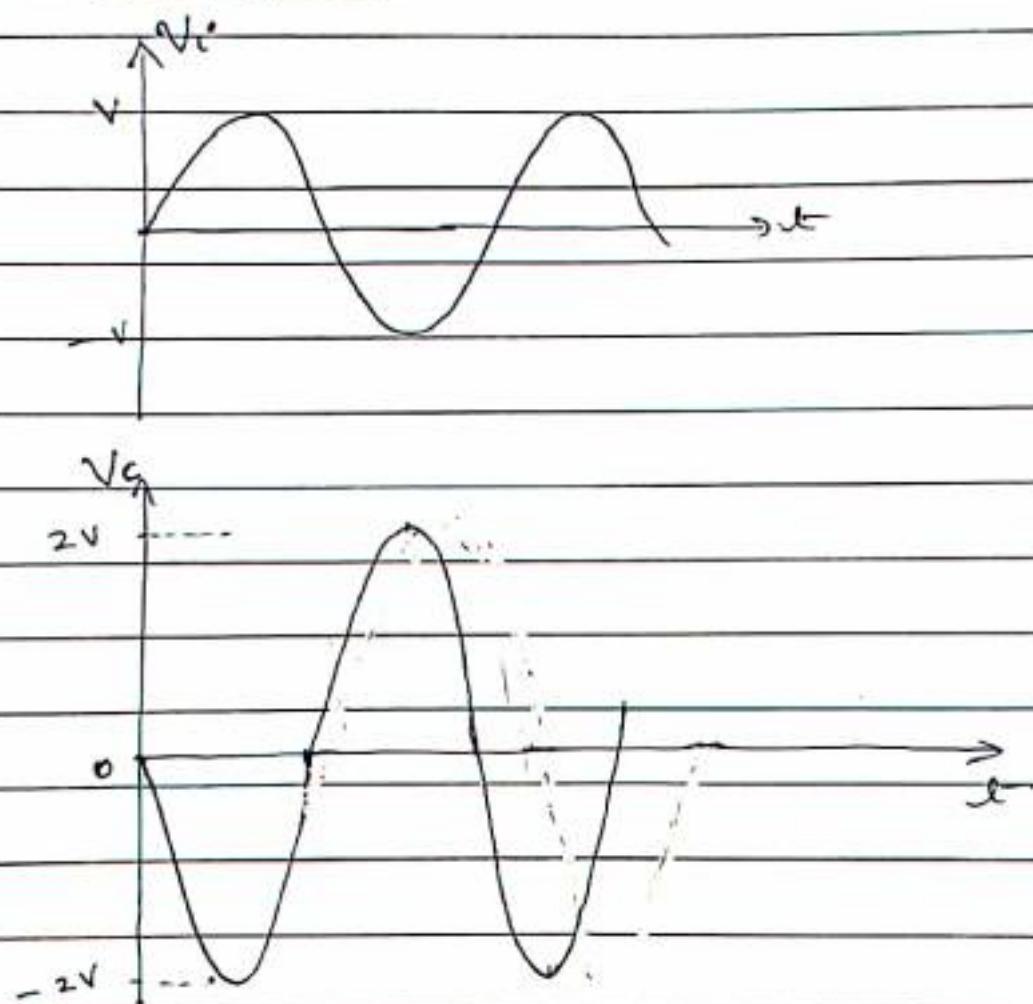
Phase reversal concept :

- * During positive half cycle of i/p signal V_i , ac and dc voltages get added together that forward biases B-E junction. This increases the base current I_B . Also collector current I_c increases since $I_c = \beta I_B$. Due to increase in I_c , it produces voltage drop $I_c R_c$ that will increase.
- * Since $V_c = V_{cc} - I_c R_c$, increase in I_c increases $I_c R_c$ voltage drop for a fixed V_{cc} . Hence, the collector terminal voltage V_c reduces (moves in -ve direction).
- * During negative (-ve) half cycle of ac i/p signal, V_i , ac and dc voltages oppose each other reducing forward bias across B-E junction. This reduces the base current I_B thereby reducing the collector current I_c . This reduces the voltage drop $I_c R_c$ across R_c . Since $V_c = V_{cc} - I_c R_c$, for a fixed value of V_{cc} , when $I_c R_c$ reduces, V_c increases. (moves in +ve direction).

Thus, as V_i increases in a positive direction, V_c goes in -ve direction and hence we get a negative half cycle of o/p voltage for positive half cycle at the i/p.

Similarly we obtain a positive half cycle at the output for a negative half cycle at the input. Hence we say that there exists a phase shift of 180° between i/p and o/p Voltage for CE amplifier.
(Inverting amplifier).

Waveforms



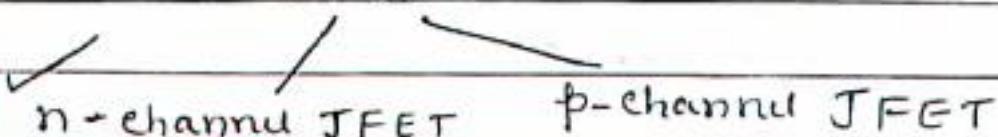
Field Effect Transistor.

- * Field Effect Transistor known as FET is a 3 terminal semiconductor device in which current flows is only due to one of the 2 kinds of charge carriers namely electrons or holes. Hence it is a unipolar device.
- * BJT is a current controlled device (I_B controls I_C in CE config) while FET is a voltage controlled device. (i/p v_g controls o/p current)
- * FET construction is simple compared to BJT.
+ less die area in an integrated circuit. (I_C)
- * It is less noisy than BJT.
- * Low power consumption & are used in CMOS circuits.
- * Input resistance is high compared to BJT

2 types of FETs are

1. Junction Field Effect Transistor (JFET)
2. Metal oxide Semiconductor Field Effect Transistor (MOSFET)

1. JFET



2. MOSFET

Depletion type

n-channel

p-channel

Enhancement type

✓ n-channel

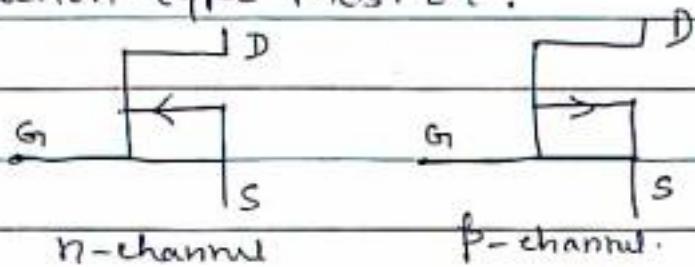
p-channel

MOSFET

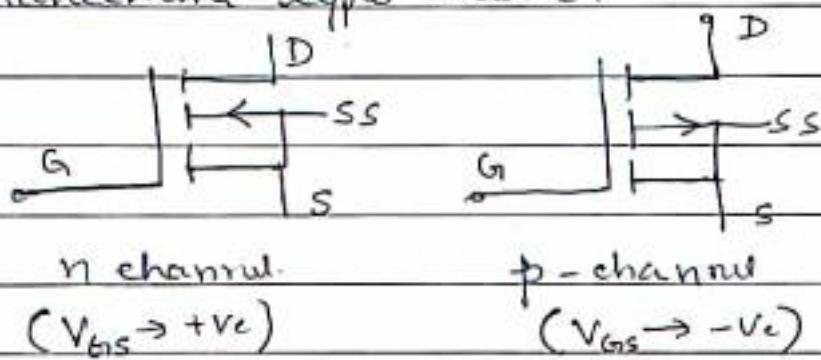
(Metal Oxide Semiconductor Field Effect Transistor)

Two types of MOSFETs based on the mode of operation are:

1. Depletion type MOSFET.

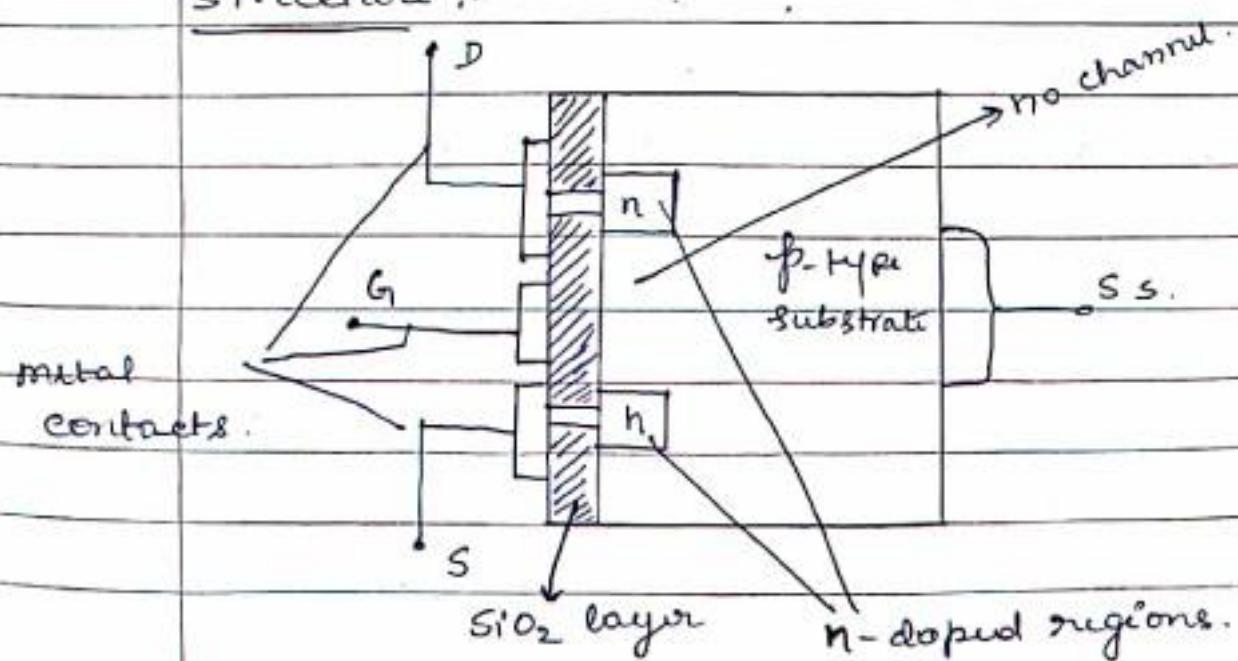


2. Enhancement type MOSFET.



n-channel Enhancement type MOSFET (n-EMOSFET)

Structure:



Basic Construction

- * A slab of p-type material is formed from a silicon base and is referred to as substrate. The substrate is internally connected to the source terminal.
- * The source and drain terminals are connected through metallic contacts to the n-doped regions. There is an absence of channel between the two n-doped regions.
- * SiO_2 layer is present to isolate the gate metallic platform from drain & the source terminals.

Basic operation and drain characteristics of n-channel MOSFET

- * If V_{GS} is set to 0V and a +ve voltage is applied between drain and source terminals, the absence of an n-channel will result in a current of zero mA.
- * Both V_{GS} and V_{DS} are set at some positive voltage greater than zero Volts. This establishes a positive potential between the drain and gate w.r.t to the source.

- * The positive potential at the gate will pressurize the holes in p-substrate along the edge of SiO_2 layer to leave the area and enter deeper regions of the p-substrate, as in fig (a)

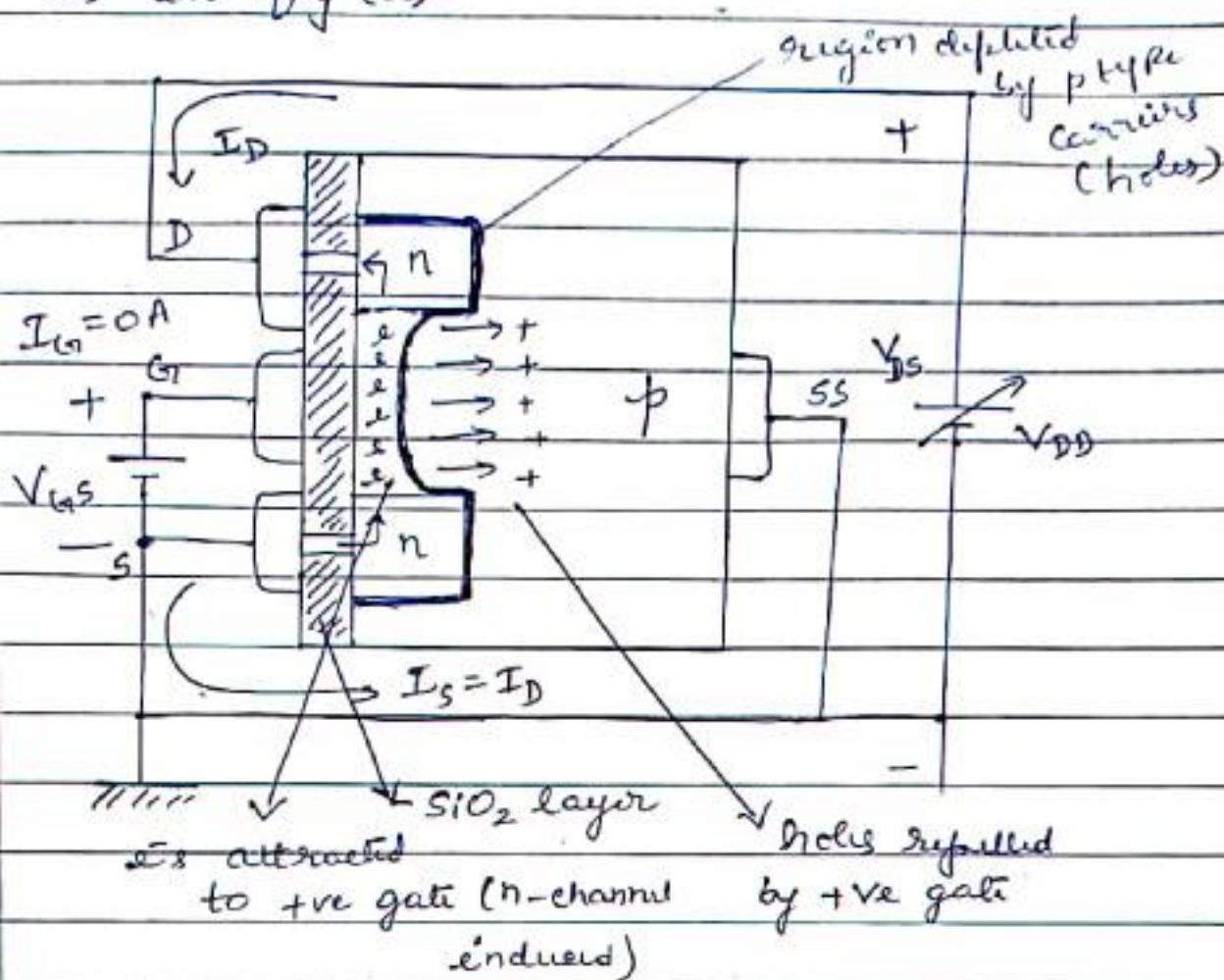


Fig (a) channel formation in n-channel MOSFET.

- * Hence this results in a depletion region near SiO_2 insulating layer void (emptied) of holes.
- * The electrons (minority carrier) in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of SiO_2 layer.

- * The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed by the gate.
- * As V_{GS} increases in magnitude, the concentration of electrons near SiO_2 surface increases until it can control the flow of current between drain and source.
- * The level of V_{GS} that results in significant increase in drain current is called as threshold voltage V_T .
- * Since the channel is non-existent with $V_{GS} = 0V$ and is enhanced by the application of positive gate to source voltage, the type of MOSFET is called as an enhancement type MOSFET.
- * As V_{GS} is increased beyond the threshold level V_T , $V_{GS} > V_T$, the density of free carriers in the induced channel will increase resulting in increased drain current I_D .
- * If V_{GS} is held constant, and V_{DS} is increased, the drain current reaches a saturation level. At this condition, pinching off.

takes place and the channel becomes narrow towards the drain as shown in Fig (b)

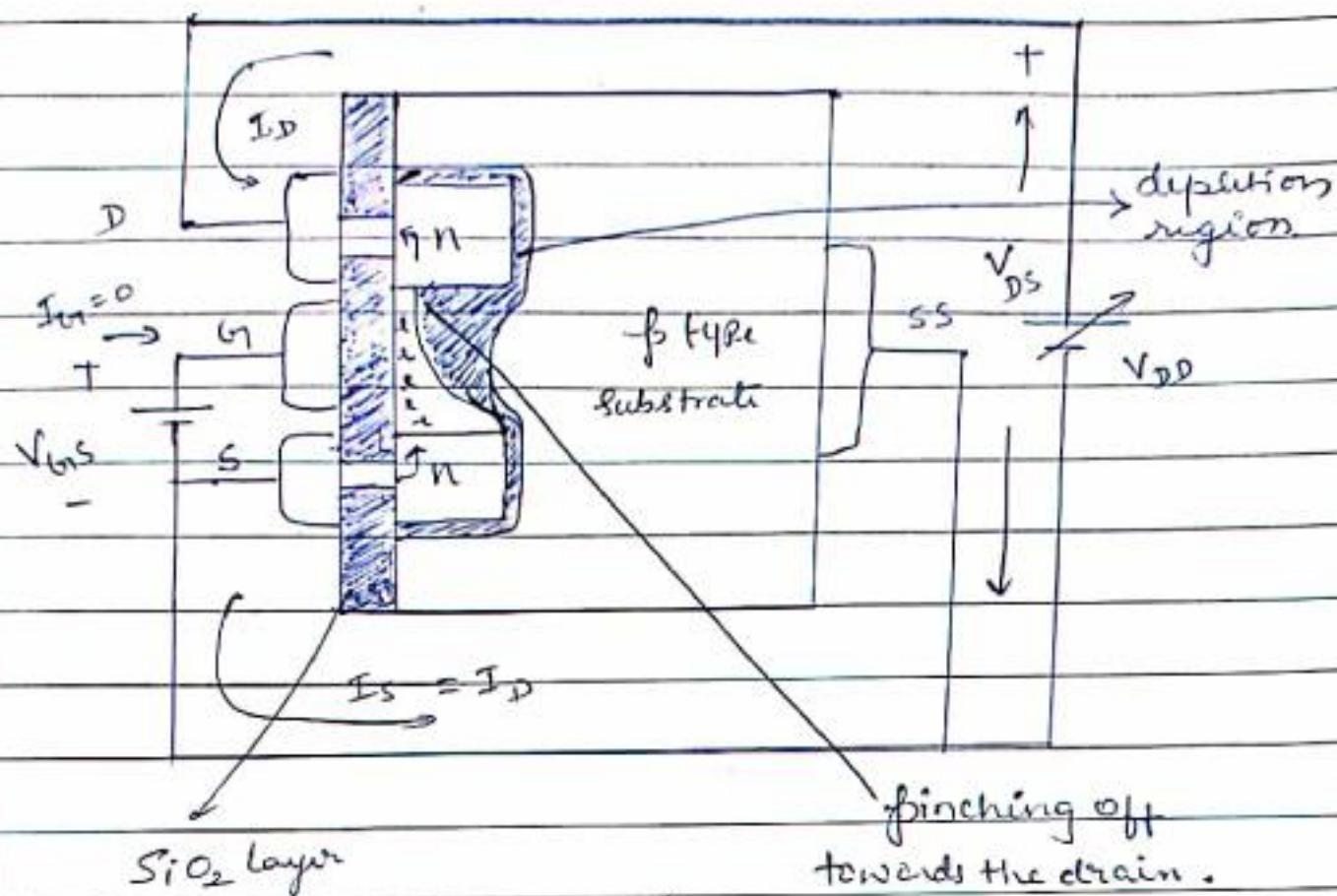


Fig 5) change in channel width near the drain at V_{GS} constant and increase in V_{DS} .

- * with V_{GS} held constant and V_{DS} is increased, the gate to drain Voltage V_{DG} will drop & gate will be less and less positive w.r.t drain.
- * This reduction in G to Drain voltage cause a reduction in channel width. Hence, the channel will be reduced to a point of pinch off and a saturation condition will be established.

$$V_{DS(\text{sat})} = V_{GS} - V_T$$

when V_{GS} is less than V_T , the drain current drops to 0mA and hence the device switching to off state.

{ For $V_{GS} < V_T$, $I_D = 0 \text{ mA}$
 For $V_{GS} > V_T$, I_D depends on V_{GS} .
 applied by a nonlinear relation

$$I_D = k (V_{GS} - V_T)^2$$

$$k \text{ is a constant} = 0.278 \times 10^{-3} \text{ A/V}^2$$

$$k = \frac{I_D(\text{on})}{(V_{GS} - V_T)^2} \quad \begin{matrix} \text{n channel} \\ \rightarrow V_{GS} + V_T \end{matrix}$$

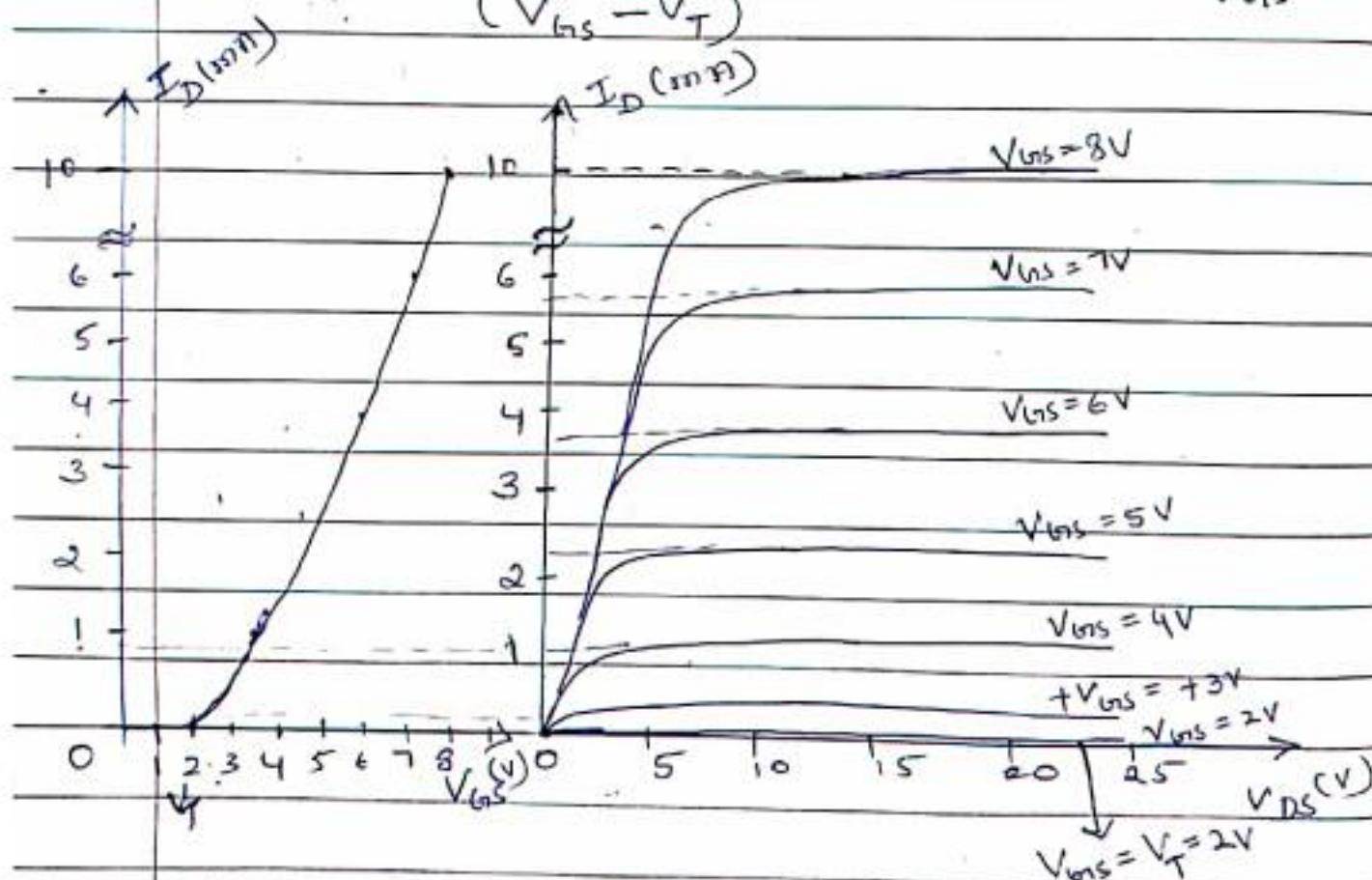


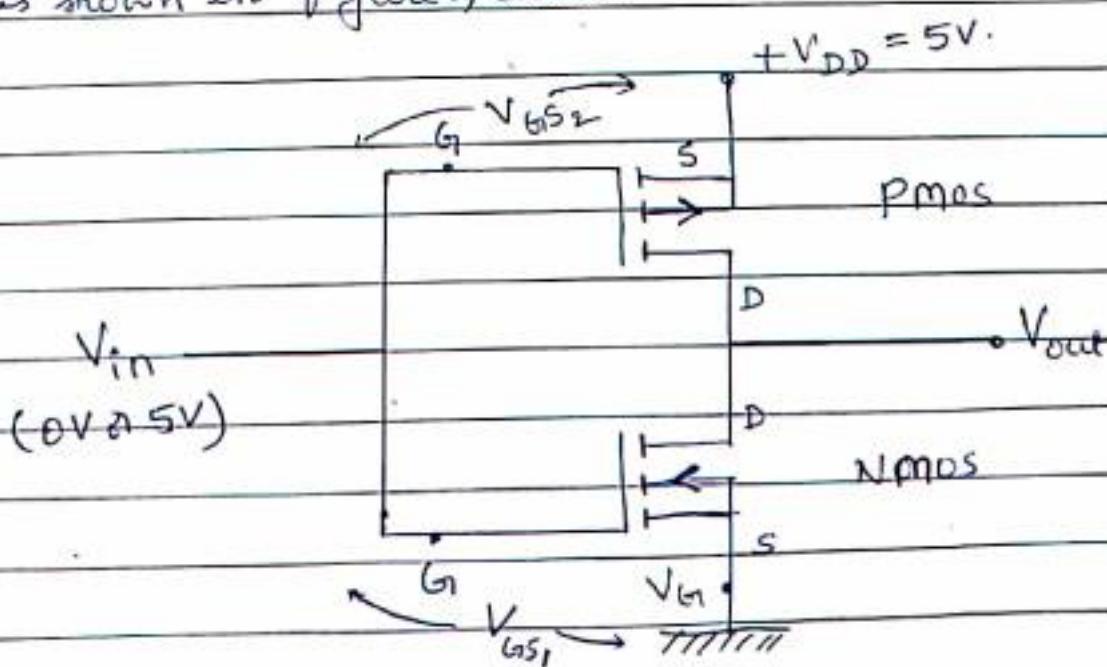
Fig 9) Drain and transfer characteristics of a n-channel MOSFET.

CMOS Inverter

(2)

CMOS \rightarrow Complementary MOS, It uses ~~two~~ MOSFETs & E-MOSFETs for its construction

- + A p-channel and n-channel E-MOSFETs when placed on the same substrate, it is known as Complementary MOS.
- + It has low input impedance, fast switching speeds and less power consumption.
- + It is used in computer logic design.
- + one n-type mos (NMOS) and one p-type mos (PMOS) are connected in pairs to form CMOS.
- + Gates of the 2 devices are connected to form input terminals and 2 drain terminals are connected together to form o/p terminal, as shown in figure a) below.



What makes you happy? Fig a) CMOS inverter. # _____
HappyCollegeDays # _____

Operation

Case 1: when $V_{in} = 5V$ (state 1)

$$\begin{aligned} V_{G_{S2}} &= V_{in} - V_{DD} \\ &= 5 - 5 = 0V. \end{aligned}$$

Hence PMOS is non conducting or OFF.

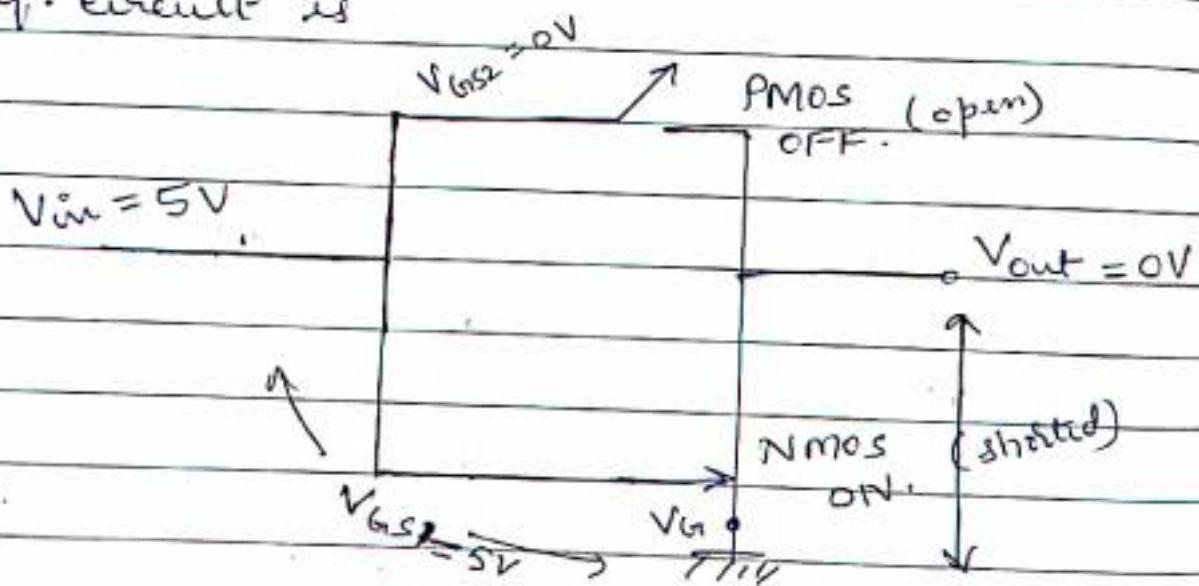
(open circuited). It offers high resistance.

+

$$\begin{aligned} V_{G_{S1}} &= V_{in} - V_G \\ &= 5 - 0 = 5V. \end{aligned}$$

Therefore for $V_{G_{S1}} = 5V$, NMOS is conducting or ON (short circuited to ground). It offers low resistance.

Eq. circuit is



\therefore NMOS is ON with low resistance. Hence

$$\underline{V_{out} = 0V} \text{ (state 0)}$$

Case 2: when $V_{in} = 0V$ (state 0)

$$V_{G_{S2}} = 0 - 5 = -5V$$

For -ve gate voltage, PMOS is ON and acts as closed switch. It conducts

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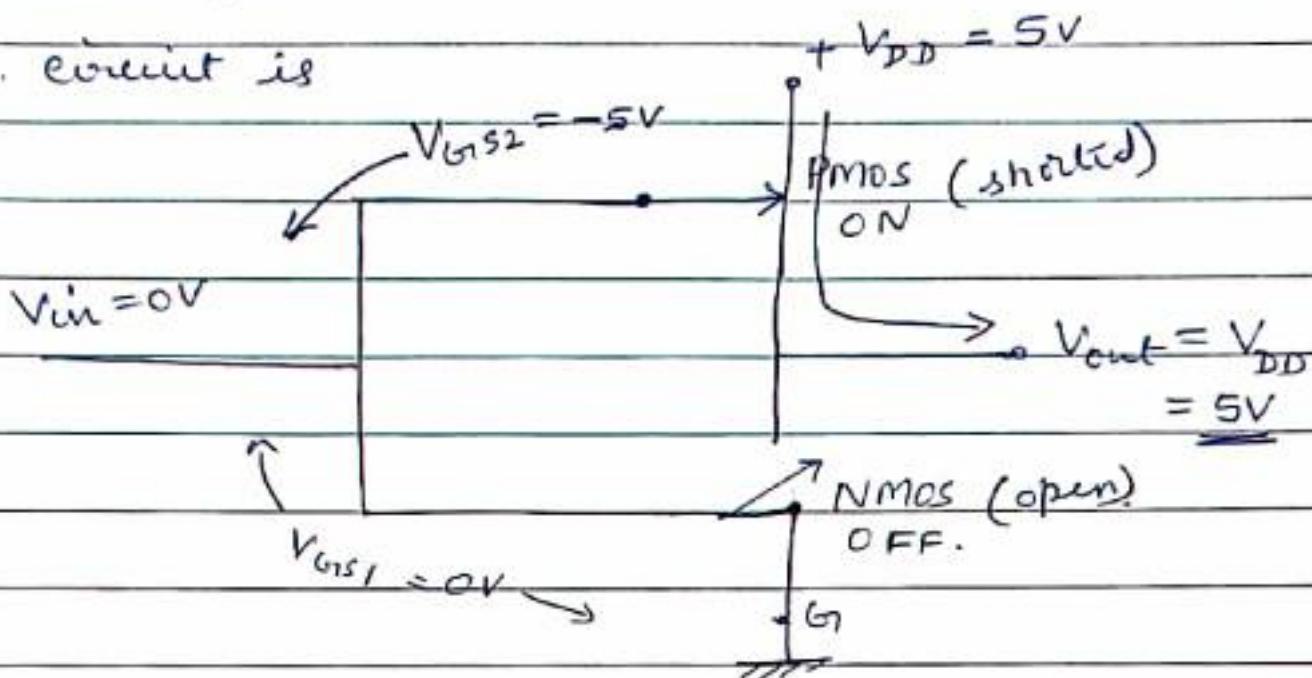
and offers low resistance.

$$\text{if } V_{GSI} = 0 - 0 = 0V.$$

Nmos is non conducting for $V_{GSI} = 0V$.

Hence it is OFF or open circuited. It offers high resistance.

Eq. circuit is



\therefore PMos is ON with $V_{out} = \underline{\underline{5V}}$ (static)