

Application of Flipflops: Design of Shift Register using D-flipflop, Design of counters: Asynchronous counters using T-flipflop, Synchronous counters using D-flipflop and T-flipflop.

#### \* Registers

Registers and counters are important applications of clocked flip-flops.

- \* A collection of flip-flops in cascade is called a register.
- \* Registers are used to store data in digital system.
- \* A cascade of  $H$  flip-flops configured as a register can store one nibble (4 bit) of data.
- \* A  $H$ -bit register can store binary bits from 0000 to 1111. These are called contents or states of a register. Thus a  $H$ -bit register has 16 possible states.

#### \* Shift registers:-

Shift registers are capable of moving or shifting the data stored in their flipflops in either direction.

- \* Consider a  $H$  bit shift register with data 0100 or decimal 4. A left shift results in .1000 or decimal 8, and a right shift results in 0010 or decimal 2.

Note: Each left shift has a "multiplication by 2" effect. Each right shift has a "division by 2" effect.

#### \* Classification of shift registers:-

##### I. Depending on data movement:-

1. Bi-directional : These are the shift registers which can shift data in both direction.

2. Unidirectional : those which can shift data in only one direction.

II. Based on whether data is input or output in-serial or in-parallel :-

1. Serial In - Serial Out (SISO) : Data entered serially and read serially.
2. Serial In - Parallel Out (SIPO) : Data entered serially and read in parallel.
3. Parallel In - Serial Out (PISO) : Data entered parallelly and read serially.
4. Parallel In - Parallel Out (PIPO) : Both entry and reading in parallel.

\* Serial In - Serial Out      Unidirectional shift register :-  
Not SISO - shift right.

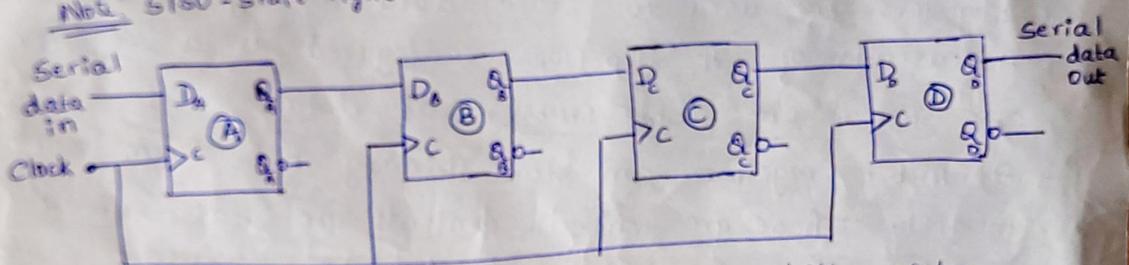


Fig: 4-bit SISO unidirectional shift register.

The D input of each flipflop is connected to the Q output of the previous stage to the left. When a clock pulse is applied to the 'C' input of flip-flop A, the data on the serial-in line gets stored in flip-flop A and appears at  $Q_A$ . Every bit is shifted one position to the right, the serial input is shifted into flip-flop A and content of flip-flop D gets shifted out and is lost.

\* SISO shift register capable of shifting data to the right and signal value shifted becomes available as an output after four clock pulses.

Eg: Let  $1011$  be the serial input. Initially  $Q_A Q_B Q_C Q_D = 0000$

Clock	Serial I/P	$Q_A$	$Q_B$	$Q_C$	$Q_D$
1	-	0	0	0	0
2	1	1	0	0	0
3	0	0	1	0	0
4	1	1	0	1	0
5	-	0	1	0	1
6	-	0	0	1	0

$Q_D$  is final serial out.  
all I/P bits appear at output  
after 7 clock pulses

→ serial out.

(2)

**★ Serial In Parallel Out Unidirectional Shift register:-**

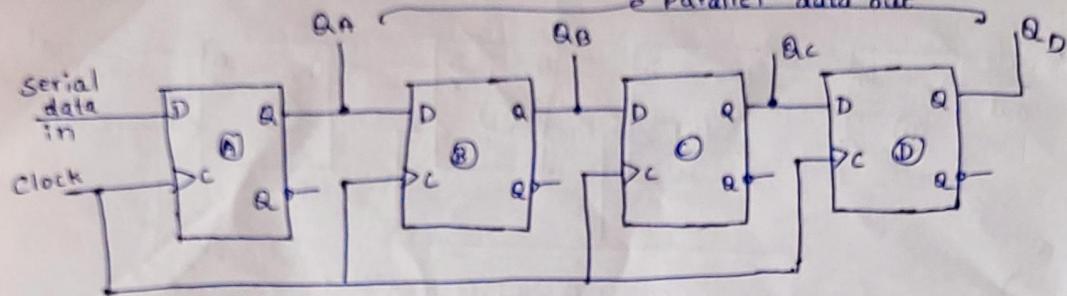


fig: SIPO shift register

4 bit serial in parallel out shift register can be used in serial to parallel conversion. Here once the 4-bit data is shifted in after 4 clock pulses, the data stored in each flip-flop is available at the respective Q outputs.

Here input is fed serially to first flip-flop and output is obtained parallelly from each flip-flop.

**★ Parallel in Parallel out Shift register:-**

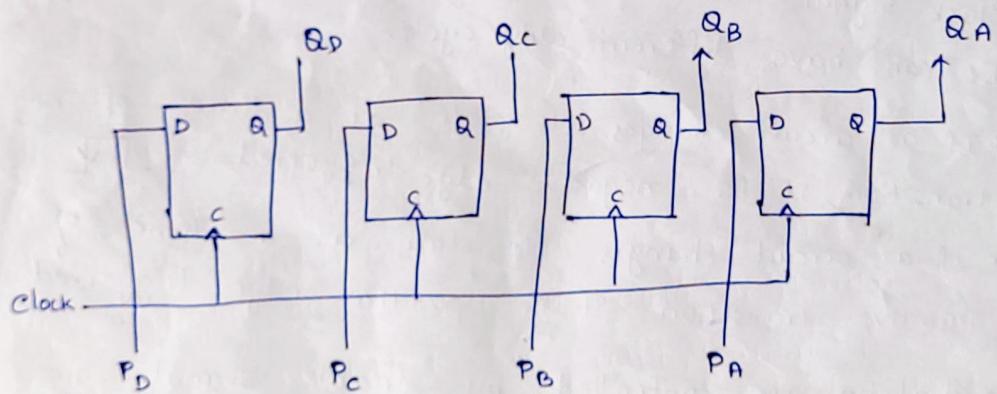


fig: PIPO shift register

Here  $P_A P_B P_C P_D$  indicates input which feed parallelly to each flip-flops and outputs are collected parallelly after the application of clock.  $Q_A Q_B Q_C Q_D$  indicates output.

Eg: If  $P_A P_B P_C P_D = 0101$  is inputs. After the application of clock  $Q_A Q_B Q_C Q_D = 0101$ .

i.e inputs appears as parallel outputs. in one clockpulse

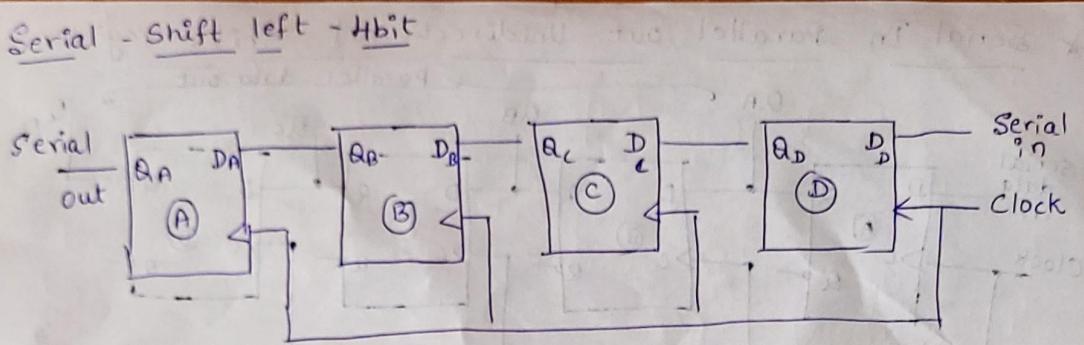
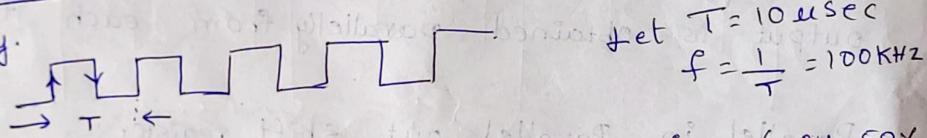


fig: SISO left shift register.

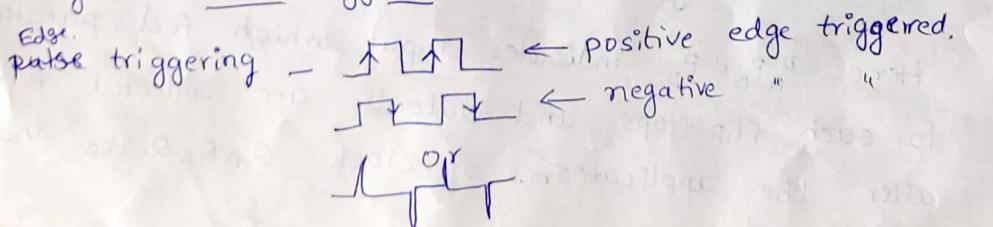
Here input is given to flipflop D. These serial inputs from flipflop D shifts left for the next stage after the application of clock. Input will appear at the last stage after 4 clock pulse.

Note:- Clock :- It is a train of pulses of fixed frequency.



Clock signal need not be a square waveform (with 50% duty cycle). It can have different duty cycle.

- \* If a circuit changes its state at a time of negative transition it is negative edge triggered.
- \* If a circuit changes its state at a time of positive transition, it is positive edge triggered.
- \* Latches are controlled by enable signal. They are level triggered.



## \* Counters

A counter is cascade of flipflops configured to output a specific sequence on application of a clock.

Each output of the sequence is dependent on the contents of the flipflops and is called state of the counter.

Modulus of a counter is the total number of states of the counter.

Eg: MOD-10 counter  $\rightarrow$  counts from 0 to 9 and then resets.

mod-6 counter  $\rightarrow$  counts from 0 to 5 and then resets.

Thus the counter with m states is called modulus-m or mod-m counter.

Counters can be represented using a state diagram.

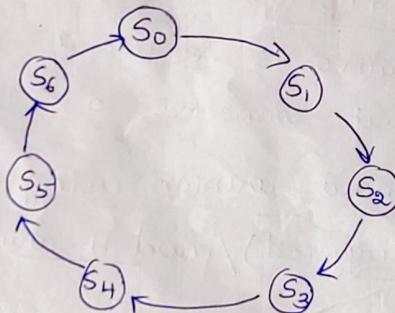


fig: State diagram of mod-7 counter.

## \* Types of counters:-

1. Synchronous counters
2. Asynchronous counters.

### 1. Synchronous counter :-

\* The common clock input is connected to all the flipflops and thus they have clocked simultaneously. Thus change of state is determined from the present state.

### 2. Asynchronous counter :-

\* Also called as ripple counter.

\* No common clock.

\* The first flipflop is clocked by the external clock pulse

and then each successive flipflop is clocked by Q &  $\bar{Q}$  o/p of previous flipflop.

- \* Thus flipflop output transition serves as a source for triggering other flipflops.

### \* Asynchronous counters :-

A binary ripple/ asynchronous counter consists of a series connection of complementing flipflops with the output of each flipflop connected to the clock input of the next higher order flipflop.

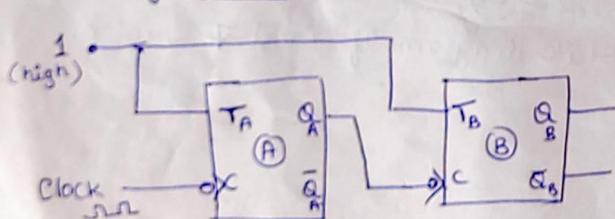
\* A flipflop holding the least significant bit receives the incoming clockpulse.

\* Complementing flipflops can be obtained from JK flipflop with J and K inputs tied together or from a T flipflop.

A third alternative is to use a D flipflop with complement output connected to D input.

### 2 bit asynchronous counter using T flipflop

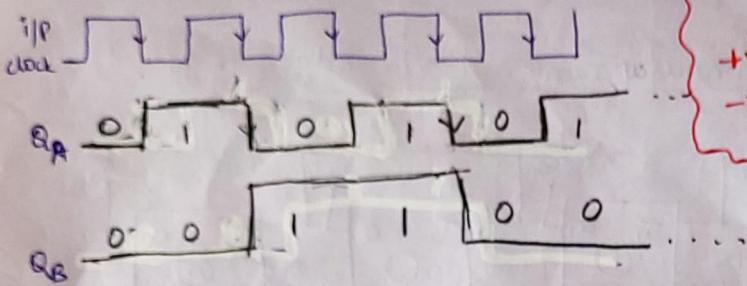
#### (Negative edge triggered) / mod 4 counter



QB	QA	count
0	0	0
0	1	1
1	0	2
1	1	3

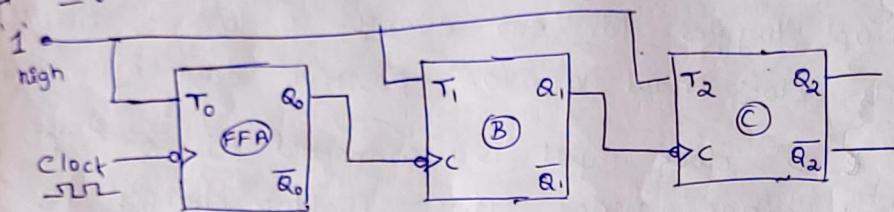
- \* The clock signal is connected to the clock input of first stage flipflop. The clock input of second stage flipflop is triggered by Q<sub>A</sub> output of first stage.
- \* Here two flipflops never triggered simultaneously.
- \* Here the changes in the state of the flipflop o/p's occur due to change in the clock.
- \* Since input T is high, output toggle for each negative edge of clock input
- \* This is a mod-4 counter counts from 0 to 4 & then resets.

## Timing diagram:-



		UP	DOWN
+ve	$\bar{Q}$	$Q$	
-ve	$Q$	$\bar{Q}$	

\* 3 bit ripple up / Asynchronous up counter (negative edge triggered) :-

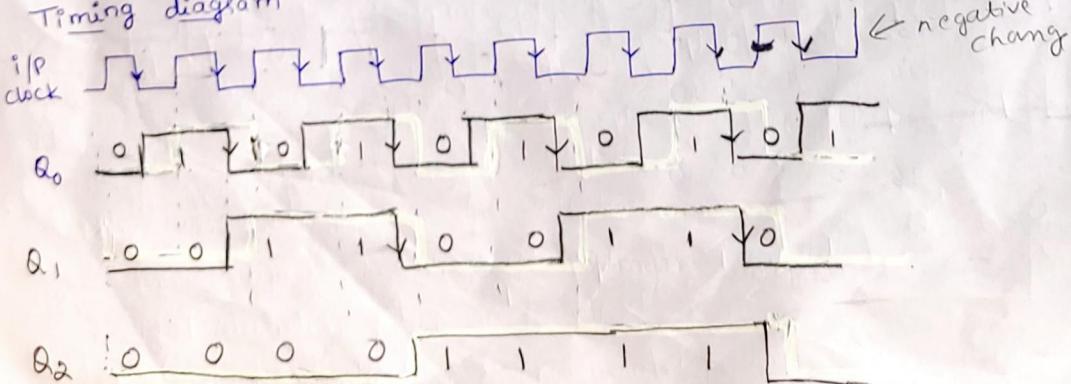


- \* This is a mod-8 counter counts from 000 to 111 and then resets.
- \* 3-bit counter has 3 T flip-flops cascaded in series
- Note:- Refer the theory given for 2 bit counter and write here.

## Count sequence

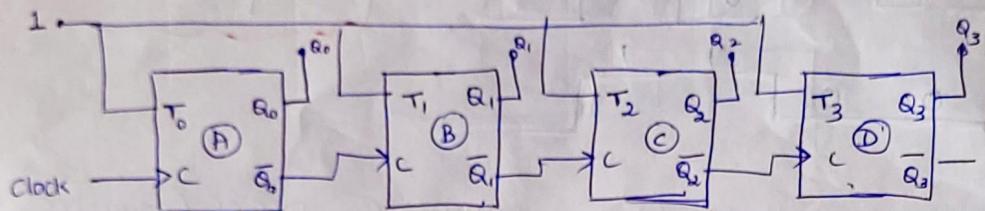
clock	MSB		LSB		$\bar{Q}_0$
	$Q_2$	$Q_1$	$Q_0$	$\bar{Q}_0$	
0	0	0	0	1	1
1	0	0	1	0	0
2	0	1	0	1	+
3	0	1	1	0	0
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	1	0
7	1	1	1	0	0
8	0	0	0	1	0

## Timing diagram



HW Design a 4-bit ripple counter using -ve edge triggered T flipflop.

\* 4 bit asynchronous upcounter (+ve edge triggered)



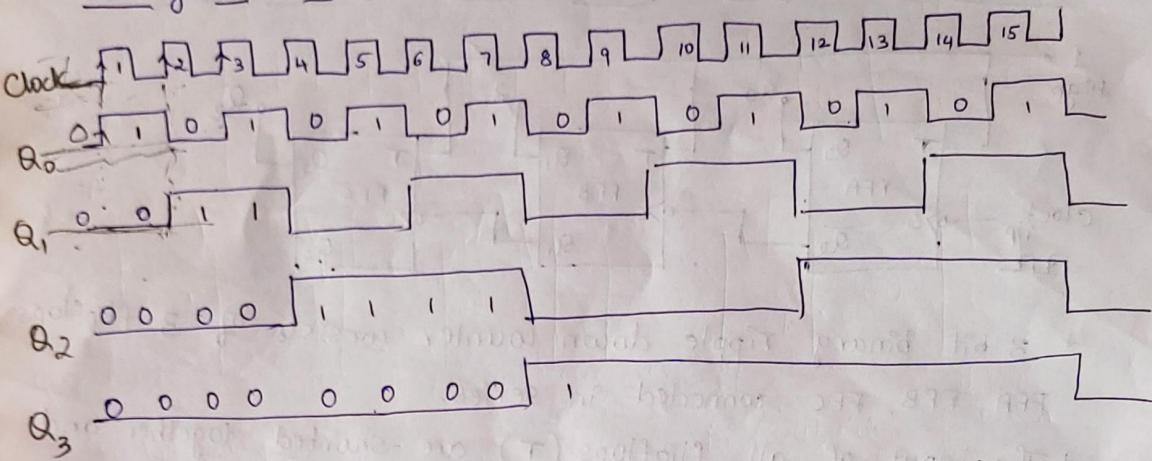
\* This is mod 16 up counter. The output of each flipflop toggles for every 0 to 1 transition of its clock input or for positive edge of clock.

\* FFB, C, D clock input is connected to  $\bar{Q}$  of previous stage. Hence these flipflop changes its state on 1 to 0 transition of  $Q$  which is same as 0 to 1 transition of  $\bar{Q}$  outputs.

Clock	$Q_3$	$Q_2$	$Q_1$	$Q_0$	$\bar{Q}_0$
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	.
3	0	0	1	1	.
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	0	1	0
11	1	0	1	0	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	0
16	0	0	0	0	1

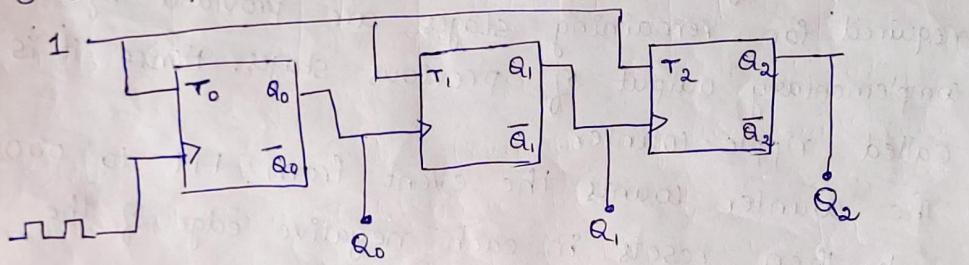
sequence repeats

## Timing diagram



\* Binary ripple down counter (+ve edge triggered) :-

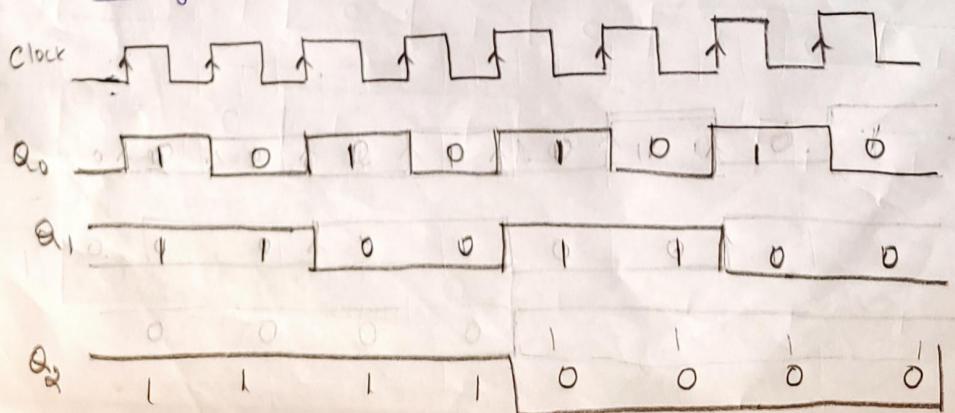
3 bit ripple down counter :-



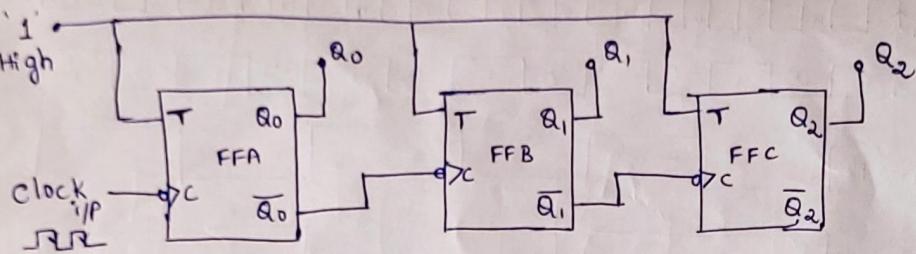
Count sequence

clock	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0

Timing diagram :-



\* 3 bit binary ripple down counter (Negative edge triggered)



\* 3 bit binary ripple down counter consists of 3 flipflops FFA, FFB, FFC connected in series.

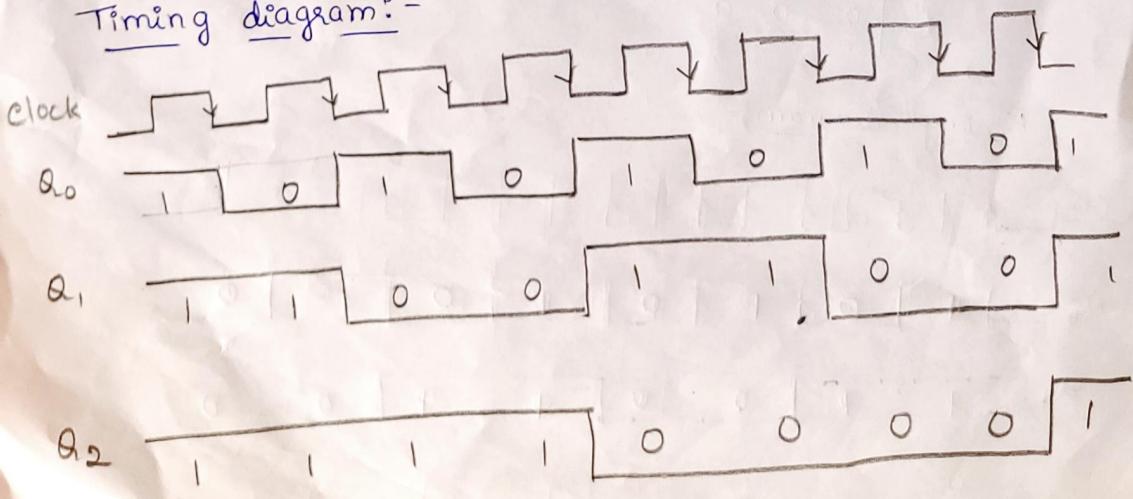
\* The input of all flipflops (T) are shorted together and a logic high '1' signal is applied.

\* The clock signal is given to FFA. The clock signal required for remaining stages are provided by the complementary output of previous stages. Hence it is called ripple counter.

\* The counter counts the event from 111 to 000 and then resets in each negative edge of the clock.

\* A 4-bit counter can be designed by connecting 4 flipflop in series. Similarly n-bit counter has 'n' flipflops. n bit counter counts from 0 to  $2^n$  values.  
Eg: 4 bit counter - counts (0 to  $2^4 = 16$ ) values ie 0000-1111  
hence it is mod-16 counter.

Timing diagram:-



## \* Design of synchronous counter:-

Besides the binary sequence, synchronous counters can be designed to output any random sequence.

Eg: Synchronous counter mod-5 with sequence 100-101-001-111 → 101 & repeat.

→ can be designed using JK, SR, D and T flipflops.

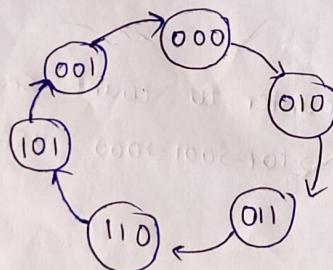
1) Design synchronous mod-6 counter which counts the events 000 → 010 → 011 → 110 → 101 → 001 using clocked D flipflops.

$$0 \rightarrow 2 \rightarrow 3 \rightarrow 6 \rightarrow 5 \rightarrow 1 \rightarrow 0$$

Step 1 :- Application table for a clocked D flipflop :-

Row. No.	$Q_2$	$Q_1$	$Q_0$	D
0	0	0	0	0
1	0	1	1	1
2	1	0	0	0
3	1	1	1	1

State diagram for the sequence is,



Step 2 : Excitation table for mod-6 counter :-

cell. No.	Present state			Next state.			Flipflop i/p's		
	$Q_2$	$Q_1$	$Q_0$	$Q_2^+$	$Q_1^+$	$Q_0^+$	$D_2$	$D_1$	$D_0$
0	0	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	0	0	0
2	0	1	0	0	1	1	0	1	1
3	0	1	1	1	1	0	1	1	0
4	1	0	0	X	X	X	X	X	X
5	1	0	1	0	0	1	0	0	1
6	1	1	0	1	0	1	1	0	1
7	1	1	1	X	X	X	X	X	X

Step 3:- Find expressions for  $D_2, D_1, D_0$  in terms of  $Q_0, Q_1, Q_2$ . using K-map.

$Q_2, Q_0$	00	01	11	10
0	0	0	1	0
1	X	0	X	1

$$D_2 = Q_1 Q_0 + Q_2 Q_1$$

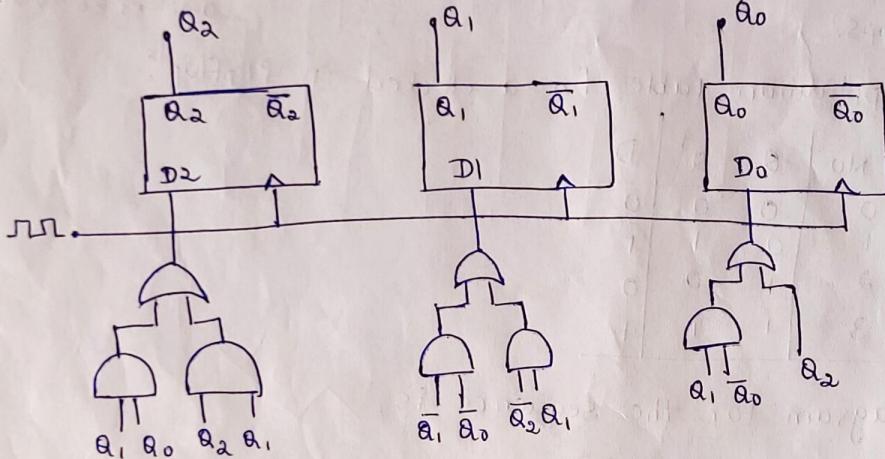
$Q_2, Q_0$	00	01	11	10
0	1	0	1	1
1	X	0	X	0

$$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_2 Q_1$$

$Q_2, Q_0$	00	01	11	10
0	0	0	0	1
1	X	1	1	X

$$D_0 = Q_2 + Q_1 \bar{Q}_0$$

Step 4:- Implementation



Ques: Design synchronous counter to count sequence

000  $\rightarrow$  010  $\rightarrow$  011  $\rightarrow$  110  $\rightarrow$  101  $\rightarrow$  001  $\rightarrow$  000 using T flipflop.

$$\text{Ans: } T_2 = Q_2 \bar{Q}_1 + Q_1 Q_0$$

$$T_1 = \bar{Q}_1 \bar{Q}_0 + Q_2 Q_1$$

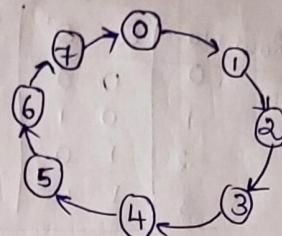
$$T_0 = Q_1 + \bar{Q}_2 Q_0$$

2) Design 3-bit synchronous up counter using T flipflop.

Step 1:- Application table for T flipflop:-

Row.No	$Q$	$Q^+$	T
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

state diagram



Step 2:- Excitation table:-

cell no.	Present state			Next state			Flipflop inputs		
	$Q_2$	$Q_1$	$Q_0$	$Q_2^+$	$Q_1^+$	$Q_0^+$	$T_2$	$T_1$	$T_0$
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	1	1	0	0	1	1
6	1	1	0	1	1	1	0	0	1
7	1	1	1	0	0	0	1	1	1

Step 3 : k-map

For  $T_2$  :-

$Q_1, Q_0$	00	01	11	10
$Q_2$	0	0	1	0
	0	0	1	0

$$T_2 = Q_1, Q_0$$

For  $T_1$  :-

$Q_1, Q_0$	00	01	11	10
$Q_2$	0	1	1	0
	0	1	1	0

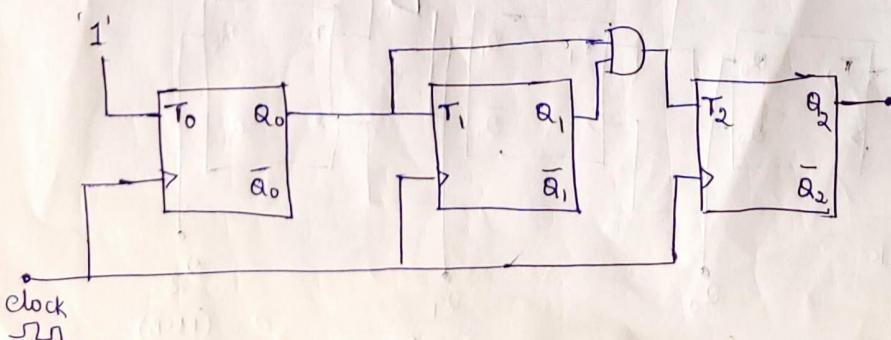
$$T_1 = Q_0$$

For  $T_0$  :-

$Q_1, Q_0$	00	01	11	10
$Q_2$	1	1	1	1
	1	1	1	1

$$T_0 = 1$$

Implementation :-

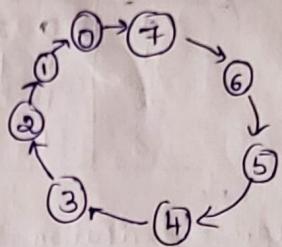


3) Design a synchronous 3-bit down counter using positive edge triggered T flipflops.

Step 1 :- Application table for TFF:

Row No.	$Q$	$Q^+$	$T$
0	0 0	0	0
1	0 1	1	
2	1 0	1	
3	1 1	0	

State diagram



Step 2 :- Excitation table

cell no.	present state			next state			flipflop input		
	$Q_2$	$Q_1$	$Q_0$	$Q_2^+$	$Q_1^+$	$Q_0^+$	$T_2$	$T_1$	$T_0$
0	0 0 0			1	1	1	1	1	1
1	0 0 1			0	0	0	0	0	1
2	0 1 0			0	0	1	0	1	1
3	0 1 1			0	1	0	0	0	1
4	1 0 0			0	1	1	1	1	1
5	1 0 1			1	0	0	0	0	1
6	1 1 0			1	0	1	0	1	1
7	1 1 1			1	1	0	0	0	1

Step 3 : K map

For  $T_2$ :

$B_1B_0$	00	01	11	10
0	1	0	0	0
1	0	0	0	0

$$T_2 = \bar{Q}_1 \bar{Q}_0$$

For  $T_1$ :

$B_1B_0$	00	01	11	10
0	1	0	0	1
1	1	0	0	1

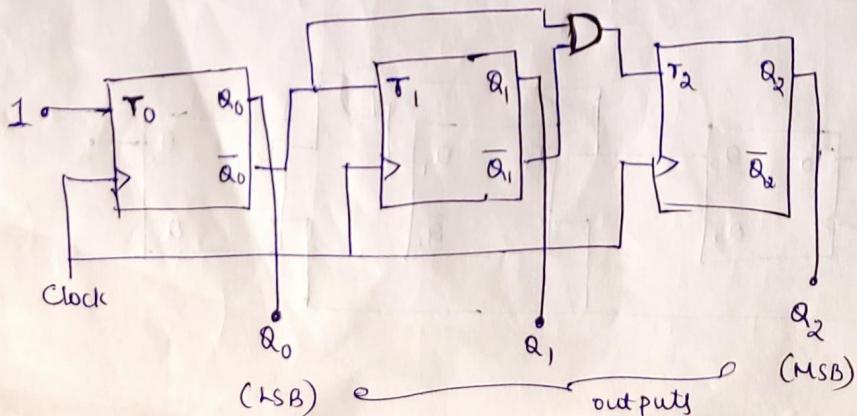
$$T_1 = \bar{Q}_0$$

For  $T_0$ :

$B_1B_0$	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$$T_0 = 1$$

Implementation :-

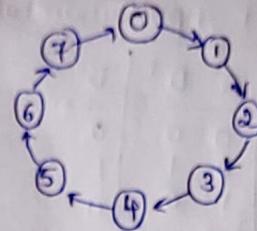


4) Design a synchronous 3-bit up counter using positive edge triggered D flipflops.

Step 1: Application table.

Row No	$Q_2$	$Q_1$	D
0	0	0	0
1	0	1	1
2	1	0	0
3	1	1	1

State diagram



Step 2: Excitation table:-

Cell No.	Present State			Next State			Flip flop input		
	$Q_2$	$Q_1$	$Q_0$	$Q_2^+$	$Q_1^+$	$Q_0^+$	$D_2$	$D_1$	$D_0$
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	0
2	0	1	0	0	1	1	0	1	1
3	0	1	1	1	0	0	1	0	0
4	1	0	0	1	0	1	1	0	1
5	1	0	1	1	1	0	1	1	0
6	1	1	0	1	1	1	1	1	1
7	1	1	1	0	0	0	0	0	0

Step 3: K-map

For  $D_2$ :

$Q_1, Q_0$	00	01	11	10
$Q_2$	0	0	1	0
0	0	1	1	0
1	1	0	0	1

$$D_2 = Q_1 Q_0 \bar{Q}_2 + Q_2 \bar{Q}_0 + Q_2 \bar{Q}_1 \\ Q_1 Q_0 \bar{Q}_2 + Q_2 (\bar{Q}_0 + \bar{Q}_1)$$

For  $D_1$ :

$Q_1, Q_0$	00	01	11	10
$Q_2$	0	0	1	1
0	0	1	0	1
1	0	1	0	1

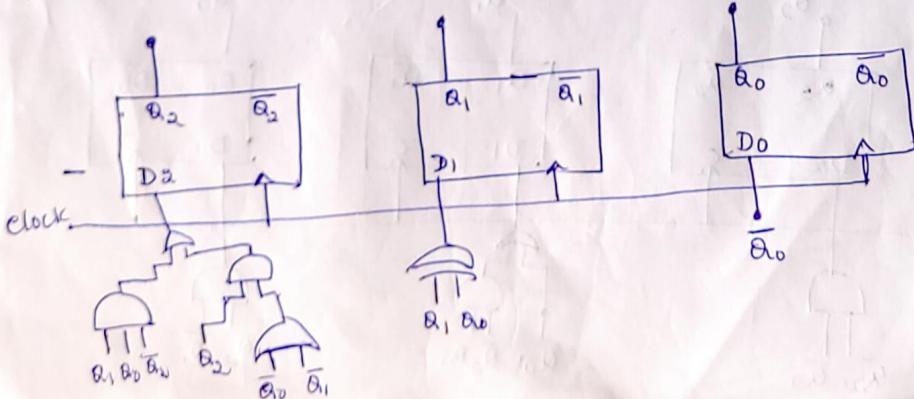
$$D_1 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0 \\ = Q_1 \oplus Q_0$$

For  $D_0$ :

$Q_1, Q_0$	00	01	11	10
$Q_2$	0	1	0	1
0	1	0	0	1
1	1	0	0	1

$$D_0 = \bar{Q}_0$$

Implementation:-



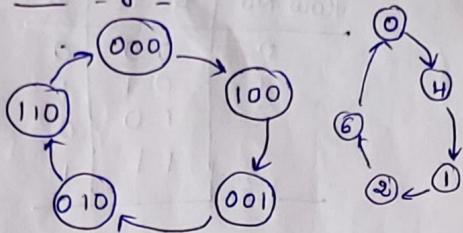
⑤ Design a synchronous counter to sequence

$0 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0$  using D flipflops with minimal combinational gating.

Step 1: Application table

R.No.	Q	$Q^+$	D
0	0	0	0
1	0	1	1
2	1	0	0
3	1	1	1

state diagram



② Excitation table

cell. No.	Present state			Next state			Flipflop inputs		
	$Q_2$	$Q_1$	$Q_0$	$Q_2^+$	$Q_1^+$	$Q_0^+$	$D_2$	$D_1$	$D_0$
0	0	0	0	1	0	0	1	0	0
1	0	0	1	0	1	0	0	1	0
2	0	1	0	1	1	0	1	1	0
3	0	1	1	X	X	X	X	X	X
4	1	0	0	0	0	1	0	0	1
5	1	0	1	X	X	X	X	X	X
6	1	1	0	0	0	0	0	0	0
7	1	1	1	X	X	X	X	X	X

③ K map

For  $D_2$ :

$Q_2$	$Q_1$	$Q_0$	00	01	11	10
0	1	0	X	1		
1	0	X	X	0		

$$D_2 = \overline{Q}_2 \overline{Q}_0$$

For  $D_1$ :

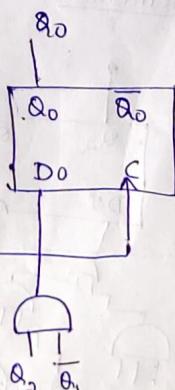
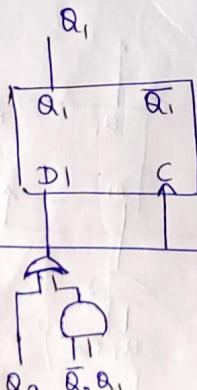
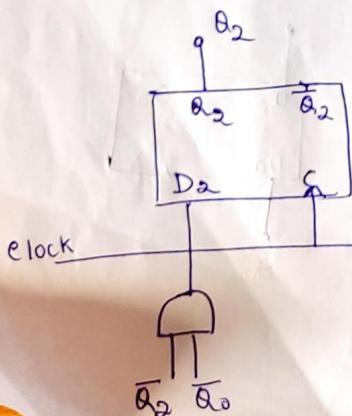
$Q_2$	$Q_1$	$Q_0$	00	01	11	10
0	0	1	(X)	1		
1	0	(X)	X	0		

$$D_1 = Q_0 + \overline{Q}_2 Q_1$$

For  $D_0$ :

$Q_2$	$Q_1$	$Q_0$	00	01	11	10
0	0	0	X	0		
1	(X)	X	X	0		

$$D_0 = Q_2 \overline{Q}_1$$



Home work  $0 \rightarrow 1 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 0$  using D FlipFlop