Problem statement : Apply PassII of a two-pass Assembler to the following given data structures and generate the machine code:

1) **Intermediate Code (IC)**

IC for Opcode	IC for Operand1	IC for Operand2
(AD,01)	(C,200)	
(IS,04)	(1)	(L,01)
(IS,05)	(1)	(S,01)
(IS,04)	(1)	(S,01)
(IS,04)	(3)	(S,03)
(IS,01)	(3)	(L,02)
(IS,04)	(1)	(S,01)

(IS,04)	(3)	(S,03)
(IS,04)	(1)	(S,01)
(IS,04)	(3)	(S,03)
(IS,04)	(1)	(S,01)
(IS,07)	(6)	(S,04)
(DL,01)	(C,5)	
(DL,01)	(C,1)	
(IS,04)	(1)	(S,01)
(IS,02)	(1)	(L,03)

(IS,07)	(1)	(S,05)
(IS,00)		
(AD,03)	(S,02)+2	
(IS,03)	(3)	(S,03)
(AD,03)	(S,06)+1	
(DL,02)	(C,1)	
(DL,02)	(C,1)	
(AD,02)		
(DL,01)	(C,1)	

2) Symbol Table (SYMTAB)

Symbol	Address
A	217
LOOP	202
B	218
NEXT	214
BACK	202
LAST	216

Literal Table (LITTAB)

Literal	Address
5	211
1	212
1	219

Solution

Intermediate Code (IC)			Machine Code			
IC for Opcode	IC for Operand1	IC for Operand2	LC	Machine code for Opcode	Machine code for Operand1	Machine code for Operand2
(AD,01)	(C,200)		No Machine Code			
(IS,04)	(1)	(L,01)	200)	04	1	211
(IS,05)	(1)	(S,01)	201)	05	1	217
(IS,04)	(1)	(S,01)	202)	04	1	217
(IS,04)	(3)	(S,03)	203)	04	3	218
(IS,01)	(3)	(L,02)	204)	01	3	212

(IS,04)	(1)	(S,01)	205)	04	1	217
(IS,04)	(3)	(S,03)	206)	04	3	218
(IS,04)	(1)	(S,01)	207)	04	1	217
(IS,04)	(3)	(S,03)	208)	04	3	218
(IS,04)	(1)	(S,01)	209)	04	1	217
(IS,07)	(6)	(S,04)	210)	07	6	214
(DL,01)	(C,5)		211)	00	0	005
(DL,01)	(C,1)		212)	00	0	001
(IS,04)	(1)	(S,01)	213)	04	1	217

(IS,02)	(1)	(L,03)	214)	02	1	219
(IS,07)	(1)	(S,05)	215)	07	1	202
(IS,00)			216)	00	0	000
(AD,03)	(S,02)+2		No Machine Code			
(IS,03)	(3)	(S,03)	204)	03	3	218
(AD,03)	(S,06)+1		No Machine Code			
(DL,02)	(C,1)		217)	No Machine Code	No Machine Code	No Machine Code
(DL,02)	(C,1)		218)	No Machine Code	No Machine Code	No Machine Code
(AD,02)			No Machine Code			

(DL,01)	(C,1)		219)	00	0	001