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TECHNOLOGY, RESEARCH, SOCIAL INNOVATION & PARTNERSHIPS

T. Y. B. Tech (Electrical and Computer Engineering)

Trimester: V **Subject: Microcontroller and Applications**
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Roll No: 52 **Batch: A3**

Experiment No: 10

Name of the Experiment: Interfacing EEPROM using SPI with C8051F340

Performed on: 05/12/2023

Submitted on: 07/12/2023

Marks	Teacher's Signature with date

Aim: Write a program to write and read data on SPI based EEPROM.

Apparatus: EPBF340 board, ASK25 board, Connectors

Theory:

The Enhanced Serial Peripheral Interface (SPI0) of C8051F340 provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus.

SPI0 four wire Master Mode Operation is used to read and write data on EEPROM. The four signals used by SPI0 are MOSI, MISO, SCK, NSS.

SPI0CFG, SPI0DAT, and SPI0CN SFRs of SPI are configured to select 4 wire master mode.

SPI clock frequency is configured using following formula.

SPI0CKR = (SYSCLK/(2*SPI_CLOCK))-1

25AA160 16 Kbit Serial Electrically Erasable PROMs is used. The memory is accessed via a simple Serial Peripheral Interface compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (CS) input.

Data written data on EEPROM and read from EEPROM is displayed on LCD.

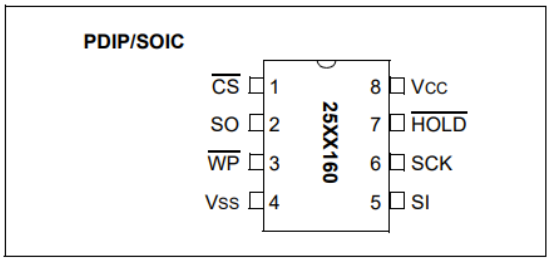

Figure 9.1 EEPROM 25AA160

Interfacing Diagram:

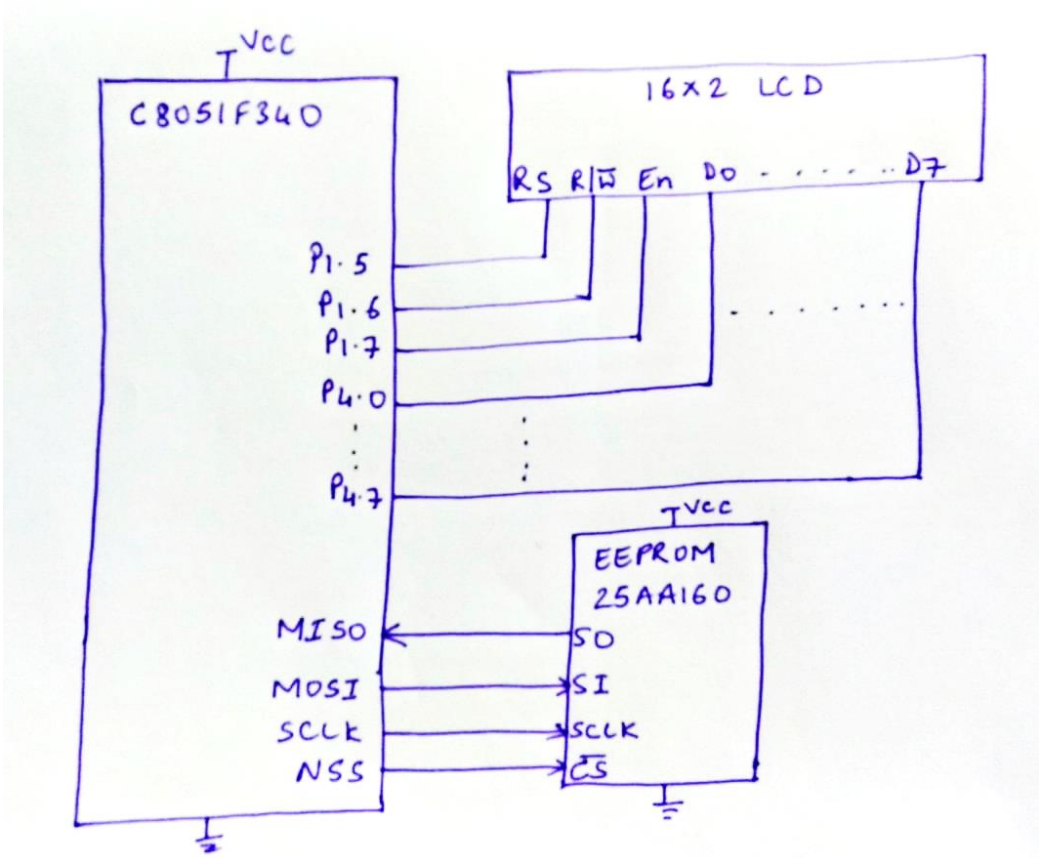

Figure 9.2 Interfacing Diagram EEPROM using SPI

Hardware Connections: Connect FRC cable between PL7 connector (SPI) of EPBF340 board and PL1 of ASK 25.
Connect flat cable between PL3 connector of ASK25 and PL3 connector of EPBF340 board.

Program: Attach printout of the tested code.

Expected Result:

EEPROM data should be displayed on LCD.

Conclusion:

Study Questions:

1. Explain SFRs of SPI0 in detail.
2. Compare SPI with I2C

Additional Links:

https://www.analog.com/en/analog-dialogue/articles/introduction-to-spi-interface.html

https://microcontrollerslab.com/introduction-to-spi-communication-protocol/

http://ww1.microchip.com/downloads/en/devicedoc/21231d.pdf

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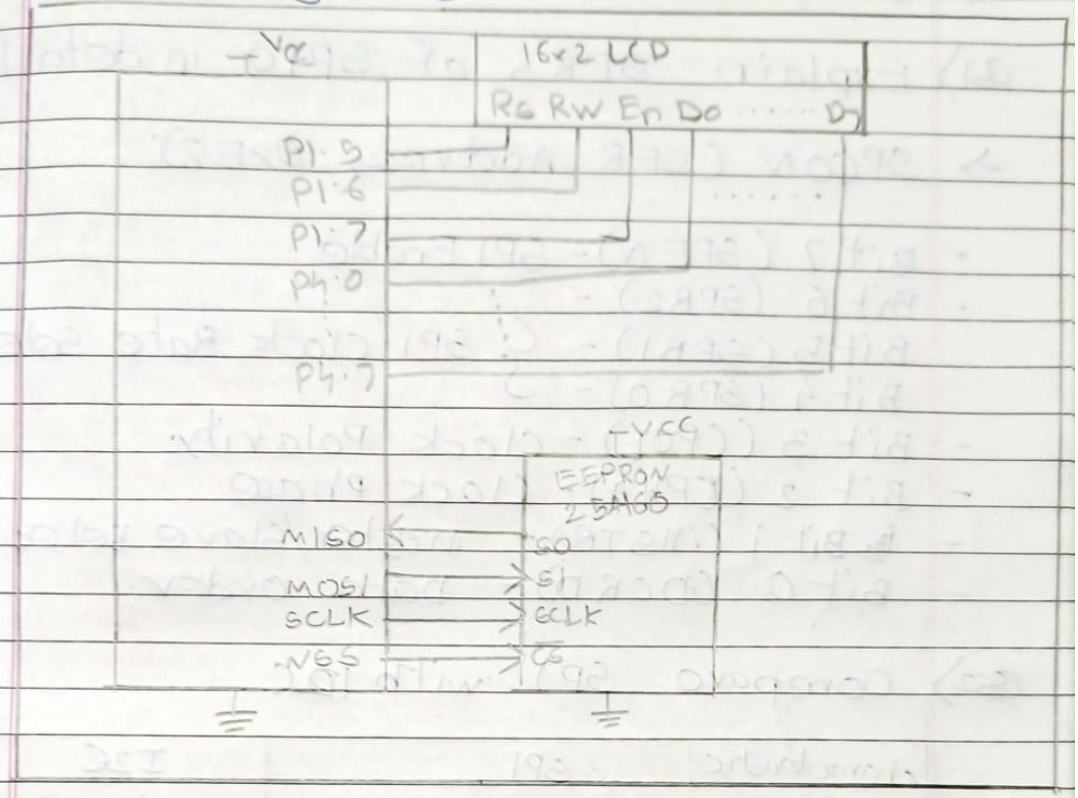
* Interfacing Diagram:



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* study Q

Q1) Explain SFRs of SPI0 in detail.

→ SPCON (SFR Address 0xE8)

- Bit 7 (SPEN) - SPI Enable
- Bit 6 (SPR2) -
  Bit 5 (SPR1) - } SPI clock Rate select
  Bit 4 (SPR0) -
- Bit 3 (CPOL) - clock Polarity.
- Bit 2 (CPHA) - Clock Phase
- Bit 1 (MSTR) - Master/Slave select
- Bit 0 (DORD) - Data order.

Q2) Compare SPI with I2C.

characteristic	SPI	I2C
Topology	Master - Slave	Master-Slave
No. of wires	Requires separate lines for data (MOSI/MISO), clock (SCK) & chip select	Requires only two wires: data (SDA) & clock (SCL)
Data Transfer	Full - duplex	Half - duplex.
Data Rate	Generally supports higher data rates	Typically operates at lower data rates
Addressing	chip select lines	Unique 7 or 10 bit