F. Y. B. Tech Academic Year 2021-22

Trimester: II **Subject:** Basics of Electrical and Electronics Engineering

Name ---------- **Division ---------**

Roll No ---------- **Batch ----------**

Experiment No: 6

Name of the Experiment: Design and implementation of full adder using basic and universal gates.

Performed on: **----------**

Submitted on: **----------**

Aim: Design and implementation of Full Adder using basic and universal gates.

Prerequisite:

- Theory of digital logic circuits

Objectives:

- Identify pins of digital logic gates ICs
- Implement Full Adder circuit with basic and universal gates

Components and equipment required:

Power supply, digital board, digital logic gate ICs: OR (IC 7432), AND (IC 7408), NOT (IC 7404), NOR (IC 7402), NAND (IC 7400), EX-OR (IC 7486), connecting wires etc.

Theory:

Logic Gates:

Logic Gates are used to implement Boolean Logic. There are six types of basic logic gates that are used in digital systems. It is a device which has the ability to produce one output level with the combinations of input levels. Table 5.1 demonstrates description, symbol and truth table of the logic gates namely AND, OR, NOT, NAND, NOR and EXOR.

Table 5.1 Symbol and truth table of the logic gates

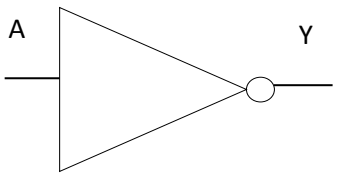
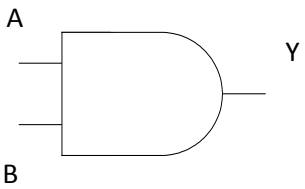
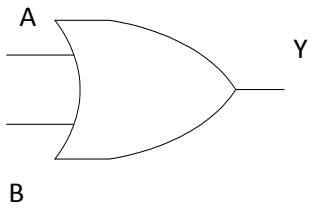
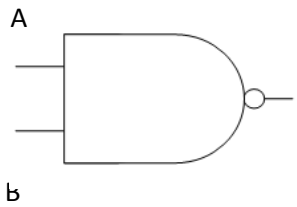
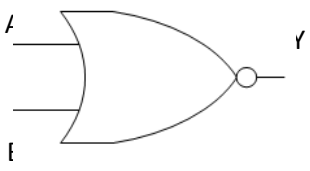
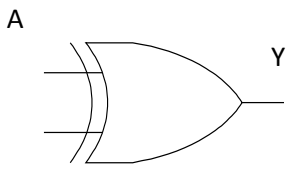
<table>
<tr><th>GATE</th><th>Description</th><th>Symbol</th><th>Truth Table</th></tr>
<tr><td>NOT</td><td>Inverts the given input A</td><td> 
</td><td>
<table>
<tr><th>A</th><th>Y = A’</th></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>AND</td><td>Logical AND of two inputs A and B</td><td> 
</td><td>
<table>
<tr><th>A</th><th>B</th><th>Y = A*B</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>OR</td><td>Logical OR of two inputs A and B</td><td> 
</td><td>
<table>
<tr><th>A</th><th>B</th><th>Y = A+B</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>NAND</td><td>Complement of logical AND of two inputs A and B</td><td> 
</td><td>
<table>
<tr><th>A</th><th>B</th><th>Y = (A.B)’</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>NOR</td><td>Complement of Logical OR of two inputs A and B</td><td>  </td><td>
<table>
<tr><th>A</th><th>B</th><th>Y = (A+B)’ (A+B)’</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>EXOR</td><td>Exclusive OR of two inputs A and B</td><td> 
</td><td>
<table>
<tr><th>A</th><th>B</th><th>Y = A⊕B</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
</table>

Figure 5.1 indicates pin diagram of IC 7404 which is NOT gate. Fig. 5.2 indicates pin diagram of IC 7400 which is quad two input NAND gate. Pin diagrams of OR gate IC 7432, AND gate IC 7408 and EX-OR gate IC 7486 are similar to that of NAND gate IC 7400. Fig. 5.3 indicates pin diagram of IC 7404 hex inverter (NOT) gate.

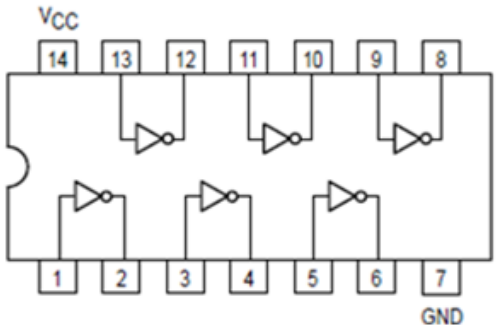


Fig 5.1 Pin diagram of IC 7404 NOT gate

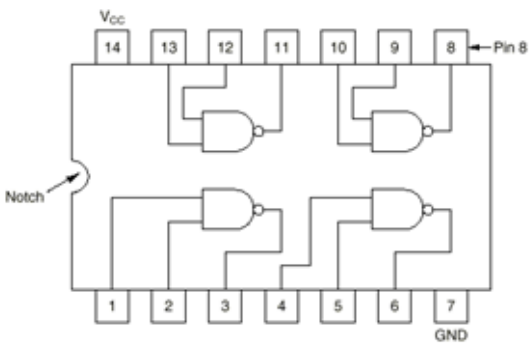


Fig 5.2 Pin diagram of IC 7400 NAND gate

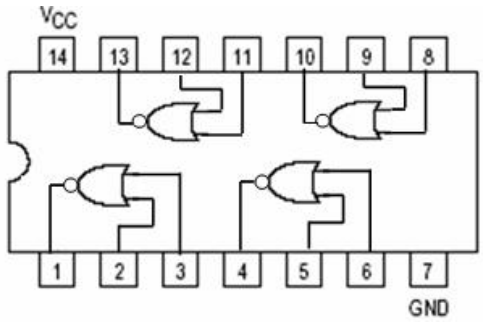


Fig 5.3 Pin diagram of IC 7402 NOR gate

Adder:

An Adder is a device that can add two binary digits. It is a type of digital circuit that performs the addition of two binary numbers. Adders are used in various applications like binary code decimal, address decoding, table index calculation etc.

There are two types of adders, half adder and full adder. Half adder is used to add two binary digits and a full adder is used to add two binary digits with third binary digit which represents carry input. The detailed explanation of the full adder is given below.

Full Adder:

A full adder circuit is an arithmetic circuit block that can be used to add three bits to produce a SUM and a CARRY output. Such a building block is needed in order to add binary numbers with a large number of bits. The full adder circuit overcomes the limitation of the half-adder, which can be used to add two bits only

There are three inputs and two outputs to a full adder as shown in Fig. 5.4. Inputs are named as A, B and Cin, outputs are named as Sum (S) and Carry (C). Truth table for the full adder is shown in Table 5.2.

Table 5.2 Truth Table of Full adder

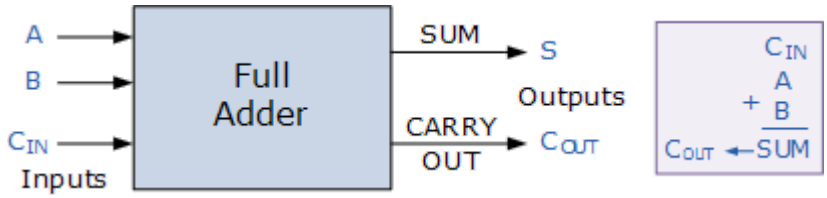
Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Using Karnaugh-maps (K-map), Boolean expressions derived for sum and carry are given by Eq. 5.1 & Eq. 5.2.

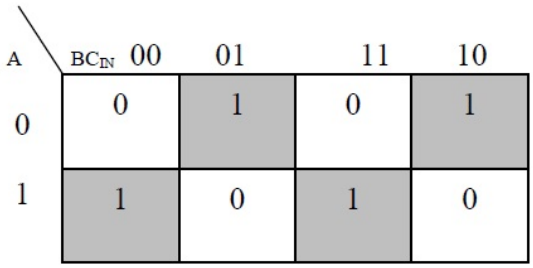
$$SUM = A\bar{B}\bar{C}in + A\bar{B}C\bar{i}n + AB\bar{C}\bar{i}n + ABCin = A \oplus B \oplus Cin \quad (5.1)$$

$$CARRY\text{-}OUT = AB + A\,Cin + B\,Cin = A.B + Cin\,(A \oplus B) \quad (5.2)$$

Full adder schematic drawn, based on the sum and carry expressions is shown in Fig. 5.5.

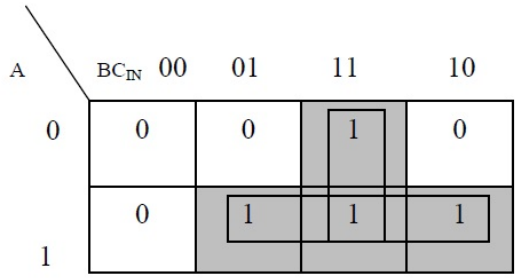


Sum = S= $\bar{A}\ \bar{B}\ Cin + \bar{A}\ B\ \bar{C}\ in + A\ \bar{B}\ \bar{C}\ in + A\ B\ Cin = A \oplus B \oplus Cin$



A \ BC_{IN}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

Carry Out = C_{out} = $A\ B + A\ Cin + B\ Cin$



A \ BC_{IN}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Fig: 5.4 Full adder block, K-map for sum and carry

After optimization we get

SUM = A XOR B XOR Cin = $A \oplus B \oplus Cin$

CARRY-OUT = A AND B OR Cin (A XOR B) = $A.B + Cin\ (A \oplus B)$

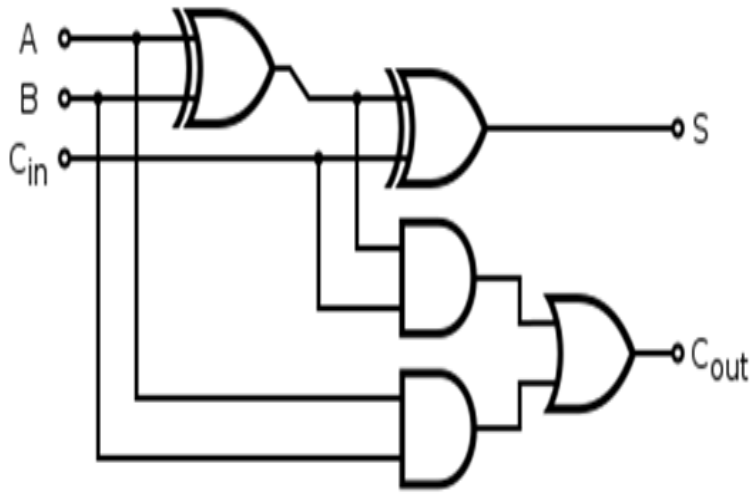


Fig. 5.5 Full adder Schematic

Procedure:

1. Identify the ICs and verify the truth table of all given ICs as per the entries in Table 5.1.
2. Build full adder circuit as shown in Fig. 5.5 on the digital board.
3. Make the connections and apply the voltage.
4. Verify the results of half adder as per the truth table entries in Table 5.2.

Conclusion:

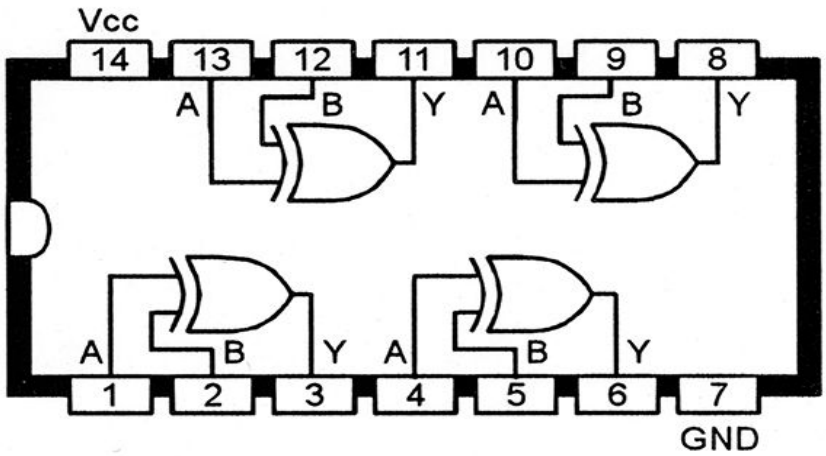
Post Lab Questions:

1. Implement the basic logic gates using Universal gates.
2. Implement NOR gate using NAND gates, NAND gate using NOR gates.
3. What is XOR gate?
4. Implement full adder using NAND gates only.
5. State and prove Dorgan's theorem.
6. Explain the operation of following gates:
   a) NOT b) AND c) OR d) NAND e) NOR

Additional links for more information:

- http://www.ee.surrey.ac.uk/Projects/CAL/digital-logic/gatesfunc/
- https://www.electronicshub.org/half-adder-and-full-adder-circuits/

EX- OR Gate(IC 7486)



VCC: 5 V

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

MC54/74HC86

Quad 2-Input Exclusive OR Gate

High–Performance Silicon–Gate CMOS

The MC54/74HC86 is identical in pinout to the LS86; this device is similar in function to the MM74C86 and L86, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates


J SUFFIX
CERAMIC PACKAGE
CASE 632–08

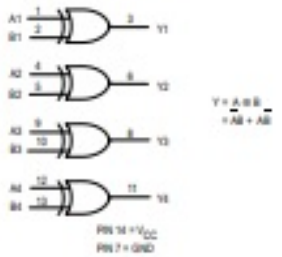

N SUFFIX
PLASTIC PACKAGE
CASE 646–06


D SUFFIX
SOIC PACKAGE
CASE 751A–03

ORDERING INFORMATION

MC54HC30J	Ceramic
MC74HC30N	Plastic
MC74HC30D	SOIC

LOGIC DIAGRAM



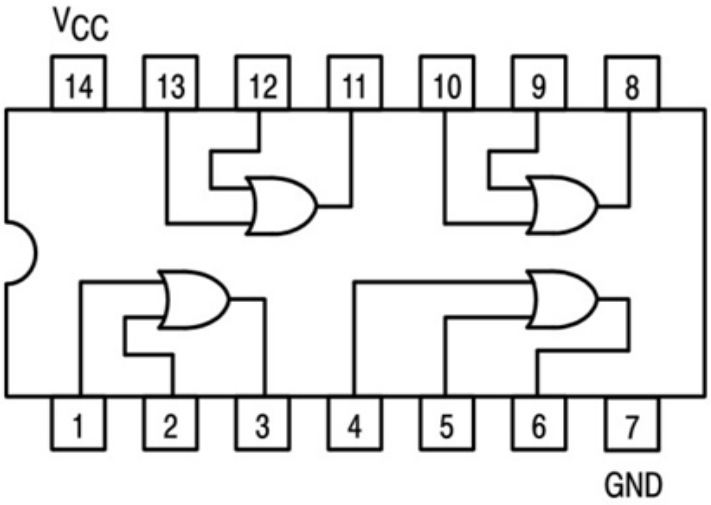
$Y = \overline{A}B + A\overline{B}$

PIN ASSIGNMENT

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

OR Gate(IC 7432)



AND Gate(IC 7408)