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SINGLE-PHASE AC REGULATOR (ACR)

AIM: To study the operation of a single-phase AC regulator (ACR) for resistive loads.

APPARATUS: 1) Circuit board.
2) DMM.
3) True RMS ammeter & voltmeter.
4) Dual trace CRO with probes.

NOMENCLATURE:

(i) $V_{o\,rms}$ **:** rms output voltage

(ii) **:** rms AC supply voltage

(iii) V_T **:** ON-state voltage drop of the SCR

(iv) α **:** firing angle

(v) R **:** total resistance of current sensing resistor, ammeter & load.

(vi) P_{rms} (P_{ac}) **:** rms (AC) output power

THEORY:

A single-phase ACR converts a fixed AC supply voltage into a variable AC voltage, using phase angle control. With this method, the rms value of the output voltage can be varied from 0 to V_S as α is varied from π to 0.

CIRCUIT DESCRIPTION:

1. Power circuit: The power circuit diagram of the single-phase ACR is shown in Fig. 1 while the power circuit waveforms are shown in Fig. 2. The ACR consists of 2 SCRs (thyristors) T31 & T32 connected in antiparallel. The mains supply is stepped-down by transformer TR5 to 18V and given to the ACR via fuse F1, as the AC supply. The load can either be **R** (R32 with switch S4 in L OFF position), or **RL LIGHT** (LIGHT inductive – R32 in series with L1, keeping switch S3 in LIGHT position and S4 in L ON position), or **RL HEAVY** (HEAVY inductive – R32 in series with L2, keeping switch S3 in HEAVY position and S4 in L ON position).

SCR T31 is turned-ON in the +ve half-cycle of the AC supply at $\omega t = \alpha$, while T32 is turned-ON in the –ve half-cycle at $\omega t = \alpha + \pi$. For a **R** load, the output current $i_O(t) = v_O(t)/R$ and hence goes to zero at the supply zero crossings at $\omega t = \pi$ and $\omega t = 2\pi$. Hence SCR T31 turns-OFF by **natural or line commutation** at $\omega t = \pi$, while T32 turns-OFF at $\omega t = 2\pi$.

Hence the output voltage is:

$$v_O(t) = 0 \qquad \text{for } 0 < \omega t < \alpha$$

$$\begin{aligned} v_O(t) &= v_S(t) \text{ ideally} && \text{for } \alpha < \omega t < \pi \\ &= v_S(t) - V_T \text{ actually} \end{aligned}$$

$$v_O(t) = 0 \qquad \text{for } \pi < \omega t < \pi + \alpha$$

$$\begin{aligned} v_O(t) &= v_S(t) \text{ ideally} && \text{for } \pi + \alpha < \omega t < 2\pi \\ &= v_S(t) + V_T \text{ actually} \end{aligned}$$

2. Control circuit: The control circuit is also shown in Fig. 3, while the control circuit waveforms are shown in Fig. 6. The control circuit delivers a **line-synchronized high frequency firing pulse train** from $\omega t = \alpha$ to $\omega t = \pi$ to SCR T31 and from $\omega t = \alpha + \pi$ to $\omega t = 2\pi$ to SCR T32.

The control circuit is based on phase control IC TCA785 (U1) whose pin configuration and block diagrams are shown in Figs. 4 & 5, respectively.

The line synchronizing input voltage, V_{SYNC} (**X3**), is obtained from the secondary winding X1 – X2 of control transformer TR1 via a high ohmic resistance R1 and inverse parallel connected clipping diodes D1 & D2.

The TCA785 zero voltage detector detects the zero crossings and transfers them to the synchronization register. This register controls a ramp generator whose capacitor C2 is charged by a constant current determined by R2 and R3, producing a positive going ramp (capacitor) voltage (**X4**). A variable control voltage (**X5**) is produced by R4 and potentiometer R5, which is filtered by R6, C4 & C5 to remove supply voltage ripple and noise.

The ramp voltage is given to the –ve input of the internal comparator, while the control voltage is given to the +ve input. In the +ve half cycle of the synchronizing voltage, the ramp voltage exceeds the control voltage at $\omega t = \alpha$, while in the –ve half cycle the same occurs at $\omega t = \pi + \alpha$.

If the inhibit input voltage, V_{IN} (**X6**), is kept high and the pulse extension input PE (pin 12) is grounded, then the +ve half cycle output Q1 (**X7**) is a rectangular pulse from $\omega t = \alpha$ to $\omega t = \pi$, while the –ve half cycle output Q2 (**X8**) is a rectangular pulse from $\omega t = \pi + \alpha$ to $\omega t = 2\pi$. However in order to reduce the SCR gate dissipation as well as reduce the size of the isolation pulse transformer, a high frequency firing pulse train is desirable. This is done by modulating the inhibit input voltage by a rectangular pulse train with duty cycle < 50% obtained from a high frequency (20 KHz) oscillator using IC555 (U2) in the astable mode. Thus the +ve half cycle output Q2 (**X8**) is a high frequency rectangular pulse train from $\omega t = \alpha$ to $\omega t = \pi$, while the –ve half cycle output Q1 (**X7**) is a high frequency rectangular pulse train from $\omega t = \pi + \alpha$ to $\omega t = 2\pi$.

The firing angle **α** can be varied from **0° to 180°** by means of potentiometer **R5**.

Output Q2 is amplified to the appropriate power level by the +ve pulse amplifier. The +ve pulse amplifier is formed by base drive resistors R9 & R11, power transistor T1 (2N1711), pulse transformer TR2, and freewheeling diodes D5 & D6. The first secondary winding of TR2 delivers the pulses to gate (G31) and cathode (K31) of SCR T31 via the gate drive circuit comprising of high speed diode D7 (BA159), current limiting power resistor R12 and shunt resistor R13. The second secondary winding of TR2 delivers the pulses to gate (G33) and cathode (K33) of SCR T33 via the gate drive circuit comprising of high speed diode D8 (BA159), current limiting power resistor R14 and shunt resistor R15.

Similarly, output Q1 is amplified to the appropriate power level by the -ve pulse amplifier. The -ve pulse amplifier is formed by base drive resistors R16 & R17, power transistor T2 (2N1711), pulse transformer TR3, and freewheeling diodes D9 & D11. The first secondary winding of TR3 delivers the pulses to gate (G32) and cathode (K32) of SCR T32 via the gate drive circuit comprising of high speed diode D12 (BA159), current limiting power resistor R18 and shunt resistor R19. The second secondary winding of TR3 delivers the pulses to gate (G34) and cathode (K34) of SCR T34 via the gate drive circuit comprising of high speed diode D13 (BA159), current limiting power resistor R21 and shunt resistor R22.

It is to be noted that the pulse transformers TR2 & TR3 provide the necessary **galvanic isolation** between the control and output sides of the control circuit.

3. Test points:

TP1 : synchronizing voltage

TP2 : ramp voltage

TP3 : control input voltage

TP4 : HFO inhibit pulse train

TP5 : Q1 –ve half cycle output pulse train

TP6 : Q2 +ve half cycle output pulse train

FORMULAE (for resistive load):

1. RMS output voltage:

$$V_{o\,rms} = \left[\frac{1}{\pi} \int_{\alpha}^{\pi} v_o^2(\omega t)\, d\omega t \right]^{1/2} = \left[\frac{1}{\pi} \int_{\alpha}^{\pi} 2V_s^2 \sin^2(\omega t)\, d\omega t \right]^{1/2}$$

$$= V_s \left[\frac{1}{\pi} \left(\pi - \alpha + \frac{\sin 2\alpha}{2} \right) \right]^{1/2} \qquad (1)$$

2. RMS output current:

$$I_{o\,rms} = \frac{V_{o\,rms}}{R}$$

$$= \frac{1}{R}\left[\frac{1}{\pi}\int_{\alpha}^{\pi} v_o^2(\omega t)d\omega t\right]^{1/2} = \frac{1}{R}\left[\frac{1}{\pi}\int_{\alpha}^{\pi} 2V_s^2 \sin^2(\omega t)d\omega t\right]^{1/2}$$

$$= \frac{V_s}{R}\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2} \qquad (2)$$

3. RMS (AC) output power:

$$P_{rms}(P_{ac}) = \frac{V_{o\,rms}^2}{R} = \frac{V_s^2}{\pi R}\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right] \qquad (3)$$

PROCEDURE:

1. Keeping the power circuit supply **OFF**, switch **ON** the control circuit supply.

2. Connect channel 1 of the CRO to the AC (line) synchronizing voltage across **X1** (live) and **X2** (ground) and channel 2 successively to test points TP2 (**X4**) (ramp voltage of TCA785), TP3 (**X5**) (control voltage input to TCA785), TP4 (X5) (high frequency oscillator input), TP5 (X7) (-ve half cycle output pulse train) & TP6 (X8) (+ve half cycle output pulse train). Vary **firing angle control potentiometer R5** and observe the variation of, and **draw to scale**, the waveforms at each of these test points.

3. Measure minimum and maximum firing angles α_{min} &. α_{max} respectively.

5. Switch **OFF** the control supply and disconnect both channels of the CRO.

6. Note that $\sqrt{2}V_S$ = measured peak voltage $+V_T$.

7. Put switch S4 in 'L OFF' position (switch closed i.e. L1 or L2 **shorted**).

8. Connect the true RMS AC ammeter (I_O) between X37 & X38, true RMS AC voltmeter (V_O) & channel 1, **inverted**, of CRO ($v_O(t)$) between X42 (live) & X37 (common). Connect channel 2 of CRO ($v_{AK\,T31}(t)$) between X34 (live) & X37 (common).

9. Switch **ON** the power circuit supply and the control circuit supply. Observe and **draw to scale** the output voltage waveform $v_O(t)$and SCR T31 voltage waveform ($v_{AK\,T31}(t)$), which is also the negative of the SCRT32 voltage waveform.

10. Measure the peak output voltage ($\sqrt{2}V_S - V_T$) and the SCR ON state voltage drop V_T on the CRO and supply voltage V_S on the meter.

11. Vary R5 to obtain 10 different firing angles and measure α & $v_O(\omega t = \alpha)$, on the CRO and V_O

and I_o on the meters.

OBSERVATIONS:

1. Minimum firing angle α_{min} = °

2. Maximum firing angle α_{max} = °

3. R = Ω, V_S = V, $\sqrt{2}V_S - V_T$ = V, V_T = V

Sr. No.	α°	$v_o(\alpha)$ V	V_o V	I_o A
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				

CALCULATIONS:

1. Calculate the ideal values of V_o, I_o & P_{rms} (absorbed by the load), for the above readings using equations (1) to (3).

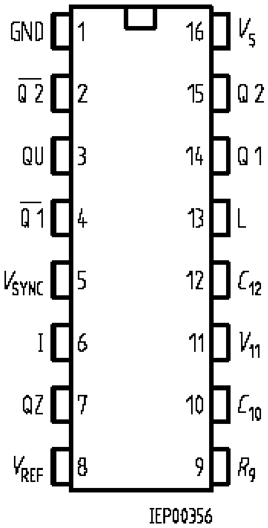
RESULT TABLE:

Sr. No.	V_o rms V		I_o rms A	
	Measured	Calculated	Measured	Calculated
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				

CONCLUSIONS:

LIST OF FIGURES:

Fig. 1	Power circuit
Fig. 2 (a, b, c & d)	Power circuit waveforms for R load
Fig. 3	Control circuit
Fig. 4	Pin configuration of IC TCA785
Fig. 5	Block diagram of IC TCA785
Fig. 6	Control circuit waveforms TCA785



Pin Configuration
(top view)

Fig. 4 Pin configuration of IC TCA785

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2 3 4	$\overline{Q2}$ Q U $\overline{Q2}$	Output 2 inverted Output U Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6 7	I Q Z	Inhibit Output Z
8	V_{REF}	Stabilized voltage
9 10	R_9 C_{10}	Ramp resistance Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14 15	Q 1 Q 2	Output 1 Output 2
16	V_S	Supply voltage

TE E&TC
PE
ACR

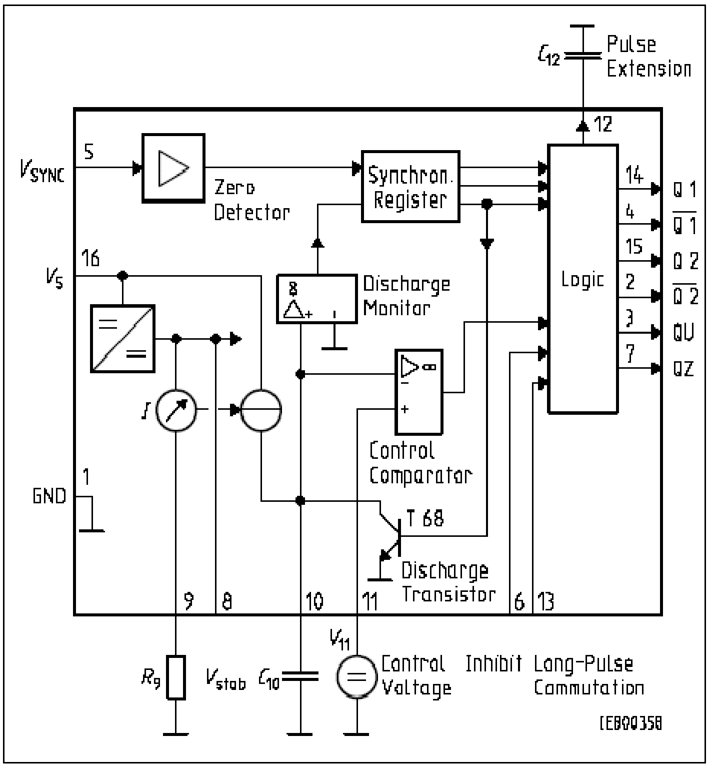


Fig. 5 Block diagram of IC TCA785

TE E&TC
PE
ACR

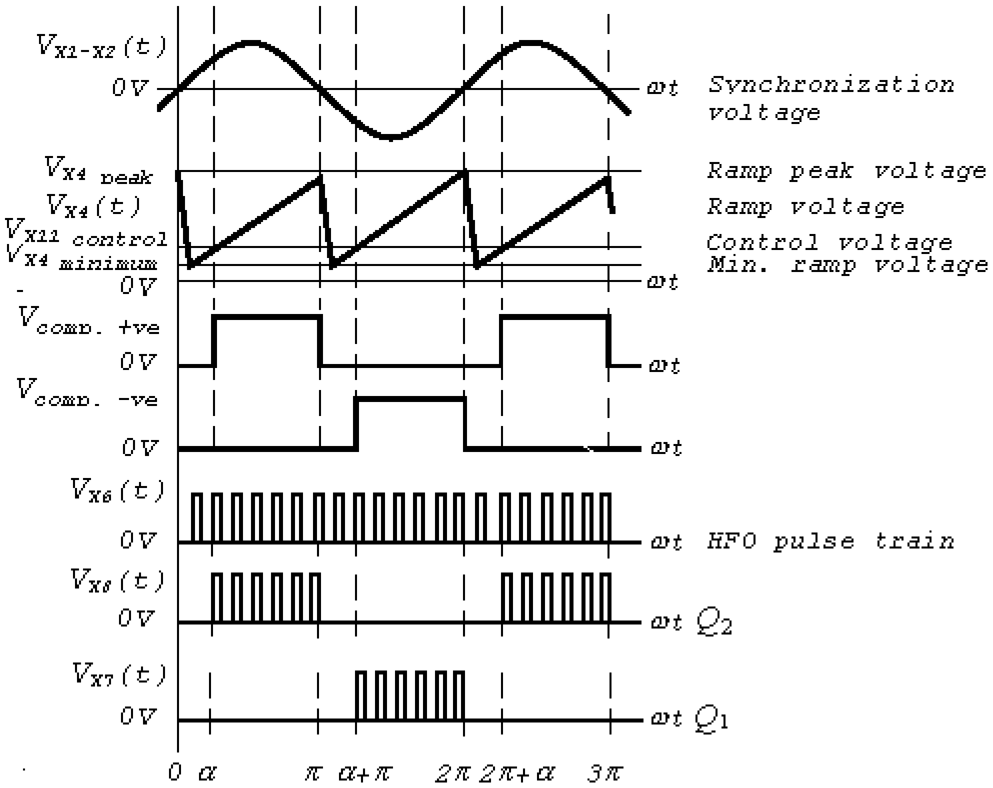
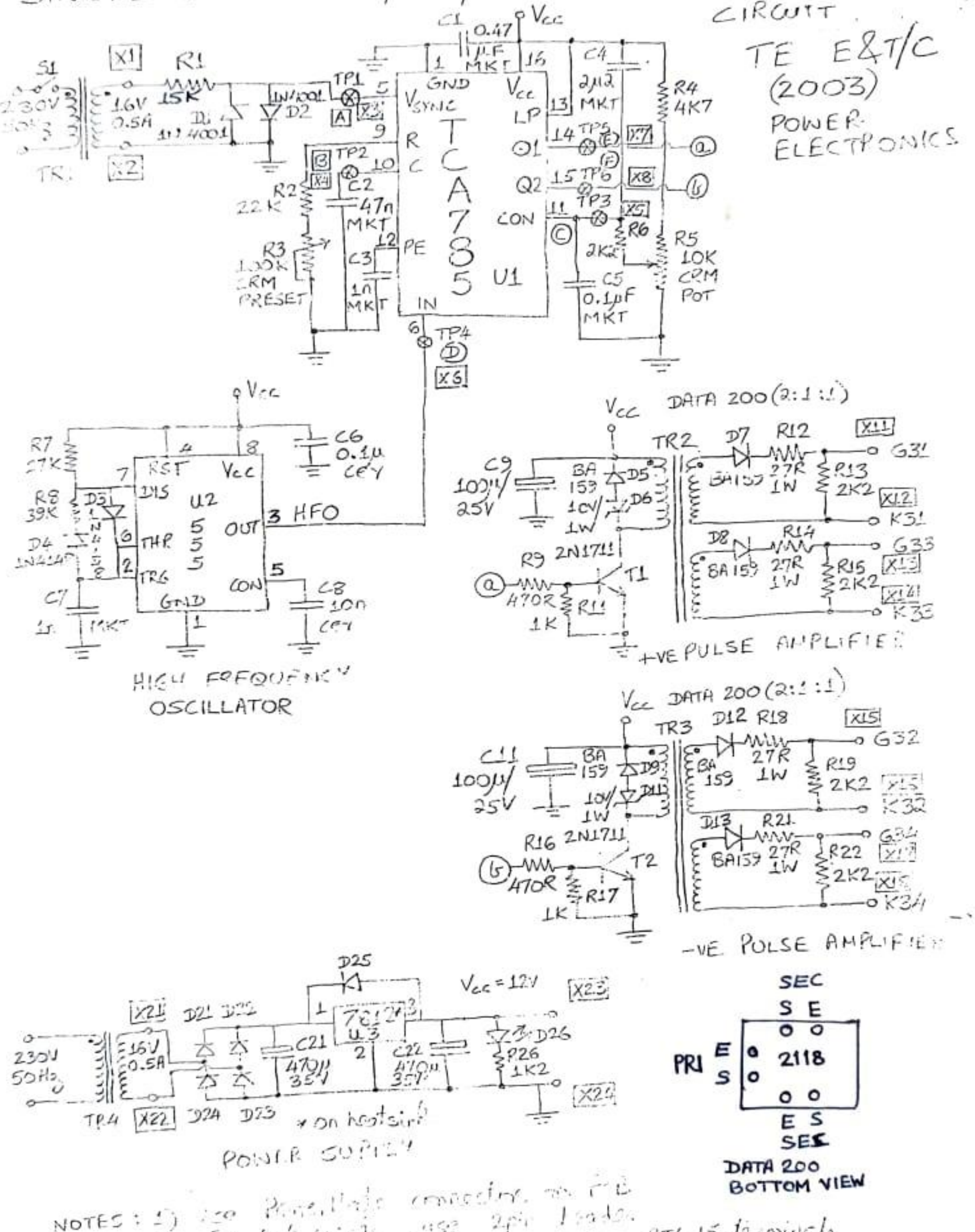


Fig.6 Control circuit waveforms TCA785

TE E&TC
PE
ACR

SINGLE-PHASE HCB/FCB/AC REGULATOR CONTROL CIRCUIT 21-3-05.

TE E&T/C (2003) POWER ELECTRONICS



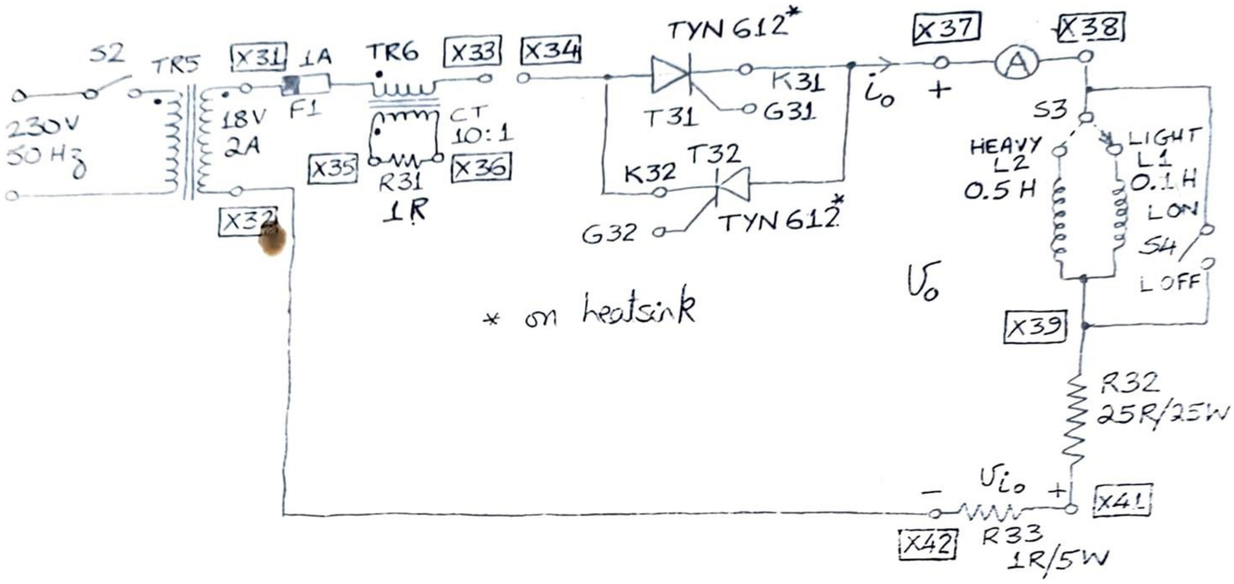
NOTES : 1) Use Phoenix/... connector on PCB

2) For test points, use 2pin 1 header ...

3) For chassis connectors ... use STI-15 terminals

26-4-05

SINGLE-PHASE AC REGULATOR POWER CIRCUIT



$$V_{orms} = V_s \sqrt{\frac{\pi - \alpha + \frac{\sin 2\alpha}{2}}{\pi}}$$

$$I_{orms} = \frac{V_{orms}}{R}$$

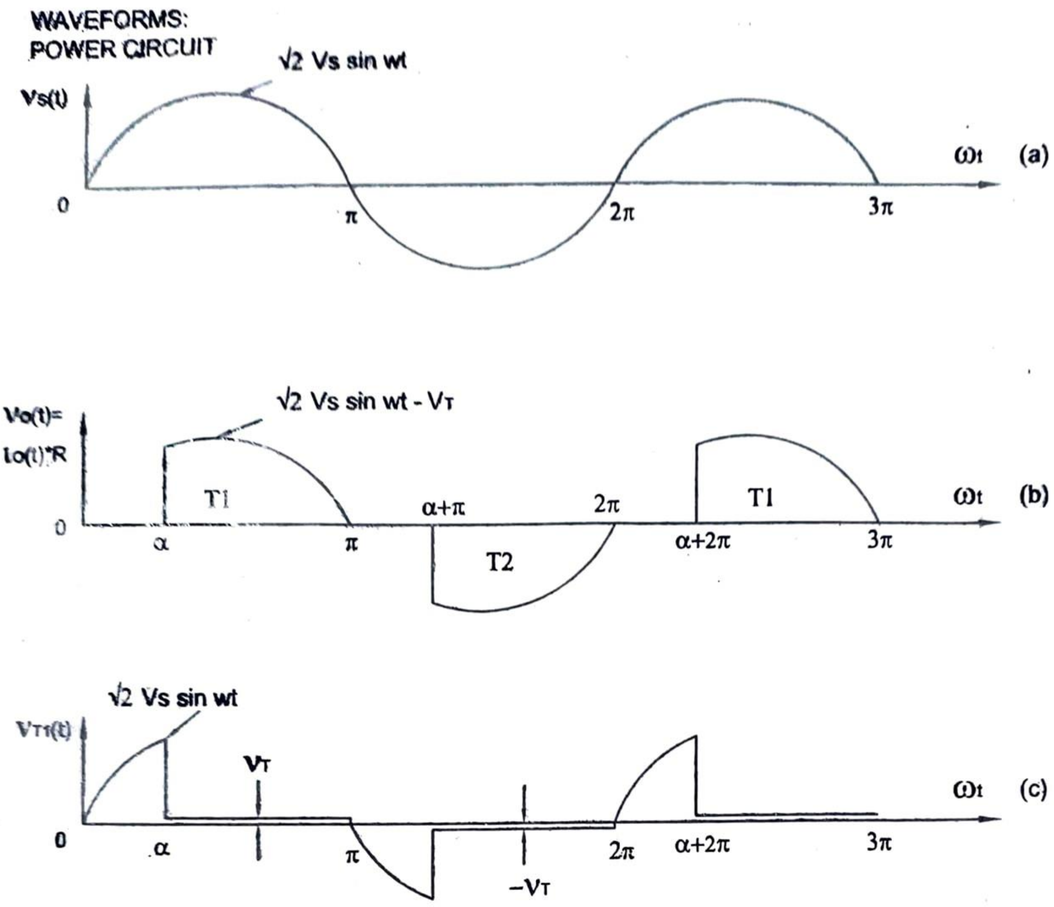


Fig.2. Power circuit waveforms for R load

TE E&TC
PE
ACR

Exp-5 Single phase ACR

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* observations -

Minimum firing angle $\alpha_{min} = 163^{\circ}$
Maximum firing angle $\alpha_{max} = 11^{\circ}$

Sr.No	α^{o}	$V_0(\alpha)$ V	V_0 V	I_0 A
1.	54	21.6	14.53	0.675A
2.	61	23.2	13.40	0.625A
3.	64	24.4	12.78	0.6A
4.	74	25.6	11.05	0.525A
5.	99	26.4	6.97	0.3A
6.	194	15.6	1.266	0.075A

$V_S = 28.8$ V
$R = 20\Omega$

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* Result Table -

Sr NO	Vo rms V		Io rms A	
	Measured	Calculated	Measured	Calculated
1	14.53	18.8	0.675	0.7
2	13.40	19.2	0.625	0.72
3	12.78	17.8	0.6	0.84
4	11.05	16.4	0.525	0.78
5	6.97	13.63	0.3	0.65
6	1.266	9.08	0.075	0.914

* Calculations -

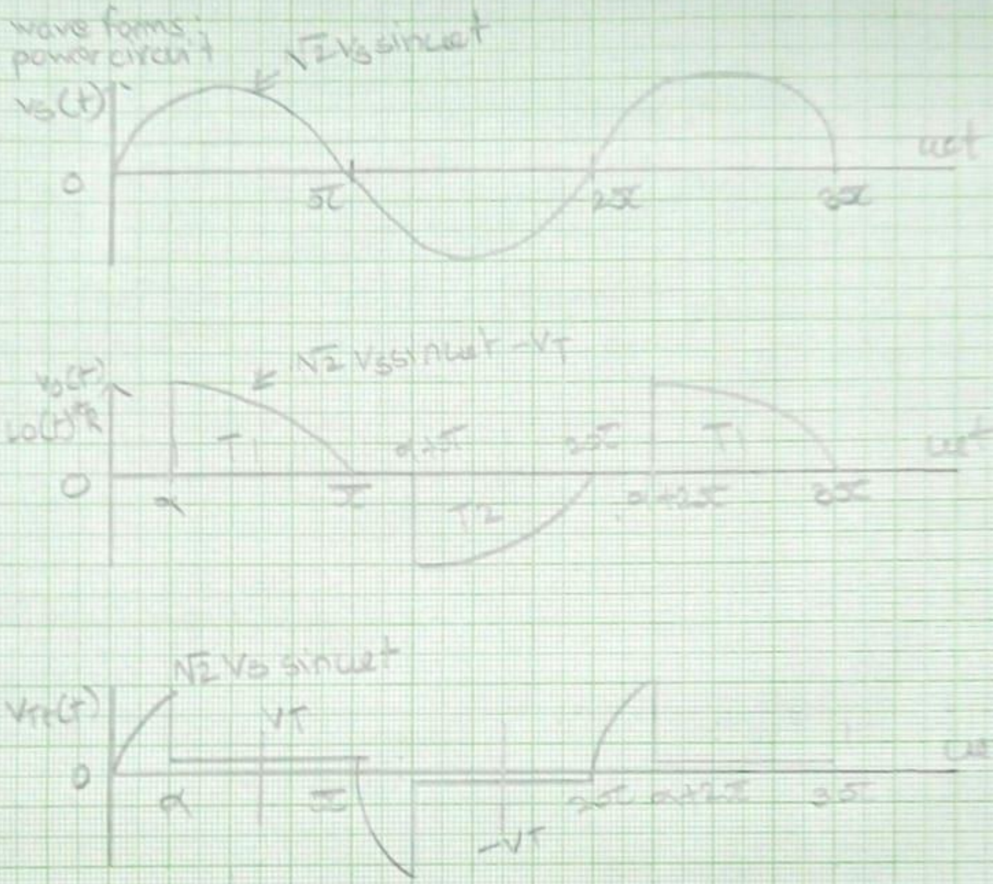
$$V_{orms} = V_s\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$

$$Eg \rightarrow 19.28\left[\frac{1}{\pi}\left(\pi - 36^0 + \frac{\sin 2(36^0)}{2}\right)\right]^{1/2}$$

$$V_{o\,rms} = 18.8\,V$$

similarly.

$$I_{rms} = \frac{V_{orms}}{R} = \frac{18.8}{21} = 0.9A$$



Power circuit waveforms
for R load

Power circuit waveforms
for R load