Unit 1

Power Devices

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Introduction to Power Electronics -1

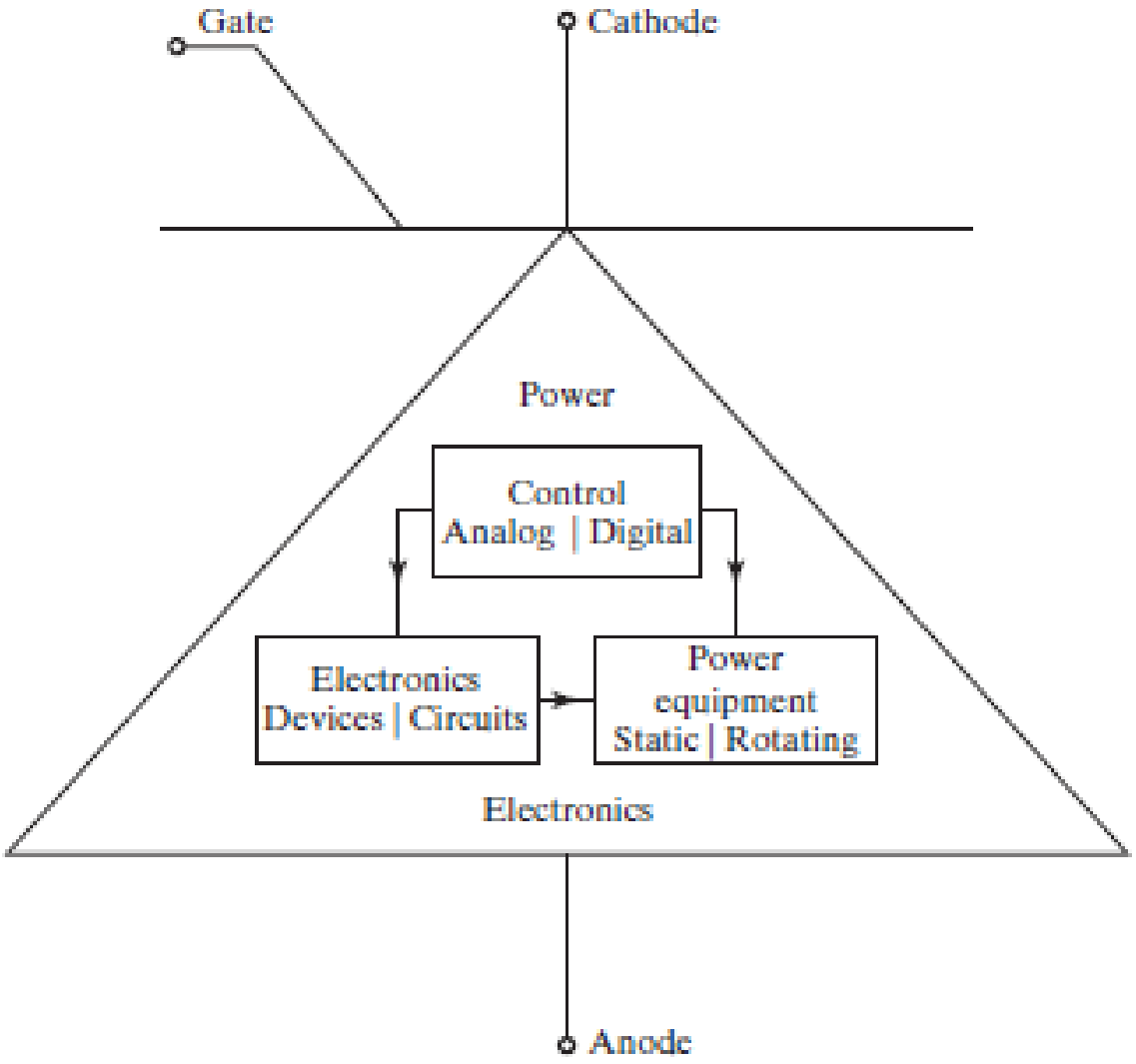


FIGURE 1.1

Relationship of power electronics to power, electronics, and control.

Introduction to Power Electronics -2

Power Electronics can be defined as the application of solid state electronics to the control and conversion of electrical power from one form to another using power semiconductor devices as switches.

These conversions are of 4 types viz.

AC – DC	Controlled and uncontrolled single and multiphase rectifiers
DC – AC	Single and three-phase inverters
DC – DC	Isolated and non-isolatedDC-DC converters or choppers
AC – AC	Single and three-phase inverters AC regulators

Introduction to Power Electronics -3

Applications areas

Home Appliances	Refrigerators, sewing machines, photography, air-conditioning, food warming trays, washing machines, lighting, dryers, vaccum cleaners, electric blankets, grinders and mixers, cooking appliances
Games and entertainment	Games and toys, televisions, movie projectors
Commercial	Advertising, battery chargers, blenders, computers, electric fans, electronic ballasts, hand power tools, photocopiers, vending machines, light dimmers
Aerospace	Aircraft power systems, space vehicle power systems, satellite power systems
Automotive	Alarms and security systems, electric vehicles, audio and Rf amplifiers, regulators

Introduction to Power Electronics -4

Industrial	Blowers, boilers, chemical processing equipment, contactor and circuit breakers, conveyors, cranes and hoists, dryers, electric furnaces and ovens, electric, vehicles, electromagnets, electronic ignitions, elevators, flashers, gas-turbine starters, generator exciters, induction heating, linear induction motion control, machine tools, mining power equipments, motor drives and starters, nuclear reactor control, oil-well drilling equipment, paper mill machinery, power-supplies, printing press machinery, pumps and compressors, servo systems, steel mill instrumentation, temperature controls ultrasonic generators, uninterruptible power supplies (UPS), welding equipment
Medical	Fitness machines, laser power supplies, medical instrumentation
Security systems	Alarms and security systems, radar/sonar
Telecommunications	Uninterruptible power supplies (UPS), solar power supplies, VLF transmitters, wireless communication power supplies
Transportation	Magnetic levitation, trains and locomotives, motor drives, trolly buses, subways
Utility systems	VAR compensators, power factor correction, static circuit breakers, supplementary energy systems (solar, wind)

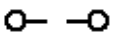
Ideal and Practical Power Switches -1

Ideal Switch

- ON resistance $R_{on} = 0$
  - Forward voltage drop $V_{on} = 0$
- OFF resistance $R_{off} = \infty$
  - Leakage current $I_l = 0$

ON state forward unidirectional

OFF state l



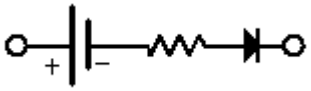
- Conducts ∞ current in both forward and reverse directions for bidirectional switches when ON, and in forward direction for unidirectional switches
- Withstands ∞ forward and reverse voltage when OFF
- Instantaneous switching
- Power dissipation in the switch in both steady and transient states is zero
- ON to OFF and OFF to ON transitions of the switch are fully controllable
- Requires zero power to control or drive the switch

Ideal and Practical Power Switches -2

Practical Power Semiconductor Switch

- ON state modelled by a low forward resistance R_{on} in series with a voltage drop V_{on} (typically 1V for power diode, SCR, IGBT but 0V for MOSFET)
- OFF state modelled by a high resistance R_{foroff} or leakage current I_{foroff} and a high resistance R_{revoff} or leakage current I_{revoff}
- In ON state conducts forward current only (power diode, SCR, IGBT , MOSFET) or both forward and reverse currents (triac)
- Withstands V_{BO} forward and V_{BR} reverse voltage when OFF
- Turn-on time t_{on} and turn-off time t_{off}
- Power dissipation in the switch during turn-on, turn-off and ON state, as well as control power

ON state forward unidirectional

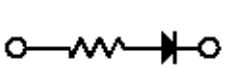


V_{on} R_{on} **a)**

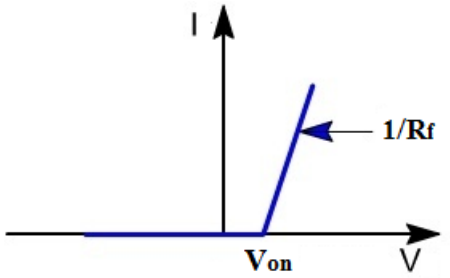
OFF state reverse unidirectional

$R_{revoff} \approx \infty$ **b)**

OFF state forward unidirectional



$R_{foroff} \approx \infty$ **c)**



Unidirectional power switch V-I characteristic **d)**

FIGURE 1.2

Power Diodes -1 (structure, symbol & characteristics)

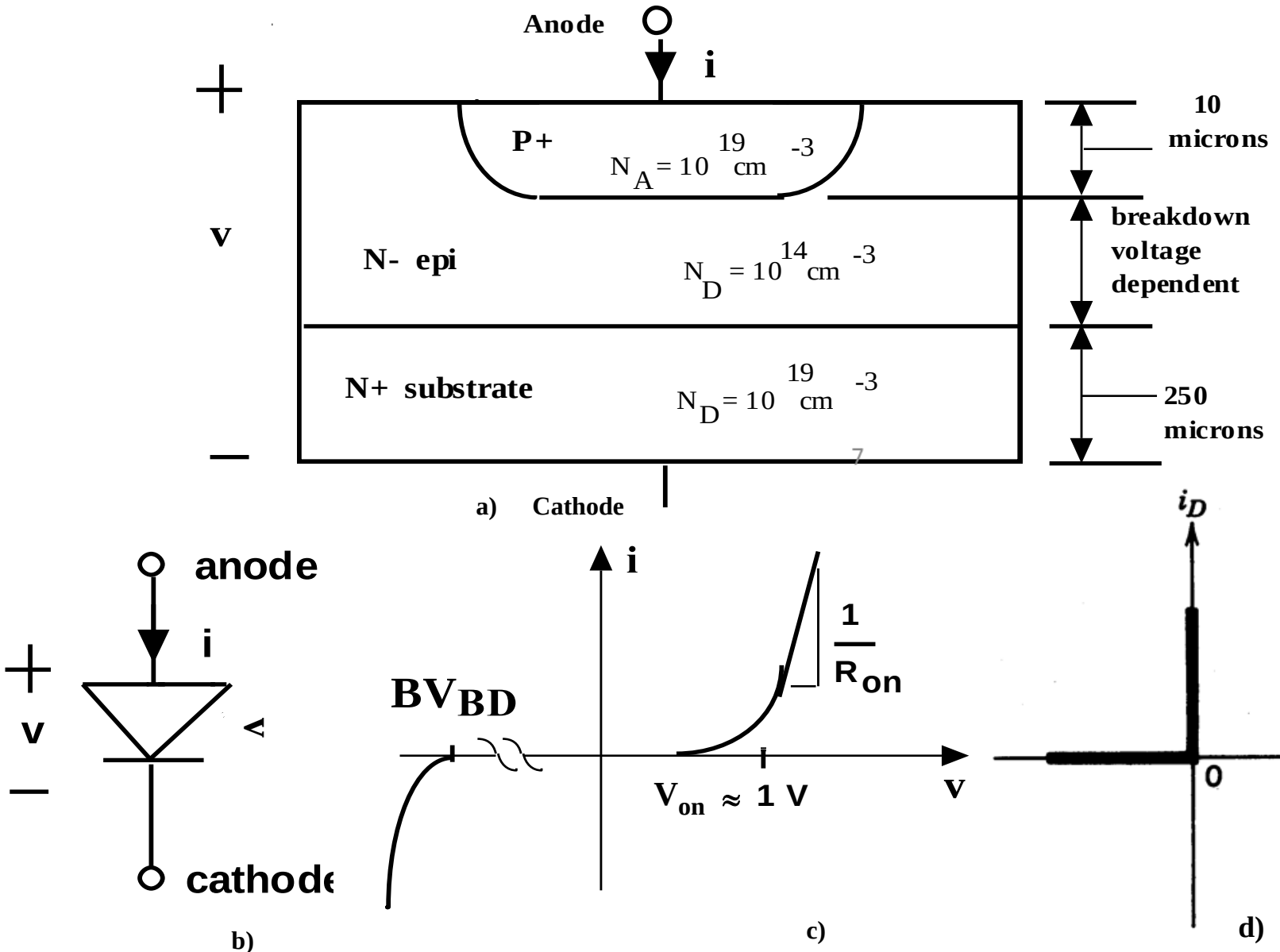
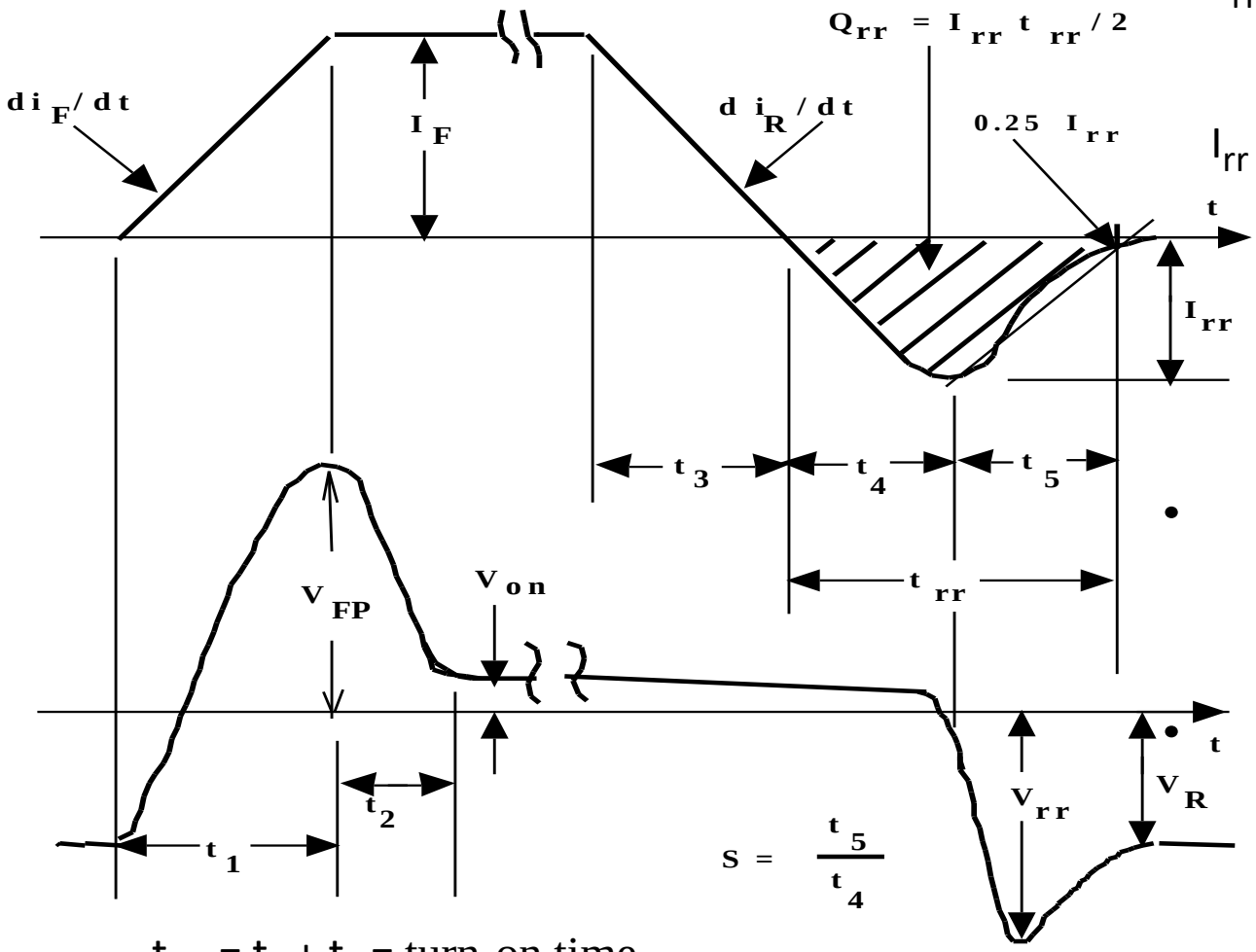


FIGURE 1.3

Power Diodes -2 (turn-on & turn-off characteristics)



Q_{rr} = reverse recovery charge

I_{rr} = reverse recovery current

- $\frac{di_F}{dt}$ and $\frac{di_R}{dt}$ determined by external circuit.

Inductances or power semiconductor devices.

$t_{on} = t_1 + t_2$ = turn-on time

$t_{rr} = t_4 + t_5$ = reverse recovery time $t_{off} = t_3 + t_4 + t_5$ = turn-off time

FIGURE 1.4

Power Diodes -3

- The main difference between power diodes and small signal diodes is the **n^- lightly doped epitaxial layer which is also known as the drift region**. This region is absent in small signal diodes. In power diodes, this region is used to absorb the wide depletion layer which occurs with large reverse voltages.

- Power diodes can be divided in three categories
  1. Standard or general-purpose diodes upto 6000V, 4500A
  2. Fast-recovery diodes upto 6000V, 1100A with reverse recovery times between 0.1us and 5us
  3. Schottky diodes upto 100V, 300A, with very low on-state voltage V_{on} and reverse recovery times in nanoseconds

- Relationship between Q_{rr}, I_{rr} and t_{rr} is $Q_{rr} = I_{rr} \times t_{rr} / 2$ (1.1)
  which is same as that for a SCR (SCR-7)

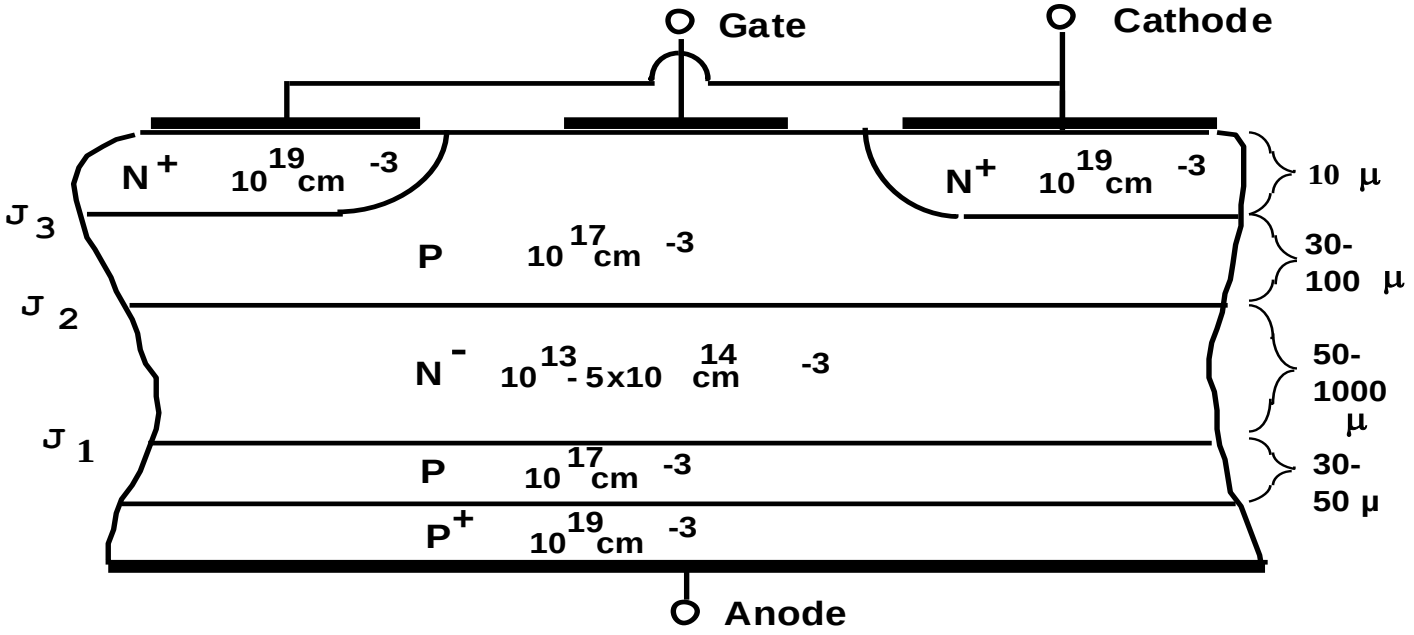
SCR -1 (general)

- SCR (silicon controlled rectifier), also known as thyristor, is a current controlled, three terminal, four layer p-n-p-n, latching type, unidirectional power semiconductor switching device.

- The output terminals are A (anode) and K (cathode) while G (gate) is the control terminal. Current can flow only from anode to cathode and not vice-versa.

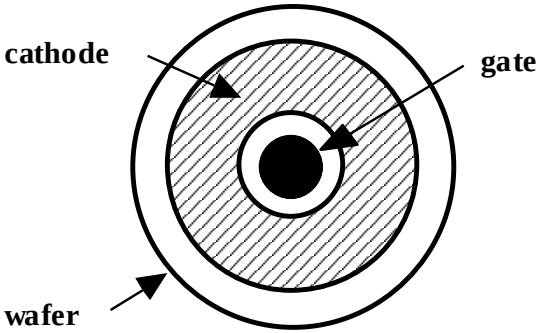
- Five ways in which SCRs can turn on of which only two are desirable:
  - a) Gate triggering — **desirable**
  - b) Forward breakover i.e. $V_{AK} > V_{BO}$ — not desirable
  - c) High dV_{AK}/dt turn on — not desirable
  - d) Thermal triggering at high junction temperatures leading to thermal runaway — not desirable
  - e) Irradiation of gate cathode junction — used for LASCRs (Light Activated SCR) for high voltage applications

SCR -2 (structure)



- Cross-sectional view showing vertical orientation of SCR.
- SCRs with kiloamp ratings have diameters of 10 cm or greater.

Gate and cathode metallization for slow (phase control) thyristor.



Gate and cathode metallization for fast (inverter grade) SCR

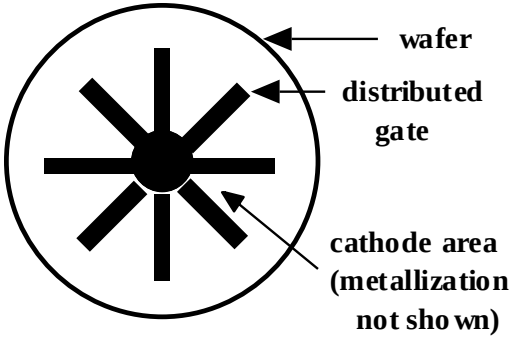
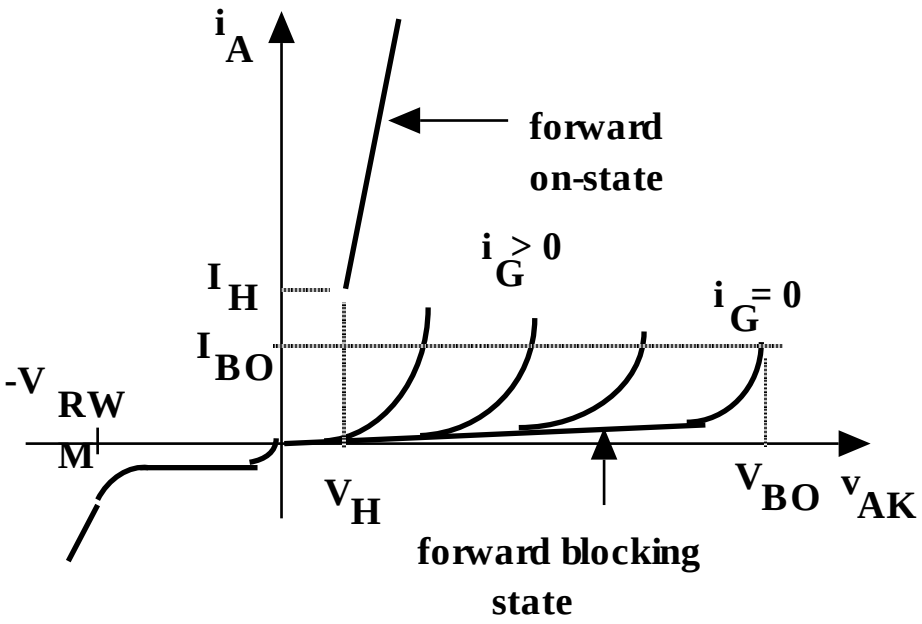


FIGURE 1.5

SCR -2 (V-I characteristics and symbol)



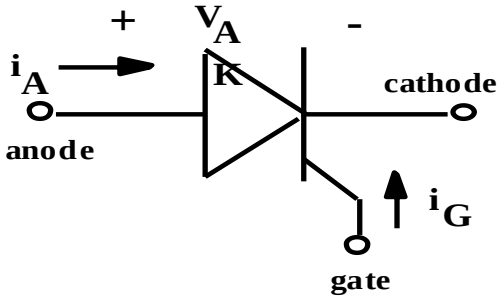


FIGURE 1.6.1

- SCR triggerable from forward blocking state to on-state by a gate current pulse.
- Thyristor latches on and gate cannot turn it off. External circuit must force SCR off.
- Current to several kiloamps for V(on) of 2-4 volts.
- Blocking voltages to 5-8 kilovolts.
- V_{BO} = breakover voltage ; I_{BO} = breakover current
- V_H = holding voltage I_H = holding current
- Maximum junction temperature = 125°C - limited by temperature dependence of V_{BO}.
- Ratings upto 8KV, 6KA

SCR -3 (V-I characteristics and symbol)

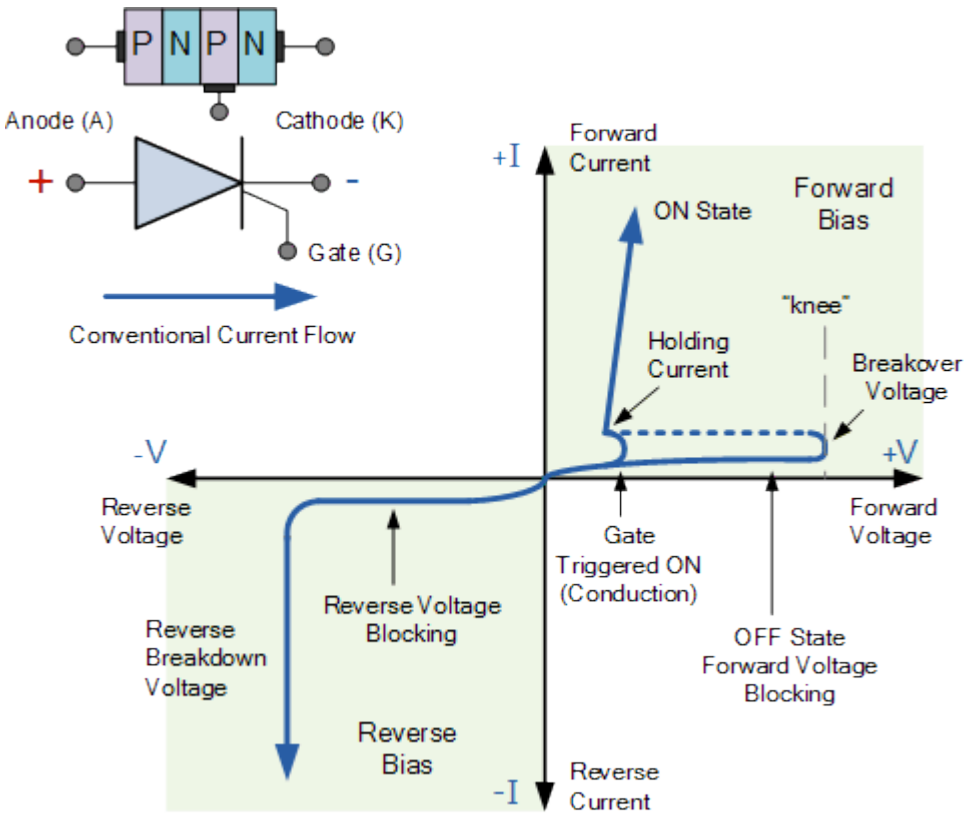
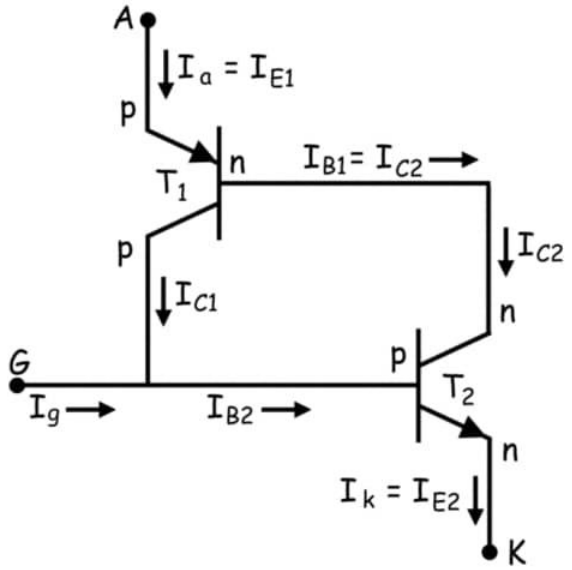
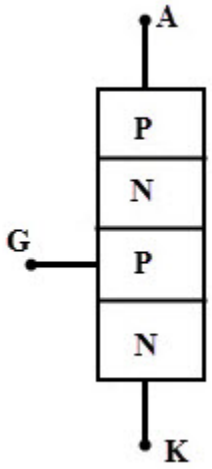


FIGURE 1.62

SCR -4 (Two transistor model)





One dimensional SCR model

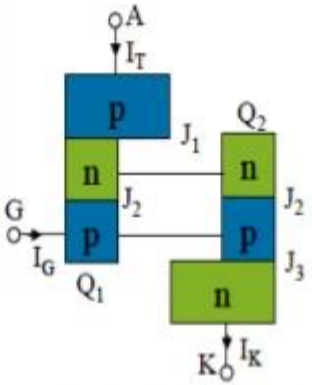
Ebers-Moll equations

Two-Transistor Model of Thyristors

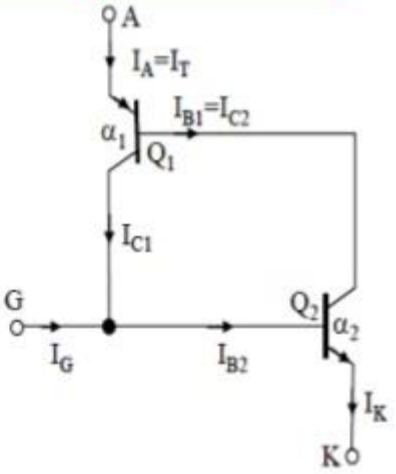
Collector-base junction leakage current

$$I_C = \alpha I_E + I_{CBO}$$

Collector current — Collector Emitter current gain — Emitter current



Basic Structure



Equivalent Circuit

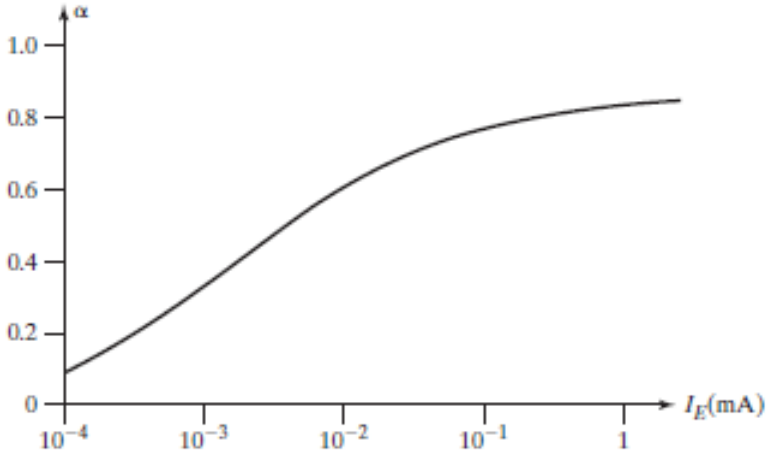
$$Q_1 \rightarrow I_{C1} = \alpha_1 I_A + I_{CBO1}$$
$$Q_2 \rightarrow I_{C2} = \alpha_2 I_K + I_{CBO2}$$

$$I_A = I_{C1} + I_{C2} = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_K + I_{CBO2}$$

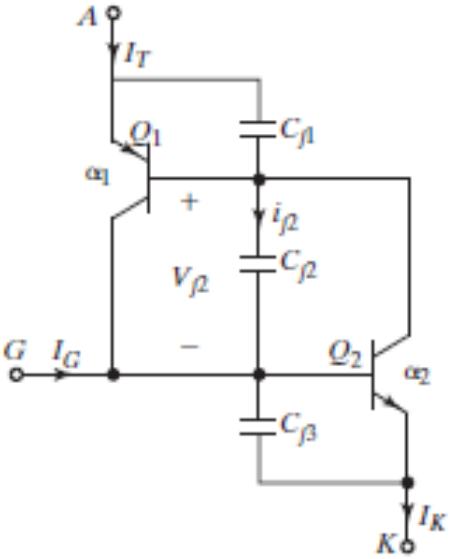
$$I_K = I_A + I_G \Rightarrow I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

FIGURE 1.7

SCR -5 (Two transistor transient model)



Typical variation of current gain with emitter current



Two transistor transient model of SCR with junction capacitances

$$i_{j2} = \frac{d(q_{j2})}{dt} = \frac{d}{dt}(C_{j2}V_{j2}) = V_{j2}\frac{dC_{j2}}{dt} + C_{j2}\frac{dV_{j2}}{dt}$$

$$= C_{j2}\frac{dV_{j2}}{dt} \quad \text{assuming } C_{j2} \text{ is constant}$$

This is the reason why high dV_{AK}/dt **spurious** triggering can occur.

FIGURE 1.8

SCR -6 (Turn-on and turn-off switching characteristics)

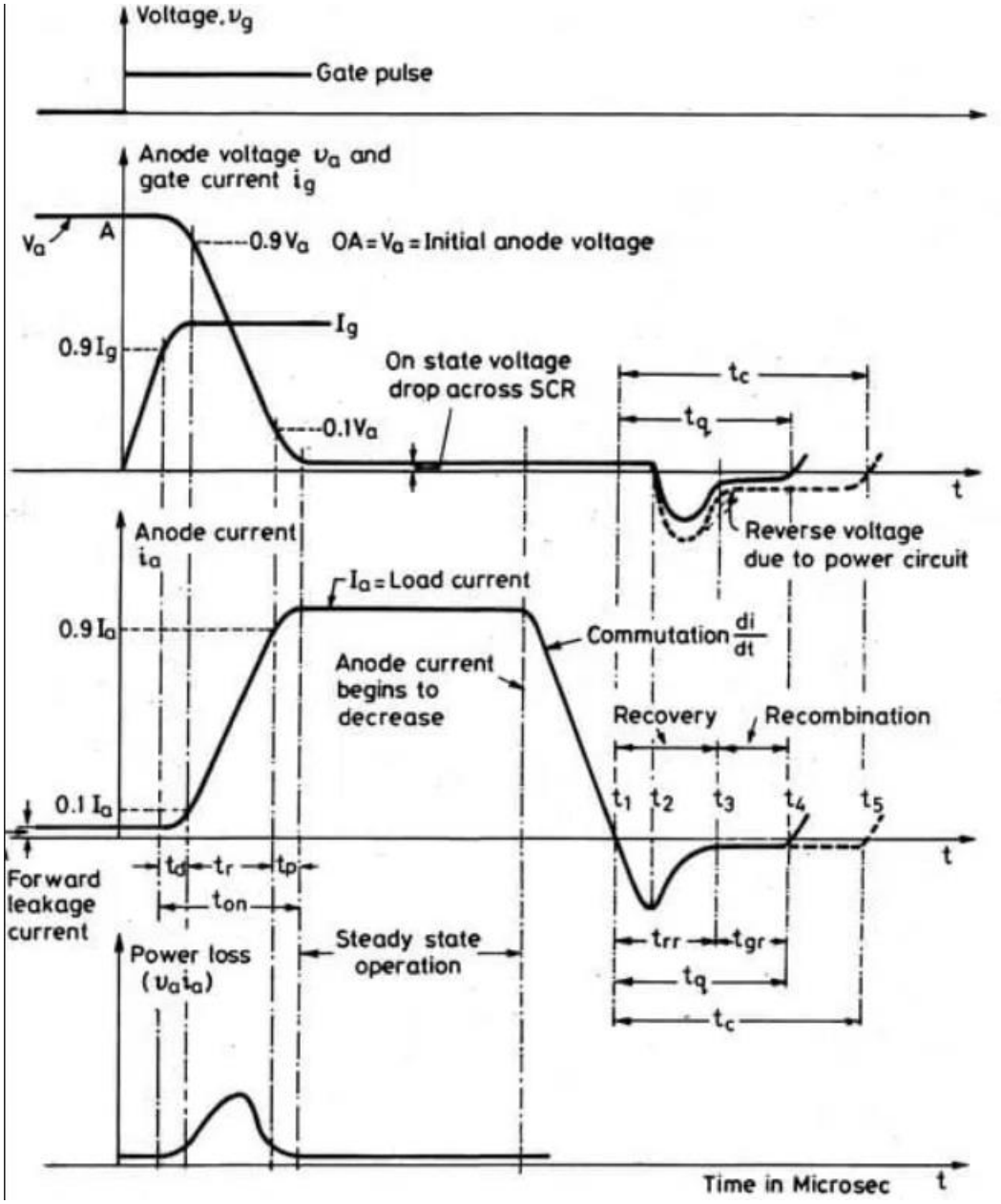


FIGURE 1.9

SCR -7 (Turn-on and turn-off switching characteristics)

- Turn-on time = Delay time + 10% - 90% Rise time + Spread time
  $t_{on} = t_d + t_r + t_p$ typically 1 – 3 us

  During t_r the anode current flows through a narrow region around the gate, while it gradually flows across the entire cross-section during t_p. Hence it necessary to limit the rate of rise of anode current dI_A/dt during t_r to a maximum value, typically 50 – 800 A/us

- Turn-off time = Reverse recovery time + Gate recovery time
  $t_q = t_{rr} + t_{gr}$ typically upto 50 us for inverter grade SCR (obsolete)
  and 50 – 100 us for converter grade SCR (50 - 400 Hz)

- Reverse recovery charge = (Reverse recovery current x Reverse recovery time)/2

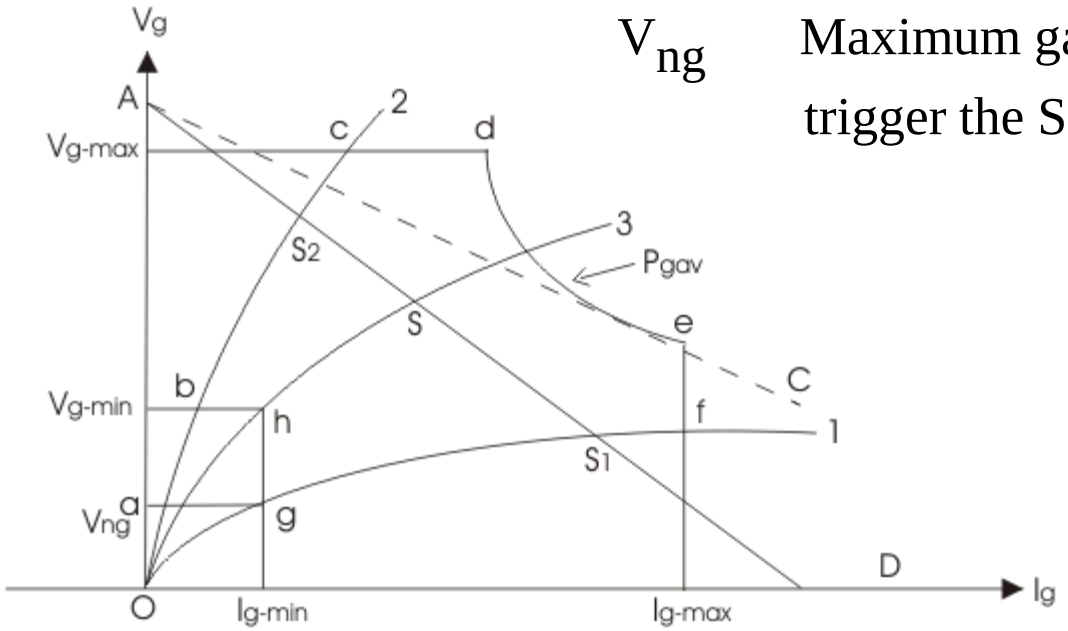
  $Q_{rr} = I_{rr} \times t_{rr} /2$ same as that for power diode (Power Diodes-3) (1.2)

SCR -8 (Turn-on and turn-off switching characteristics)

- Maximum permissible value of re-applied dV_{AK}/dt, typically 100 V/us – few KV/us, is related to the J_2 junction capacitance C_{J2} and the limiting value of the gate charging current to turn on the SCR I_{J2} as follows:

$$I_{J2} = C_{J2} \times dV_{AK}/dt \qquad (1.3)$$

SCR -9 (Gate characteristics)



V_{ng} Maximum gate voltage which will not trigger the SCR

$V_{g\text{-}max}$ Maximum allowable gate voltage

$I_{g\text{-}max}$ Maximum allowable gate current

P_{gav} Maximum allowable average gate power dissipation

$V_{g\text{-}min}$ Minimum gate voltage for proper operation

$I_{g\text{-}min}$ Minimum gate current for proper operation

V_{GT} Recommended gate voltage for turn-on

I_{GT} Recommended gate current for turn-on

FIGURE 1.10

SCR -10 (Gate characteristics)

Curve 1 corresponds to characteristics at maximum temperature

Curve 2 corresponds to characteristics at minimum temperature

Curve 3 corresponds to characteristics at normal operating temperature

Hence operating point must lie inside the region b-c-d-e-f-g-h-b

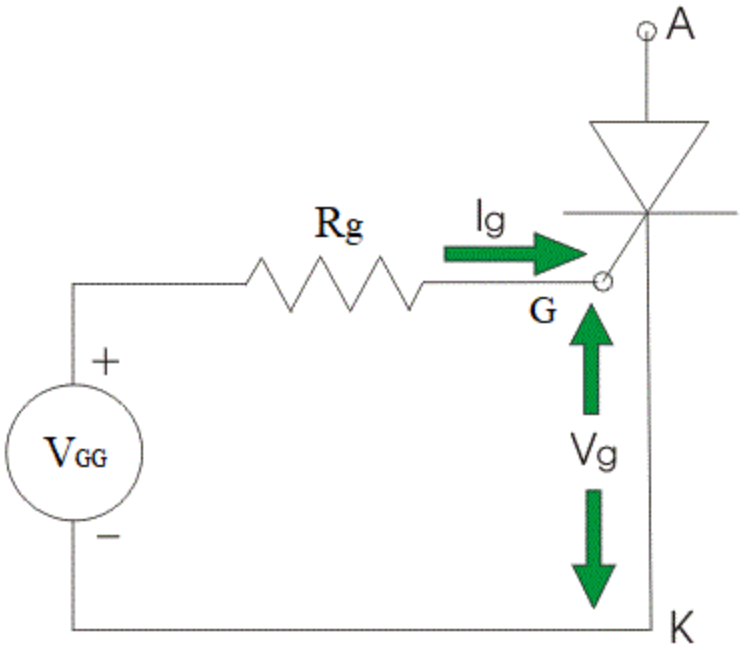


FIGURE 1.11

Now, from the triggering circuit, we get

$$V_{GG} = Vg + Ig \times Rg \qquad (1.4)$$

where V_{GG} = gate source voltage

Vg = gate cathode voltage

Ig = gate current

Rg = gate source resistance

For the SCR, Vg vs Ig curve may be expressed graphically or by equations $Vg = A + B \times Ig$, $Vg = A + B \times Ig + C \times Ig^2$, etc.

SCR -10 (Gate characteristics)

The load line of gate source voltage is drawn as AD where OA = V_{GG} and OD = V_{GG} /Rg which is gate trigger circuit short circuit current.

Slope of load line AD = -Rg

The V-I characteristic of gate circuit is given by curve 3.

The intersection point of load line (AD) and curve 3 is called as operating point S which lies between S1 and S2 on the load line.

For decreasing the turn-on time and to avoid unwanted turn-on of the device, operating point should be as close to P_{gav} as possible.

For a rectangular pulse train at a triggering frequency F = 1/T Hz with on-time of T_{on} and peak gate power of P_{gpeak} , the average gate power is given by

$P_{gav} = K \times P_{gpeak}$ where the duty cycle $K = T_{on}/T = F \times T_{on}$ (1.5)

SCR -11 (Ratings)

1. Peak Repetitive Forward Blocking Voltage (V_{DRM})

It specifies the peak forward transient voltage that a SCR can block repeatedly or periodically in forward blocking mode.
This rating is specified at a maximum allowable junction temperature with gate circuit open.
During commutation process, due to high decreasing rate of reverse anode current a voltage spike Ldi/dt is produced which is the cause of V_{DRM} generation.

2. Peak Non-Repetitive or Surge Forward Blocking Voltage (V_{DSM})

It is the peak value of the forward transient voltage that does not appear periodically.
This type of over voltage generated at the time of switching operation of circuit breaker. This voltage is 130 % of V_{DRM}), although it lies under the forward break over voltage (V_{BD}).

3. Peak Repetitive Reverse Voltage (V_{RRM})

It is the value of transient voltage that can be withstand by SCR in reverse bias at maximum allowable temperature.

SCR -12 (Ratings)

4. Peak Non Repetitive Reverse Voltage (V_{RSM})

It is the value of the reverse transient voltage that does not appear repetitively. Though this voltage value is 130% of V_{RRM}, it lies under reverse break over voltage, V_{BR}.

5. Forward ON State voltage Drop (V_T)

This is the voltage drop across the anode and cathode when rated current flows through the SCR at rated junction temperature. Generally this value lies between 1 to 1.5 volts.

6. Re-applied Forward dv/dt Rating

When a forward voltage is applied to the thyristor, Junction J_1 and J_3 are forward biased whereas junction J_2 is reverse biased and hence it acts a capacitor.
So due to $C_{J2} \times dV_{AK}/dt$ action, an equivalent gate current is injected into the junction which can cause spurious turn-on, which is highly undesirable.

SCR -13 (Ratings)

7. Maximum RMS Current Rating (I_{RMS})

The power loss in the SCR is $I_{RMS}^2 R$ where R is the equivalent resistance of the device, and this power loss causes temperature rise. The I_{RMS} rating is such that the maximum junction temperature is not exceeded with the case temperature T_C at 25ºC.

8. Maximum Average Current Rating (I_{AV})

It is the allowable average current that can be applied safely such that maximum junction temperature and rms current limit cannot be exceeded. Generally manufacturer of SCR, provides a characteristic diagram which shows I_{AV} as a function of the case temperature T_C with the current conduction angle φ as a parameter.
This characteristic is known as "forward average current de-rating characteristic".

SCR -14 (Ratings)

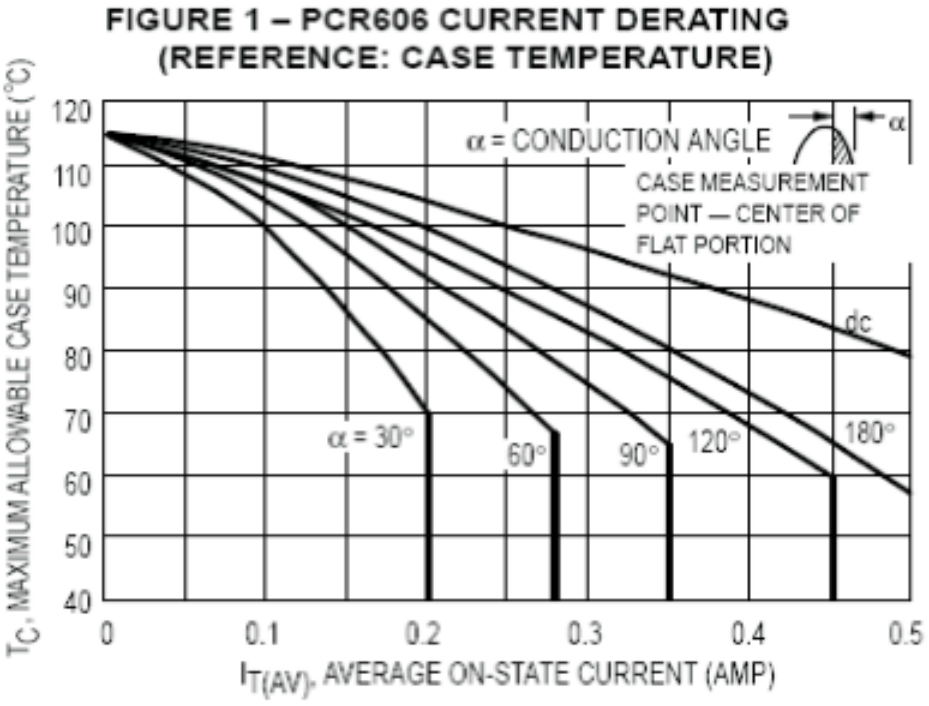


FIGURE 1.12

SCR -16 (Ratings)

9. Maximum Surge Current (I_{SM})

If a thyristor operates under its repetitive voltage and current ratings, its maximum allowable temperature is never exceeded.
However, an SCR may fall into a abnormal operating condition due to fault in the circuit.
To overcome this problem, a maximum allowable surge current rating is also specified by manufacturer.
This rating specifies maximum non repetitive surge current, that the device can withstand. This rating is specified dependent upon the number of surge cycles e.g.
I_{SM} = 3,000A for 1/2 cycle
I_{SM} = 2,100A for 3 cycles
I_{SM} = 1,800A for 5 cycles
A plot between I_{SM} and cycle numbers is also provided for dealing with the various cycle surge current.

SCR -15 (Ratings)

10. I^2t Rating of SCR

This rating is the measure of energy that can be handled by a thyristor for a short while.
If an HRC (high rupturing capacity) electrical fuse is used to protect a SCR, the fuse I^2t rating must be less than that of thyristor for proper protection.

11. di/dt Rating

During SCR turn on, conduction stays in a very small area nearer to the gate during the rise time t_r.
This small area of conduction spreads throughout the whole area of the junction during the spread time t_f.
In case the spreading velocity of the charge carriers is smaller than the di/dt, then local hot spot may arise nearer to the gate which may destroy the device.
Hence this di/dt rating is necessary.

SCR -16 (Ratings)

12. Latching Current I_L

This is an OFF to ON specification i.e. during turn-on.
It is the minimum anode current for which the SCR remains on when the gate current is reduced to zero after turn-on.
If the anode current is less than I_L , then the SCR will conduct as long as the gate current is present, but will turn-off as soon as the gate current is reduced to zero i.e. the **SCR does not latch-on**.

13. Holding Current I_H

This is an ON to OFF specification i.e. during turn-off.
It is the minimum anode current for which the SCR remains on with zero gate current after it has latched-on.
If the anode current falls below I_H , the SCR will turn-off **immediately**.

14. Recommended Gate Current to Trigger (I_{GT})

The gate circuit should deliver this current for proper operation.
It is specified at a particular forward break down voltage.

SCR -17 (Ratings)

15. Recommended Gate Voltage to Trigger (V_{GT})

The gate circuit should deliver this voltage for proper operation.
It is specified at a particular forward break down voltage.

16. Non Triggering Gate Voltage (V_{NG})

This is the maximum value of gate circuit source voltage below which the device must be in off state.
All unwanted noise signals must lie under this voltage to avoid unwanted turn on of the device.

17. Peak Reverse Gate Voltage (V_{GRM})

This is the value of maximum reverse voltage which can be applied across the cathode and gate.

18. Average Gate Power Dissipation (P_{GAR})

This is the value of average power dissipation which cannot be exceeded by a gate circuit for a gate current pulse wider than 100 microseconds.

SCR -18 (Ratings)

Peak Forward Gate Current (I_{GRM})

This is the value of maximum forward gate current that should not be exceeded for reliable and safe operation.

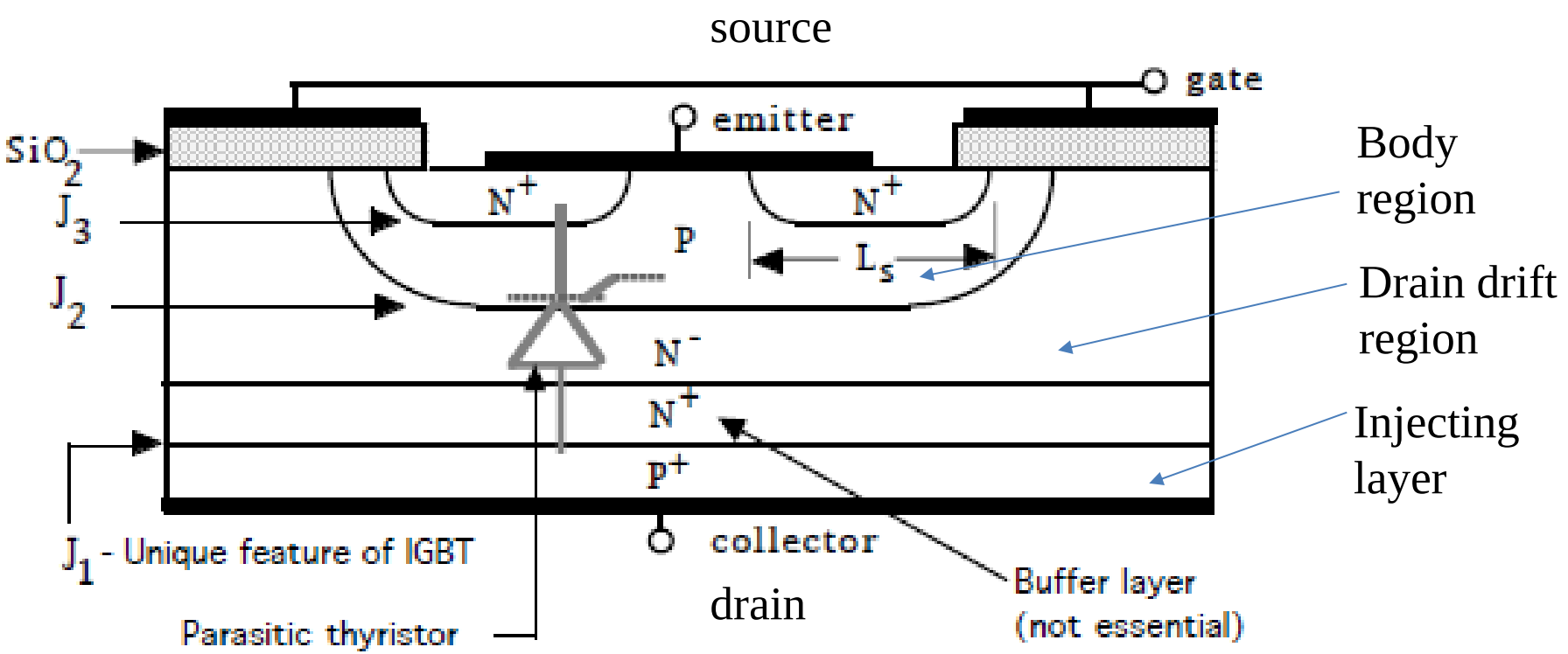
IGBT -1 (general)

- IGBT (insulated gate bipolar transistor), is a voltage controlled, three terminal, four layer p-n-p-n, non-latching type, unidirectional power semiconductor switching device.
- The output terminals for the MOSFET type symbol of IGBT are D (drain) and S (source) while G (gate) is the control terminal.
- The output terminals for the BJT type symbol of IGBT are C (collector) and E (source) while G (gate) is the control terminal.
- Current can flow only from D (C) to S (E) and not vice-versa.
- IGBT combines the best features of the MOSFET and BJT
- Gate circuit is voltage controlled like a MOSFET and hence control power is minimal as compared to a BJT
- Output circuit is like a BJT i.e. in the ON state, it is modelled as a voltage sink in series with a small resistance unlike a MOSFET which is modelled as a resistor which can be large for high voltage devices. Thus ON state losses are proportional to I_D like a BJT and not to I_D^2 like MOSFETS

IGBT -2 (general)

- Unlike a BJT which suffers from second breakdown, the IGBT does not suffer from the same. In this respect it is similar to a power MOSFET.
- Ratings of IGBTs are upto 6500V and 2400A with switching frequencies upto 20KHz.
- IGBT has switching speeds faster than BJTs but slower than MOSFETs.

IGBT -3 (Structure)



- Cell structure similar to power MOSFET (VDMOS) cell.
- P-region at collector end unique feature of IGBT compared to MOSFET.
- Punch-through (PT) IGBT - N^+ buffer layer present. Anti-symmetric
- Non-punch-through (NPT) IGBT - N^+ buffer layer absent. Symmetric

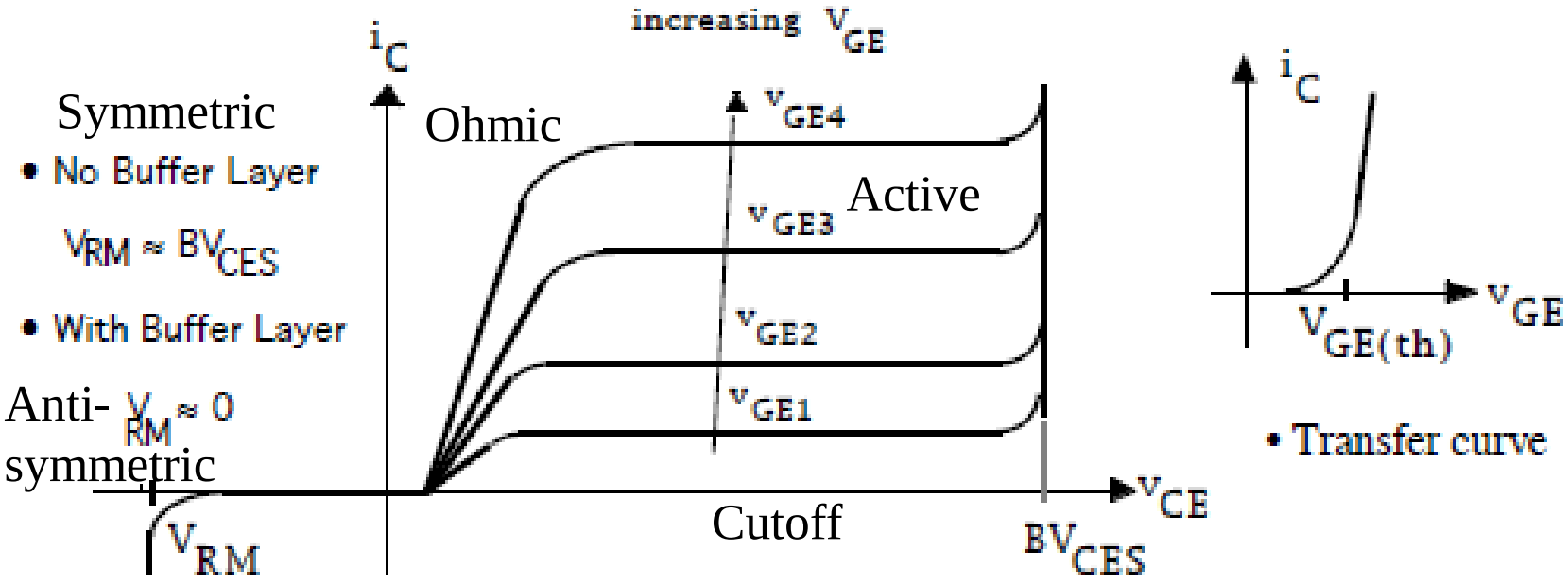
FIGURE 1.13

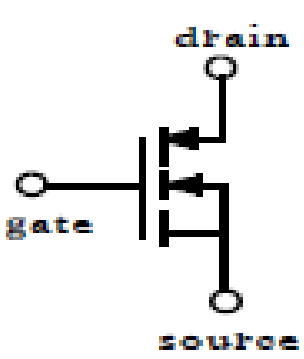
IGBT -4 (Symmetric and asymmetric types)

- Blocking state operation - $V_{GE} < V_{GE(th)}$
- Junction J_2 is blocking junction - n^+ drift region holds depletion layer of blocking junction.
- Without N^+ buffer layer, IGBT has large reverse blocking capability - so-called symmetric IGBT
- With N^+ buffer layer, junction J_1 has small breakdownvoltage and thus IGBT has little reverse blocking capability - anti-symmetric IGBT
- Buffer layer speeds up device turn-off

IGBT -6 (Output and control characteristics & symbols)

IGBT I-V Characteristics and Circuit Symbols





MOSFET type symbol

• N-channel IGBT circuit symbols

BJT type symbol

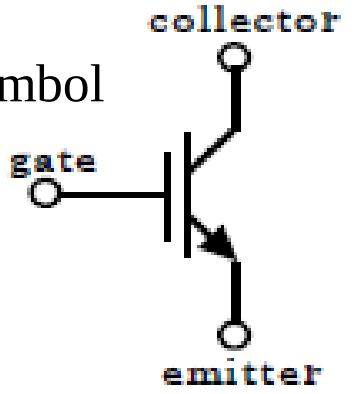
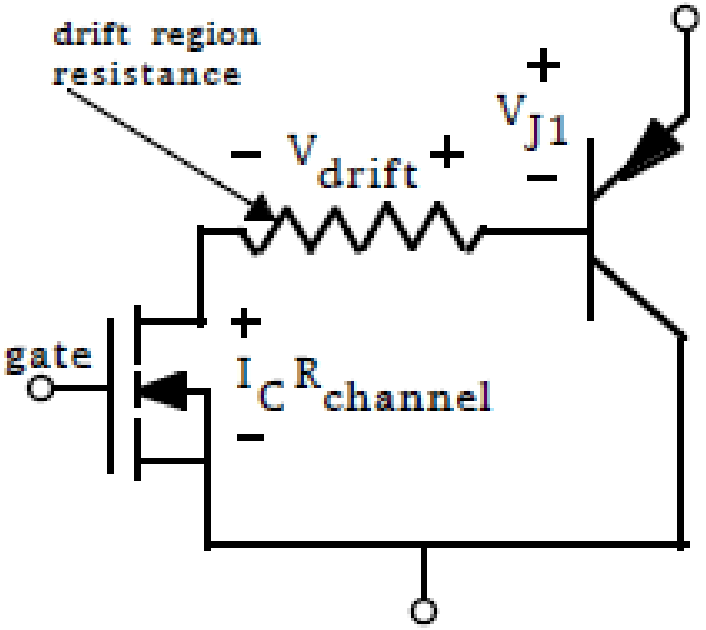
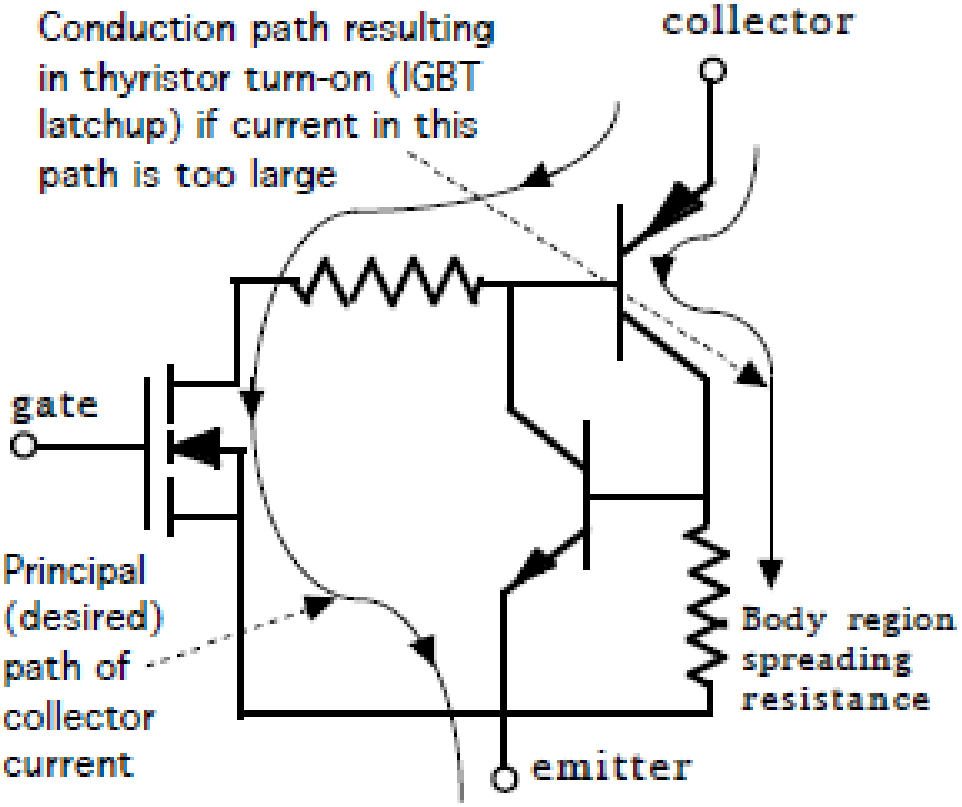


FIGURE 1.14

IGBT -5 (Equivalent circuits – drain/collector)

Approximate Equivalent Circuits for IGBTs





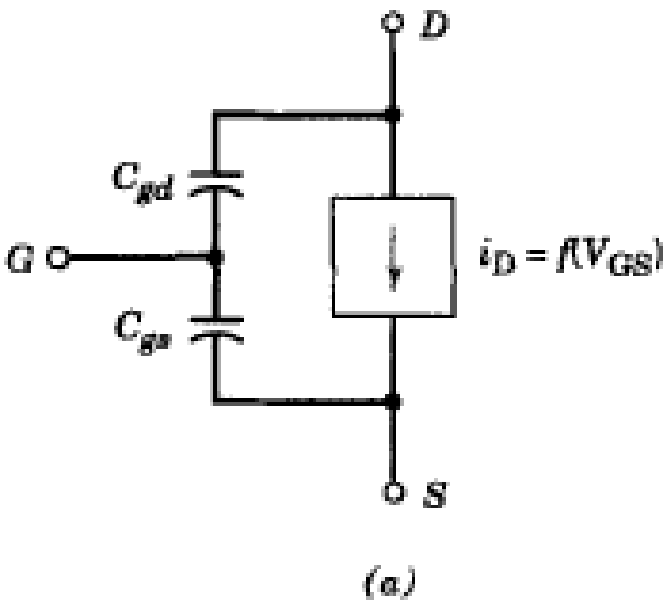
- Approximate equivalent circuit for IGBT valid for normal operating conditions.

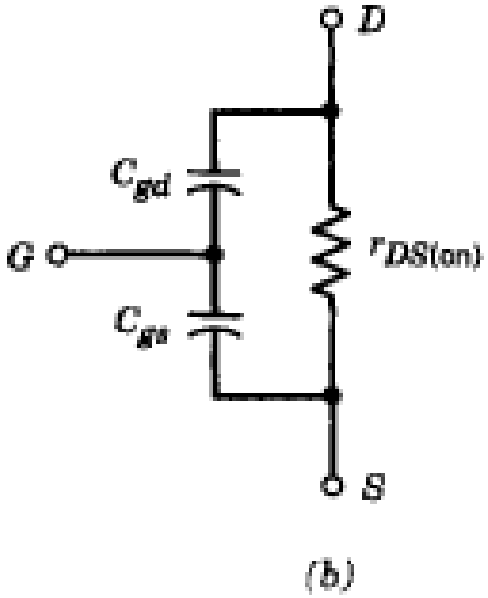
- $V_{CE(on)} = V_{J1} + V_{drift} + I_C R_{channel}$

FIGURE 1.15

• IGBT equivalent circuit showing transistors comprising the parasitic thyristor.

IGBT -7 (Equivalent circuits - gate)





Ohmic (ON) region

Cutoff (OFF) and active regions

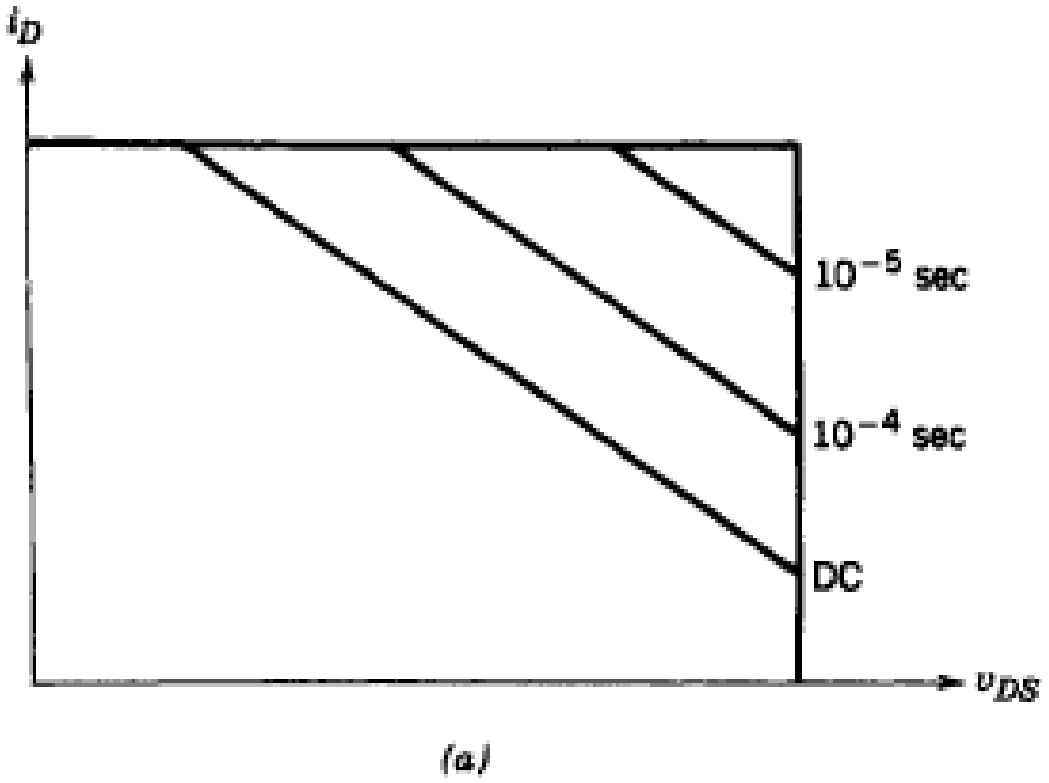
Equivalent gate input capacitance during turn-on and turn-off

$C_{gin} = C_{gs} \,||\, C_{gd} = C_{gs} + C_{gd}$ (same as power MOSFET) (1.6)

Hence gate circuit charging (turn-on) and discharging (turn-off) time constant is $\tau = R_g \times C_{gin}$ (same as power MOSFET) (1.7)

FIGURE 1.16

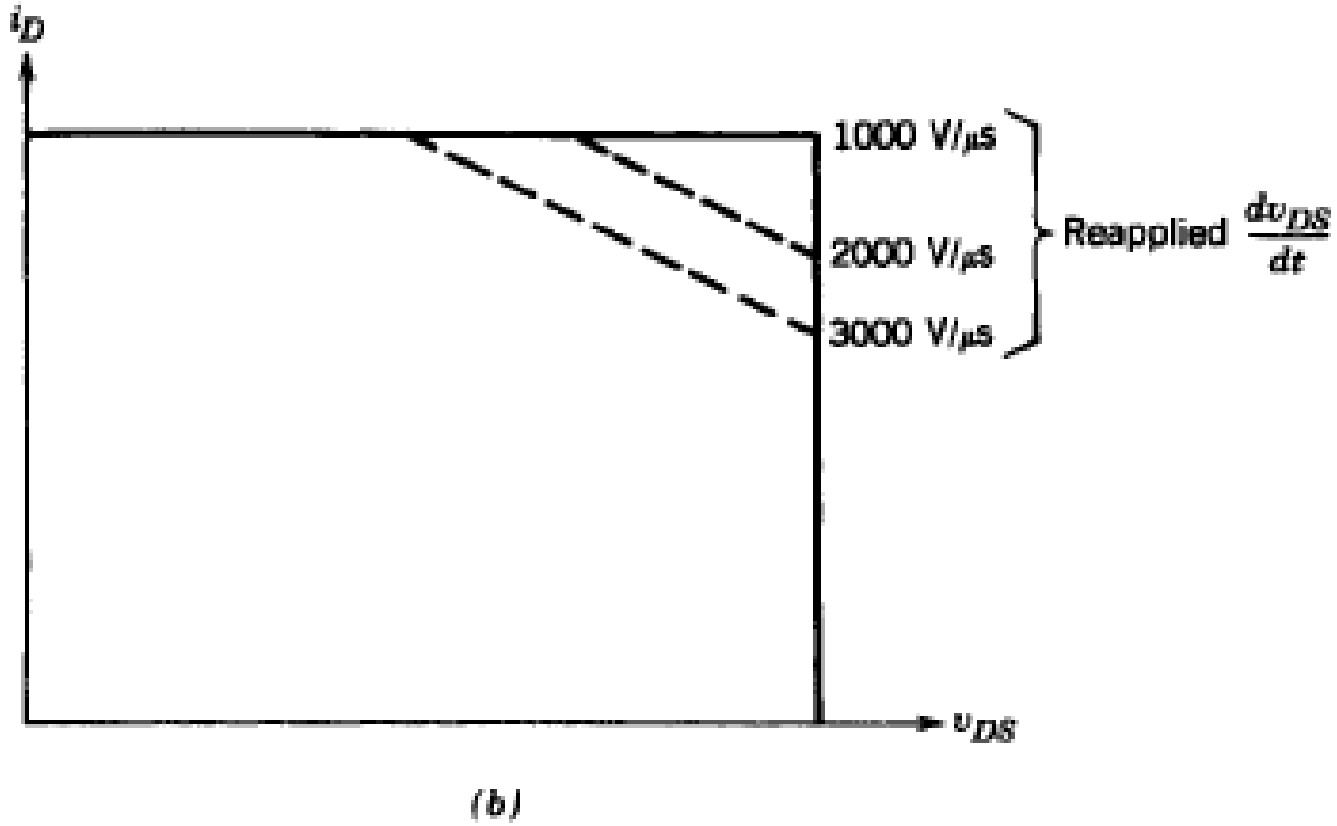
IGBT -8 (Forward biased safe operating area)



FBSOA

FIGURE 1.17

IGBT -9 (Reverse biased safe operating area)



(b)

RBSOA

FIGURE 1.18

Gate triggering and gate drive circuits with isolation -1

- **Reducing noise interference (conducted EMI)**

  Modern power converters depend on a PWM scheme to control output voltage and current. However, in higher power applications, di/dt and dv/dt signal introduced by power switching can introduce noise in the control circuits via parasitic parameter coupling in the PCB layout. The same is true in case of lightning strikes, voltage surges and sags in the power circuits. By adopting **galvanic isolation between power and control circuits**, the noise in control circuits can be reduced.

- **Voltage levels**

  Power circuits of are usually connected to dangerous voltages ranging from typically 230 V / 415 V AC to several hundred KV and the rectified DC bus voltage can range from 325 V to several hundred KV and can carry large currents upto several KA. On the other hand, the control circuit is usually at 3.3 V to 24 V and the Control Ground is connected to Safety Ground (earth). Thus, **galvanic isolation is needed between power and control circuits** to protect the control circuit and the operators from dangerous voltages.

- **Elimination of ground loops** – These ground loops can cause the control and power circuits to **malfunction**.

Gate triggering and gate drive circuits with isolation -2

- **Control ground and power device ground at different potentials**

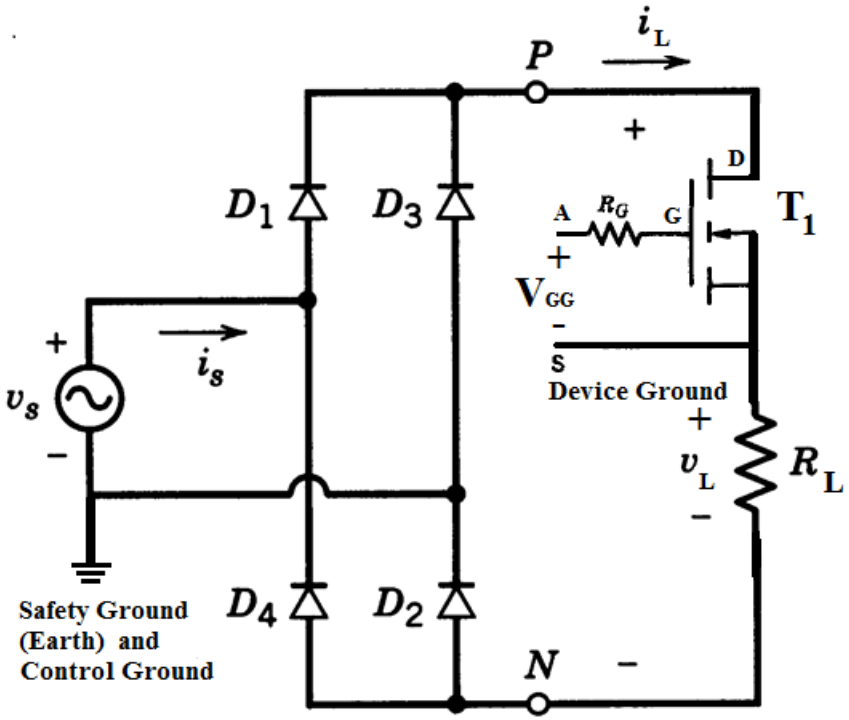


FIGURE 1.19

- Diodes D1 to D4 and switch T1 are considered to be **ideal switches**.
- During +ve half cycle when D1 & D2 are ON, P and drain D of T1 is connected to upper (+) terminal of mains supply v_S and varies from 0 V to +ve peak to 0 V.
- As long as T1 is OFF, $i_L = 0$, $v_L = 0$, and hence Device Ground S and N is connected to lower (-) terminal of mains supply which is at Safety and Control Ground.

- When T1 is turned ON, Device Ground S gets shorted to drain D and its potential varies as the mains supply v_S. Thus Device Ground S is no longer connected to Safety and Control Ground.

Gate triggering and gate drive circuits with isolation -3

- **Control ground and power device ground at different potentials (contd.)**

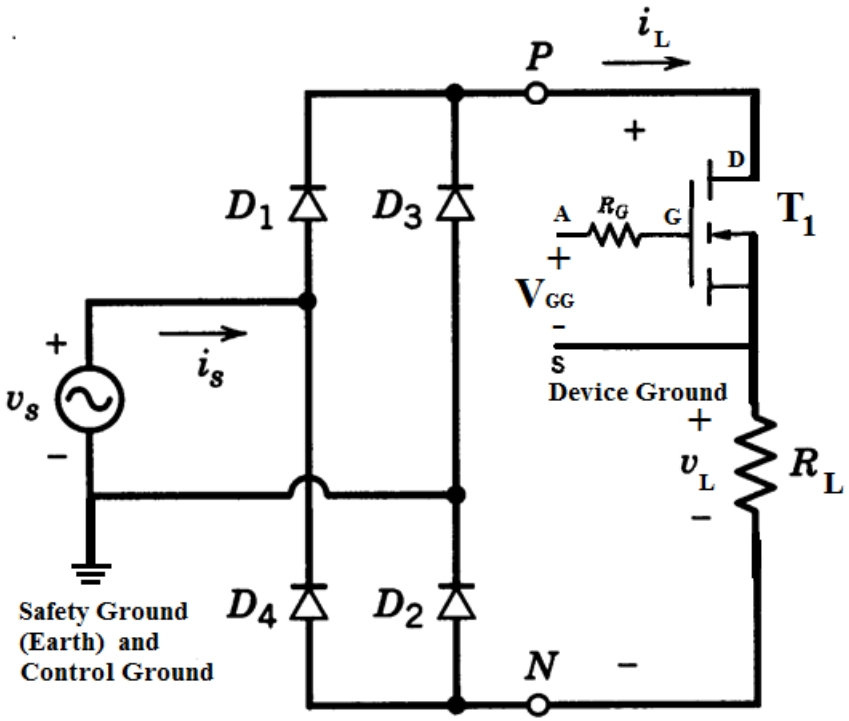


FIGURE 1.19

- During -ve half cycle when D3 & D4 are ON, P and drain D of T1 is connected to lower (-) terminal of mains supply v_S and is at Safety and Control Ground.
- As long as T1 is OFF, $i_L = 0$, $v_L = 0$, and hence Device Ground S and N is connected to upper (+) terminal of mains supply v_S and varies from 0 V to -ve peak to 0 V. Thus Device Ground S is no longer connected to Safety and Control Ground.

- When T1 is turned ON, Device Ground S gets shorted to drain D and P which is connected to Safety and Control Ground.
- Since the Device Ground is **not always at the same potential** as the Control Ground, **galvanic isolation is necessary between power and control circuits**.

Gate triggering and gate drive circuits with isolation -4

- Galvanic isolation can be provided by:
  Pulse transformers (PT)
  Optocouplers
  Fibre optics

- In PT circuits, a high frequency (10 KHz to 1 MHz) rectangular pulse train from a high frequency oscillator (HFO) is modulated by a control signal, and this modulated signal is applied to the primary of the transformer. The isolated secondary voltage can be stepped-up or stepped-down and is applied to the gate circuit of a SCR. Multiple secondary windings permit several switches to be simultaneously turned-ON and OFF.

  The main advantage of PTs is that both the control signal as well as control power can be transferred from primary to the secondary side. Hence a separate isolated power supply is not needed on the secondary side.

  For proper operation, the PT should have a very small leakage inductance and fast rise-time.

Gate triggering and gate drive circuits with isolation -5

- An optocoupler comprises of a infrared photodiode at the input and a silicon phototransistor at the output, whose base-emitter is irradiated by photons emitted by the photodiode when input current flows through the diode. This turns ON the phototransistor which goes into saturation from its earlier OFF state (cut-off).
- The rise and fall times of optocouplers are very small viz. t_{on} = 2 – 5 us and t_{off} = 300 us, which limits the upper frequency of operation.
- The capacitance between the input photodiode and the base of the phototransistor should be as small as possible to avoid **spurious operation** of the device during turn-ON and turn-OFF of the power switch. This requires electrical shields between the photodiode and the phototransistor.
- The main drawback of optocouplers is that they can only transmit the control signal but not the control power like PTs. Therefore all optocouplers require isolated power supplies on the output side, which add to the complexity, cost and weight of the gate drive circuit.

Gate triggering and gate drive circuits with isolation -6

- The fibre optic gate triggering circuit is basically the optocoupler cicuit "opened-out". Whereas in the optocoupler, the input photodiode and the output phototransistor and in the same IC package, here the photodiode transmitter is mounted on the control circuit PCB while the phototransistor receiver is mounted on the drive circuit PCB with the transmitter and receiver being connected by a fibre optic cable.

  The main advantage of this method is the ability to provide very high electrical isolation and creepage distances between the control circuit and power circuit. Also the problem of **spurious operation** which is present in optocouplers during turn-ON and turn-OFF of the power switch is completely eliminated.

  This technique is extensively used for simultaneously triggering banks of series connected SCRs used in HVDC converter stations.

SCR -19 (Pulse transformer isolated HF gate trigger circuit)

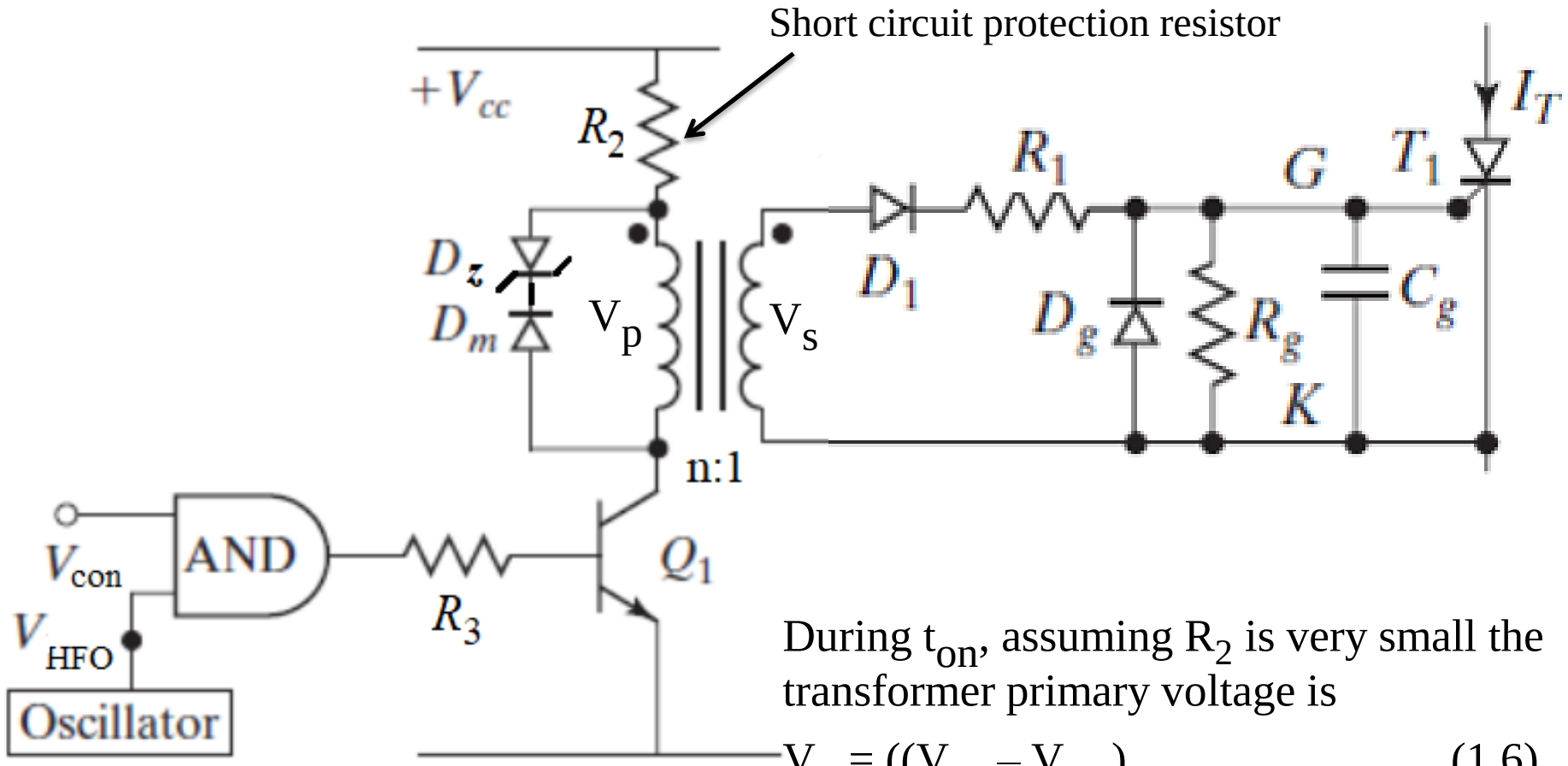


FIGURE 1.19

During t_{on}, assuming R_2 is very small the transformer primary voltage is

$$V_p = ((V_{cc} - V_{sat}) \qquad (1.6)$$

Using Faraday's law $V_p = N\, d\Phi/dt$ or $d\Phi = V_p\, dt/N$

Hence flux increase during t_{on} is $V_p \times t_{on}/N$ (1.7)

SCR -20 (Pulse transformer isolated HF gate trigger circuit)

During t_{on}, assuming R_2 is very small and R_g is very large, the gate current is:

$$I_g = V_p/n - V_D - V_{GT}) / R_1 = ((V_{cc} - V_{sat}) /n - V_D - V_{GT}) / R_1 \quad (1.8)$$

As far as possible this value should be equal to $I_{GT.}$

During t_{off} , as the switch Q_1 starts opening, the primary current and flux start reducing resulting in –ve $d\Phi/dt$ and –ve V_p . Hence diode D_m and zener diode D_m become forward biased and conduct, clamping the primary voltage to $V_p = -(V_D + V_Z)$.

Thus flux decrease during t_{off}' is $(V_D + V_Z) \times t_{off}'/N$ (1.9)

In the steady state, to prevent the transformer core from saturating, the net flux change over a complete cycle should be zero.

Hence $(V_{cc} - V_{sat}) \times t_{on}/N = (V_D + V_Z) \times t_{off}'/N$

or $t_{on} / t_{off}' = (V_D + V_Z) / (V_{cc} - V_{sat})$ (1.10)

with $t_{off}' < t_{off} = (1 - K) \times T$ (1.11)

in the limiting case of $t_{off}' = t_{off}$, $K_{max} = (t_{on} / (t_{on} + t_{off}))$

thus $K_{max} = (V_D + V_Z) / (V_D + V_Z + V_{cc} - V_{sat})$ (1.12)

SCR -21 (Pulse transformer primary voltage waveforms)

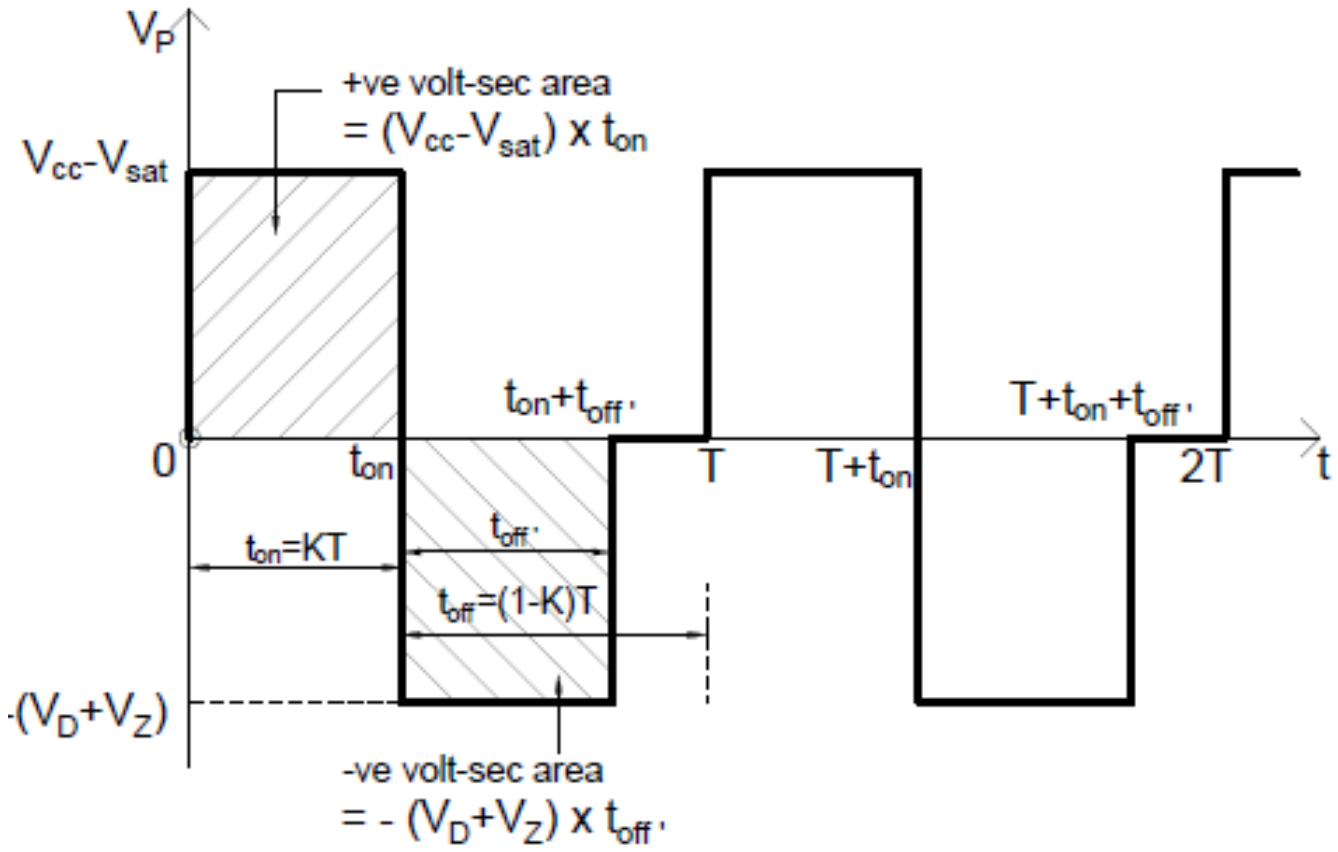


FIGURE 1.20

MOSFET / IGBT -1 (Optocoupler isolated gate trigger circuit)

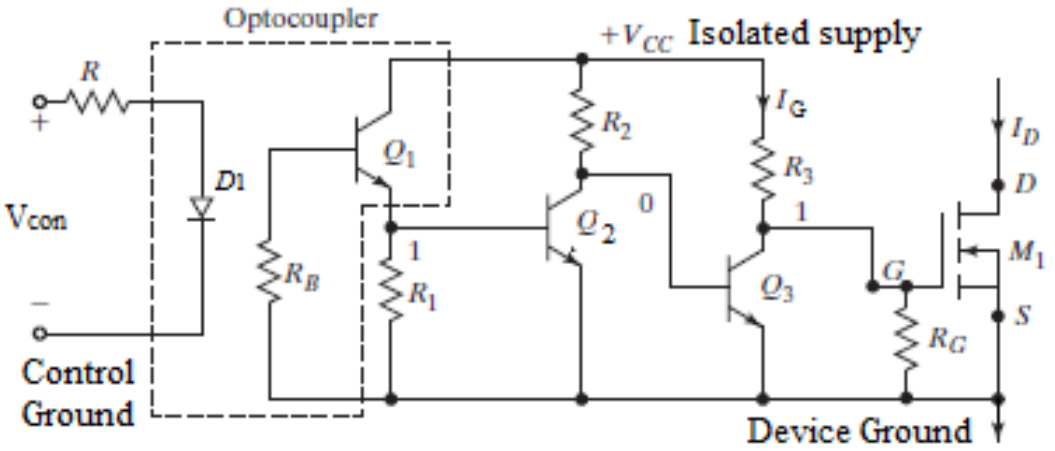


FIGURE 1.21

During t_{on}, the control voltage V_{con} goes high and the diode D1 of the optocoupler conducts through input resistor R and turns-ON the output phototransistor Q_1 which then turns-ON signal transistor Q_2 whose collector goes low. This then turns-OFF driving transistor Q_3 and thus gate current I_G flows through R_3 to turn-ON the MOSFET / IGBT M_1 by charging the internal gate input capacitance.

During t_{off}, the control voltage V_{con} goes low and the diode D1 of the optocoupler turns-OFF which then turns-OFF signal transistor Q_2 whose collector is pulled-up high. This then turns-ON driving transistor Q_3 and thus reverse gate current flows through Q_3 to turn-OFF the MOSFET / IGBT M_1 by discharging the internal gate input capacitance.

MOSFET / IGBT -2 (Optocoupler isolated gate trigger circuit)

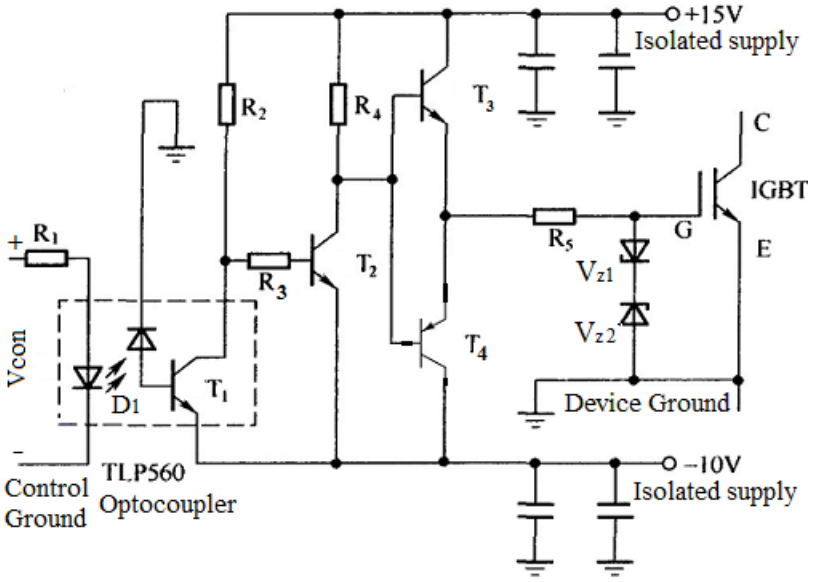


FIGURE 1.22

During t_{on}, the control voltage V_{con} goes high and the diode D1 of the optocoupler conducts through input resistor R_1 and turns-ON the output phototransistor T_1 which then turns-OFF signal transistor T_2 whose collector goes high. This then turns-ON driving transistor T_3 and turns-OFF driving transistor T_4 of the complementary npn-pnp emitter follower pair T_3-T_4 .Thus gate current I_G flows through R_5 to turn-ON the MOSFET / IGBT by charging the internal gate input capacitance.

MOSFET / IGBT -3 (Optocoupler isolated gate trigger circuit)

During t_{off}, the control voltage V_{con} goes low and the diode D1 of the optocoupler goes off and turns-OFF the output phototransistor T_1 whose collector is pulled-up which then turns-ON signal transistor T_2 whose collector goes low. This then turns-OFF driving transistor T_3 and turns-ON driving transistor T_4 of the complementary npn-pnp emitter follower pair T_3-T_4 .Thus gate current I_G reverses through R_5 to turn-OFF the MOSFET / IGBT by discharging the internal gate input capacitance.

Protection of Power Devices -1

- Power devices have to be protected against the following conditions which can result in catastrophic failure:

  a) thermal runaway
  b) high di/dt , dv/dt and reverse recovery transients
  c) supply and load transients
  d) short circuit and overload conditions

- Thermal runaway can occur if the heat dissipated in the device due to various losses such as turn-on loss, turn-off loss and conduction loss is not properly dissipated resulting heat building up in the semiconductor die. This can cause the junction temperature to exceed the upper permissible limit causing runaway.

  Heat sinks as well as forced air/liquid cooling systems are employed to cool the device by convection.

  Cooling of power devices and selection of heat sinks is based on the heat flow from the equivalent junction to the case of the device, from the case of the device to the heat sink and from the heat sink to the ambient atmosphere.

Protection of Power Devices -2

- In the steady state i.e. all temperatures have stabilized and are constant. In this case the heat flow is modelled by the static electrical equivalent circuit shown below:

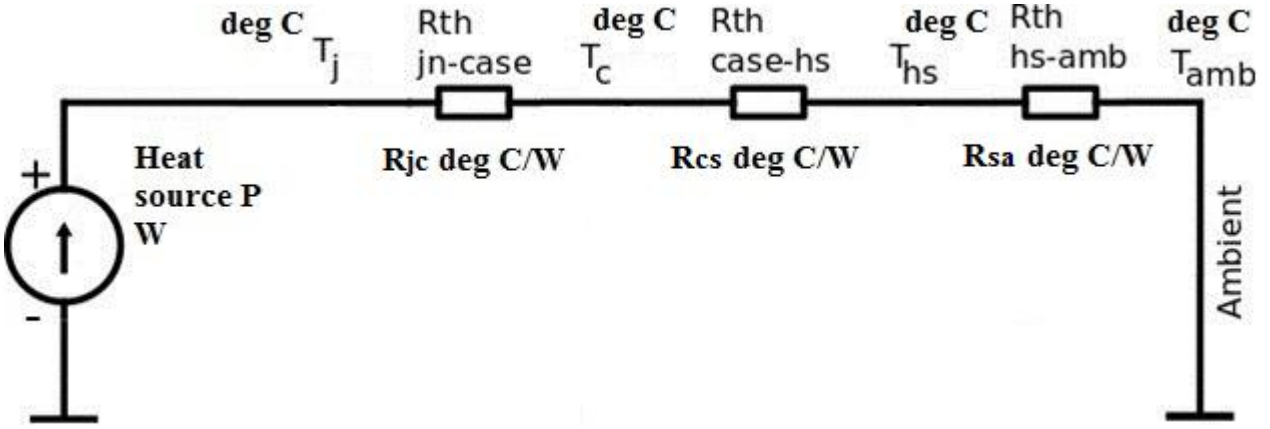


FIGURE 1.23

- The equivalent junction temperature T_J of the power semiconductor device is given by $T_J = P \times (R_{JC} + R_{CS} + R_{SA}) + T_A$ (1.13)

where P = average power loss in the device
R_{JC} = thermal resistance from junction to case °C/W
R_{CS} = thermal resistance from case to heat sink °C/W
R_{SA} = thermal resistance from heat sink to ambient °C/W
T_C = case temperature °C
T_S = heat sink temperature °C
T_A = ambient temperature °C

Protection of Power Devices -3

- The above equation can be re-arranged in the following equivalent ways to obtain various parameters:

$$P = (T_J - T_A)/(R_{JC} + R_{CS} + R_{SA}) \quad (1.14)$$

$$T_C = T_J - (P \times R_{JC}) = T_A + P \times (R_{CS} + R_{SA}) \quad (1.15)$$

$$T_S = T_J - P \times (R_{JC} + R_{CS}) = T_A + P \times R_{SA} \quad (1.16)$$

- In the dynamic state i.e. the device is operating under pulsed conditions, then the power loss will have the nature of a rectangular pulse train, with the height of each pulse depending on peak power loss at that instant. In such a case the heat capacity of the three junctions viz. junction-to-case, case-to-heat sink and heat sink-to-ambient are considered in the form of junction thermal capacitances as shown in the dynamic electrical equivalent circuit shown below.

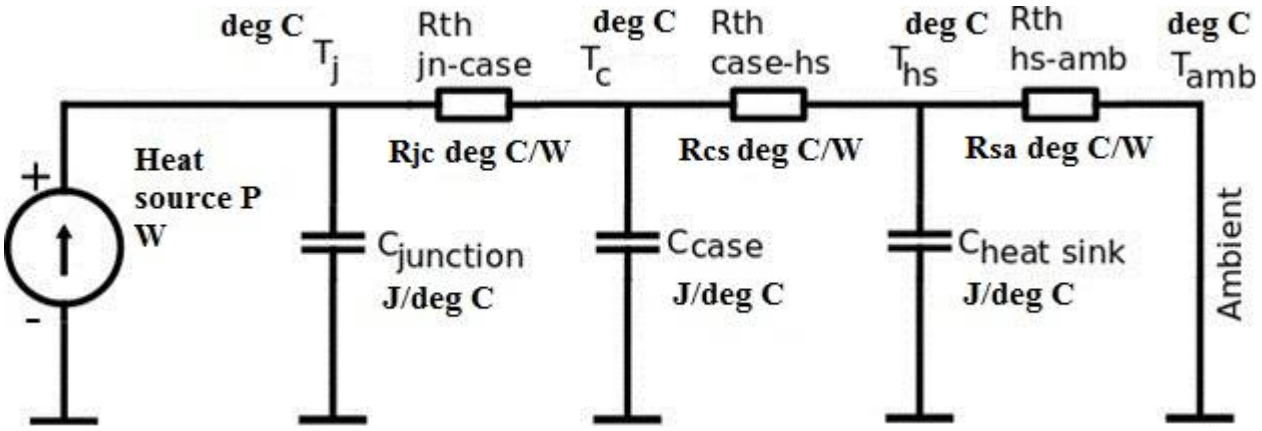


FIGURE 1.24

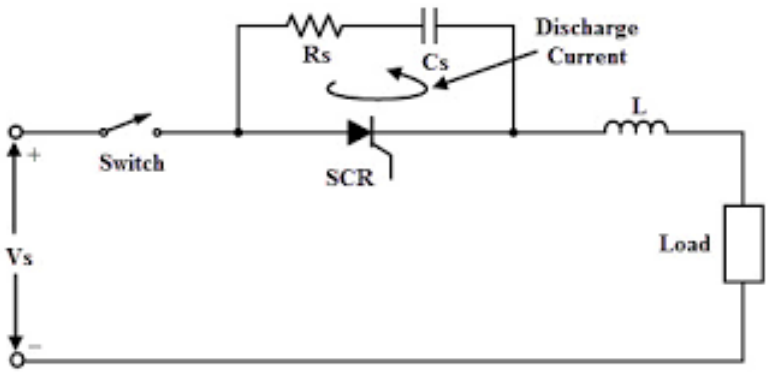
Protection of Power Devices -4

- High di/dt , dv/dt and reverse recovery transients occur due to switch turn-ON and turn-OFF as well due to the presence of stray inductance and feedback diodes. Snubbers are used to protect against them which fall into three types:

a) turn-off snubbers which fall into two categories viz. non-polarized R-C snubbers for SCRs and diodes and polarized R-C-D snubbers for BJTs, MOSFETS and IGBT.

b) turn-on snubbers which are polarized L-R-D types

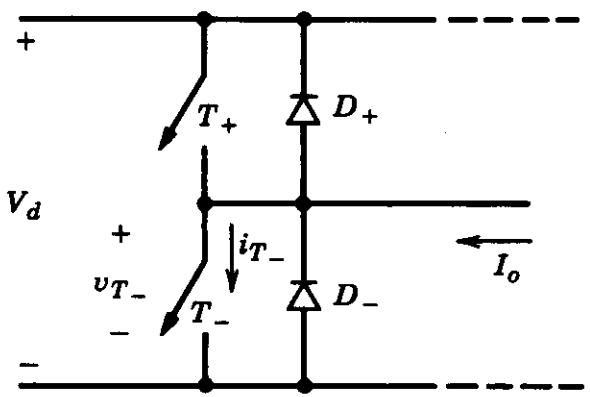
c) overvoltage snubbers which are polarized R-C-D types



Non-polarized R-C turn-off and overvoltage snubber for SCRs, triacs and diodes

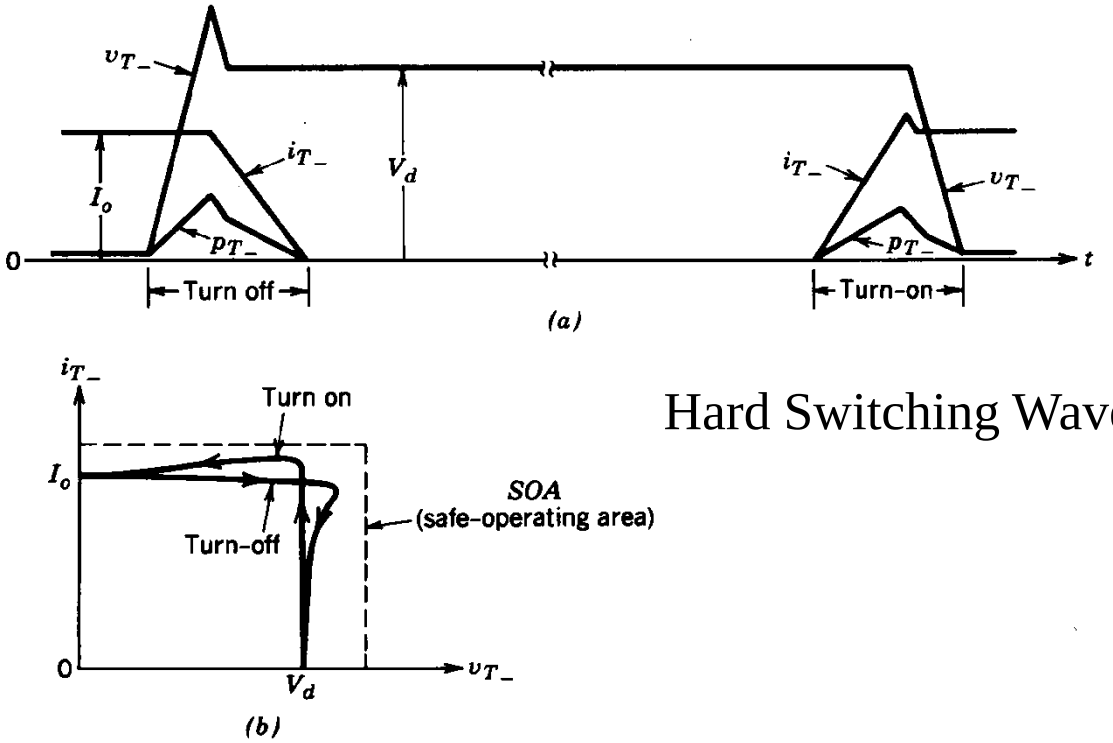
FIGURE 1.25

Protection of Power Devices -5



- Clamped inductive load
- The output current can be positive or negative

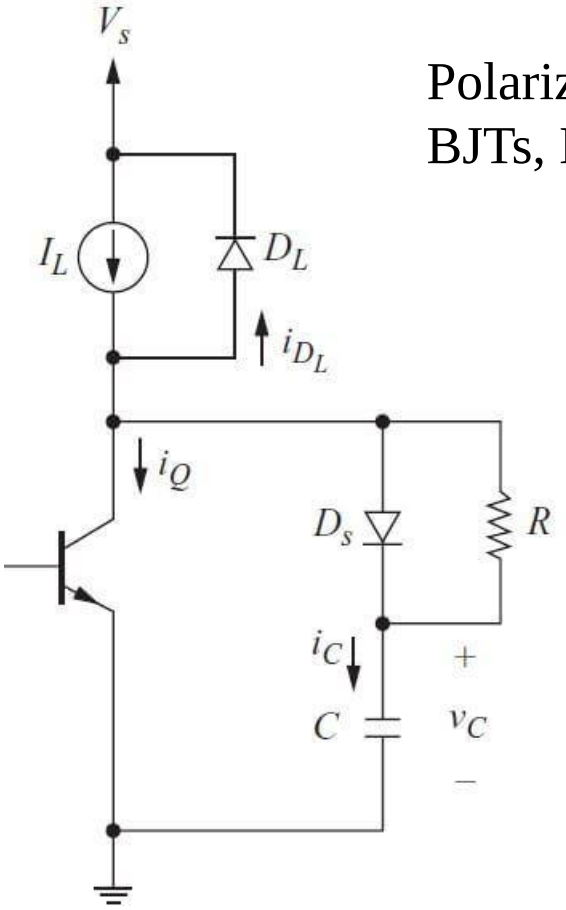
Figure 9-1 One inverter leg.



Hard Switching Waveforms

Figure 9-2 Switch-mode inductive current switchings.

Protection of Power Devices -6



Polarized R-C-D turn-off snubber for BJTs, MOSFETs and IGBTs

FIGURE 1.26

Protection of Power Devices -7

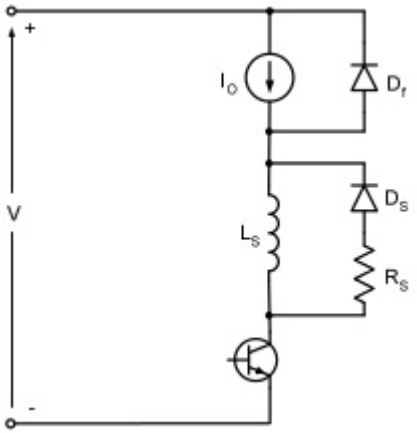


FIGURE 1.27

Polarized R-L-D turn-on snubber for BJTs, MOSFETs and IGBTs

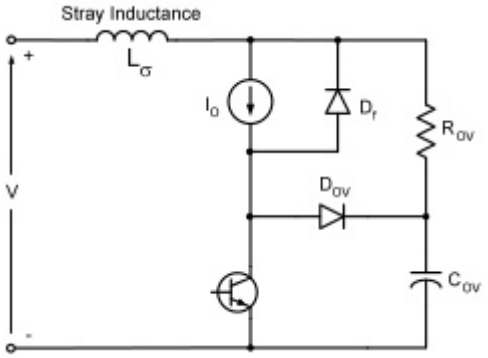


FIGURE 1.28

Polarized R-C-D over-voltage snubber for BJTs, MOSFETs and IGBTs

Protection of Power Devices -8

- Supply side switching transients occur when power supply to the transformer feeding the power converter is switched off thereby abruptly interrupting the flow of magnetizing current which causes the $L_m di_m/dt$ voltage spike. Similarly, load transients can occur when an inductive load is disconnected from the converter output.

  Both these transients can be reduced by connecting an unpolarized R-C snubber across the primary or secondary winding of the supply transformer.

  In addition back-to-back selenium diodes, MOVs (metal oxide varistors) and gas arrestors can be connected across the input to absorb voltage transients.

Protection of Power Devices -9

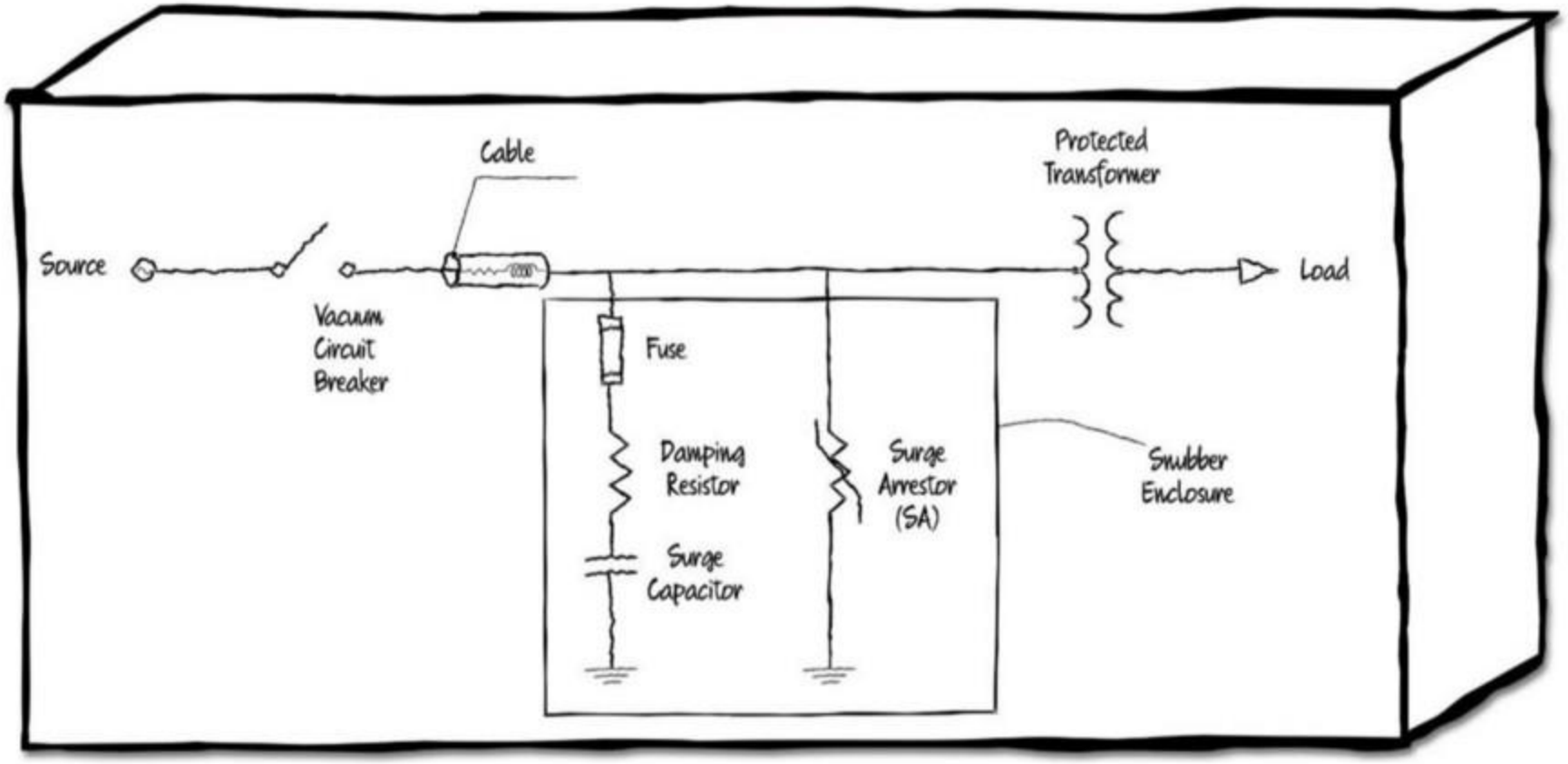


FIGURE 1.29

Protection of Power Devices -10

- Current protection can be divided into:
  a) Over load protection
  b) Short circuit protection

- Over load protection is normally provided by slow acting fuses ("slo blo") and or MCBs (miniature circuit breakers) or MCCBs (moulded case circuit breakers).

- Short circuit protection for devices such as diodes, SCRs, triacs, GTOs, which have a relatively higher overcurrent capability, is provided by fast acting semiconductor fuses. These fuses must satisfy the following requirements:

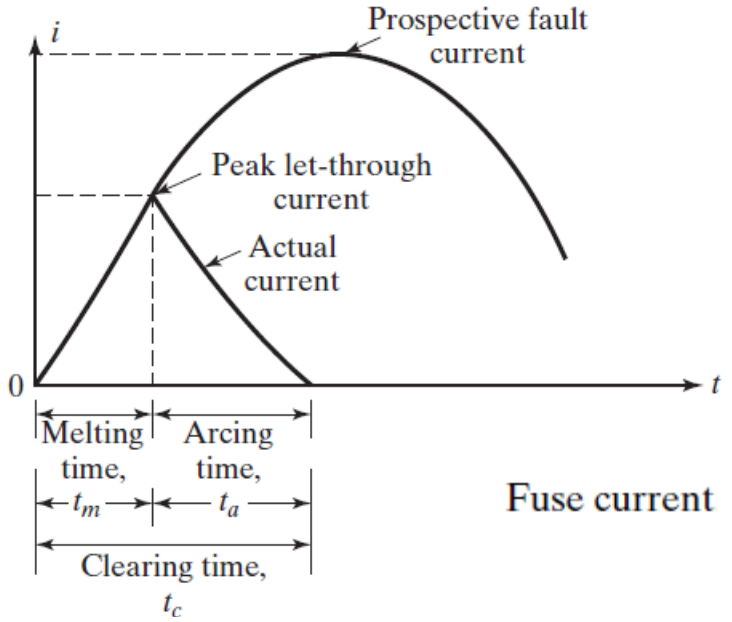
  a) the fuse should be able to continuously carry the device rated current without blowing off

  b) the i^2t let-through value of the fuse before the short circuit is cleared should be less than the rated i^2t value of power semiconductor device being protected

  c) the fuse must be able to withstand the restriking voltage which appears after the arc is extinguished

  d) the peak arc restriking voltage should be less than the voltage rating of the device

Protection of Power Devices -11



Fuse current

FIGURE 1.30

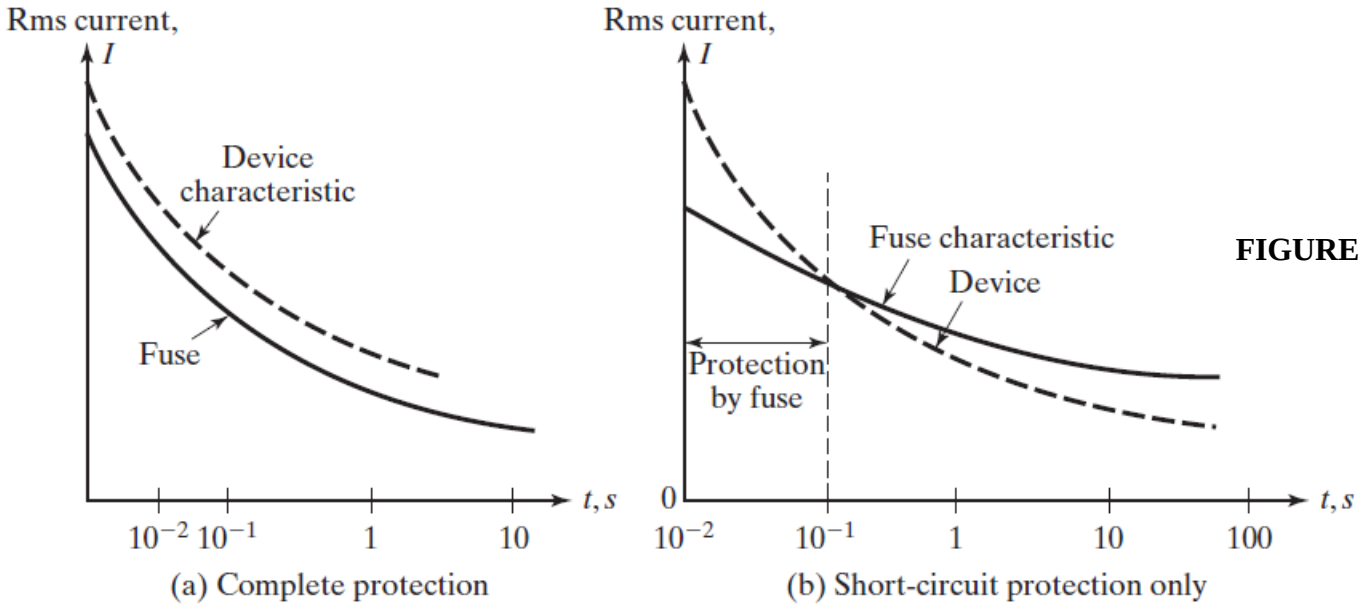


FIGURE 1.31

Current–time characteristics of device and fuse

Protection of Power Devices -12

- Short circuit protection for devices such as Power MOSFETs and IGBTs, which have relatively low overcurrent withstand capability cannot be provided by fast semiconductor fuses as they are not fast enough.
- Here protection is provided by sensing the drain-source or collector-emitter voltage. Under normal conditions, when the device operating point is in the ON or ohmic region, this voltage is very small. However, under short circuit conditions, the drain or collector current suddenly increases forcing the operating point to move into the active or saturation region. In the active region, the drain-source or collector-emitter voltage is quite large and this increased voltage is sensed and used to cut-off the gate-source or gate-emitter voltage which then reduces the drain or collector current to a safe value.
- Another way of providing very fast acting protection to Power MOSFETs and IGBT is by the use of a crowbar circuit which consists of a SCR connected across the power device to be protected. Here, as soon as the short circuit current is sensed, the SCR is fired which shorts the power device and diverts the short circuit current into itself. Effectively, this short circuits the input supply thereby blowing the protection fuse connected in series and opens the supply circuit.

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