T. Y. B. Tech (Electrical and Computer Engineering)

Trimester: V **Subject: Microcontroller and Applications**
Name: Shreerang Mhatre **Class: TY**

Roll No: 52 **Batch: 3**

Experiment No: 06

Name of the Experiment: Programming of on chip ADC

Performed on: 21/11/2023

Submitted on: 24/11/2023

Marks	Teacher's Signature with date

Aim: Write C program for programming of on chip ADC of C8051F340.

Apparatus: EPBF340 Board, ASK25 board, Connectors

Theory:

Analog to digital converter is among the most widely used device for data acquisition. It is used to convert the analog signals to digital numbers so that microcontroller can read and process them.

On-chip ADC Features:

- 10-Bit ADC
- Up to 200 ksps
- Built-in analog multiplexer with single-ended and differential mode
- V_{REF} from external pin, internal reference, or VDD

Interfacing Diagram:

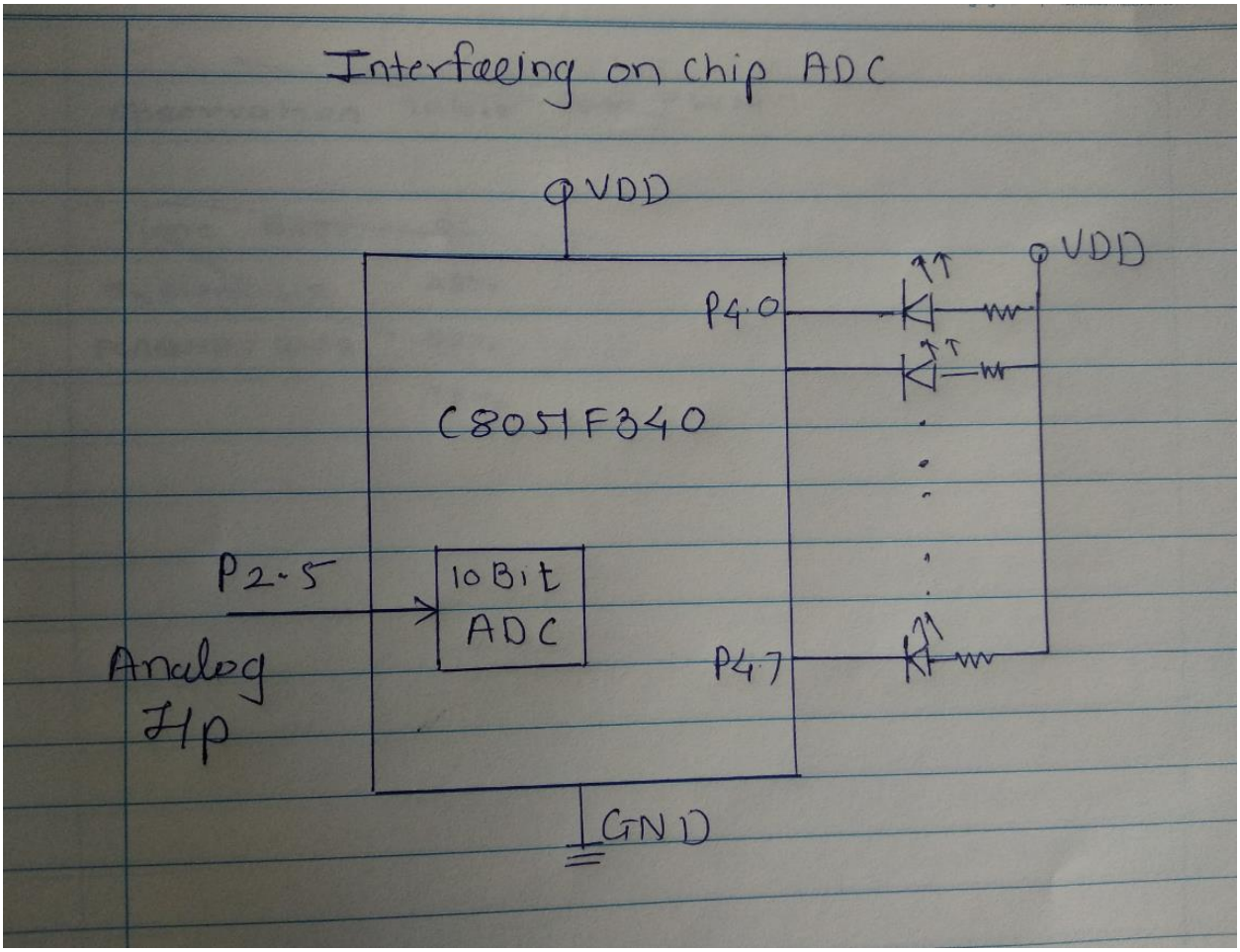


Figure 5.1 Interfacing Diagram for onchip ADC programming

Algorithm:

Hardware Connections: Connect single lead wire between P2.5 (Pin15 of PL3 connector) of EPBF340 board and Pin1 of PL10 connector of ASK25. To provide the ground also connect 20pin flat cable between PL6 connector of EBF340 board and PL8 connector of ASK25.

Connect USB cable between PL8 connector of EPBF340 board and PC.

F340 Reference	Device ASK25
P2.5 (Pin15 of PL3 connector)	Pin 1 of PL10 connector (Pot RV2)
PL6	PL8

Program: Attach the tested code.

Calculations:

Dout= (Vin/Vref)*1023

Table 1

Vin(Given)	Dout (Decimal)	Dout (Hex)	Dout (Binary)
3.3 V	**1023**	**3FF**	**1111111111**
1V			
2.3V			
2V			
1.3 V			

Table 2

Dout (Binary)	Dout (Hex)	Dout (Decimal)	Vin (Calculated)
0011101101			
1110001100			
0101100110			
1100011100			
1010011011			
1111111111			

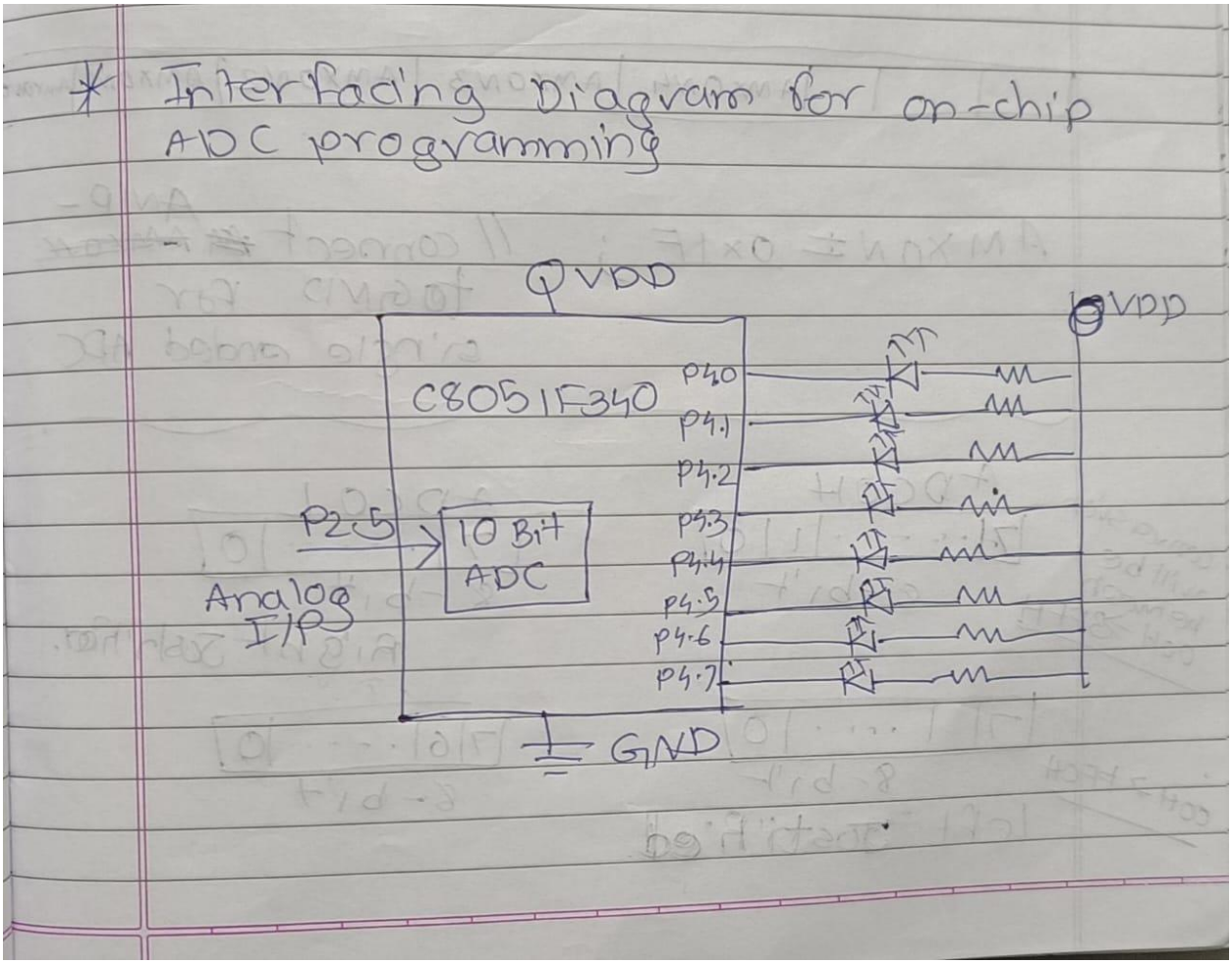
Conclusion:

Study Question:

1. Give the main factor affecting the step size of ADC in C8051F340.

2. Give the formats for control registers associated with C8051F340 ADC.

Interfacing Diagram:



Code For ADC:

```
// Exp - 5 ADC Interfacing with C8051F340
/*
Name: Shreerang Mhatre
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*/

#include "C8051F340.h"
#define SYSClk 12000000
sbit Buzzer= P3^3;
void delay(unsigned int Ms);
void main()
{
    XBR1= 0X40;
    P4MDOUT= 0XFF;
    www.mitwpu.edu.in
    Buzzer= 0;
    P2SKIP= 0X20;
    P2MDIN= 0XD0;
    AMX0P= 0X04;
    AMX0N= 0x1F;
    ADC0CF= (((SYSClk/3000000)-1)<<3);
    REF0CN= 0x08;
    ADC0CN= 0x80;
    AD0EN= 1;
    {
        ADC0CN =0x90;
        while (AD0BUSY == 1);
        delay(50);
        P4= ~ ADC0L;
        delay(50);
        P4= ~ ADC0H;
        delay(50);
    }
while(1);
}
void delay(unsigned int Ms)
{
```
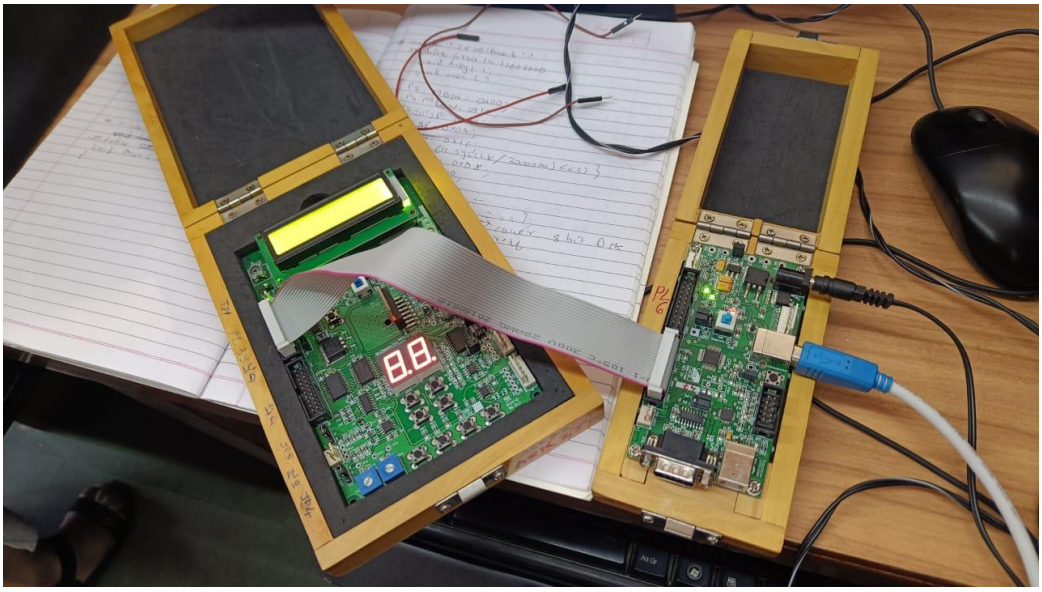
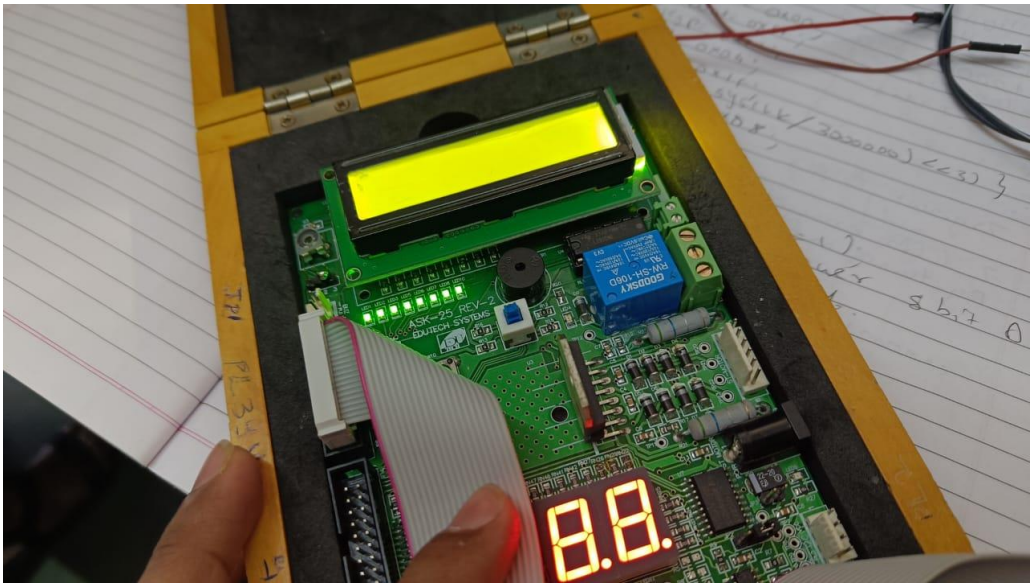

```
    unsigned int n;
    unsigned int i;
    for (n-0; n<Ms; n++)
    {
        for (i=0; i<65; i++);
        www.mitwpu.edu.in
    }
}
```

Demonstration Of ADC:





Exp 5 ADC

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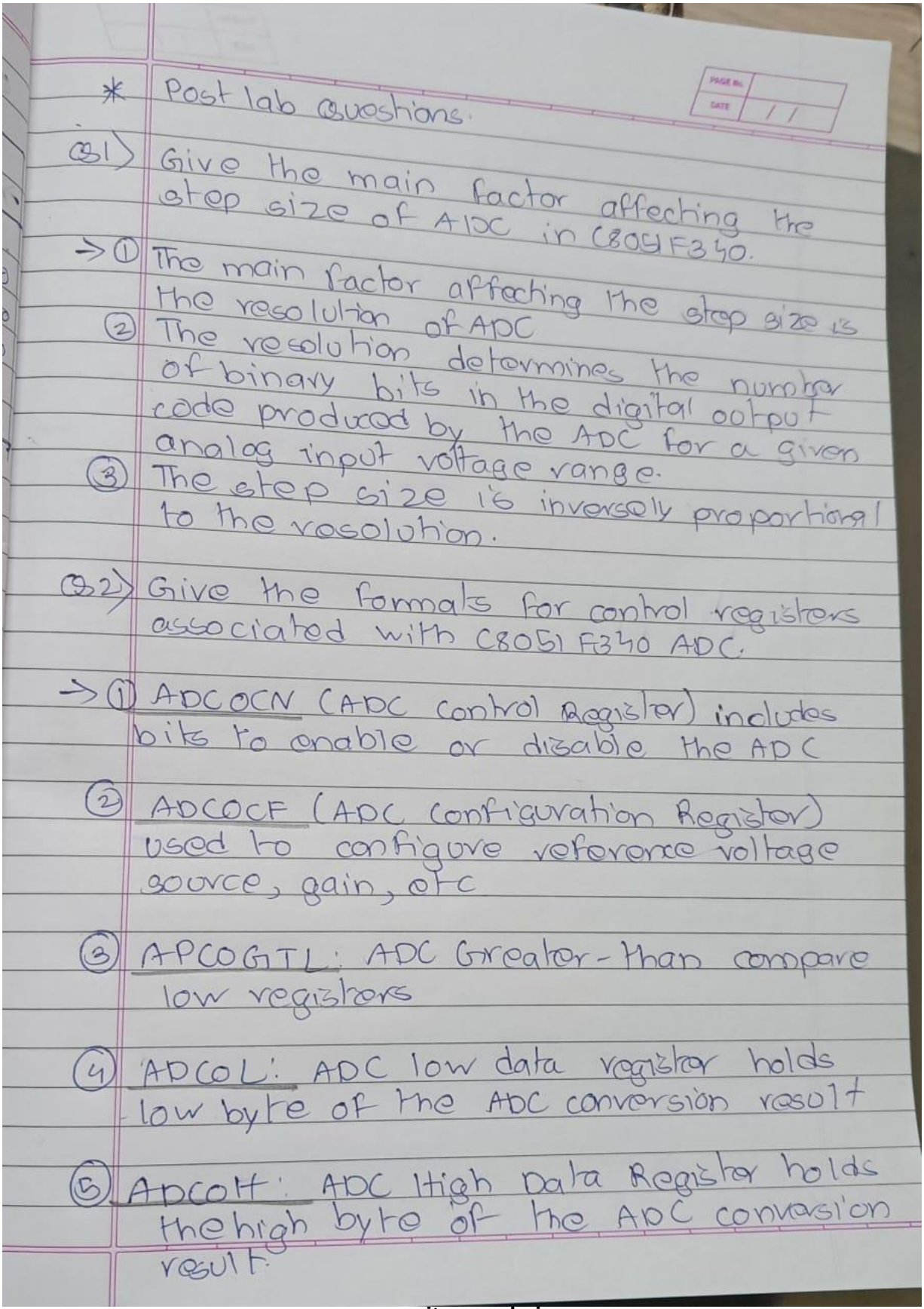
* observation table.

Dout Binary	Decimal	Vin (app)	Vin (calc)	% error
0110010110	406	1.24	1.30	4.83%
1000111010	570	1.75	1.83	4.57%
1010010100	660	2.08	2.12	1.92%
1100100110	806	2.53	2.6	2.76%
1110111111	959	3.03	3.09	1.98%

$$Dout = \frac{Vin}{Vref} \times 1023$$

$$Vin(calc) = \frac{Dout \times Vref}{1023}$$

$$= \frac{406 \times 3.3}{1023}$$



* Post lab questions.

Q1) Give the main factor affecting the step size of ADC in C8051F340.

→ ① The main factor affecting the step size is the resolution of ADC
② The resolution determines the number of binary bits in the digital output code produced by the ADC for a given analog input voltage range.
③ The step size is inversely proportional to the resolution.

Q2) Give the formats for control registers associated with C8051 F340 ADC.

→ ① ADC0CN (ADC control Register) includes bits to enable or disable the ADC

② ADC0CF (ADC configuration Register) used to configure reference voltage source, gain, etc

③ ADC0GTL: ADC Greater-than compare low registers

④ ADC0L: ADC low data register holds low byte of the ADC conversion result

⑤ ADC0H: ADC High Data Register holds the high byte of the ADC conversion result.