

# Unit 1

## Performance Parameters of Op Amp

# Lesson Plan

Topic	Sub points	Book-Page Nos.
Technology Based classification of Op Amp	BJT, JFET, CMOS	TI PPT
OpAmp Parameters(DC)	Difference between ideal and practical Op Amp and its equivalent circuit. <sup>13</sup> different DC Parameters	T <sub>1</sub> -109 T <sub>2</sub> -98 to 100
Effect of Temperature supply voltage and time on Parameters	Thermal Drift and Error voltage	T <sub>1</sub> -133
Op-amp Parameters(AC)	Frequency Response , Band width and slew Rate	T <sub>1</sub> -163, T <sub>2</sub> -120
Frequency Response of Op Amp	Compensated and Non compensated Op Amps. Closed loop and Open loop frequency response. Difference between bandwidth, transient Response and Slew Rate	T <sub>1</sub> -161
<sup>12/21/2022</sup> Stability and Offset Nulling Techniques		T <sub>1</sub> -111to122

# Op Amp Classification

- Classification of Op-Amp



**Based on Function:**    **Based on manufacturing Technology**

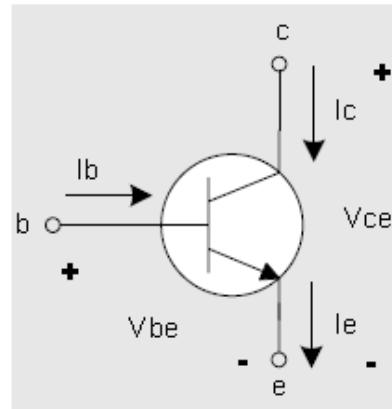
- 1. General Purpose
- 2. Low input Current
- 3. Low Noise
- 4. Low Power
- 5. Low Drift
- 6. Wide Bandwidth
- 7. Single DC Supply
- 8. High Voltage
- 9. Multiple Devices

# Classification of Op Amp based on application

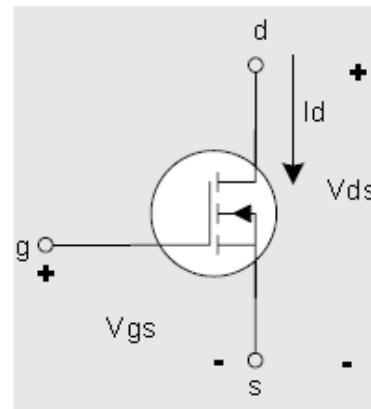
	Opamp Type	Description	Example
1	General Purpose	Internally Compensated and default choice for an application	741
2	Low input Current	Quiescent current needed is low. Typically uses MOSFET, JFET, Super Beta darlington transistors at input stage	LTC 2064
3	Low Noise	Optimized to reduce internally generated noise	AD 795, OP27
4	Low Power	Uses internal Circuitry to reduce power consumption	TLV 8541
5	Low Drift	Devices are internally compensated to minimize drift due to temperature	ADA 4522
6	Wide Bandwidth	Also called video Opamps and have very high gain bandwidth level	LF 351
7	Single DC Supply	Designed to operate from single DC power supply	LM 158/258
8	High Voltage	The power supply for these devices can be as high as 44V.	LM 143
9	Multiple Devices	Two or Quad Arrangement in one IC	LM 324, LM148

Depending on type of differential Amplifier at the input block of Op Amp there are three types of OpAmp

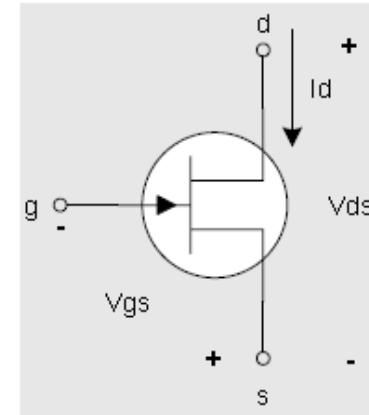
## Bipolar, CMOS, JFET (Op Amp input device structures)



NPN **Bipolar**



N-Channel **CMOS**



N-Channel **JFET**

- 1) Current Controlled Device
- 2) "Current Controlled Current Source"
- 3)  $I_c = I_b \cdot h_{fe}$
- 4)  $I_b = 0A$  turns bipolar off
- 5) Base is op amp +/- input
- 6) Highest Op Amp input current

- 1) Voltage Controlled Device
- 2) "Voltage Controlled Resistor"
- 3)  $V_{gs} > 2V$  controls  $R_{ds\_on}$
- 4)  $V_{gs}=0V$  turns MOSFET off
- 5) Gate is op amp +/- input
- 6) Very Low Op Amp input current

- 1) Voltage Controlled Device
- 2) "Voltage Controlled Resistor"
- 3)  $0V < V_{gs} < -2V$  controls  $R_{ds\_on}$
- 4)  $V_{gs} < -2V$  turns JFET off
- 5) Gate is op amp +/- input
- 6) Very Low Op Amp input current

# Classification of Op Amp based on technology

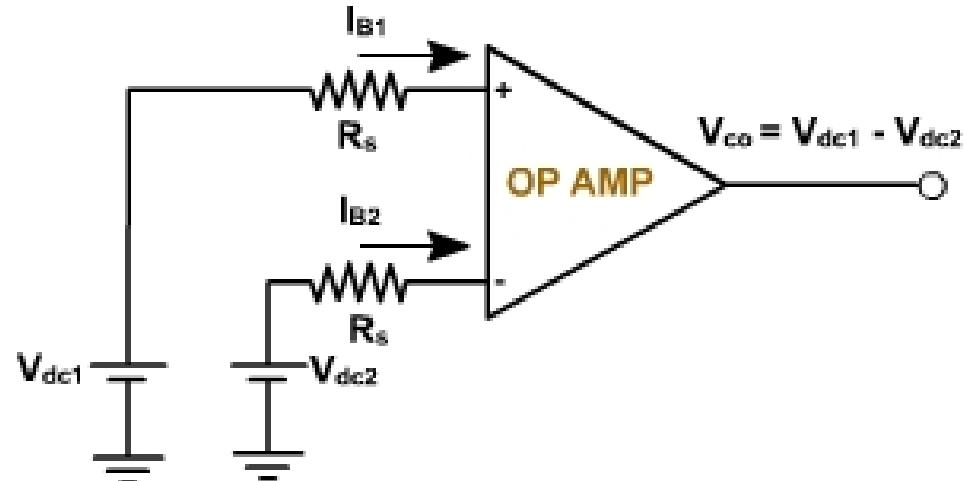
Sr. No	Parameter	Bipolar Op Amp	JFET Op Amp	CMOS Op Amp
1.	Differential Input Stage	Uses BJT	Uses JFET	Uses MOSFET
2.	Offset Voltage $V_{os}$	Smaller than JFET and CMOS	Larger than Bipolar	Larger than Bipolar
3.	$V_{os}$ Drift	Linear	Larger than Bipolar	Larger than Bipolar
4.	$I_b$	Much Larger 100 nA	Low 1pA	Low 1pA
5.	$I_b$ Drift	Small	Doubles every 10 degrees Celsius	Doubles every 10 degrees Celsius
6	Broad Band Noise	Smaller and decreases with $I_c$	Slightly higher than bipolar	Larger than bipolar decreases to square root of $ID$
7	Rail to Rail input	Not Common Difficult	yes	yes
8	Rail to Rail Output	Close to rail 200 mV	Same as Bipolar	Very close to rail 10 mV

# Classification of Op Amp based on technology Continued...

Sr. No	Parameter/Characteristic	Bipolar Op Amp	JFET Op Amp	CMOS Op Amp
9	Output Vs Load	Relatively flat until you reach current limit	Same as Bipolar	Falls off Quickly
10	Bandwidth	Increases linearly with Collector Current	Same as Bipolar	Increases by increasing W/L ratio or $\sqrt{I_D}$
11	Zo	Flatest and Lowest Zo	low	Higher and not Flat as bipolar
12	Advantage	Large output Swings	Extremely low bias currents	Requires very small power supply currents
13	Example	OPA 227	LF 357	OPA 350

# 1. Input Offset Voltage:

**Input offset voltage of Op-Amp  $V_{io}$  is the Differential input voltage that exists between Two input terminals of OpAmp with out any External inputs applied.**



Input offset voltage is also defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output .fig shows that two dc voltages are applied to input terminals to make the output zero.

$$V_{io} = V_{dc1} - V_{dc2}$$

$V_{dc1}$  and  $V_{dc2}$  are dc voltages and  $R_s$  represents the source resistance.  $V_{io}$  is the difference of  $V_{dc1}$  and  $V_{dc2}$ .

It may be positive or negative. For a 741C OPAMP the maximum value of  $V_{io}$  is 6mV. It means a voltage  $\pm 6$  mV is required to one of the input to reduce the output offset voltage to zero. The smaller the input offset voltage the better the differential amplifier, because its transistors are more closely matched.

## 2. Output Offset Voltage:

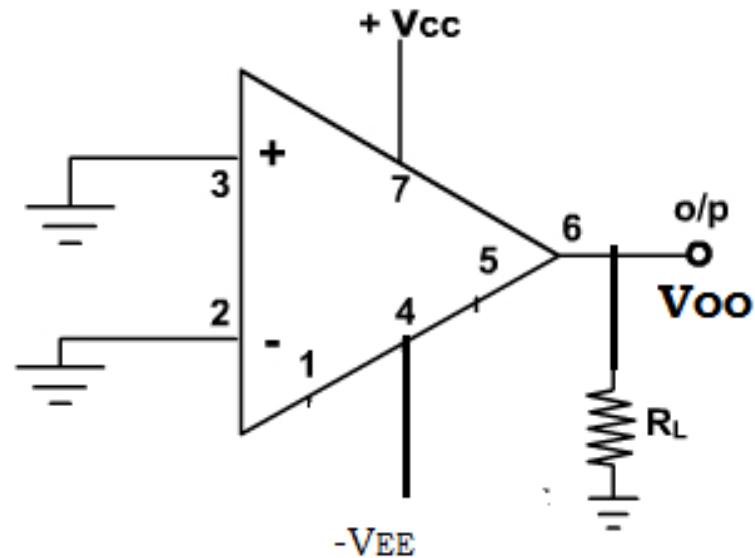
Due to input offset voltage  $V_{IO}$  output offset Voltage  $V_{OO}$  exists between output terminals of Opamp.

It is caused by mismatch between input terminals of opamp. The two transistors between input differential stage do not have exactly similar characteristics. Hence collector currents in two transistors are not same. Which causes differential output voltage from first stage.

The output of first stage is amplified by following stages And aggrevates more mismatch in them.

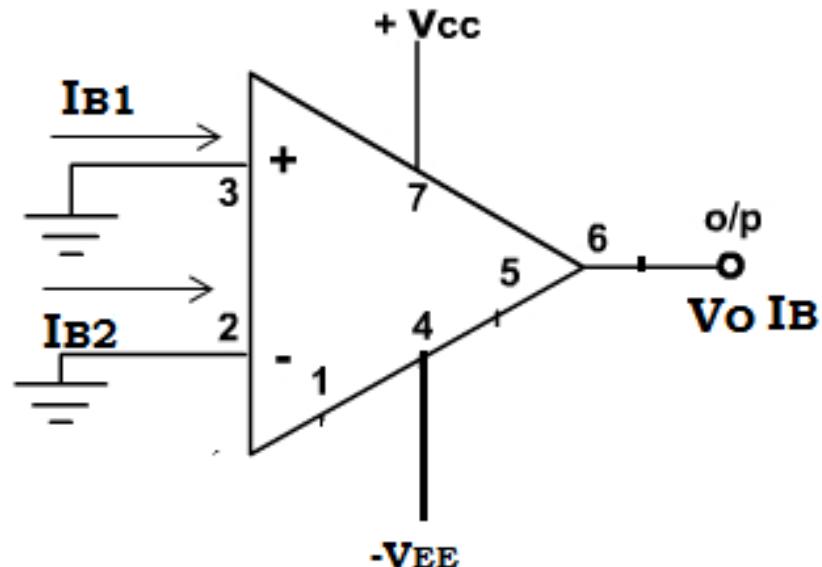
Hence output offset voltage  $V_{OO}$  is defined as output voltage caused by mismatching between two input terminals.

$V_{OO}$  is DC voltage and it may be positive or negative



### 3. Input Bias Current:

As shown in figure both input terminals are Grounded and no input is applied to opamp



The input bias current  $I_B$  is the average of the current entering the input terminals of a balanced amplifier i.e.

$$I_B = (I_{B1} + I_{B2}) / 2$$

**IB1:DC bias current entering into non-inverting input**

**IB2: DC bias current entering into inverting input**

For 741C  $I_{B(\max)} = 700 \text{ nA}$  and for precision 741C  $I_B = \pm 7 \text{ nA}$

## 4. Input offset Current:

The input offset current  $I_{io}$  is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier.

$$I_{io} = | I_{B1} - I_{B2} |$$

The  $I_{io}$  for the 741C is 200nA maximum. As the matching between two input terminals is improved, the difference between  $I_{B1}$  and  $I_{B2}$  becomes smaller, i.e. the  $I_{io}$  value decreases further. For a precision OPAMP 741C,  $I_{io}$  is 6 nA

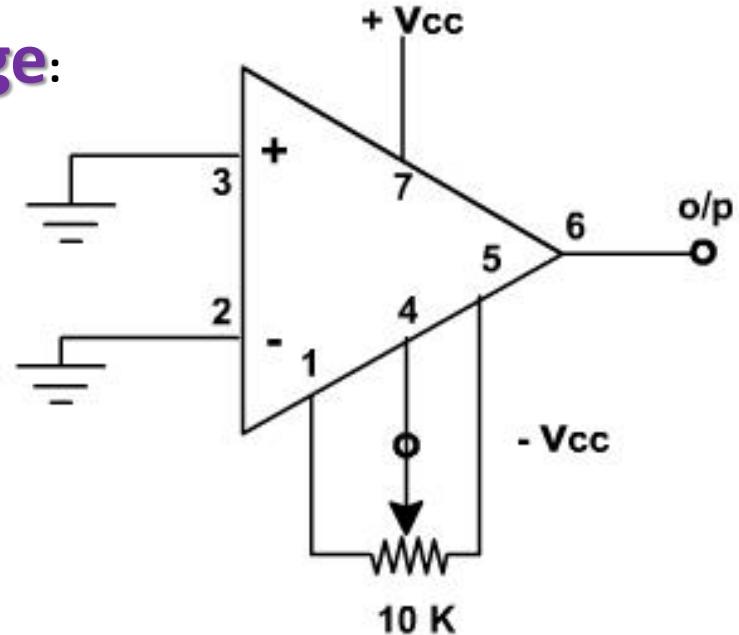
## 5. Differential Input Resistance: ( $R_i$ )

$R_i$  is the equivalent resistance that can be measured at either the inverting or non-inverting input terminal with the other terminal grounded. For the 741C the input resistance is relatively high  $2\text{ M}\Omega$ . For some OPAMP it may be up to  $1000\text{ G ohm}$ .

## 6. Input Capacitance: ( $C_i$ )

$C_i$  is the equivalent capacitance that can be measured at either the inverting and non-inverting terminal with the other terminal connected to ground. A typical value of  $C_i$  is  $1.4\text{ pf}$  for the 741C.

## 7. Offset Voltage Adjustment Range:



741 OPAMP have offset voltage null capability. Pins 1 and 5 are marked offset null for this purpose. It can be done by connecting 10 K ohm pot between 1 and 5 as shown in **figure**

By varying the potentiometer, output offset voltage (with inputs grounded) can be reduced to zero volts.

Thus the offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying 10 K pot.

For the 741C the offset voltage adjustment range is  $\pm 15$  mV.

## 8. Input Voltage Range

Input voltage range is the range of a common mode input signal for which a differential amplifier remains linear.

It is used to determine the degree of matching between the inverting and non-inverting input terminals. For the 741C,

the range of the input common mode voltage is  $\pm 13V$  maximum. This means that the common mode voltage applied at both input terminals can be as high as  $+13V$  or as low as  $-13V$ .

## 9. Common Mode Rejection Ratio (CMRR)..

CMRR is defined as the ratio of the differential voltage gain  $A_d$  to the common mode voltage gain  $A_{CM}$

$$CMRR = A_d / A_{CM}.$$

For the 741C, CMRR is 90 dB typically.

The higher the value of CMRR the better is the matching between two input terminals and the smaller is the output common mode voltage.

## 10. Supply voltage Rejection Ratio: (SVRR)/PSRR

Power Supply sensitivity is the ratio of the change in the input offset voltage to the corresponding change in power supply voltages. This is expressed in m V / V or in decibels, SVRR can be defined as

$$\text{Supply voltage Sensitivity} = \frac{\Delta V_{io}}{\Delta V}$$

Where  $\Delta V$  is the change in the input supply voltage and  $\Delta V_{io}$  is the corresponding change in the offset voltage.

**Reciprocal of power supply sensitivity is supply voltage rejection ratio (SVRR)**

For the 741C, SVRR = 150  $\mu$  V / V.

For 741C, SVRR is measured for both supply magnitudes increasing or decreasing simultaneously, with  $R_3 \leq 10K$ . For same OPAMPS, SVRR is separately specified as positive SVRR and negative SVRR.

## 11. Large Signal Voltage Gain

Since the OPAMP amplifies difference voltage between two input terminals, the voltage gain of the amplifier is defined as

$$\text{Voltage Gain} = \frac{\text{Output Voltage}}{\text{Differential Voltage}}$$

$$A = \frac{V_o}{V_{id}}$$

Because output signal amplitude is much large than the input signal the voltage gain is commonly called large signal voltage gain.

For 741C is voltage gain **is 200,000** typically.

## 12. Output voltage Swing:

The ac output compliance  $PP$  is the maximum unclipped peak to peak output voltage that an OPAMP can produce. Since the quiescent output is ideally zero, the ac output voltage can swing positive or negative. This also indicates the values of positive and negative saturation voltages of the OPAMP. The output voltage never exceeds these limits for a given supply voltages  $+V_{CC}$  and  $-V_{EE}$ . For a 741C it is  $\pm 13$  V.

## 13. Output Resistance: ( $R_o$ )

**$R_o$**  is the equivalent resistance that can be measured between the output terminal of the OPAMP and the ground. It is **75 ohm** for the 741C OPAMP.

## 14. Output Short circuit Current :

In some applications, an OPAMP may drive a load resistance that is approximately zero. Even its output impedance is 75 ohm but cannot supply large currents. Since OPAMP is low power device and so its output current is limited. The 741C can supply a maximum short circuit output current of only **25mA**.

## 15. Supply Current :

$I_s$  is the current drawn by the OPAMP from the supply. For the 741C OPAMP the supply current is **2.8 mA**.

## 16. Power Consumption:

Power consumption (PC) is the amount of quiescent power ( $v_{in} = 0V$ ) that must be consumed by the OPAMP in order to operate properly. The amount of power consumed by the 741C **is 85 m W**.

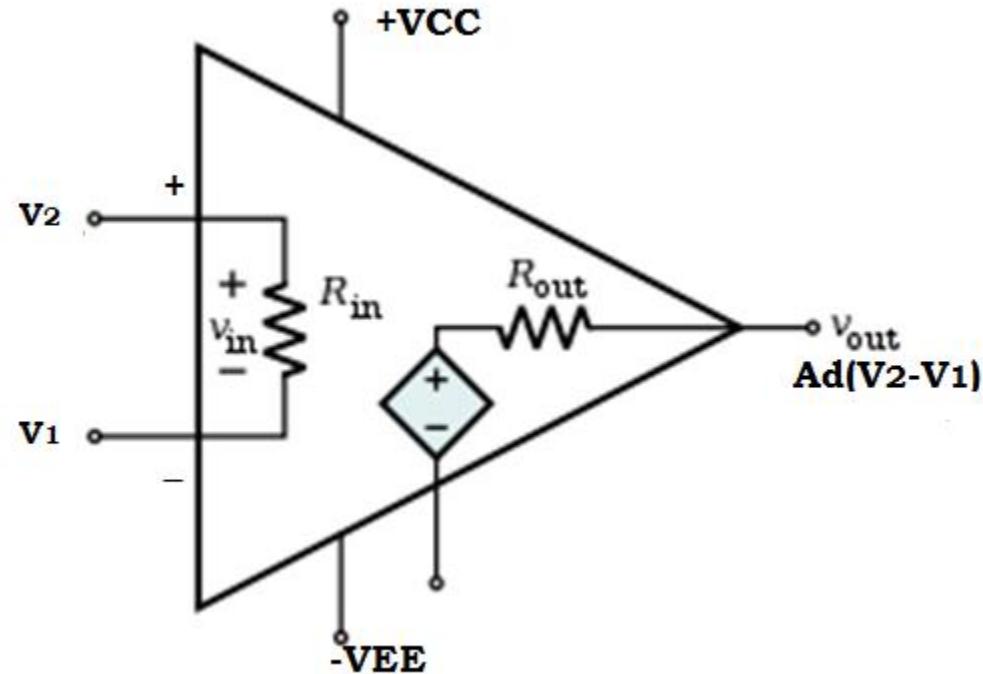
# Equivalent Circuit of Non Ideal Op Amp

The equivalent circuit model of an op amp is shown in Figure.

- The output section consists of a voltage-controlled source in series with the output
- input resistance  $R_i$  is the Thevenin equivalent resistance seen at the input terminals.
- the output resistance  $R_o$  is the Thevenin equivalent resistance seen at the output.
- The differential input voltage  $v_{id}$  is given by

$$V_{id} = V_2 - V_1$$

where  $V_1$  is the voltage between the inverting terminal and ground and  $V_2$  is the voltage between the non-inverting terminal and ground.



# Equivalent Circuit of Op Amp

The op amp senses the difference between the two inputs, multiplies it by the gain  $A$ , and causes the resulting voltage to appear at the output. Thus, the output  $v_o$  is given by

$$V_o = A_d(V_2 - V_1)$$

$A_d$  is called the open-loop voltage gain because it is the gain of the Op Amp without any external feedback from output to input. Table below gives typical range of OpAmp Parameters

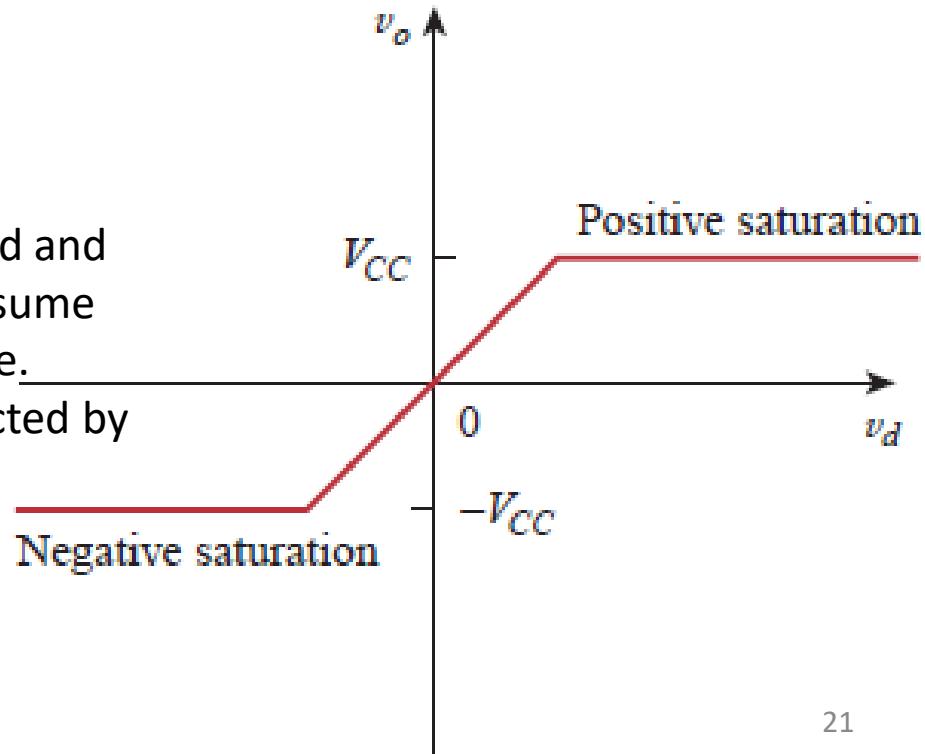
Parameter	Typical range	Ideal values
Open-loop gain, $A$	$10^5$ to $10^8$	$\infty$
Input resistance, $R_i$	$10^5$ to $10^{13} \Omega$	$\infty \Omega$
Output resistance, $R_o$	10 to 100 $\Omega$	$0 \Omega$
Supply voltage, $V_{CC}$	5 to 24 V	

# Ideal voltage Transfer Curve

A practical limitation of the op amp is that the magnitude of its output voltage cannot exceed  $|V_{CC}|$ . In other words, the output voltage is dependent on and is limited by the power supply voltage. Figure 1.4 illustrates that the opamp can operate in three modes, depending on the differential input voltage  $v_{id}$ :

1. Positive saturation,  $V_o = V_{CC}$ .
2. Linear region,  $-V_{CC} \leq V_o = A v_{id} \leq V_{CC}$ .
3. Negative saturation,  $V_o = -V_{EE}$ .

If we attempt to increase  $v_{id}$  beyond the linear range, the op amp becomes saturated and yields  $v_o = V_{CC}$  or  $v_o = -V_{CC}$ . Here, we will assume that our op amps operate in the linear mode. This means that the output voltage is restricted by  $-V_{CC} \leq V_o \leq V_{CC}$



# Numerical on DC PSRR/SVRR

1. For certain opamp PSRR is 70dB. What is numerical value of PSRR.
2. For 741 opamp supply voltage rejection ratio is  $150\mu\text{V/V}$ . Calculate change in opamps input offset voltage  $V_{io}$  if supply voltages are varied from  $\pm 10\text{V}$  to  $\pm 12\text{V}$ .
3. For certain opamp change in opamp's input offset voltage  $V_{io}$  caused by variation in supply voltage is  $60\mu\text{V}$ . Determine change in supply voltages. Assume that SVRR for opamp is 104dB.

# Numerical

1. For certain opamp , CMRR is 100dB, and differential gain is  $10^5$ , Find common mode gain of opamp.
2. An opamp has  $I_{B1}=400\text{nA}$ ,  $I_{B2}= 300\text{nA}$ . Determine bias current  $I_B$  and offset current  $I_{os}$ .

# AC Parameters of Op-Amp

Frequency Response , Band width and slew Rate

# Op-amp Frequency Response

## Frequency Response

- The gain of the op-amp is **complex number and a function of frequency**.
- At a given **frequency**, **gain  $A$  has a certain magnitude and a phase angle**.

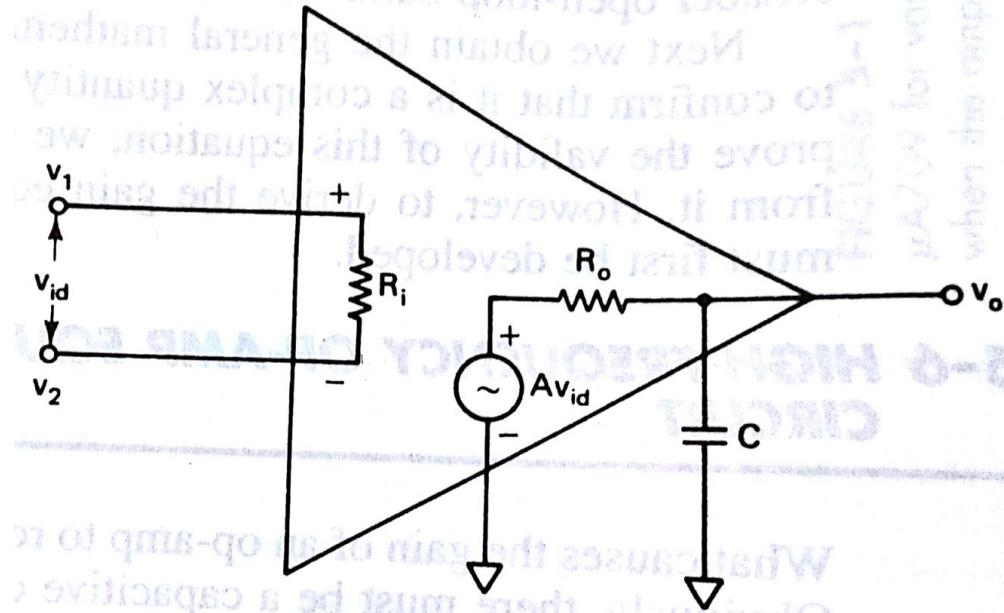
**Frequency response is defined as the manner in which, the gain of the op-amp responds to different frequencies.**

- Ideally, an op-amp has an infinite bandwidth
- However, the gain of a practical op-amp decreases or *roll-off* at higher frequencies, **due to the capacitive component**.

**The major sources responsible –**

- **junction capacitances**
- **parasitic capacitances**
- They act as open-circuits at low frequencies and reactive paths at higher frequencies.
- The combined effect reduces the gain of op-amp at high frequencies.

# High frequency model of opamp with single break frequency



1. The capacitive component in the equivalent circuit causes decrease in gain as frequency increases.
2. Two Major sources of capacitive effects are junction and parasitic capacitances and effectively shown as  $C$  .

## **Two major sources responsible for capacitor C in high frequency model**

- 1. Physical Characteristics of semiconductor devices:** As Op Amp is made up of BJTs and FETs the junction capacitances of these devices become dominant at high frequency.
- 2. Internal Construction of Op Amp:** All resistors transistors and some times capacitors are integrated on single substrate. Substrate acts as insulator and separates these components. The components are connected by conducting paths. These conducting paths separated by substrate act as capacitor.
- 3. Op Amp with single break frequency is represented by one capacitor in the model.**

# Compensating Networks

For Op Amps as the operating frequency increases ,two effects become evident.

- 1. The gain (magnitude ) of amplifier decreases**
- 2. The phase shift between the output and input increases.**

- The change in phase and magnitude is attributed to internally integrated capacitors as well as stray capacitances. These capacitances are due to physical characteristics of Semiconductor devices(BJTs and FETs)and the internal construction of the Op Amp
- The rate of change of gain as well as the phase shift of an Op Amp can be changed by using specific components.
- The most common components are Resistors and capacitors
- Network formed by such components and used for modifying gain and phase shift are called **compensating networks**

# Compensating Networks

Two common types of compensating networks are

1. Phase lead :Negative Phase Angle
2. Phase lag :Positive phase angle

First generation Op Amps used external compensating networks.

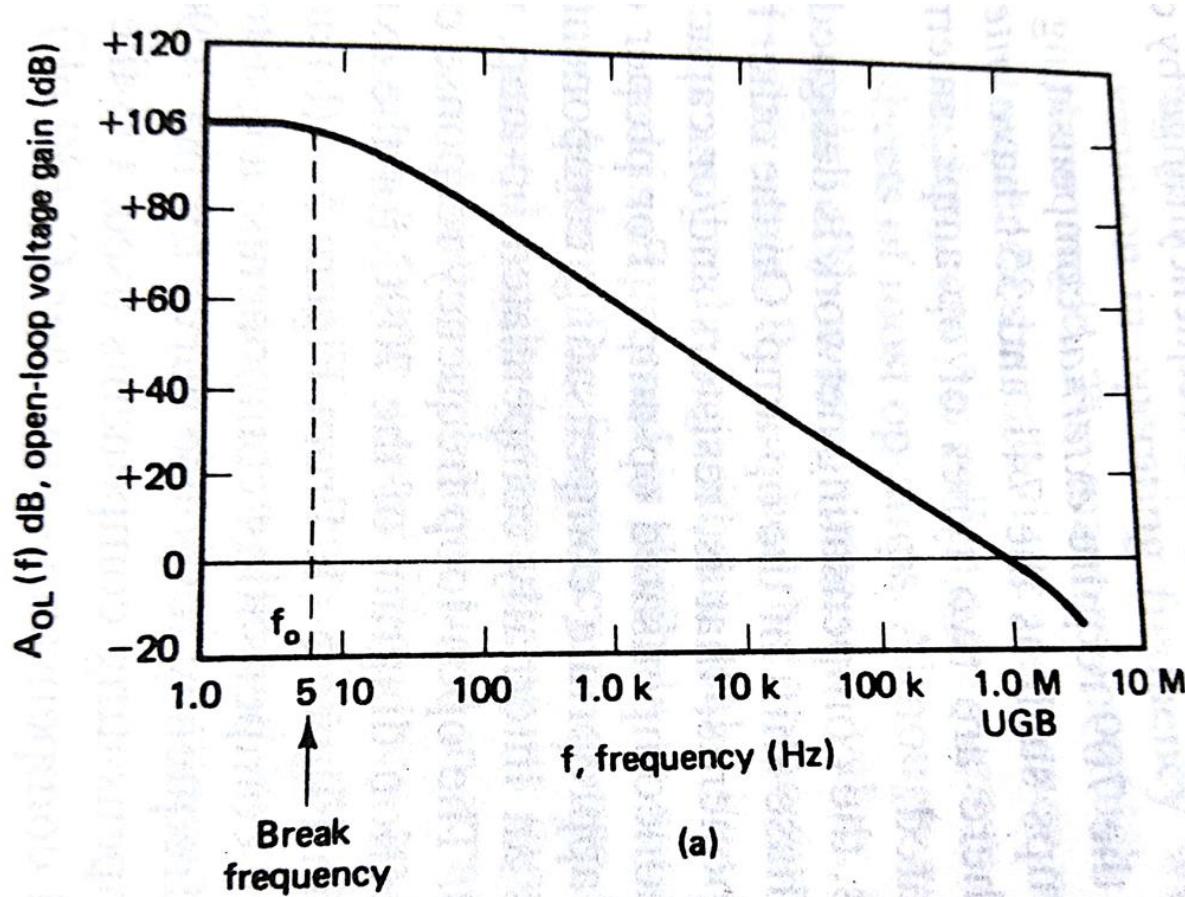
Later Generation of Op Amps use internal compensating network.

Therefore there are two types of Op Amps

1. **Internally Compensated (741)**
2. **Externally Compensated (709)**

# Frequency Response of internally compensated Op Amp(741)

Frequency Response of 741 C Internally compensated Op Amp has unity gain bandwidth of 1 MHz and single break frequency **fo before unity gain bandwidth**



- At break frequency The open loop gain Is down 3dB or 0.707 of its value at 0 Hz dc.
- Gain of opamp remains Constant till break frequency.
- The gain rolls off at the rate 20 db per decade after fo .
- For 741 C break frequency is 5 Hz

# Frequency Response of internally compensated Op Amp

- In 741 Op Amp 30 pf capacitor is internal compensating component.
- It controls open loop gain to allow it to roll off at a rate of 20 dB /decade.
- Internally compensated Op Amps have very small open loop bandwidth.
- They are simply called compensated Op Amps

# Open loop voltage gain as a function of frequency

$$\bullet \quad A_{OL}(f) = \frac{A}{1+j(\frac{f}{f_o})} \dots \dots \dots (3)$$

Where  $A_{OL}(f)$ = Open loop voltage gain as function of frequency

**A = Gain of Op Amp at 0 Hz.**

**f = Operating Frequency (Hz)**

$f_o$ = Break frequency of Op Amp.

The break frequency depends on value of  $C$  and output resistance  $R_o$

Equation (3) is important because it indicates that open-loop gain of Op Amp is complex quantity and is function of frequency.

## Open loop voltage gain of OPAMP as a function of frequency

- Being complex in nature the gain can be expressed in a polar form as follows
- The open loop gain magnitude is
- $A_{OL}(f) = \frac{A}{\sqrt{1 + (f/f_o)^2}} \dots\dots\dots(4)$
- And Phase angle  $\phi(f) = -\tan^{-1}(\frac{f}{f_o}) \dots\dots\dots(5)$
- Where f is used to indicate magnitude of gain and phase angle of gain are functions of frequency. Using equation (4)and(5) magnitude and phase Vs frequency plots can be obtained.

## Open loop voltage gain as a function of frequency

- $A_{OL}(f) = \frac{A}{\sqrt{1 + (f/f_o)^2}} \dots\dots\dots(4)$
- The same equation in dB can be expressed as

$$A_{OL}(f) \text{ dB} = 20 \log A - 20 \log \sqrt{1 + (f/f_o)^2} \dots\dots\dots(5)$$

If  $f_0=5 \text{ Hz}$ ,  $A=200,000$  for the 741 C.  
Substituting these values in equation 5

We get DC gain of 106 dB. ( $f=0\text{Hz}$ )

## Gain in decibel at different frequencies , including at $f_0$

At  $f = 0 \text{ Hz}$ ,

$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 20 \log \sqrt{1 + \left(\frac{0}{5}\right)^2} \cong 106$$

At  $f = 5 \text{ Hz} = f_o$ ,

$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 3.01 \cong 103$$

At  $f = 50 \text{ Hz}$ ,

$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 20.04 \cong 86$$

At  $f = 500 \text{ Hz}$ ,

$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 40 \cong 66$$

At  $f = 5 \text{ kHz}$ ,

$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 60 \cong 46$$

At  $f = 50 \text{ kHz}$ ,

$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 80 \cong 26$$

At  $f = 100 \text{ kHz}$ ,

$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 86.02 = 20$$

At  $f = 1 \text{ MHz}$ ,

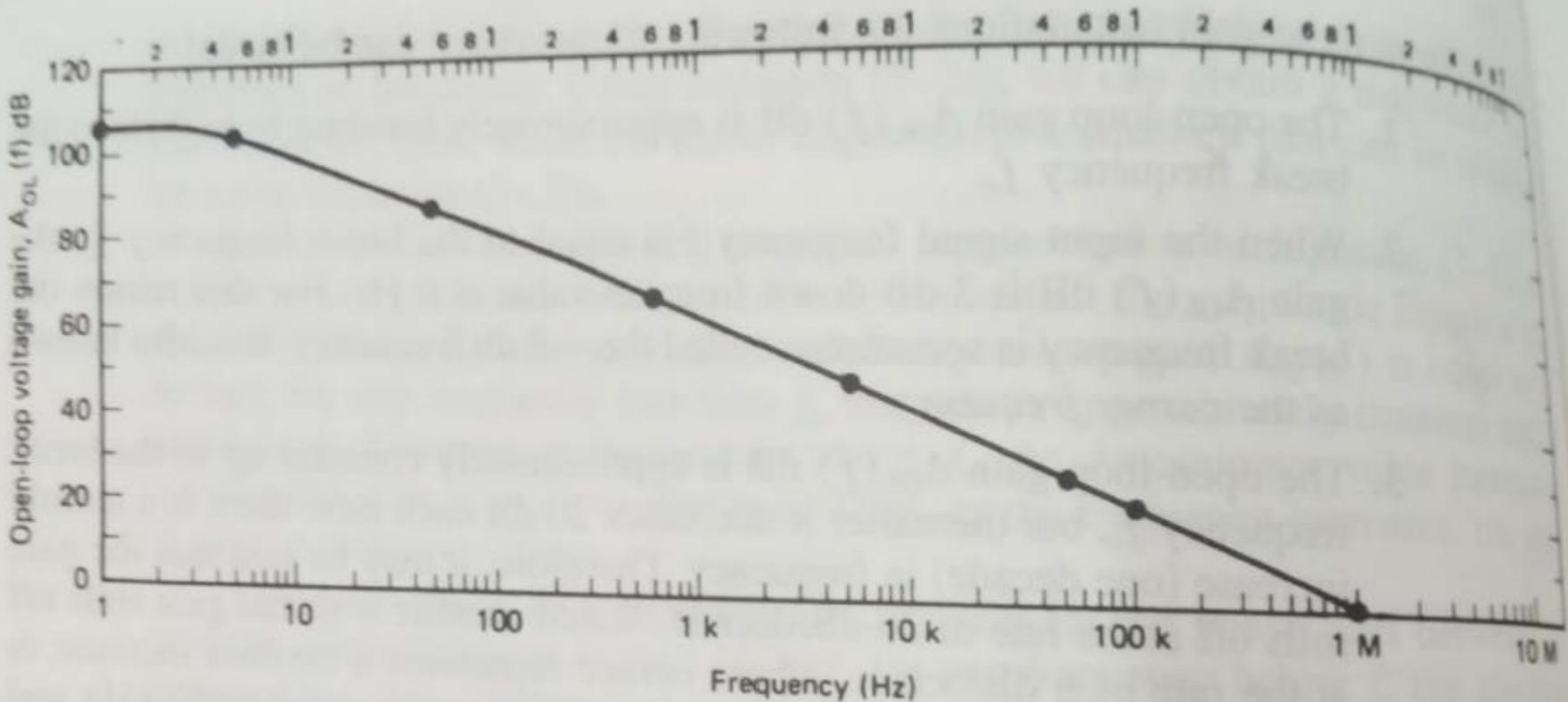
$$A_{\text{OL}}(f) \text{ dB} = 106.02 - 106.02 = 0$$

# Observations from gain Calculations

1. The open loop gain  $A_{OL}(f)$  in decibel is approximately constant from 0 Hz to break frequency .
  2. When the input signal frequency  $f$  is equal to break frequency  $A_{OL}(f)$  in decibel is 3 decibel down from its value at 0 Hz. For this reason it is sometimes called -3dB frequency. It is also known as corner frequency.
  3. The open loop gain  $A_{OL}(f)$  is approximately constant upto break frequency  $f_o$  , but there after it decreases 20 dB each time there is tenfold increase (one decade) in frequency. The gain rolls off at a rate of 20db / decade or gain rolls off at a rate of 6 dB/octave , where octave represents twofold increase in frequency.
  4. At some specific value of the input signal frequency , the open loop gain  $A_{OL}(f)$  dB is zero. This specific frequency is called unity gain bandwidth also called gain bandwidth product.
  5. UGB of 741 Op Amp is 1MHz. Unity gain bandwidth is provided as part of data sheet.
  6. The product of open loop gain A of opamp and the frequency of operation f provides the bandwidth.
- 7.  $BW = A \times f$**
8. Bandwidth is also determined from rise time specification by using the relation

$$BW = \frac{0.35}{t_r}$$

# Gain in decibels vs Frequency for 741 Op Amp



## Phase Angles at various frequencies for 741 Op Amp

$$\phi(f) = -\tan^{-1}\left(\frac{f}{5}\right)$$

At  $f = 0 \text{ Hz}$ ,  $\phi(f) = -\tan^{-1}\left(\frac{0}{5}\right) = 0^\circ$

At  $f = f_o = 5 \text{ Hz}$ ,  $\phi(f) = -\tan^{-1}\left(\frac{5}{5}\right) = -45^\circ$

At  $f = 50 \text{ Hz}$ ,  $\phi(f) = -84.29^\circ$

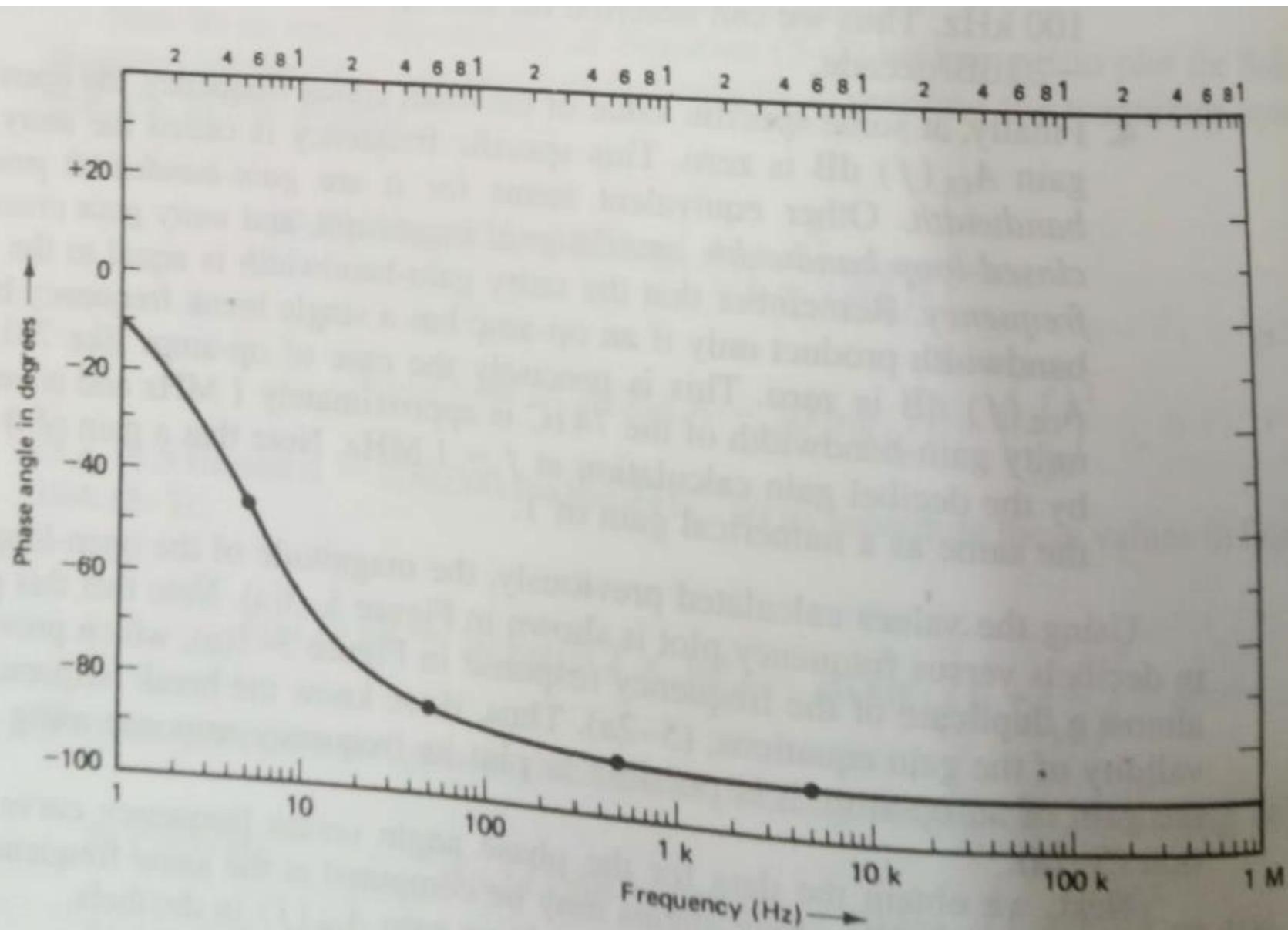
At  $f = 500 \text{ Hz}$ ,  $\phi(f) = -89.43^\circ$

At  $f = 5 \text{ kHz}$ ,  $\phi(f) = -89.94^\circ$

At  $f = 50 \text{ kHz}$ ,  $\phi(f) = -89.99^\circ$

At  $f = 100 \text{ kHz}$ ,  $\phi(f) = -90^\circ$

At  $f = 1 \text{ MHz}$ ,  $\phi(f) = -90^\circ$



## Observations from Phase Plot

1. Phase angle of Op Amp with single break frequency varies between  $0^\circ$  and  $-90^\circ$ . Phase shift between the input and output voltages is  $90^\circ$  that is output voltage lags input voltage by  $90^\circ$ .
2.  $f_o$  can be calculated as  $\frac{U_{GB}}{A}$

# Numerical

**Problem 1: An opamp has a rise time( $t_r$ ) of 0.7μs. Determine unity gain bandwidth.**

$$BW = \frac{0.35}{t_r}$$

Ans:500KHz

## Limitations of Op Amp Open loop configuration

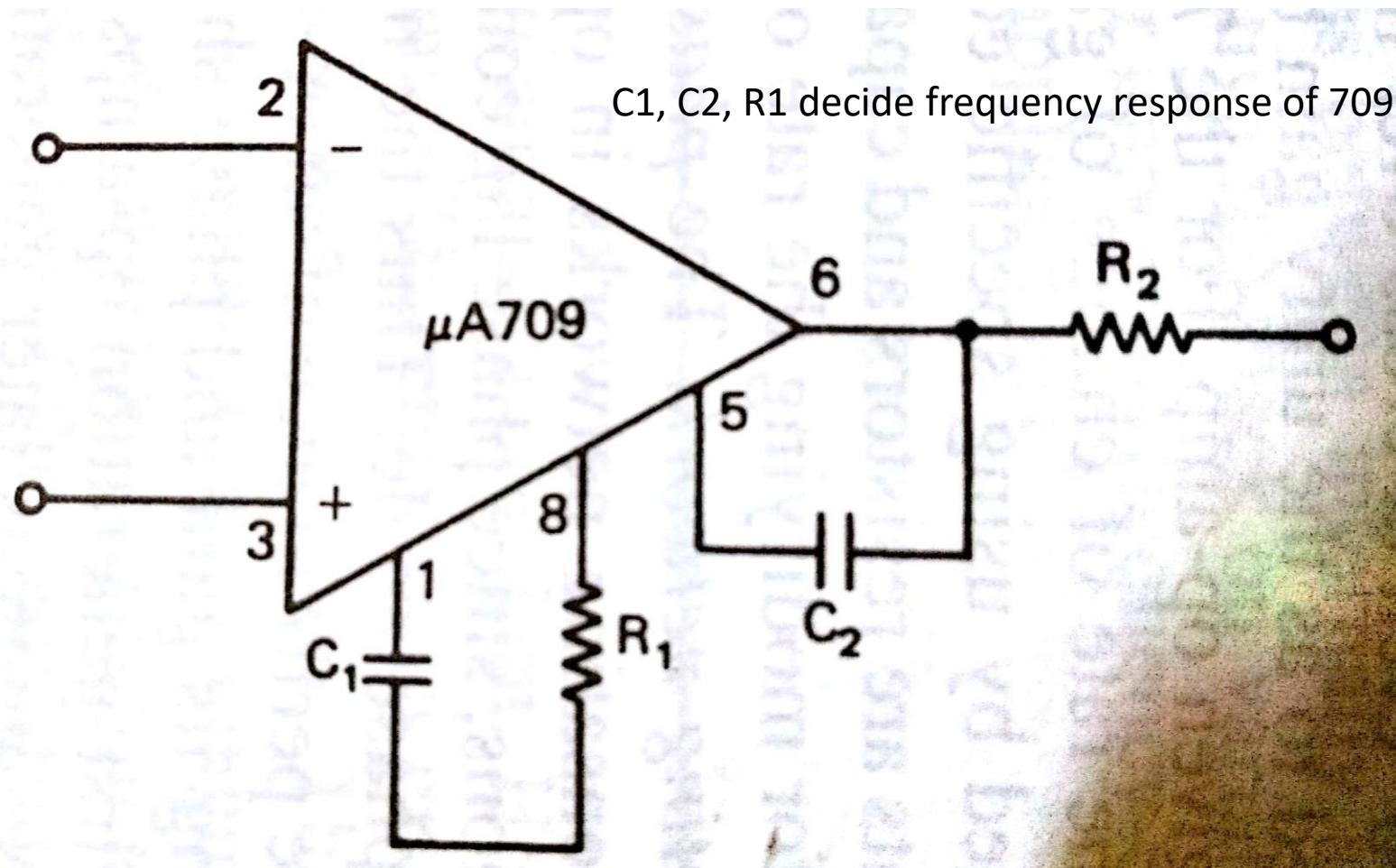
1. In open loop configurations due to high gain of Op Amp, clipping of output waveform can occur when output exceeds saturation level of Op Amp.
2. This feature actually makes it possible to amplify very low frequency signal of the order of microvolts or even less and amplification can be achieved accurately without any distortion. However , signals of such magnitudes are susceptible to noise and amplification from those applications is almost impossible to obtain in laboratory

## Limitations of Op Amp Open loop configuration

3. Open loop gain of Op Amp is not a constant and varies with temperature and variations in power supply.
4. The bandwidth of open loop Op amps is negligibly small. This makes open loop configuration of Op Amp unsuitable for AC applications open loop bandwidth of 741 is only 5 Hz but in almost all AC applications bandwidth requirement is very large.

# Frequency Response of Non-compensated Op Amps

- Op Amps requiring external compensating components are called non compensated Op Amps.
- Also called **tailored frequency response** Op Amp.



## Slew Rate

- Slew rate **limits the bandwidth** for large signals
- It is defined as **the maximum rate of change of output voltage realized by a step input voltage** - usually specified in units of  $V/\mu s$ .
- The slew rate of the op-amp is related to its **frequency response**. The op-amps with wide bandwidth have better slew rates.
- The general purpose op-amps have a maximum slew rate of  $0.5V/\mu s$
- The slew rate is usually specified **at unity gain and no-load**

## Cause of slew rate limiting

- The amplifier gain
- compensating capacitors
- the change in polarity of output voltage
- a function of temperature
- Generally reduces due to rise in temperature.

The rate at which the voltage across the capacitor  $V_c$  increases is given by  $\frac{dV_c}{dt} = \frac{I}{C}$  where I is the current furnished by the internal circuit

## Slew Rate

- **Slew Rate:** Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions and is expressed in volts /  $\mu$  secs.

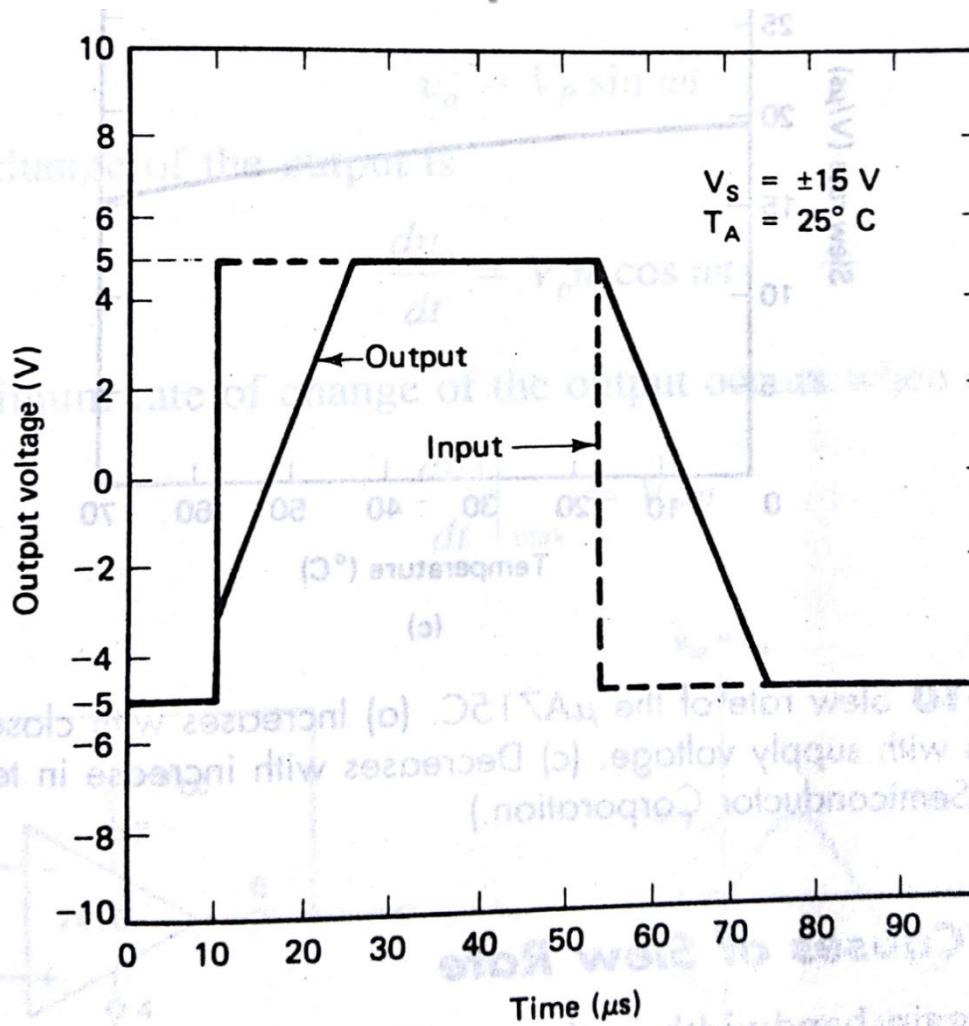
$$S.R = \frac{dV_o}{dt} \Big|_{\max} \quad V/\mu s$$

- Slew rate indicates how rapidly the output of an OPAMP can change in response to changes in the input frequency with input amplitude constant. The slew rate changes with change in voltage gain
- If the slope requirement is greater than the slew rate, then distortion occurs. For the 741C the slew rate is low 0.5 V /  $\mu$ s. which limits its use in higher frequency applications.

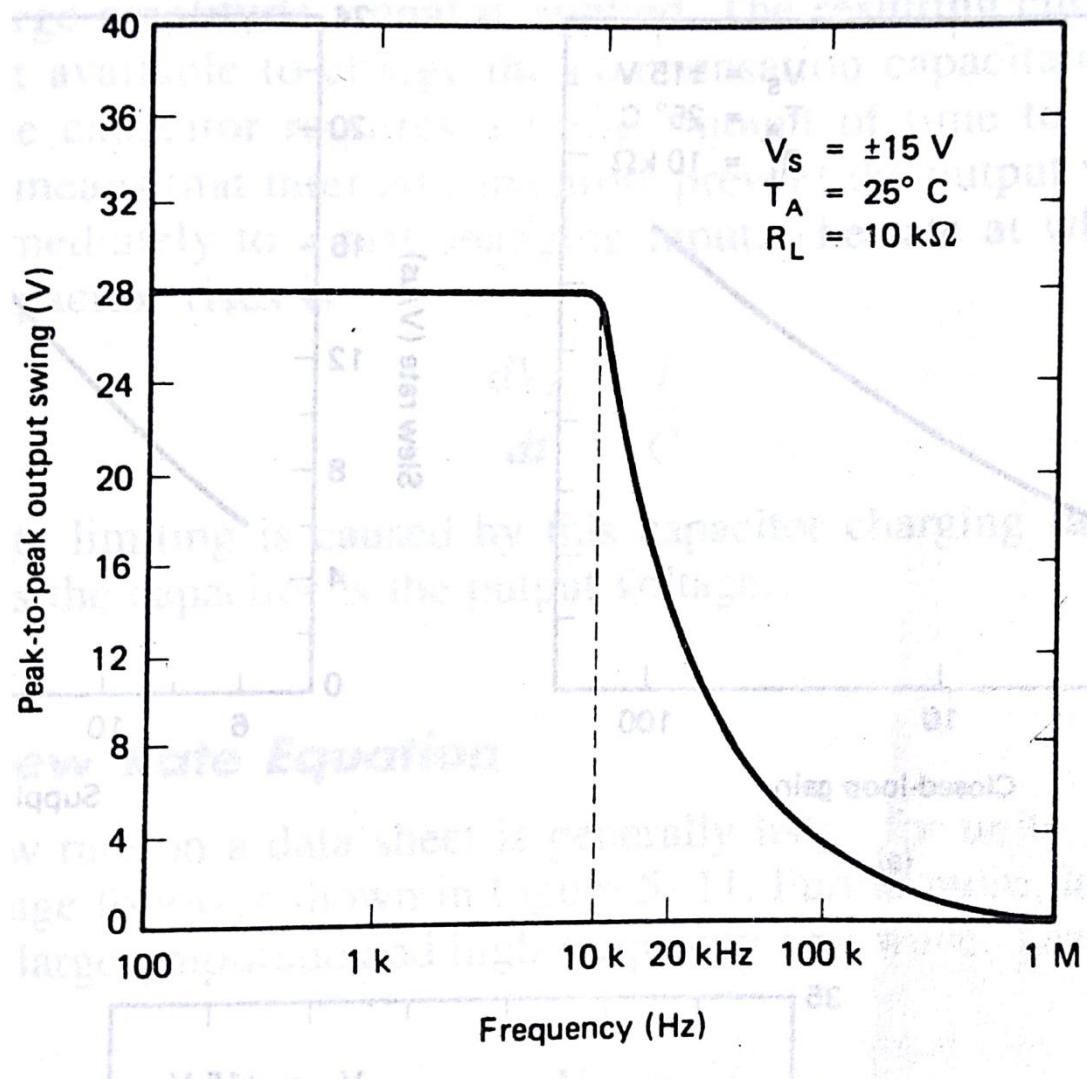
# Slew Rate

- Slew rate of Op Amp is related to its frequency response .
- The Op Amps with wide bandwidth have better slew rate.
- It is determined by number of factors such as amplifier gain , compensating capacitors and the change in polarity of output voltage.
- It is also function of temperature and reduces due to rise in temperature.

# Slew rate specified as Voltage follower large-signal Pulse Response

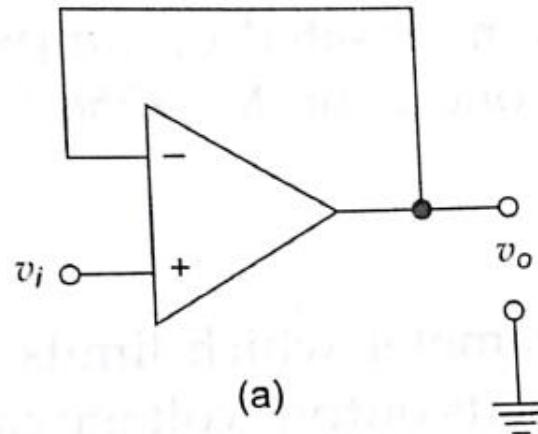


# Specifying Slew Rate indirectly

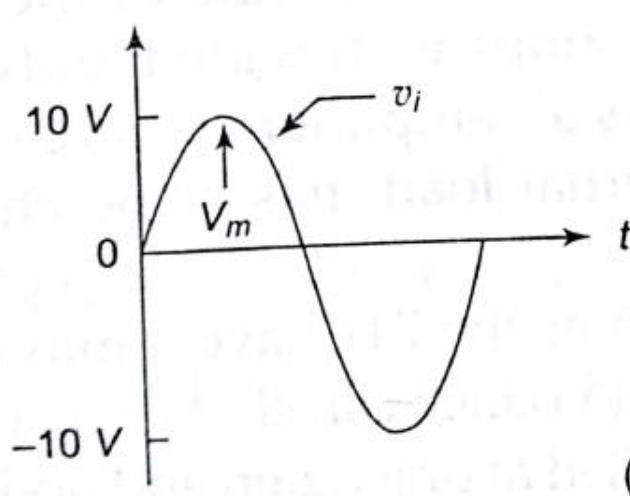


Specified as peak to peak output voltage swing as a function of frequency

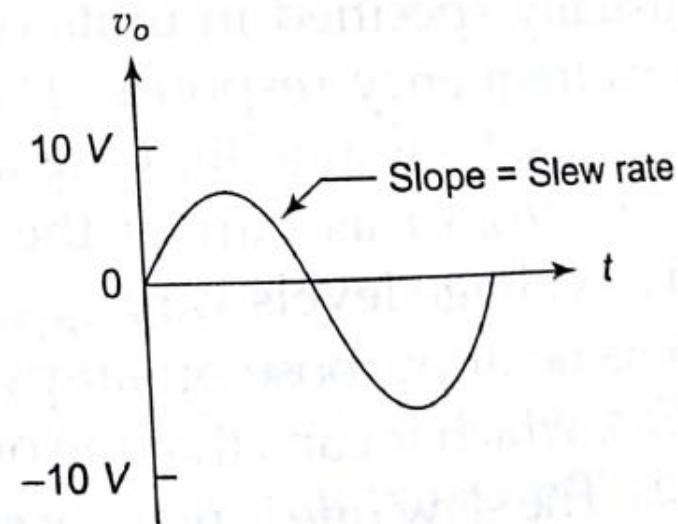
# Slew Rate limiting of Sine Wave



(a)



(b)



# Slew Rate limiting of Sine Wave

- Figure shows  $V_i$  as a large amplitude high frequency sine wave with peak amplitude of  $V_m$ .

$$V_i = V_m \sin \omega t \dots \dots \dots (1)$$

Therefore the output is given by

$$V_o = V_m \sin \omega t \dots \dots \dots (2)$$

The rate of change of output is given by

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t \dots \dots (3)$$

## Slew Rate limiting of Sine Wave

- The maximum rate of change of the output occurs when  $\cos \omega t = 1$ .

That is,  $\text{Slew Rate} = \frac{dV_O}{dt} |_{max} = V_m \omega \dots\dots(5)$

Or Slew Rate,  $SR = 2\pi f V_m$  V/S

The maximum frequency  $f_{max}$  at which an undistorted output voltage with a peak value  $V_m$  can be obtained is determined by

$$f_{max} = \frac{\text{Slew Rate}}{2\pi V_m} \dots\dots(6)$$

## Slew Rate limiting of Sine Wave

The maximum peak sinusoidal voltage that can be obtained at frequency  $f$  is given by

$$V_{m(max)} = \frac{\text{Slew Rate}}{2\pi f} \dots\dots\dots(7)$$

For 741 opamp slew rate is 0.5 V/  $\mu$ sec

# Slew Rate limiting of Sine Wave

**Problem 1:** Assuming slew rate for 741 is 0.5V/ $\mu$ sec , what is the maximum undistorted sine-wave that can be obtained for (a) 12V peak, and (b) 2V peak      **Ans :6.63KHz, 39.8KHz**

- $$f_{max} = \frac{Slew\ Rate}{2\pi V_m} = \frac{0.5V/\mu\text{sec}}{2\pi \times 12}$$

**Problem 2:** IC 741 is used as inverting amplifier with a gain of 100 dB, The voltage gain vs frequency characteristic is flat up to 10 KHz. Determine the maximum peak to peak input signal that can be applied without any distortion in the output.      **Ans:7.96V**

- $$V_{m(max)} = \frac{Slew\ Rate}{2\pi f}$$

# Comparison of AC Parameters of Opamp

Sr No	Bandwidth	Transient response (Rise Time tr)	Slew RATE
1	A small signal phenomenon	A small signal Phenomenon	A large signal phenomenon
2	Band of frequencies for which gain remains constant	That part of the total response before the response reaches steady state	The maximum time rate of change of output voltage
3	Depends on compensating components and closed loop gain	Composed of overshoot and rise time	Slew rate limiting depends on both frequency and amplitude often increases with closed loop gain and power supply voltages
4	If exceeded , results in reduction of output voltage	Affects settling time	If Exceeded results in distortion

# A list of parameters that must be considered for AC and DC Applications

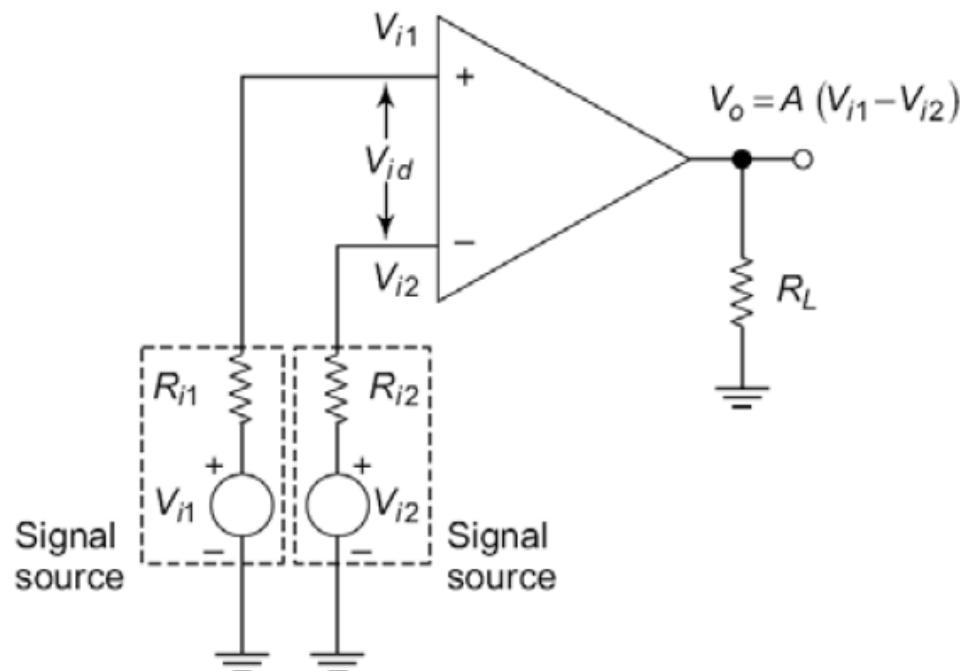
Sr. no.	For AC APPLICATIONS Consider	For DC Applications Consider
1.	Input Resistance	Input Resistance
2.	Output Resistance	Output Resistance
3.	Large Signal Voltage Gain	Large Signal Voltage Gain
4.	Output Voltage Swing	Output Voltage Swing
5.	Average Input Offset Voltage and current drifts	Input Offset Voltage and current drifts
6.	Long-Term input offset voltage stability	Long-Term input offset voltage stability
7.	Transient Response, Slew Rate , Equivalent input noise voltage and current	-

## **OPEN-LOOP OP-AMP CONFIGURATIONS**

- The term *open-loop* indicates that no feedback is fed to the input from output.
- The op-amp functions as a very high gain amplifier.
- There are three open-loop configurations of op-amp, namely,
  - i) **Differential amplifier**
  - ii) **Inverting amplifier and**
  - iii) **Noninverting amplifier**

# Open-loop Differential Amplifier

- The input voltages are represented by  $v_{i1}$  and  $v_{i2}$ .  $R_{i1}$  and  $R_{i2}$  are negligibly small
- $V_o = A(V_{i1} - V_{i2})$  where  $A$  is large-signal voltage gain.



## Determine the output voltage in each of following cases for open loop differential amplifier

a]  $V_{i1}=5 \mu V$  DC,  $V_{i2}=-7 \mu V$

b]  $V_{i1}=10mV$  RMS,  $V_{i2}=20mV$  RMS opamp is 741 with  $A=200000$ .

$$V_O = A \times V_{id} = A \times (V_1 - V_2)$$

A: Large signal voltage gain

$V_{id}$ :Difference input VoltageV

Using above equation DC output voltage :2.4V

AC output voltage considering both the signals of same frequency AC Output voltage is :-2000V RMS

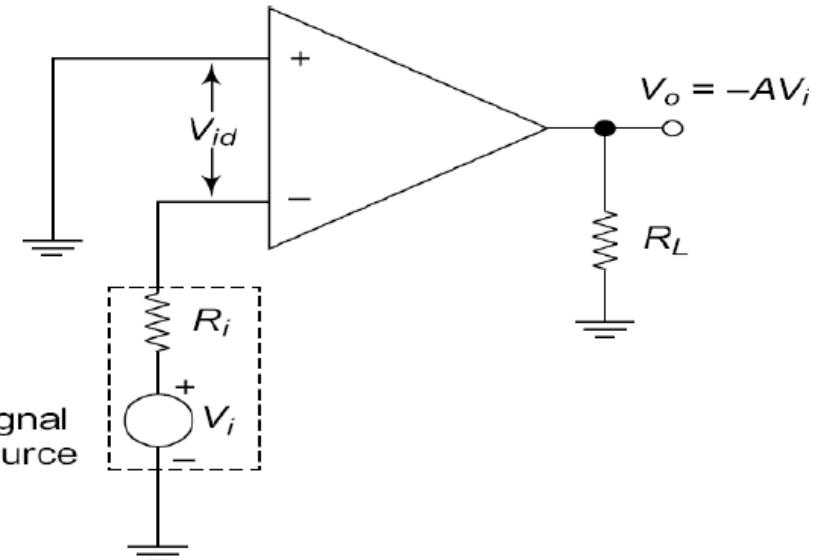
However opamp saturates at  $\pm 14$  V

## Inverting Amplifier

The output voltage is  $180^\circ$  out-of-phase output voltage  $V_o$  is given by

$$V_o = -AV_i$$

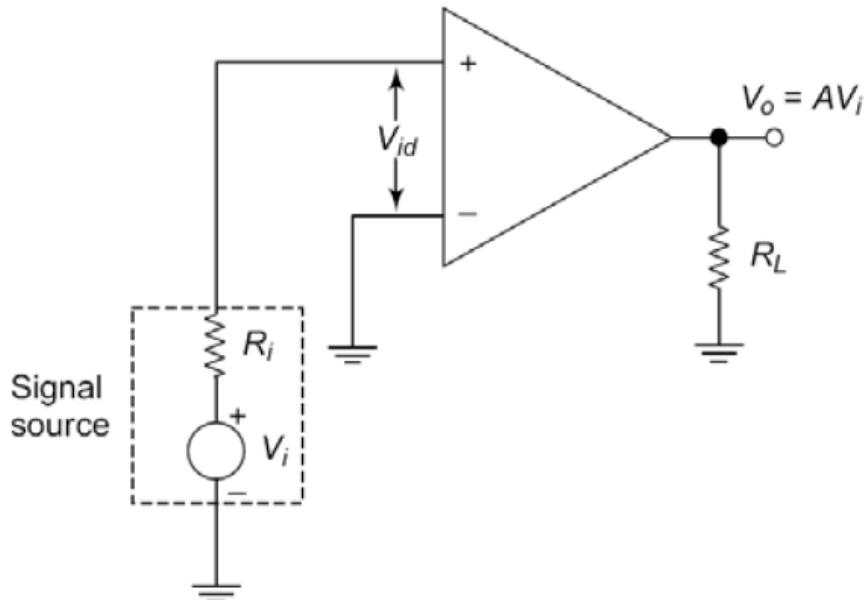
The input is amplified by open-loop gain  $A$  and is phase-shifted by  $180^\circ$ .



## Noninverting Amplifier

$$V_o = AV_i$$

The input signal is amplified by  $A$  and the output is in-phase with input



# Limitations of Open-loop Op-amp Configurations

- In all the above open-loop configurations, only very small values of input voltages can be applied. Or, clipping of the output waveform can occur.
- When operated so, the output is either in negative or positive saturation. This prevents the use of open-loop configurations of op-amps in linear applications.
- The open-loop gain is not constant - it varies with changing temperature and variations in power supply.

## CLOSED-LOOP OP-AMP CONFIGURATIONS

- The op-amp can be effectively utilized in linear applications by providing a feedback, either directly or through another network.
- If the signal fed-back is **out-of-phase by  $180^\circ$** , then the feedback is **negative or degenerative feedback**.
- If feedback is **in-phase**, then it is **positive or regenerative feedback**
- An op-amp with **feedback** is a **closed-loop amplifier**

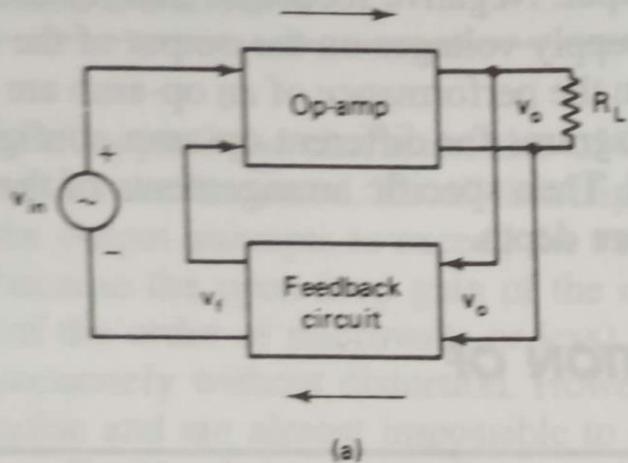
\*Benefits of negative feedback: decrease in harmonic or nonlinear distortion, reduction in the effect of input offset voltage at the output, also reduces effect of variation in temperature and supply voltages on

## Closed loop Op Amp

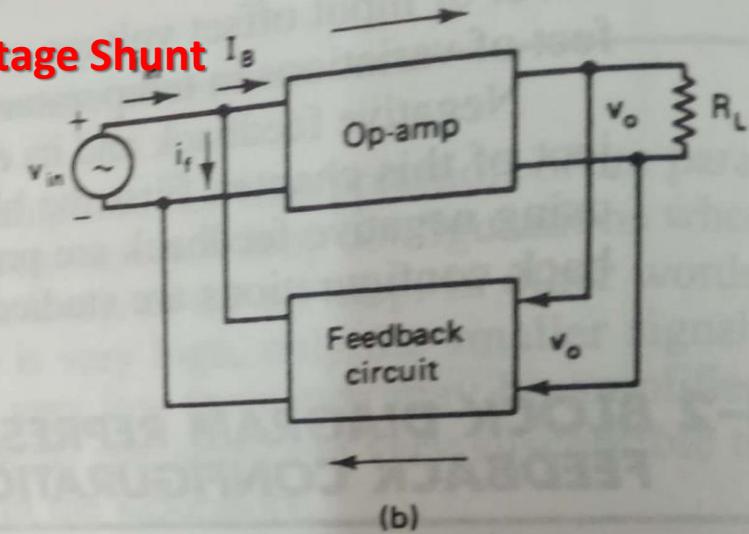
- As open loop gain of Op Amp is very high only the smaller signals of microvolts or less can be amplified.
- For the reasons mentioned earlier in slide no 44 and 45 open loop Op Amp is not used in linear applications.
- We can select as well as control the gain of the Op Amp if we introduce the modification in the basic circuit
- Hence Op Amp may be used with **Negative Feedback.**

# Closed loop Op Amp Configurations

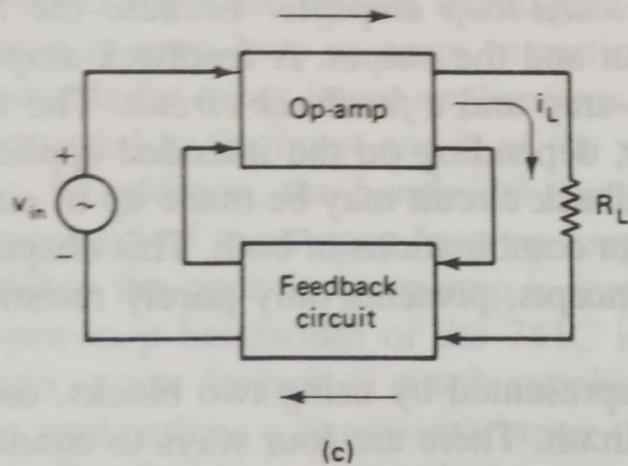
## Voltage Series



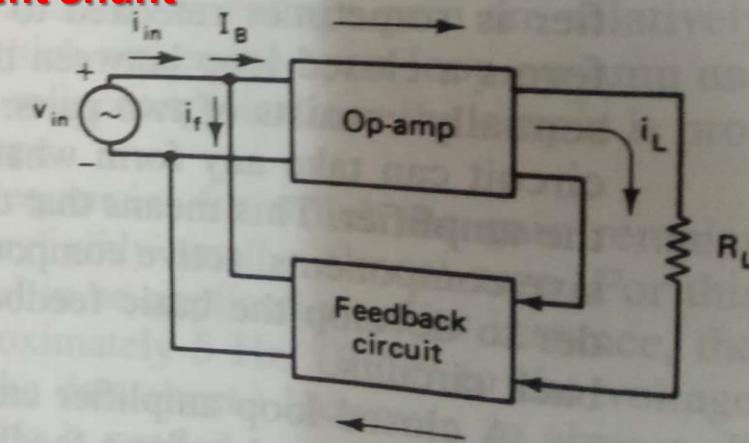
## Voltage Shunt



## Current Series



## Current Shunt



# Closed loop Op Amp Configurations

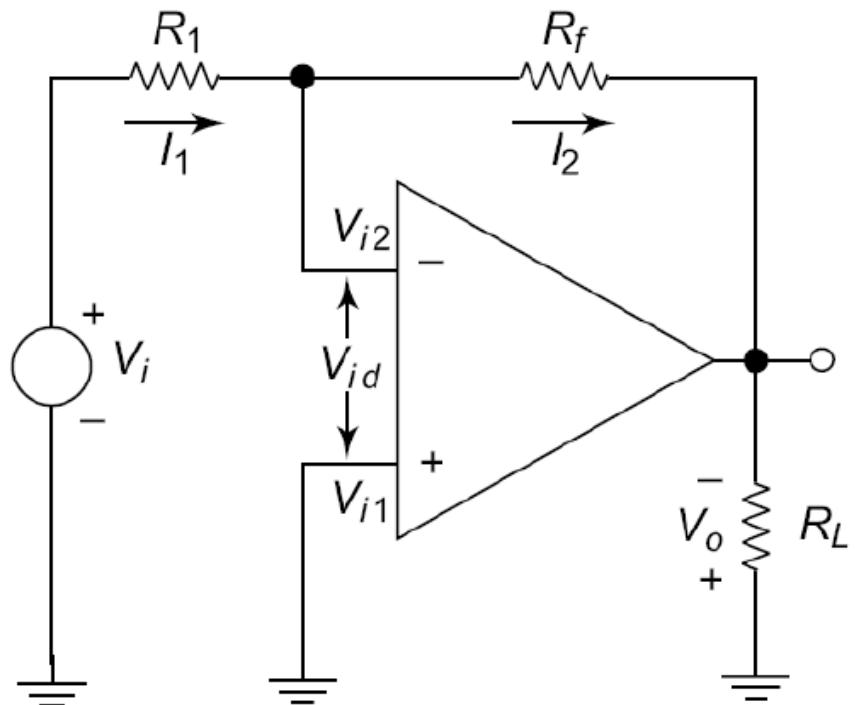
Out of four topologies two commonly used topologies for Op Amp are

1. Voltage Series (Used in Non Inverting Configuration)
2. Voltage Shunt(Used in inverting configuration)

- The most commonly used configurations are
  - Inverting amplifier (voltage-shunt feedback) and
  - Noninverting amplifier (voltage-series feedback).

## Inverting Amplifier

- Input signal drives the inverting input through  $R_1$
- Because of the phase inversion, the output signal is  $180^\circ$  out-of-phase with the input signal
- This means that the feedback signal opposes the input signal and the feedback is *negative* or *degenerative*



## Practical considerations

- i) Setting the input impedance  $R_1$  to be too **high** will pose problems with the bias current, and it is usually restricted to  $10k\Omega$ .
- ii) The **gain can not be set very high** due to the upper limit set by the **gain-bandwidth** ( $GBW = A_v \times f$ ) product.  $A_v$  is normally below 100.
- iii) The peak output of the op-amp is about 2V less than supply
- iv) Heavy output current may damage the op-amp

## Noninverting Amplifier

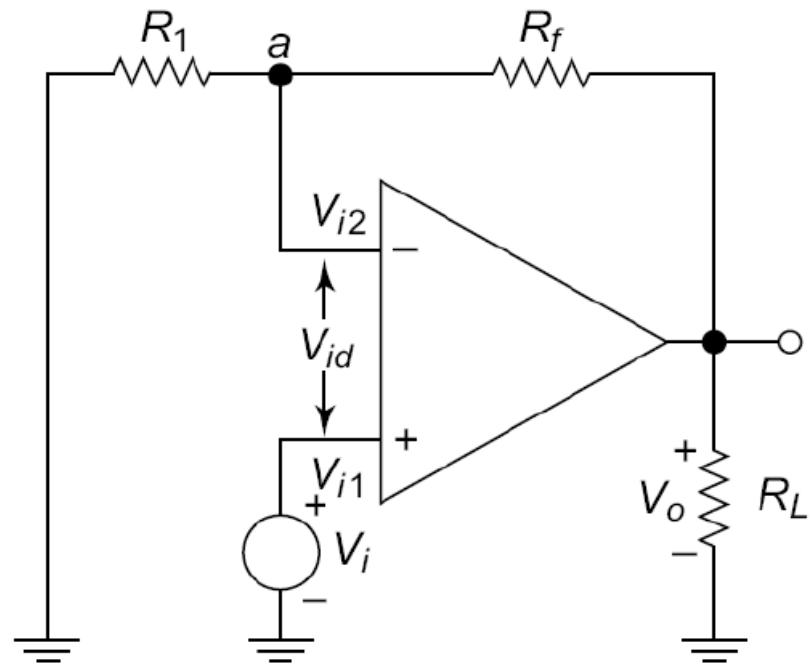
The feedback is negative or degenerative

$$V_i = \frac{R_1}{R_1 + R_f} \times V_o$$

$$\frac{V_o}{V_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}.$$

Hence, the voltage gain is

$$A_v = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$



## DIFFERENTIAL AMPLIFIER

Let  $R_1 = R_2 = R_3 = R_f = R$

Using the superposition principle,

If  $V_{i1} = 0$ ,  $V_{o2} = -V_{i2}$

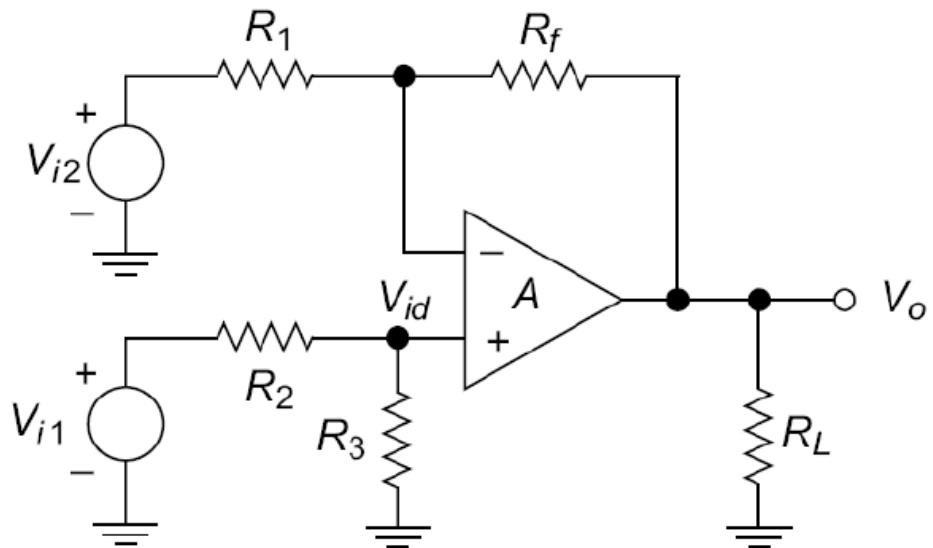
If  $V_{i2} = 0$ ,  $V_{o1} = [V_{i1}/2](1 + R/R) = V_{i1}$

If both inputs are applied,

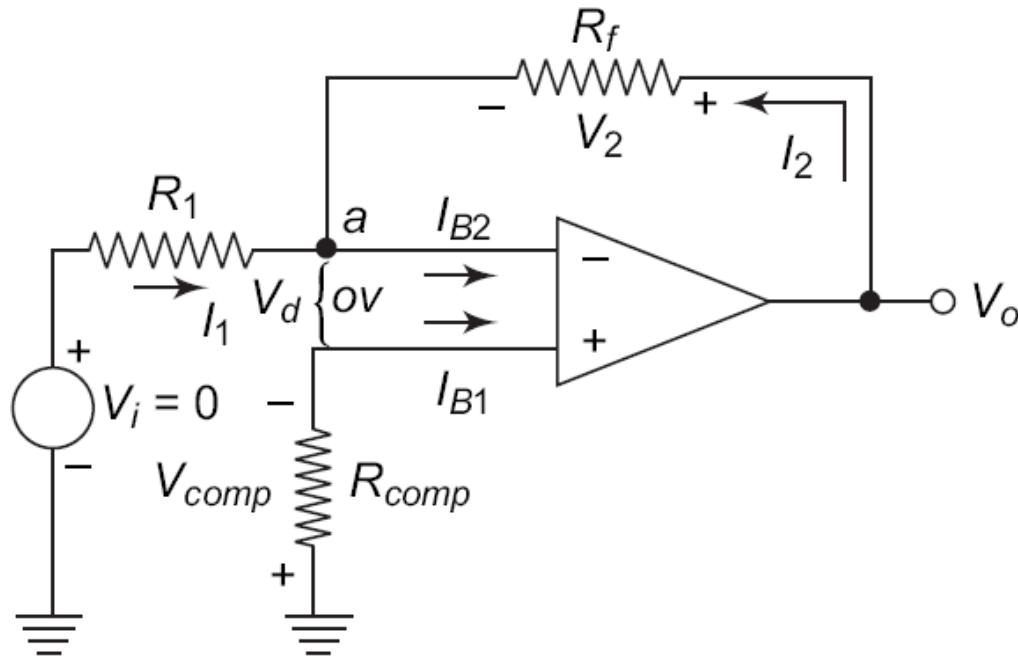
$$V_o = V_{o1} + V_{o2} = V_{i1} - V_{i2}$$

If  $R_f \neq (R_1 \neq R_2 \neq R_3)$ ,

$$V_o = \left(1 + \frac{R_f}{R}\right) \left( \frac{R_3}{R_3 + R_2} \right) V_{i1} - \frac{R_f}{R} V_{i2}$$



# Bias Current Compensation



The compensating resistor  $R_{comp}$  = the parallel combination of input and feedback resistors  
is connected at non-inverting terminal of op-amp.

$$\text{Input bias current } I_B = \frac{I_{B1} + I_{B2}}{2}$$

The output voltage  $V_o$  must be 0V. However,  $V_o$  is offset by  $V_o = I_{B2}R_f$   
Normally, 500nA of bias current generates 500mV across 1MΩ of  $R_f$ .

## Finding Maximum or total Output Offset Voltage due to bias current and Input offset Voltage

### Total Output Offset Voltage

The total output offset voltage  $V_{OT}$  is due to either the input bias current or the input offset voltage. Then, the maximum output offset voltage will be

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B$$

However, with  $R_{comp}$  included,  $V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os}$

Since  $I_{os} < I_B$ , it can be seen that the use of  $R_{comp}$  ensures a reduction in the output offset voltage generated due to bias current.

**Example** Let  $R_f = 10k\Omega$  ,  $R_1 = 2k\Omega$  , input offset voltage and current  $V_{os} = 5mV$  ,  $I_{os} = 50nA(\text{max})$  and bias current  $I_B = 200nA(\text{max})$  at  $T_A = 25^\circ C$ . Calculate the maximum output offset voltage and with  $R_{comp}$  included.

**Solution** Using the Eqn below, the total output offset voltage without the compensating resistor  $R_{comp}$  is

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B = \left(1 + \frac{10 \times 10^3}{2 \times 10^3}\right) 5 \times 10^{-3} + 10 \times 10^3 \times 200 \times 10^{-9} = 32mV$$

## Maximum output offset voltage with Rcomp

When  $R_{comp}$  is used, the maximum output offset voltage is

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right)V_{OS} + R_f I_{OS} = \left(1 + \frac{10 \times 10^3}{2 \times 10^3}\right)5 \times 10^{-3} + 10 \times 10^3 \times 50 \times 10^{-9} = 30.5mV$$

**It is obvious that the output offset voltage due to input offset voltage is a more serious problem than the input bias current or input offset current.**

# Offset Voltage Compensation for Op Amp

The two methods

1. Op Amp with offset null terminal
2. Providing externally connected offset compensation network

# Op Amp with offset null terminal

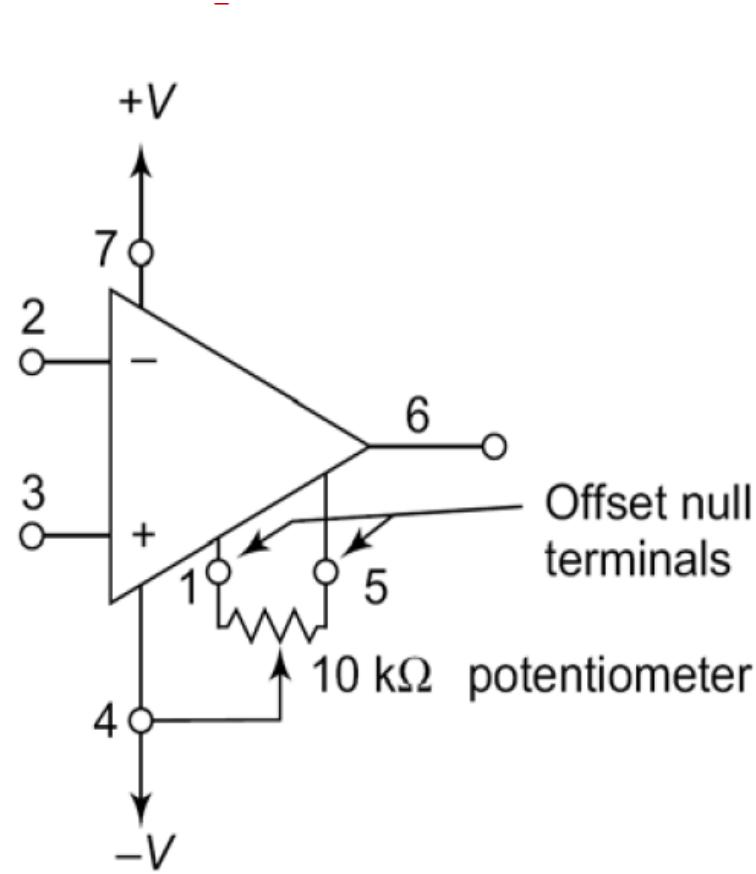
A 10 K trimming potentiometer is connected between Offset null pins 1 and 5.

## Offset Voltage Compensation

The method is by the use of

- i) an op-amp with *offset null terminals*
- ii) an externally connected *offset compensation network*.

A  $10k\Omega$  trimming potentiometer is connected between pins 1 and 5 and variable terminal of the potentiometer is connected to the negative supply pin 4. The position of the variable terminal is so adjusted that the output voltage is zero or *nulled*, when both the input voltages are zero.



# Output Offset Nulling Procedure

## Nulling procedure

- i) Connect the circuit by including  $R_{comp}$  and the voltage offset null circuit
- ii) Make all generator (source) signals zero
- iii) Connect the load to the output and turn the circuit ON
- iv) Connect a dc voltmeter or an oscilloscope across the load to measure  $V_o$
- v) Vary the offset voltage adjustment trimming potentiometer until  $V_o = 0$

## **Drift in Op-Amp Parameters**

Op Amp input offset voltage ,Bias currents and offset currents are function of following.

1. Change in temperature  $\Delta T$
2. Change in supply voltage
3. Change in time

Change in Op-amp parameters with respect to above is called as drift.

## Thermal Drift

- It was assumed so far that the parameter  $V_{OS}$  and  $I_B$  and  $I_{OS}$  are constant for a given op-amp. However, in practice, the following operating conditions pose a great challenge to these parameters:
- Change in temperature  $\Delta T$ , ii) Change in supply voltage  $\Delta V_{OS}$  and
- Change in time  $\Delta T$
- The change in temperature causes the most serious variation in  $V_{OS}$ ,  $I_B$  and  $I_{OS}$ . *Thermal drift* is defined as the **average rate of change of input offset voltage per unit change in temperature**. It is denoted by  $\frac{\Delta V_{OS}}{\Delta T}$  in  $\mu V / {}^\circ C$ .

## Practice Problems

An op-amp has the drift specifications as given below:

$$\frac{\Delta I_{OS}}{\Delta T} = 0.4 \text{ nA}/^{\circ}\text{C}$$

$$\frac{\Delta V_{OS}}{\Delta T} = 20 \mu\text{V}/^{\circ}\text{C}$$

and temperature span of variation =  $25^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

$$R_f = 1M\Omega$$

$$R_i = 200K\Omega$$

Assuming that after nulling at  $25^{\circ}\text{C}$ , the output voltage  $V_o = 0$ . At a temperature of  $60^{\circ}\text{C}$ , calculate what would be the maximum change in output voltage due to  
(a) drift in  $V_{OS}$  and (b) drift in  $I_{OS}$ .

## Problem1 solution

### Solution

(a) The change in  $V_{OS}$  is given by

$$\pm 20 \mu V / {}^\circ C \times (75 - 25) {}^\circ C = \pm 20 \times 10^{-6} \times 50 = \pm 1 mV$$

Then, the error voltage in the output due to  $V_{OS}$  is given by

$$\begin{aligned} V_o &= V_{OS} \left( 1 + \frac{R_f}{R_i} \right) \\ &= \pm 1 \times 10^{-3} \left( 1 + \frac{1 \times 10^6}{200 \times 10^3} \right) = \pm 6 mV \end{aligned}$$

(b) Change in  $I_{OS}$  is given by

$$\Delta I_{OS} = \pm 0.4 \times 10^{-9} / {}^\circ C \times 50 {}^\circ C = \pm 20 nA$$

Change in  $V_o$  due to change in  $I_{OS}$  is

$$\Delta V_{OS} = \pm 20 nA \times R_f = \pm 20 \times 10^{-9} \times 1 \times 10^6 = \pm 20 mV$$

The changes in  $V_o$  caused by variations due to  $V_{OS}$  and  $I_{OS}$  can either add or subtract from one another. Hence, the worst case drift is given by

$$+6 mV + 20 mV = 26 mV$$

or  $-6 mV - 20 mV = -26 mV$

## Problem2

Assume that an op-amp 741 connected as a unity gain inverting amplifier has an input change of 8V. What is the time taken for the output to change by 8V?

### Solution

Given output voltage change = 8V

For the op-amp 741, slew rate =  $0.5V/\mu s$

$$\text{We know } \text{Slew rate} = \frac{\text{Output voltage change}}{\text{Time}}$$

$$\text{Therefore, } \text{Time} = \frac{\text{Output voltage change}}{\text{Slew rate}} = \frac{8V}{0.5V/\mu s} = 16\mu s$$

### Problem 3

Assuming the slew rate for an op-amp is  $0.6V/\mu s$ , what is the maximum undistorted sine-wave that can be obtained for a) 10V peak and b) 1V peak?

#### Solution

Given the slew rate for 741 is  $0.5V/\mu s$ .

a) For the sine wave of 10V peak,

$$f_{max} = \frac{Slew\ rate}{2\pi V_m} = \frac{0.5V/\mu s}{2\pi \times 10V} = \frac{0.5}{2\pi \times 10 \times 10^{-6}} = 7.96\text{kHz}$$

b) For the sine wave of 1V peak,

$$f_{max} = \frac{0.5V/\mu s}{2\pi \times 1V} = \frac{0.5}{2\pi \times 1 \times 10^{-6}} = 79.6\text{kHz}$$

## Problem 4

The output voltage of a certain op-amp circuit changes by 10V in  $3\mu s$ . What is its slew rate?

### Solution

$$\text{The slew rate} = \frac{dV_o}{dt} = \frac{10V}{3\mu s} = 3.33V/\mu s$$

## Problem 5

An op-amp has a unity gain-bandwidth of  $2MHz$  for a signal of frequency  $1kHz$ . What is the open-loop gain?

### Solution

Given UGB=2MHz and  $f_l = 1kHz$ .

$$\text{The open-loop dc voltage gain, } A_o = \frac{UGB}{f_l} = \frac{2 \times 10^6}{1 \times 10^3} = 2000$$

## Problem 6

For an inverting amplifier using op-amp, assume  $R_1 = 470\Omega$  and  $R_f = 4.7k\Omega$ . Calculate the closed-loop voltage gain of the amplifier.

### Solution

$$A_V = -\frac{R_f}{R_1} = -\frac{4.7K}{470\Omega} = -10$$

## Problem 7

For a non-inverting amplifier using an op-amp, assume  $R_1 = 120\Omega$  and  $R_f = 5.6k\Omega$ . Calculate the closed-loop voltage gain of the amplifier.

### Solution

$$\begin{aligned}\text{The closed-loop voltage gain } A_v &= 1 + \frac{R_f}{R_1} \\ &= 1 + \frac{5.6 \times 10^3}{120} = 47.67\end{aligned}$$

## Problem 8

For a given op-amp,  $CMRR = 10^4$  and differential gain  $A_{dm} = 10^4$ . Determine the common-mode gain  $A_{cm}$  of the op-amp.

### Solution

$$CMRR = \frac{A_{dm}}{A_{cm}} = 10^4$$

Therefore, the common-mode gain  $A_{cm} = \frac{A_{dm}}{CMRR} = \frac{10^4}{10^4} = 1$ .

## Problem 9

In response to a square wave input, the output of an op-amp changes from -3V to +3V over a time interval of  $0.25\ \mu s$ . Determine the slew rate of the op-amp.

### Solution

Given the change in output voltage =  $3 - (-3) = 6V$

The time interval =  $0.25\ \mu s$

Therefore, the slew rate,  $SR = \frac{\Delta V_o}{\Delta t} = \frac{6}{0.25} = 24V/\mu s$

37. Assuming slew rate for Op-amp IC 741 is 0.5V/ $\mu$ sec , what is the maximum undistorted sine-wave that can be obtained for 2V input?

$$\text{Slew rate} = 2\pi f \cdot V_m$$
$$\therefore f = \frac{\text{Slew-rate}}{2\pi V_m} = \frac{0.5\text{V}/\mu\text{sec}}{2\pi \times 2}$$
$$= 39.8^\circ \text{kHz}$$

- Assuming slew rate for LF 356 is 12V/ $\mu$ sec , what is the maximum undistorted sine-wave frequency that can be applied for 1V input.

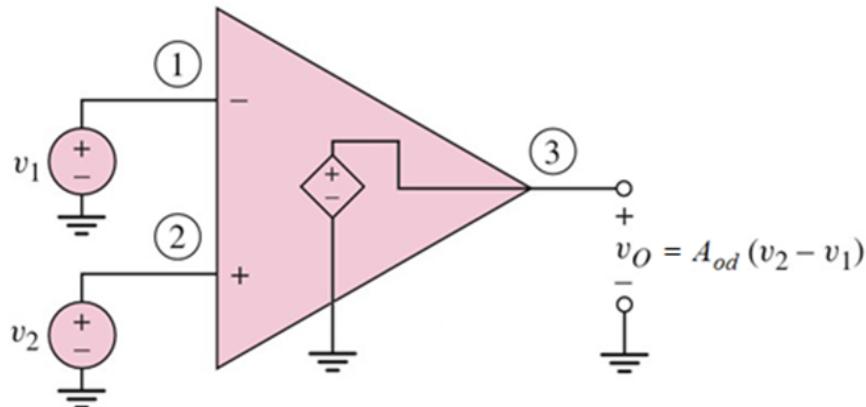
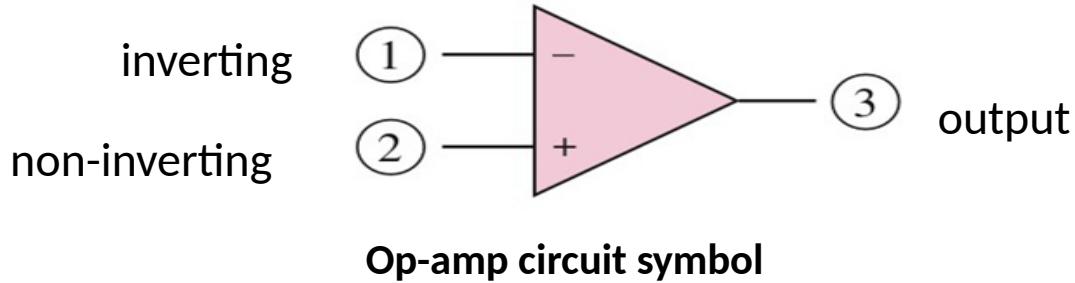
Slew Rate :  $2\pi f \cdot V_m$

$$\therefore f = \frac{S.R}{2\pi \cdot V_m} = \frac{12}{2\pi \cdot 1} = 1.91 \text{ MHz}$$

## 2. Linear Applications of op-Amp

# Lesson Plan

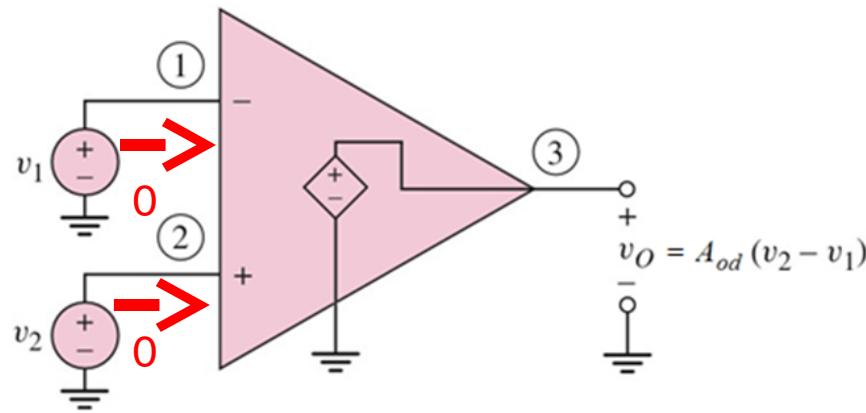
Topic	Sub points	Book-Page Nos.
Inverting and Non Inverting Configurations of Opamp Summing ,Scaling		T1-141 T1-193
Voltage follower,Difference Amplifier,		T1-203 T1- 195
Instrumentation Amplifiers		T1-197
Ideal Integrator and Practical Integrator		T1-229 & T2-203
Numericals		T2
Ideal differentiator,practical differentiator		T1-234, T2-209
Numericals		T2



- Open loop mode
- $V_o = A_{od} (v_2 - v_1)$ 
  - $A_{od}$  is referred to as the open loop gain.
  - Notice that if  $v_2 = v_1$ , the open loop gain equals to  $\infty$

- Op amp can be configured to be used for different type of circuit applications:
  - Inverting Amplifier
  - Non - inverting Amplifier
  - Summing Amplifier
  - Difference
  - Integrator
  - Differentiator

- Two main characteristics:
  - We want the open loop gain to be equal to  $\infty$  which means that  $v_2 = v_1$



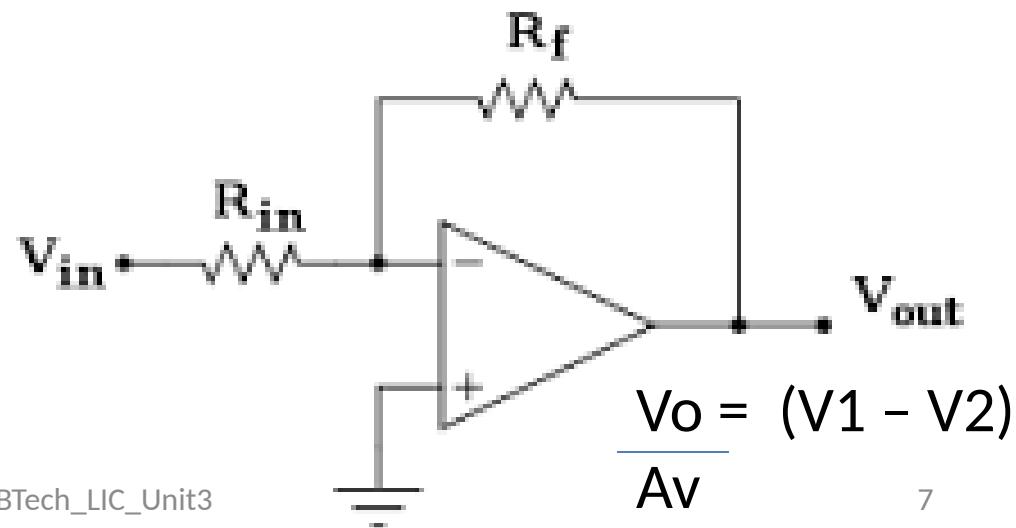
- We also want the input resistance to be equal to  $\infty$ .

# Virtual short and Virtual ground

- Voltage between inverting and non-inverting terminals of OPAMP is output voltage divided by open loop gain of OPAMP. Open loop gain being very large, this voltage is very small. Practically zero. This is virtual short.
- Virtual ground concept is NOT valid for positive feedback or open loop operation of OPAMP.
- Unlike actual short, there is no current through this short. Hence the term VIRTUAL.

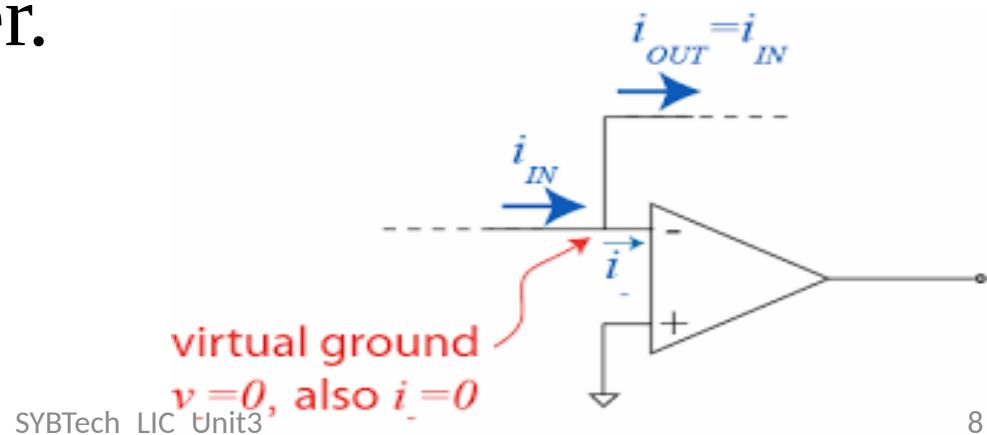
# Virtual Ground

- If the non-inverting (+) terminal of OP-AMP is connected to ground, then due to the "virtual short" existing between the two input terminals, the inverting (-) terminal also be at ground potential. hence it is said to be as "**virtual ground**".



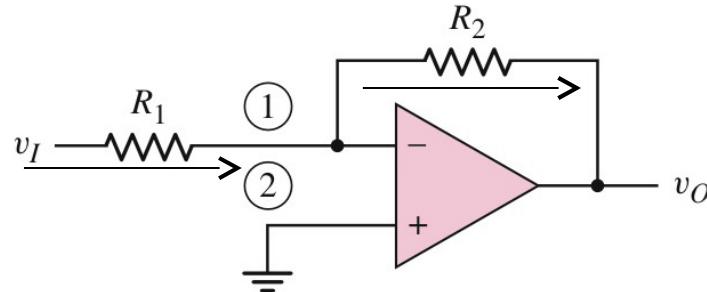
# Virtual Short

- The input impedance ( $R_i$ ) of an OP-AMP is ideally infinite. Hence current "I" flowing from one input terminal to the other will be zero.
- Thus the voltage drop across  $R_i$  will be zero and both input terminals will be at the same potential. In other words they are **virtually shorted** to each other.



- Why the applications are called as Linear Applications?

# Inverting Amplifier



Op-amp as an inverting amplifier

Voltage at node 1 (inverting) = voltage at node 2 (non-inverting )

KCL at node 1:

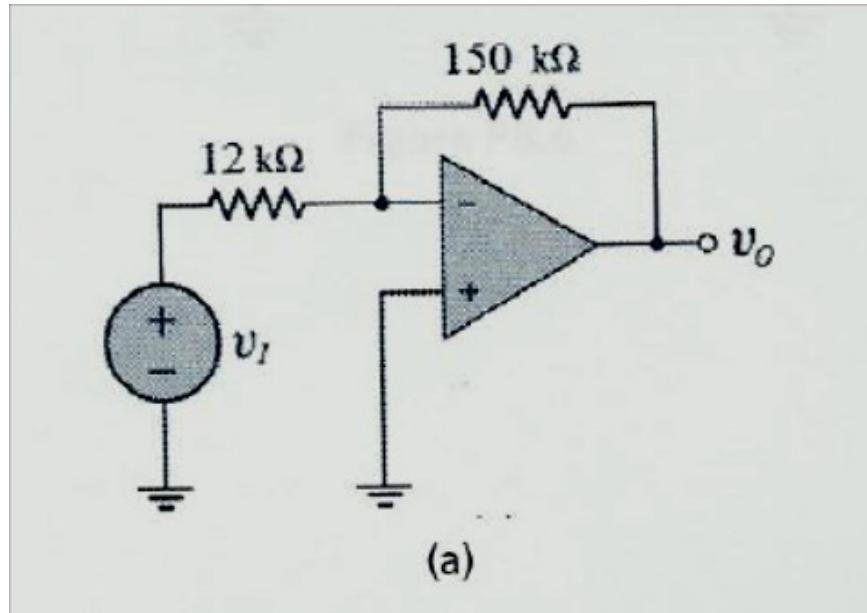
$$(V_i - 0) / R_1 = (0 - V_o) / R_2$$

$$V_i / R_1 = - V_o / R_2$$

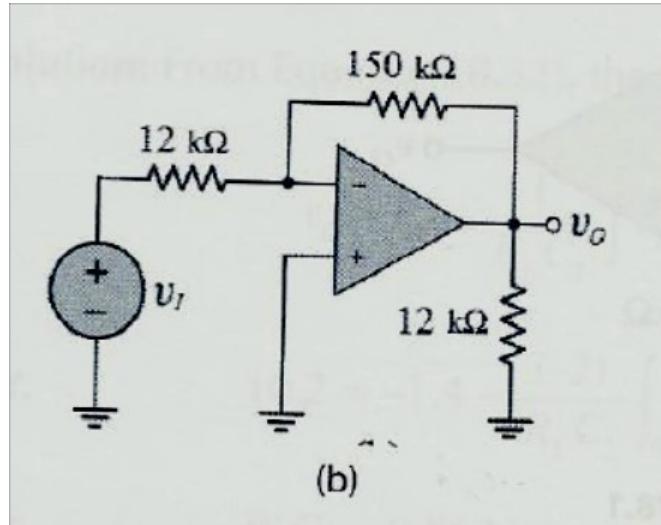
$$\frac{V_o}{V_i} = - \frac{R_2}{R_1}$$



# Exercise



$$\text{Gain} = - (R_2 / R_1) = -(150/12) = -12.5$$



Can the voltage gain be calculated using the same formula?  
 Try and use the same method in deriving  $V_o/V_i$

# Non - Inverting Amplifier

Voltage at node 1 (inverting) = voltage at node 2 (non-inverting )

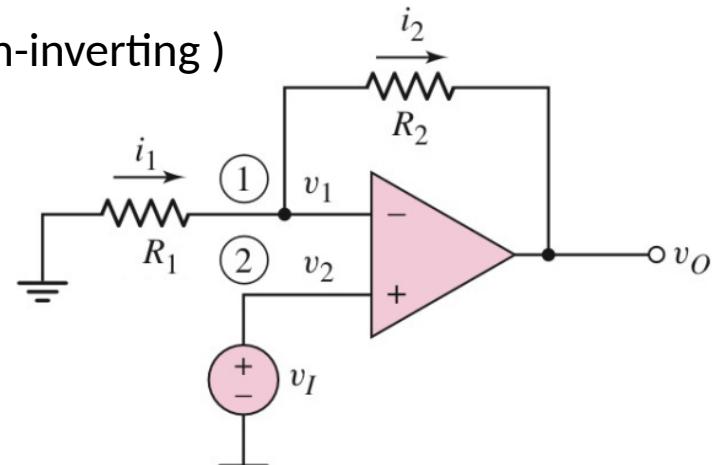
KCL at node 1:

$$(0 - V_i) / R_1 = (V_i - V_o) / R_2$$

$$-(V_i / R_1) = (V_i / R_2) - (V_o / R_2)$$

$$V_o / R_2 = (V_i / R_2) + (V_i / R_1) = V_i \left( \frac{1}{R_2} + \frac{1}{R_1} \right)$$

$$V_o / V_i = R_2 \left( \frac{1}{R_2} + \frac{1}{R_1} \right)$$



Noninverting amplifier

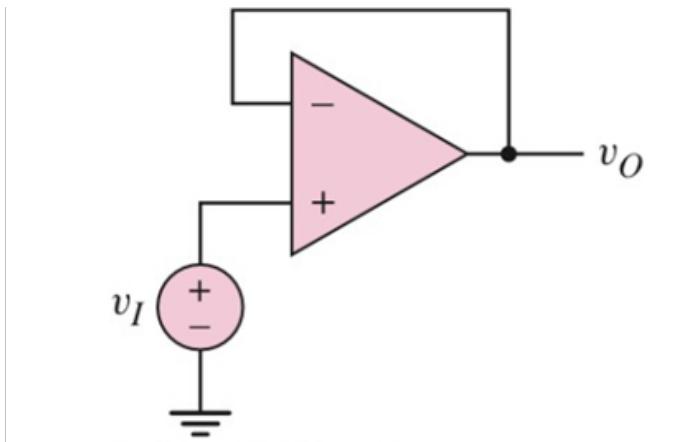
Voltage gain,

$$A_v = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$$

# Comparison of Inverting and Non Inverting Amplifier

Sr. No.	Parameter	Inverting Amplifier	Non Inverting Amplifier
1	Voltage Gain		
2	Phase shift between input and output		
3	Input resistance	Equal to R1	Very large

# Voltage Follower / Buffer Amplifier

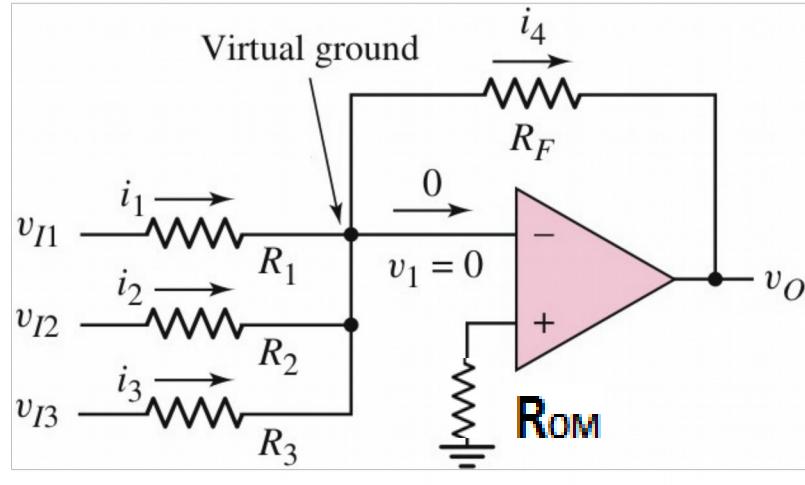


A voltage follower circuit/Buffer amplifier

$$V_o = V_i$$

Hence, gain = 1

# Summing Amplifier



$$i_1 + i_2 + i_3 - i_4 - 0 = 0$$

Output voltage

$$V_o = -R_F \left( \frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} + \frac{V_{i3}}{R_3} \right)$$

## Example

Design a summing amplifier as shown in figure to produce a specific output signal, such that  $v_o = 1.25 - 2.5 \cos \omega t$  volt. Assume the input signals are  $v_{i1} = -1.0$  V,  $v_{i2} = 0.5 \cos \omega t$  volt. Assume the feedback resistance  $R_F = 10$  k $\Omega$



**Solution:** output voltage

$$v_0 = -R_F \left( \frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \frac{v_{I3}}{R_3} \right) = -R_F \left[ \frac{(-1)}{R_1} + \frac{0.5 \cos \omega t}{R_2} \right]$$

Or,  $1.25 - 2.5 \cos \omega t = R_F \left[ \frac{1}{R_1} - \frac{0.5 \cos \omega t}{R_2} \right]$

Or,  $1.25 - 2.5 \cos \omega t = \frac{R_F}{R_1} - \left( \frac{R_F}{R_2} \right) (0.5 \cos \omega t)$

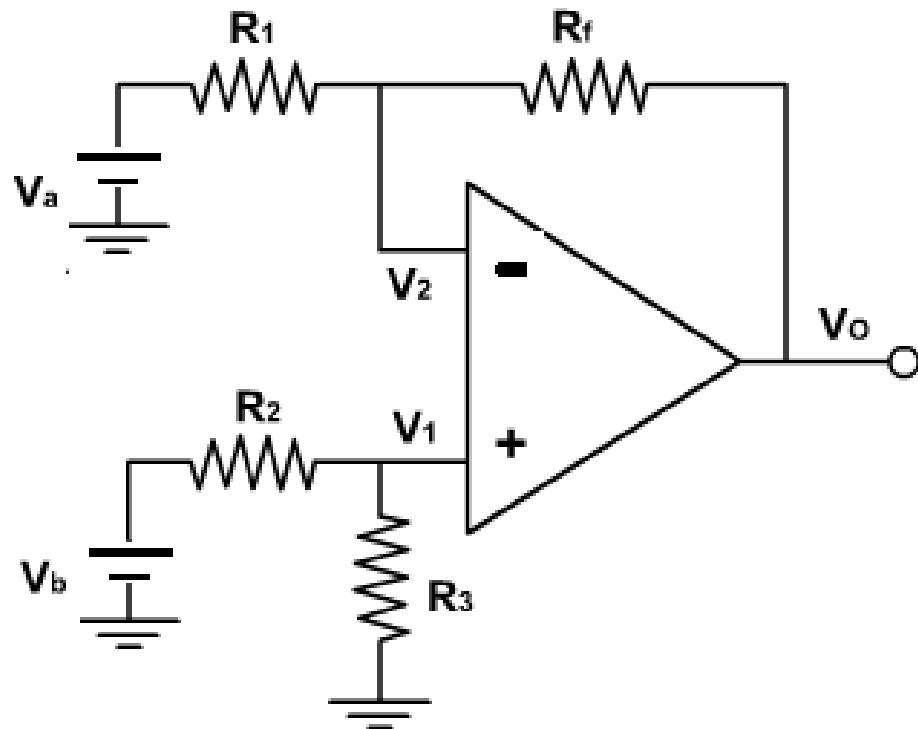
So, the DC input line contains the resistance  $R_1$  can be calculated as

$$\frac{R_F}{R_1} = 1.25 \quad \text{Or,} \quad R_1 = \frac{R_F}{2.5} = \frac{10}{1.25} = 8 \text{ k}\Omega$$

Similarly the time varying signal input line contains the resistance  $R_2$  as

$$\left( \frac{R_F}{R_2} \right) (0.5 \cos \omega t) = 2.5 \cos \omega t \quad \text{Or,} \quad R_2 = R_F \times \frac{0.5 \cos \omega t}{2.5 \cos \omega t} = 10 \times \frac{0.5}{2.5} = 2 \text{ k}\Omega$$

# Difference Amplifier



<https://nptel.ac.in/courses/117107094/12>

- Since there are two inputs superposition theorem can be used to find the output voltage. When  $V_b = 0$ , then the circuit becomes inverting amplifier, hence the output due to  $V_a$  only is
- $V_{o(a)} = -(R_f / R_1) V_a$
- Similarly when,  $V_a = 0$ , the configuration is a non-inverting amplifier having a voltage divided network at the non-inverting input

$$V_1 = \frac{R_3}{R_2 + R_3} V_b$$

The output due to  $V_b$  only is

$$\begin{aligned} V_{o(b)} &= \left(1 + \frac{R_f}{R_1}\right) \left(\frac{R_3}{R_2 + R_3}\right) V_b \\ &= \left(\frac{R_1 + R_f}{R_1}\right) \left(\frac{R_3}{R_2 + R_3}\right) V_b \end{aligned}$$

$f R_1 = R_2$  &  $R_f = R_3$  then

$$V_{o(b)} = \frac{R_f}{R_1} V_b$$

Therefore the total output voltage  $V_o$  is given by

$$V_o = V_{o(a)} + V_{o(b)}$$

$$V_o = \frac{R_f}{R_1} (-V_a + V_b)$$

Exaples: <https://nptel.ac.in/courses/117107094/12>

# Instrumentation Amplifier

- Why IA?

-An **instrumentation amplifier** is a differential **amplifier** optimized for high input impedance and high CMRR. An **instrumentation amplifier** is typically used in applications in which a small differential voltage and a large common mode voltage are the inputs.

-An instrumentation amplifier is a type of differential amplifier that has been outfitted with input buffer amplifiers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use

- There are many commercially available single chip instrumentation amplifiers in the market like AD 620. Several issues have to be taken into consideration for the design of a signal conditioning circuit. Linearity, sensitivity, loading effect, bandwidth, common mode rejection are the important issues that affect the performance of the signal conditioning circuits.



It is basically a difference amplifier

In many industrial and consumer applications – Temperature , Pressure, flow etc.

It is used to amplify low level output signal of transducer

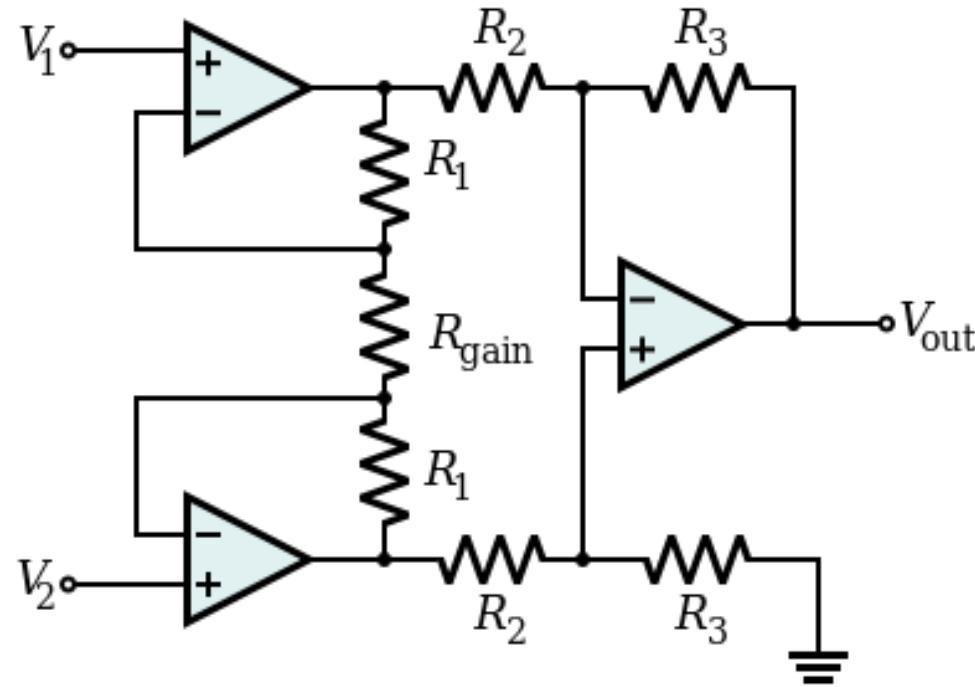
### **Requirement of IA:**

- Precise low level signal amplification
- Low noise
- Low thermal drift
- High input impedance
- Accurate closed loop gain
- Low power dissipation
- High CMRR
- High Slew rate
- Monolithic IA are AD521/524/624/625/620 – AMP - 01

# Specifications

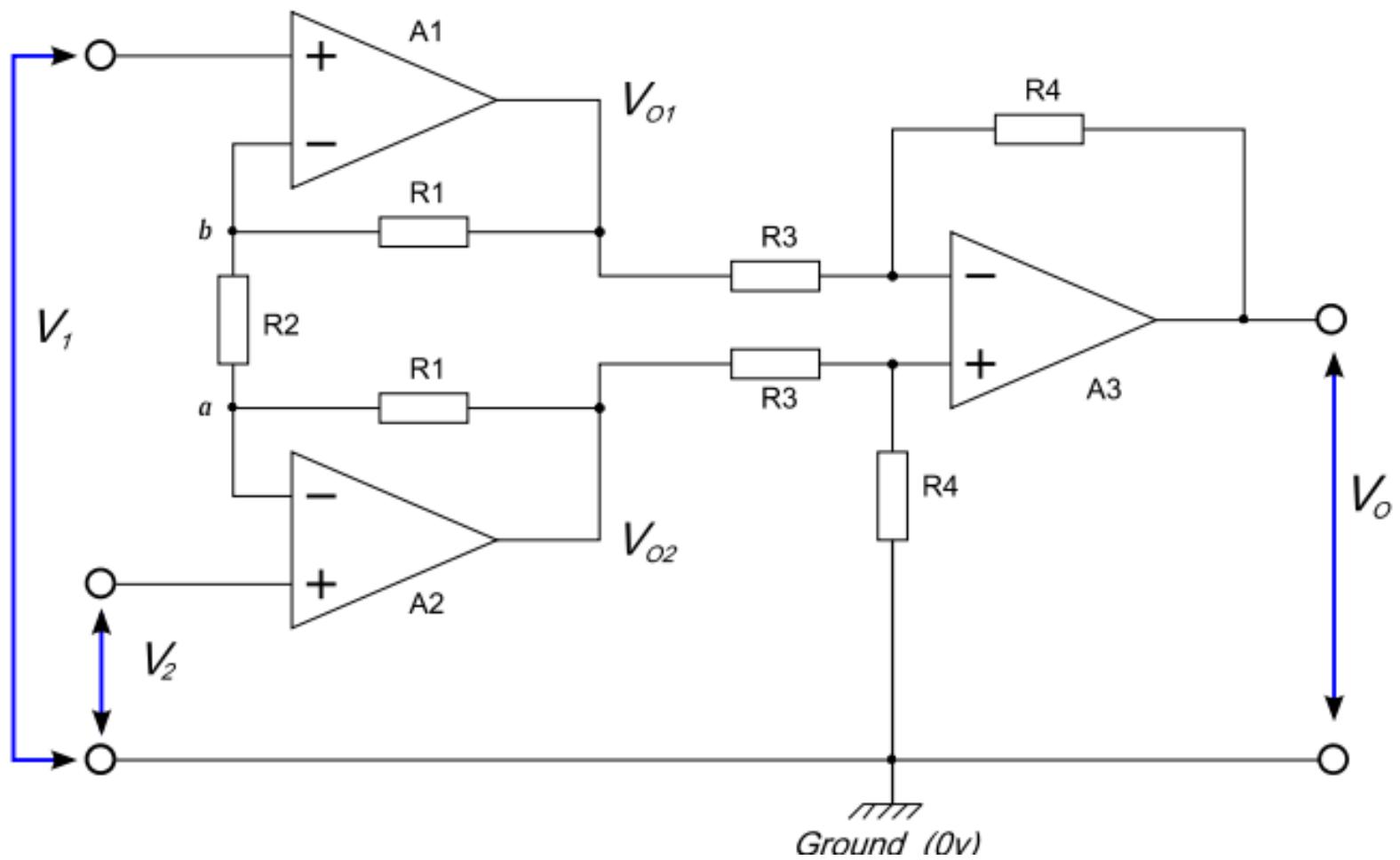
- CMRR is a very important parameter for instrumentation circuit applications and it is desirable to use amplifiers of high CMRR when connected to instrumentation circuits.
- High  $R_i$
- Low  $R_o$
- Low offsets
- High gain

### 3 Op Amp based diagram



The gain of the circuit is

$$\frac{V_{\text{out}}}{V_2 - V_1} = \left( 1 + \frac{2R_1}{R_{\text{gain}}} \right) \frac{R_3}{R_2}$$



The first stage is a balanced input, balanced output amplifier formed by A1 and A2 which amplifies the differential signal but passes the common mode signal without amplification. The second stage formed by A3 is a differential amplifier which largely removes the common mode signal.

The voltage VO1 consists of two components, the voltage due to V1 and the voltage due to V2.

If V2 = 0 then point a will be a virtual earth and amplifier A1 will act as a non inverting amplifier with a gain of

$$V_{o1} = V_1 \left( \frac{R1 + R2}{R2} \right)$$

If V1 = 0 then point b will be a virtual earth and **amplifier A1** will act as an inverting amplifier with a gain of

$$V_{o1} = - \left( \frac{R1}{R2} \right) V_2$$

the output from amplifier A1 with respect to ground (0v) will be

$$V_{o1} = \frac{RI + R2}{R2} V_1 - \frac{RI}{R2} V_2$$

$$V_{o1} = \frac{(RI + R2)V_1 - RI V_2}{R2}$$

$$V_{o1} = \left( \frac{RI}{R2} + 1 \right) V_1 - \frac{RI}{R2} V_2$$

$$V_{o1} = \frac{RI}{R2} [V_1 - V_2] + V_1$$

Similarly the output from amplifier A2 with respect to ground will be

$$V_{o2} = \frac{RI}{R2} [V_2 - V_1] + V_2$$

These two voltages are fed into a differential amplifier A3, the gain of this amplifier is given by

$$V_o = \frac{R4}{R3} (V_{o2} - V_{o1})$$

If we substitute the equations for VO<sub>2</sub> and VO<sub>1</sub> we get

$$V_o = \frac{R4}{R3} \left( \left( \frac{RI}{R2} \{V_2 - V_1\} + V_2 \right) - \left( \frac{RI}{R2} \{V_1 - V_2\} + V_1 \right) \right)$$

After simplification

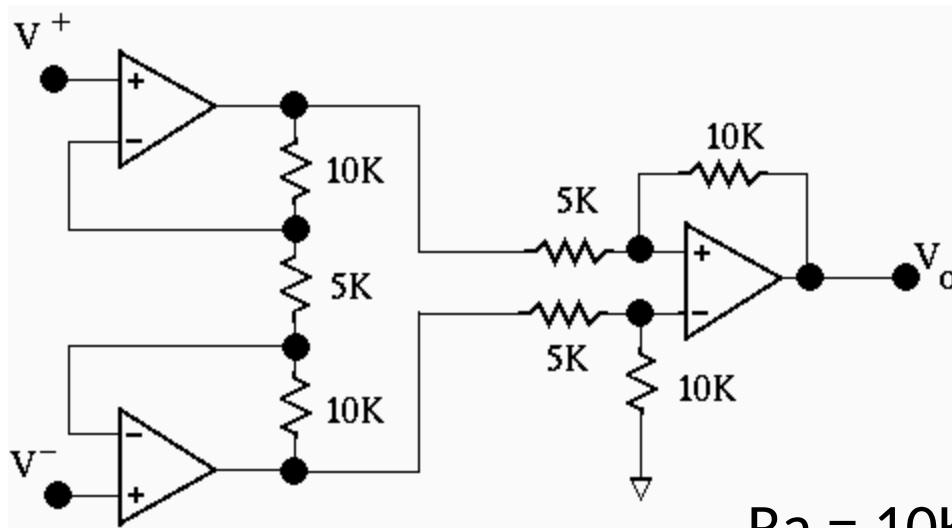
$$V_o = (V_2 - V_1) \frac{R4}{R3} \left[ 1 + \frac{2RI}{R2} \right]$$

Therefore the differential gain G is

$$G = \frac{R4}{R3} \left[ 1 + \frac{2RI}{R2} \right]$$

# Numericals on IA

- What is the gain of the instrumentation amplifier shown in Figure 2?



$$R_a = 10K$$

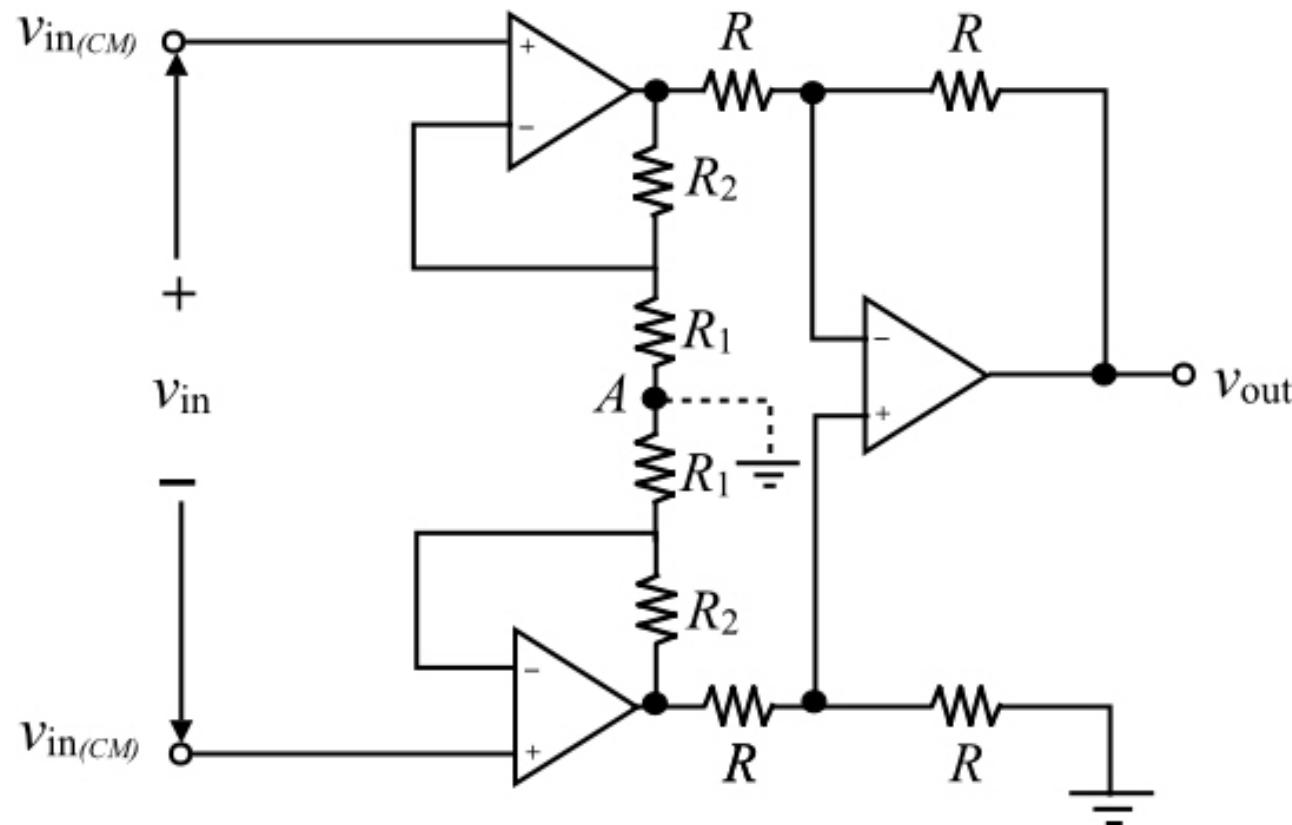
$$R_b = 5k$$

$$R_1 = 5K$$

$$R_2 = 10K$$

$$A_v = (1 + 2R_a/R_b)(R_2/R_1) = (1 + 4)2 = 10$$

In the instrumentation amplifier of Fig. 20-18,  $R_1 = 1 \text{ k}\Omega$  and  $R_2 = 99 \text{ k}\Omega$ . What is the output voltage if  $v_{in} = 2 \text{ mV}$ ? If three OP-07A op amps are used and  $R = 10 \text{ k}\Omega \pm 0.5 \text{ percent}$ , what is the CMRR of the instrumentation amplifier?



# Applications of IA

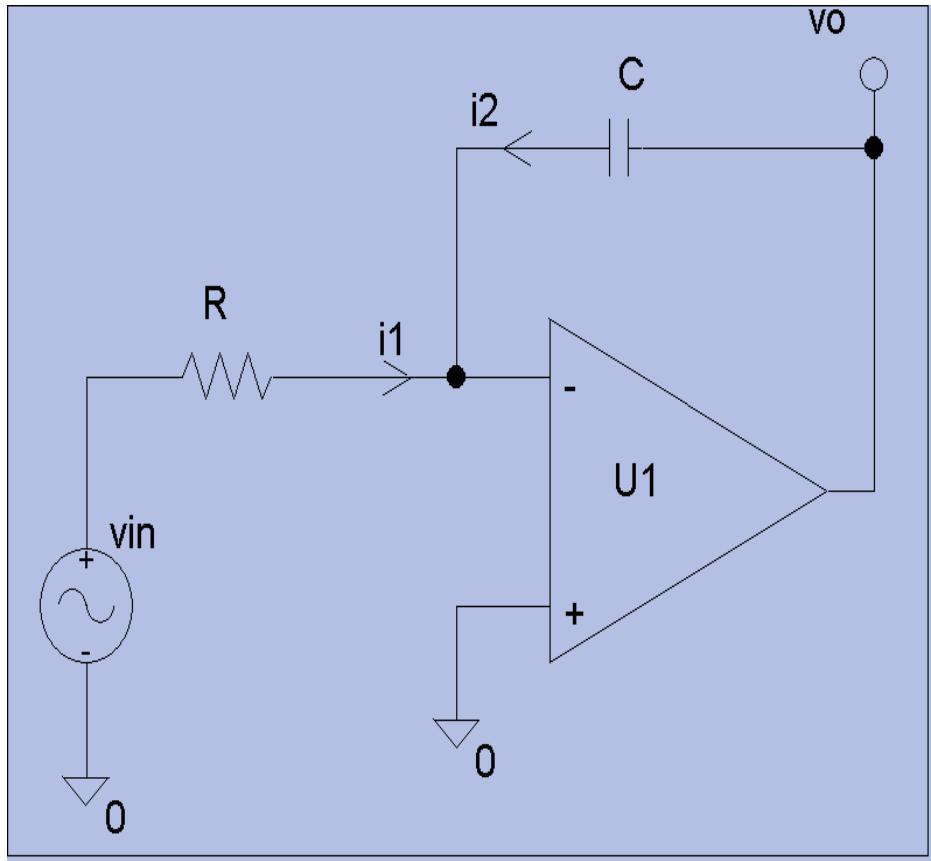
- Strain gauge bridge interface for pressure and temperature sensing.
- A variety of low side and high side current sensing application
- Medical instrumentation, used in ECG connection
- Current/voltage monitoring
- Audio application involving weak audio signal
- High speed signal conditioning

# Applications of IA...

- In Data acquisition from low output transducers such as strain gauges, Thermocouples, Wheatstone bridge measurements e.t.c
- In Medical instrumentation, Navigation, Radar instrumentation e.t.c
- In Audio applications involving low amplitude audio signals in noisy environments to improve the signal to noise ratio;
- High-speed signal conditioning for video data acquisition and imaging
- High frequency signal amplification in cable RF systems.

# Integrator

The inverting input is at virtual ground. Hence,



$$i_1 = \frac{v_{in}}{R} = i_2$$

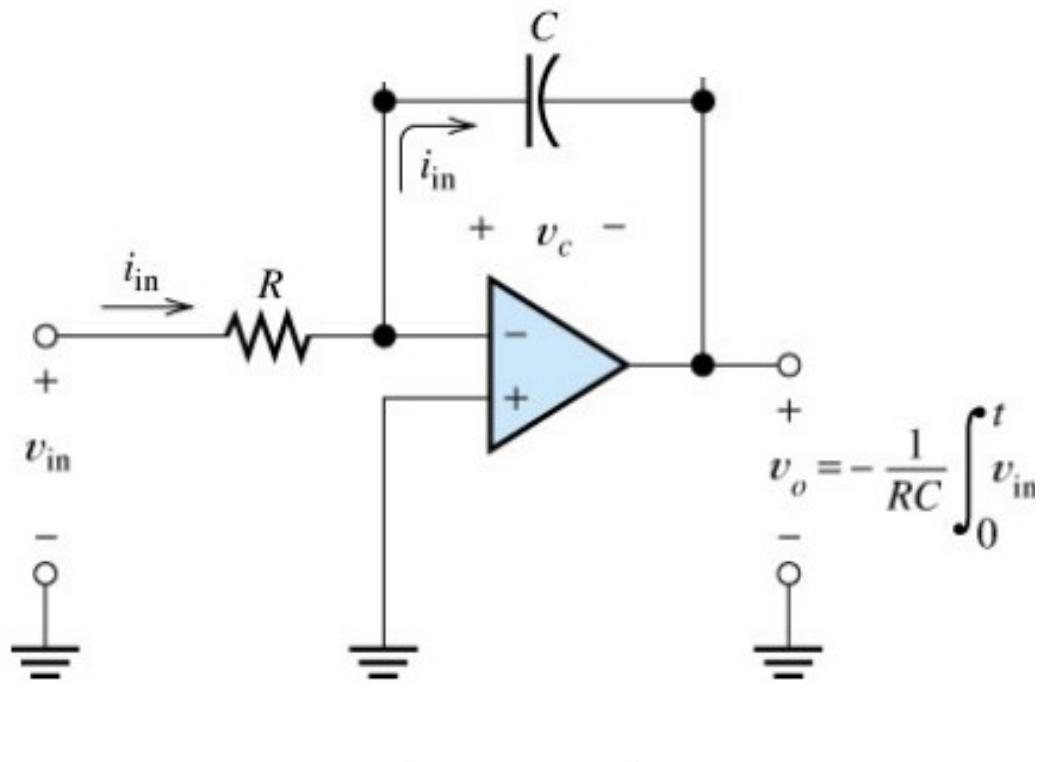
$$i_2 = C \frac{dv_o}{dt}$$

Applying KCL at the inverting input

$$i_1 + i_2 = 0$$

$$\Rightarrow v_o = -\frac{1}{RC} \int v_{in} dt + v_o(\text{initial})$$

# Ideal Integrator

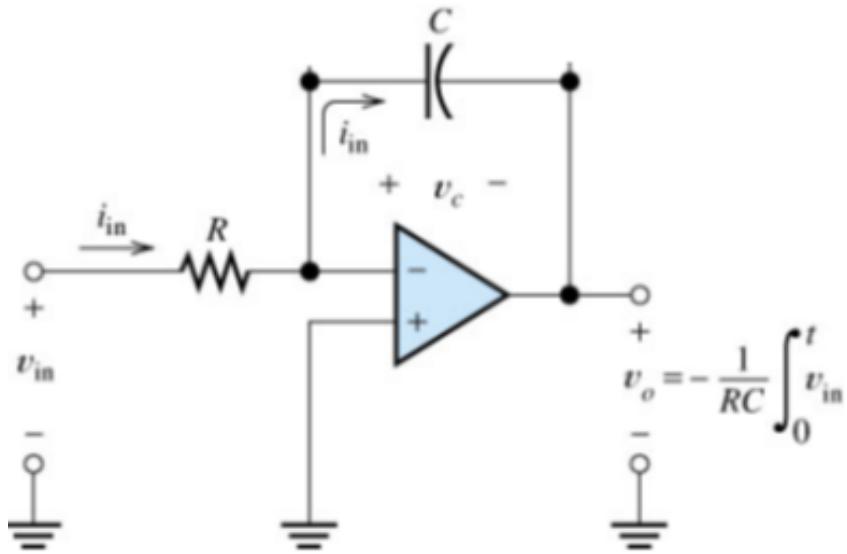


$$i_{in}(t) = \frac{v_{in}(t)}{R}$$

$$v_c(t) = \frac{1}{C} \int_0^t i_{in}(x) dx$$

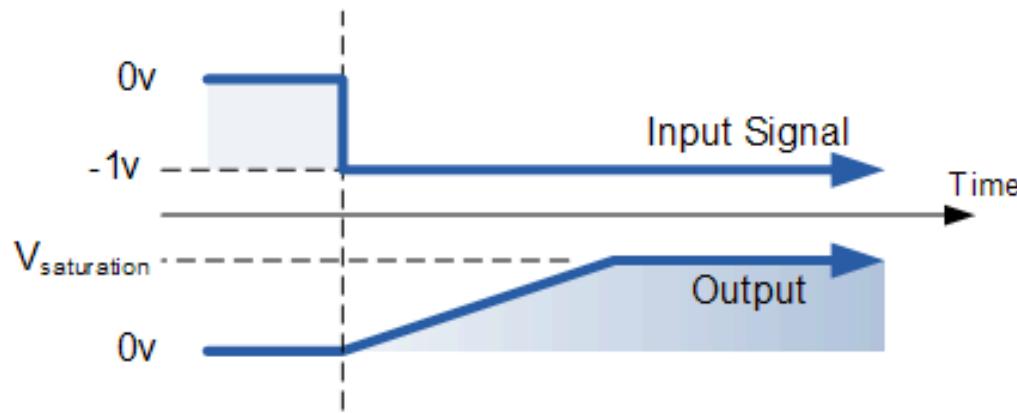
$$v_o(t) = -v_c(t)$$

$$v_o(t) = -\frac{1}{RC} \int_0^t v_{in}(x) dx$$



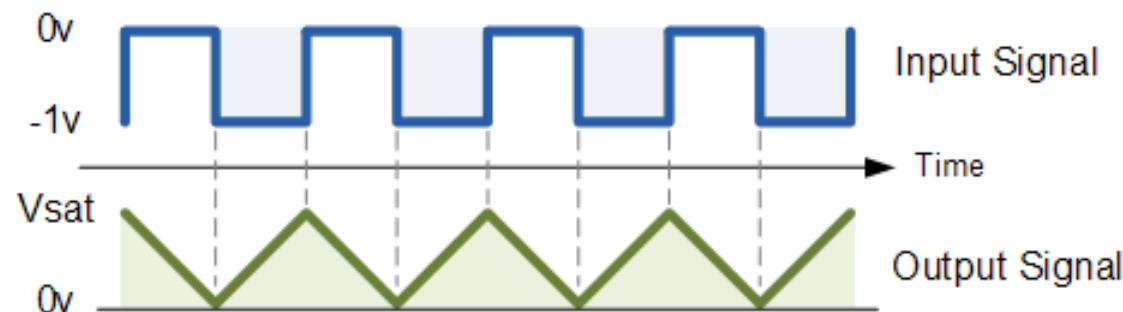
- As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance  $X_c$  slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, ( $\tau$ ) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input.
- Since the capacitor is connected between the op-amp's inverting input (which is at earth potential) and the op-amp's output (which is negative), the potential voltage,  $V_c$  developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of  $X_c/R_{in}$  increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

- At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input resistor (  $XC/RIN$  ) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).



- If we apply a constantly changing input signal such as a square wave to the input of an Integrator Amplifier then the capacitor will charge and discharge in response to changes in the input signal. This results in the output signal being that of a sawtooth waveform whose output is affected by the RC time constant of the resistor/capacitor combination because at higher frequencies, the capacitor has less time to fully charge. This type of circuit is also known as a Ramp Generator and the transfer function is given below.

### Op-amp Integrator Ramp Generator

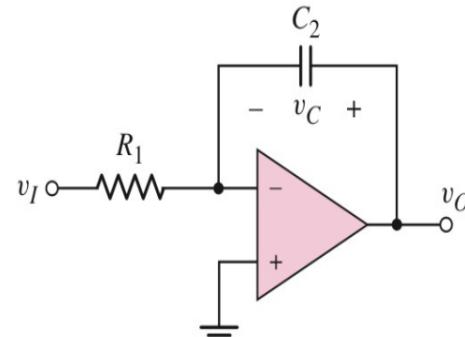


# Integrator

Output voltage,  $v_0 = -\frac{1}{R_1 C_2} \int v_I dt$

If the capacitor has some initial voltage,  $V_C$

$$v_0 = V_C - \frac{1}{R_1 C_2} \int v_I dt$$



Integrator circuit

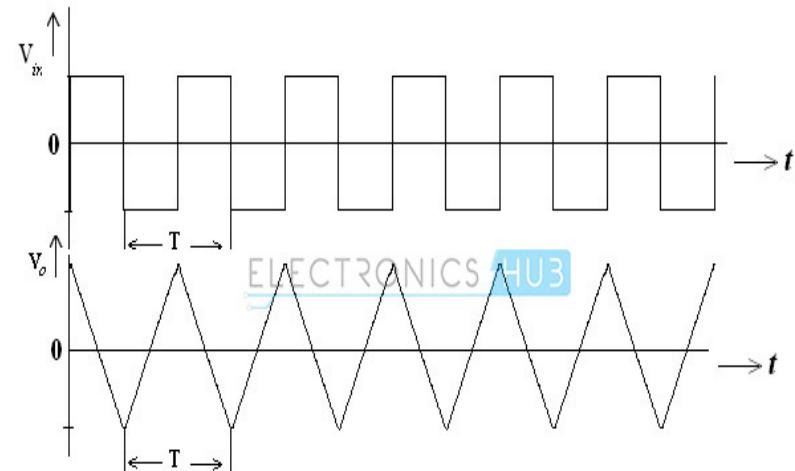
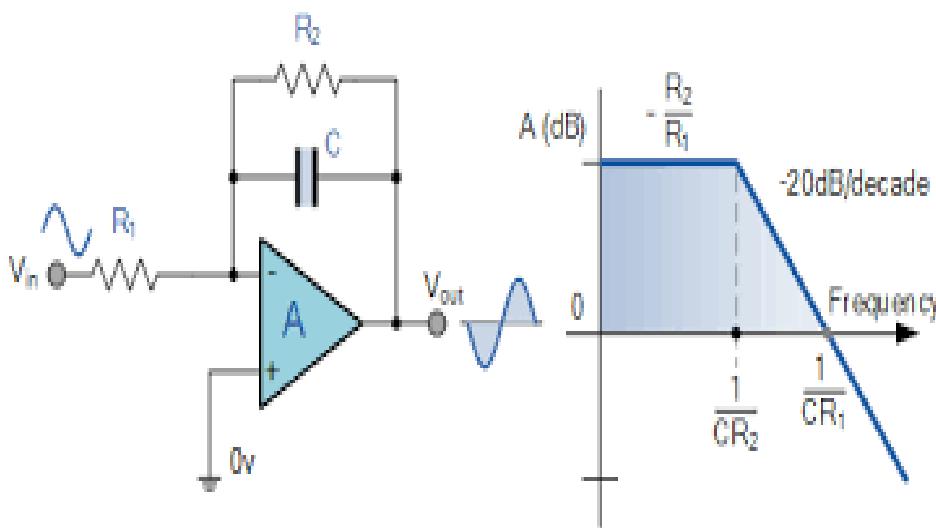
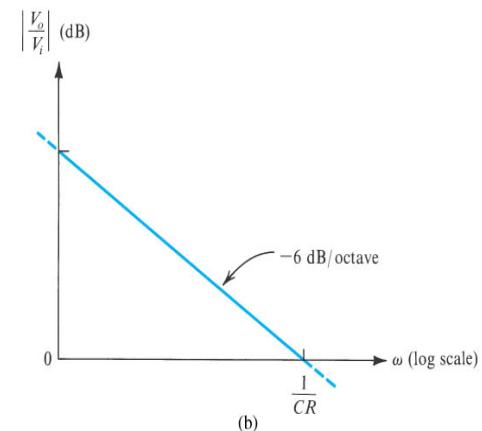
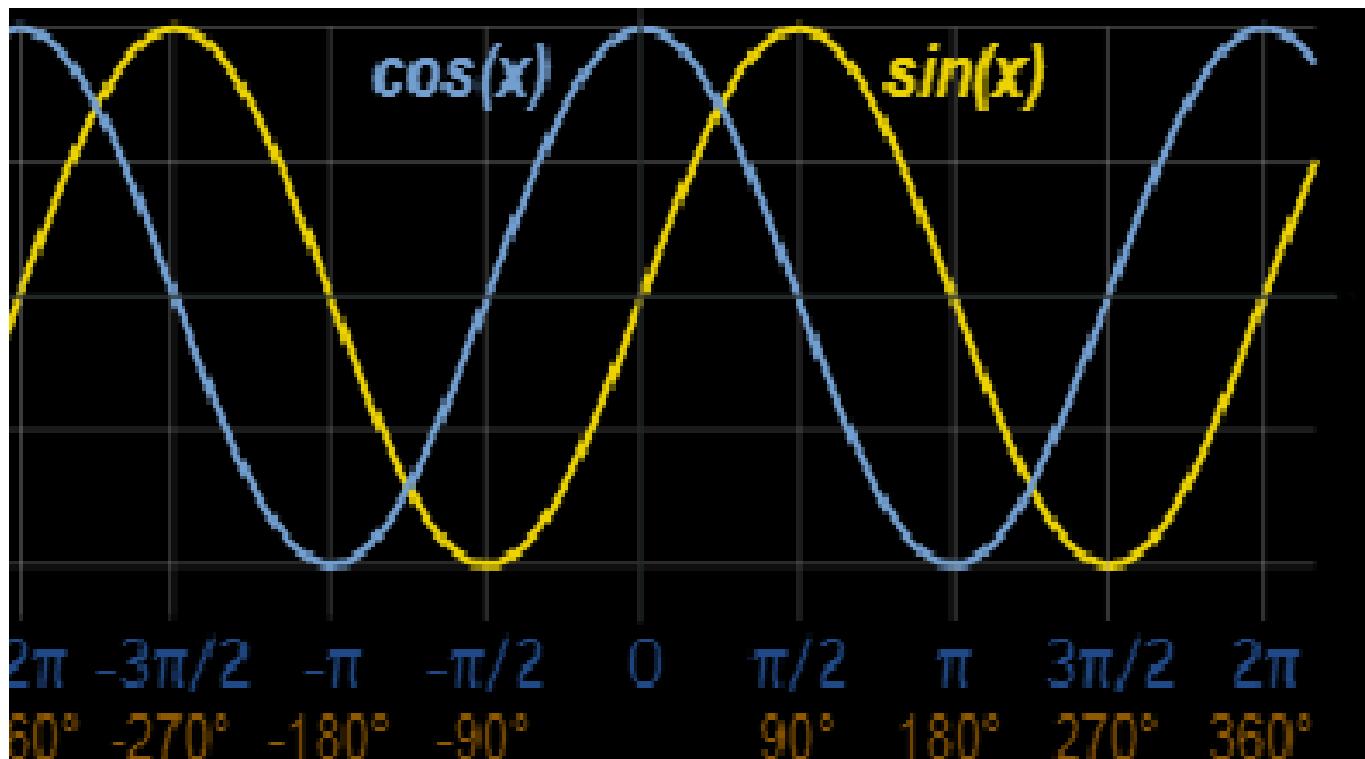


Fig: Input and Output Waveforms of an Integrator

The feedback resistor limits the low frequency gain and hence minimizes the variations in the output voltage



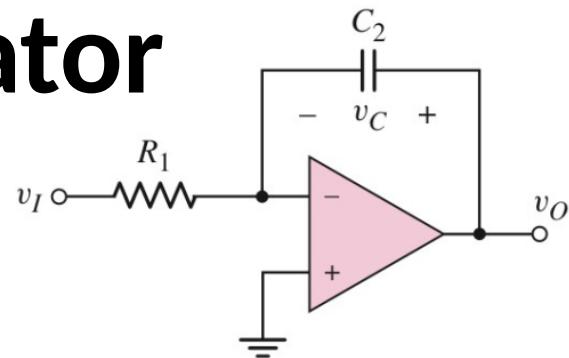
# Ideal Integrator

Output voltage,

$$v_0 = -\frac{1}{R_1 C_2} \int v_I dt$$

If the capacitor has some initially voltage,  $V_C$

$$v_0 = V_C - \frac{1}{R_1 C_2} \int v_I dt$$



## EXAMPLE 8.3

An integrator circuit as shown in figure has a voltage  $V_C = -1.4$  V across the capacitor at time  $t = 0$ . A step input voltage  $v_I = -2$  V is applied at time  $t = 0$ . Determine the  $RC$  time constant necessary such that the output voltage reaches  $+10.2$  V at time  $t = 5$  ms.

**Solution:** output voltage

$$v_0 = V_C - \frac{1}{R_1 C_2} \int v_I dt = V_C - \frac{1}{R_1 C_2} \int_0^5 v_I dt$$

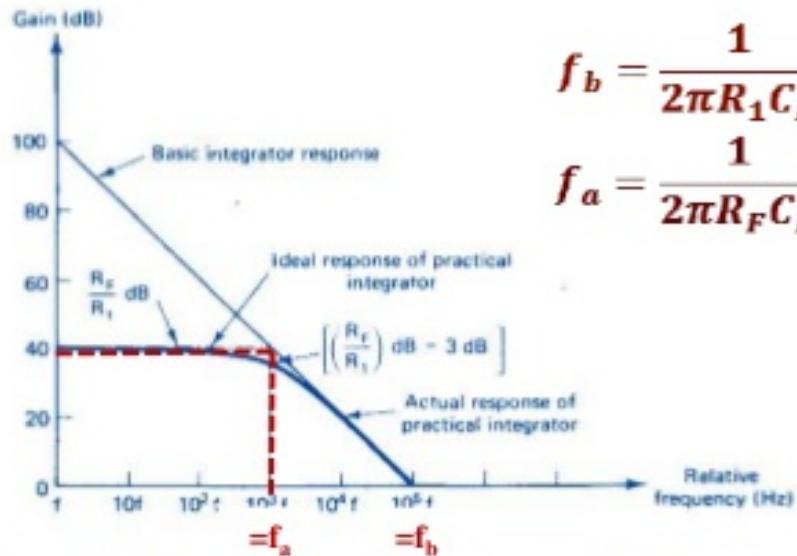
Or,

$$10.2 = -1.4 - \frac{(-2)}{R_1 C_2} \int_0^5 dt = -1.4 + \frac{2}{R_1 C_2} [5]$$

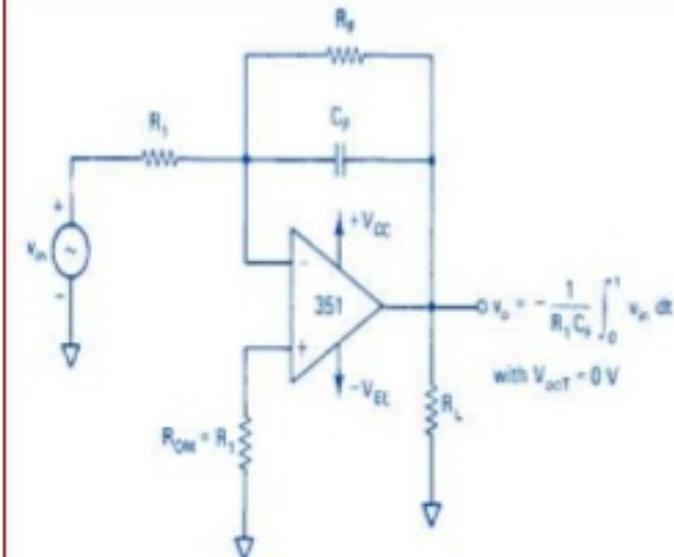
Or,

$$R_1 C_2 = 0.862 \text{ ms.}$$

# Practical Integrator



**Figure 7-24** Frequency response of basic and practical integrators.  $f_a = 1/(2\pi R_F C_F)$  and  $f_b = 1/(2\pi R_1 C_F)$ .



**Figure 7-25** Practical integrator.

If the op-amp was ideal, an integrator as shown in above Figure would require just one resistor,  $R$ , and one capacitor,  $C$ , and the relation between the output and input voltages would be given by  $f_a = \frac{1}{2\pi R F C_F}$ , the gain limiting frequency

$f_a < f_b$ . If  $f_a = f_b/10$ , then  $R_F = 10R_1$ . The input signal will be integrated properly, if time period T of the input signal

$$T \geq R_F C_F = \frac{1}{2\pi f_a}$$

12/20/2022

The Integrating range is in between  $f_a$  &  $f_b$   
SYBTech\_LIC\_Unit3

# The AC or Continuous Op-amp Integrator

- If we changed the above square wave input signal to that of a sine wave of varying frequency the Op-amp Integrator performs less like an integrator and begins to behave more like an active “Low Pass Filter”, passing low frequency signals while attenuating the high frequencies.
- At 0Hz or DC, the capacitor acts like an open circuit blocking any feedback voltage resulting in very little negative feedback from the output back to the input of the amplifier. Then with just the feedback capacitor, C, the amplifier effectively is connected as a normal open-loop amplifier which has very high open-loop gain resulting in the output voltage saturating.
- This circuit connects a high value resistance in parallel with a continuously charging and discharging capacitor. The addition of this feedback resistor, R2 across the capacitor, C gives the circuit the characteristics of an inverting amplifier with finite closed-loop gain of  $R2/R1$ . The result is at very low frequencies the circuit acts as an standard integrator, while at higher frequencies the capacitor shorts out the feedback resistor, R2 due to the effects of capacitive reactance reducing the amplifiers gain.

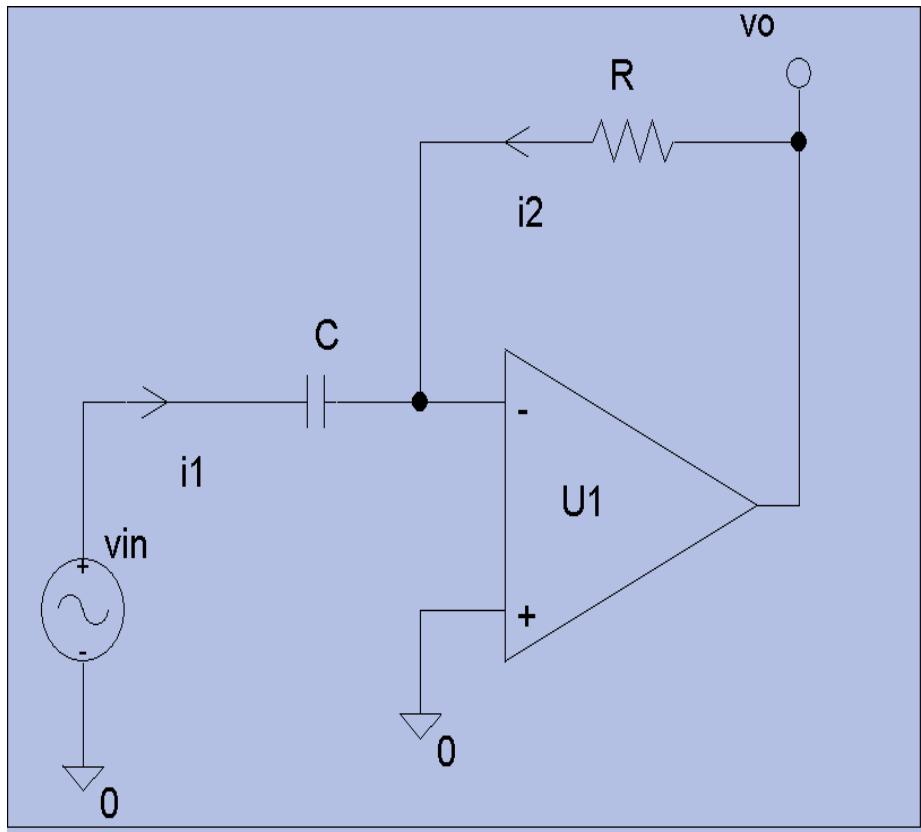
# Applications of Integrator

- In Analog Computers
- Analog to Digital Converters
- Signal Wave shaping circuits

# Numericals on integrator

# Differentiator

Since the inverting input is at virtual ground



$$i_1 = C \frac{dv_{in}}{dt}$$

$$i_2 = \frac{v_o}{R}$$

Applying KCL at the inverting input

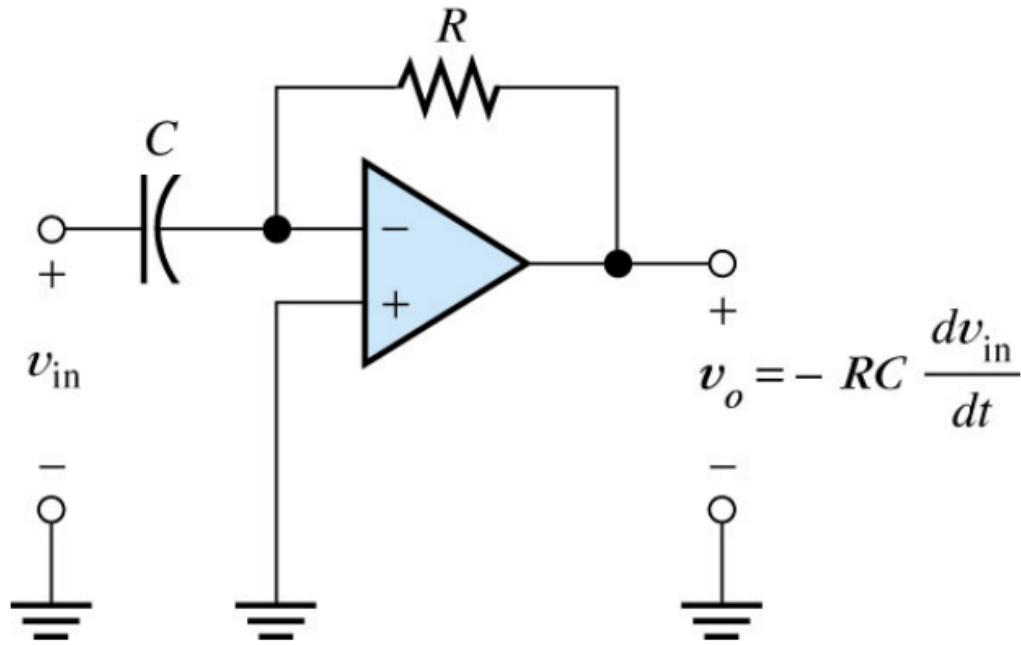
$$i_1 + i_2 = 0$$

$$\therefore C \frac{dv_{in}}{dt} + \frac{v_o}{R} = 0$$

$$\Rightarrow v_o = -RC \frac{dv_{in}}{dt}$$

Differentiators are not preferred in practice as they amplify noise (high frequencies)

$$v_o(t) = -RC \frac{dv_{in}}{dt}$$

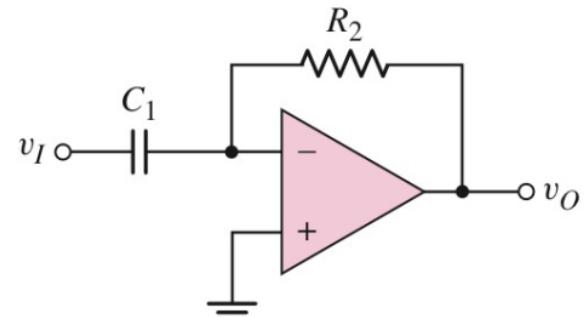
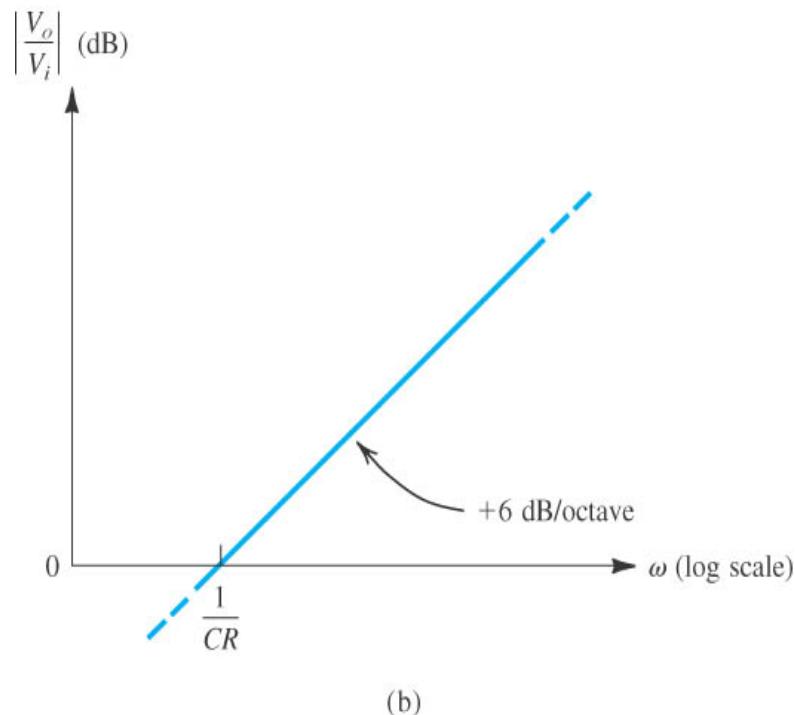


Rf/Xc- unstable  
High freq noise susceptible

# Differentiator

Output voltage,

$$v_0 = -R_2 C_1 \frac{dv_I}{dt}$$



Differentiator circuit

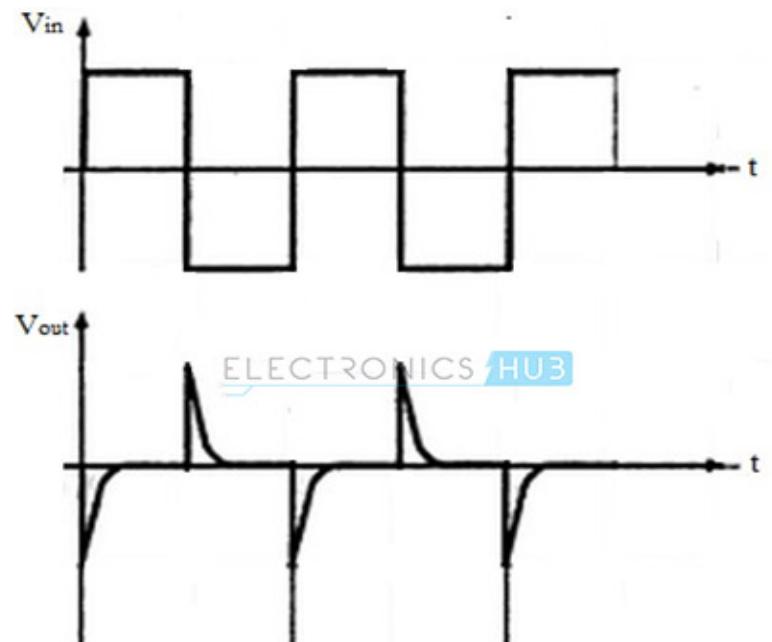
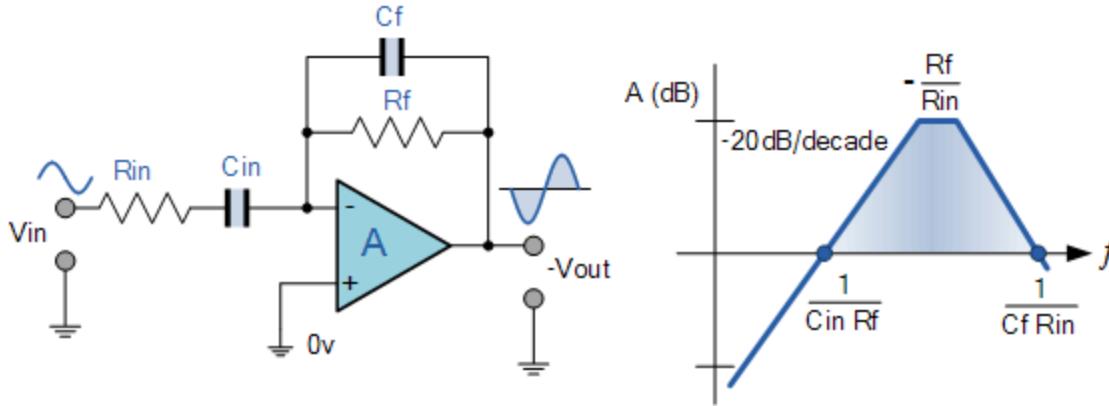


Fig: Input and Output waveforms for Square wave

- For an ideal differentiator, the gain increases as frequency increases. Thus, at some higher frequencies, the differentiator may become unstable and cause oscillations which results in noise.

# Frequency Response of Practical Differentiator

- The gain of the practical differentiator increases with increasing frequency and at a particular frequency,  $f_1$ , the gain becomes the unity (0 dB). The gain continues to increase at a rate of 20dB per decade till the input frequency reaches a frequency,  $f_2$ .
- Beyond this frequency of the input signal, the gain of the differentiator starts to decrease at a rate of 20dB per decade. This effect is due to the addition of the resistor  $R_1$  and capacitor  $C_f$ . The frequency response curve of a practical differentiator is as shown in the figure below.
- in order to reduce the overall closed-loop gain of the circuit at high frequencies, an extra resistor,  $R_{in}$  is added to the input



Adding the input resistor  $R_{in}$  limits the differentiator's increase in gain at a ratio of  $R_f/R_{in}$ . The circuit now acts like a differentiator amplifier at low frequencies and an amplifier with resistive feedback at high frequencies, giving much better noise rejection. Additional attenuation of higher frequencies is accomplished by connecting a capacitor  $C_f$  in parallel with the differentiator feedback resistor,  $R_f$ . This then forms the basis of an Active High Pass Filter.

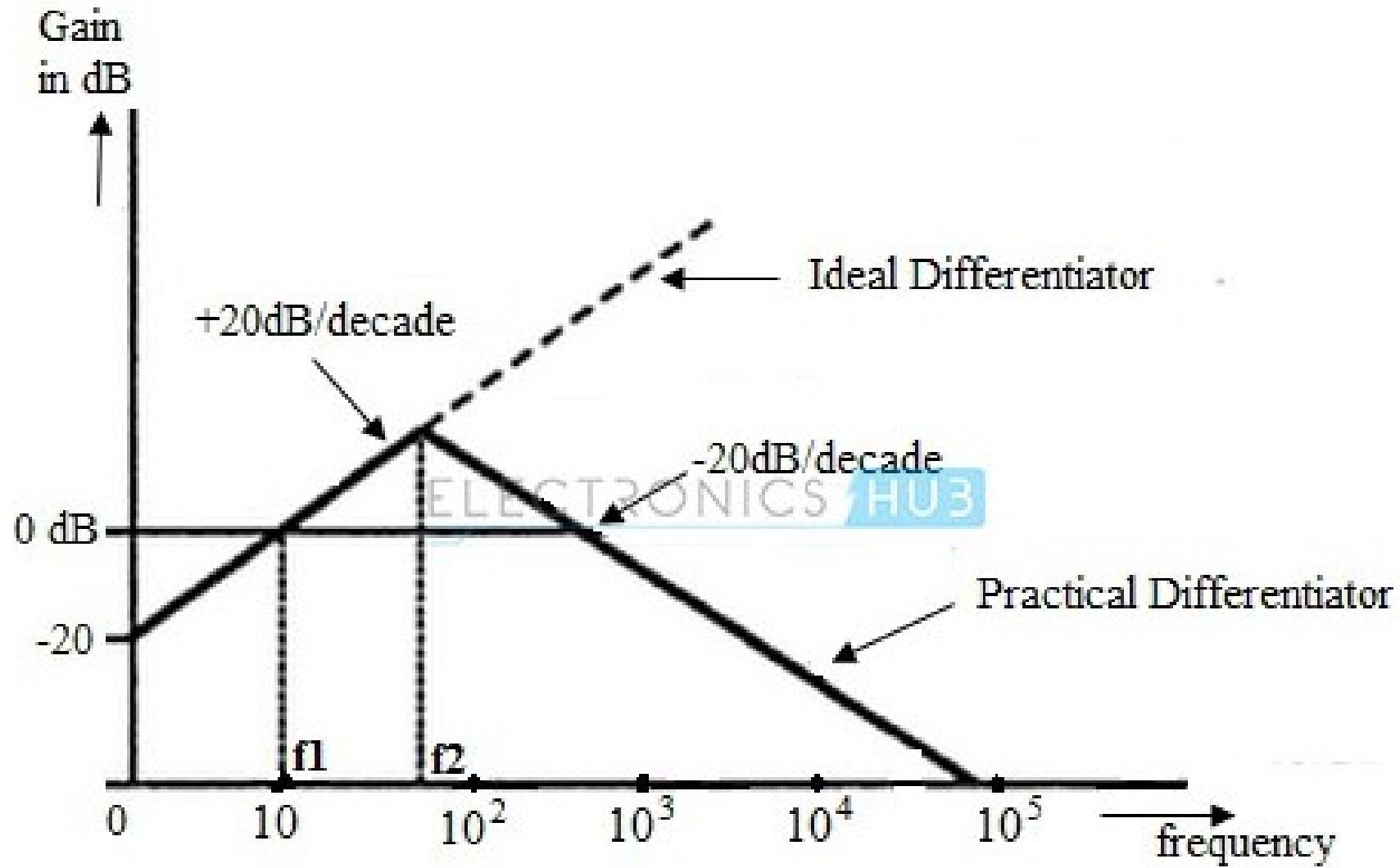
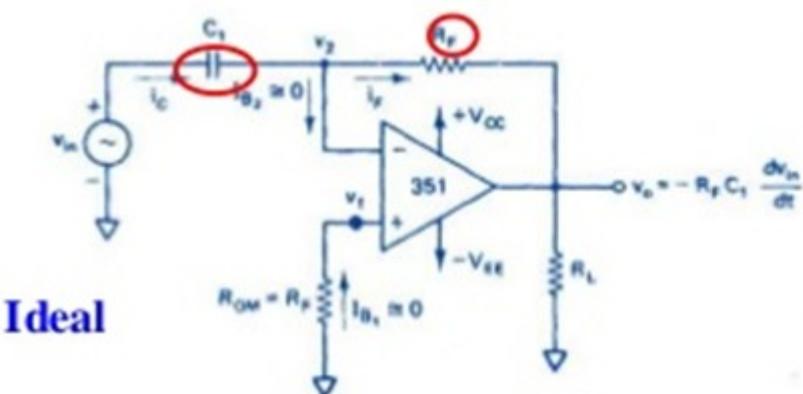


Fig: Frequency Response of Practical Differentiator

# Differentiator Circuit

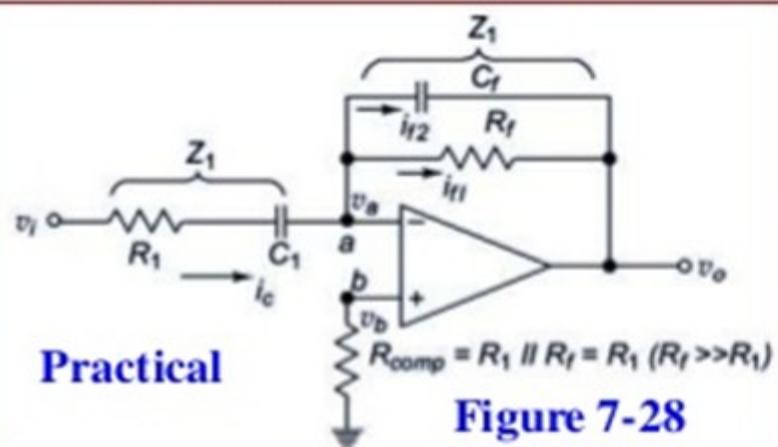


$$f_a = \frac{1}{2\pi R_F C_1}$$

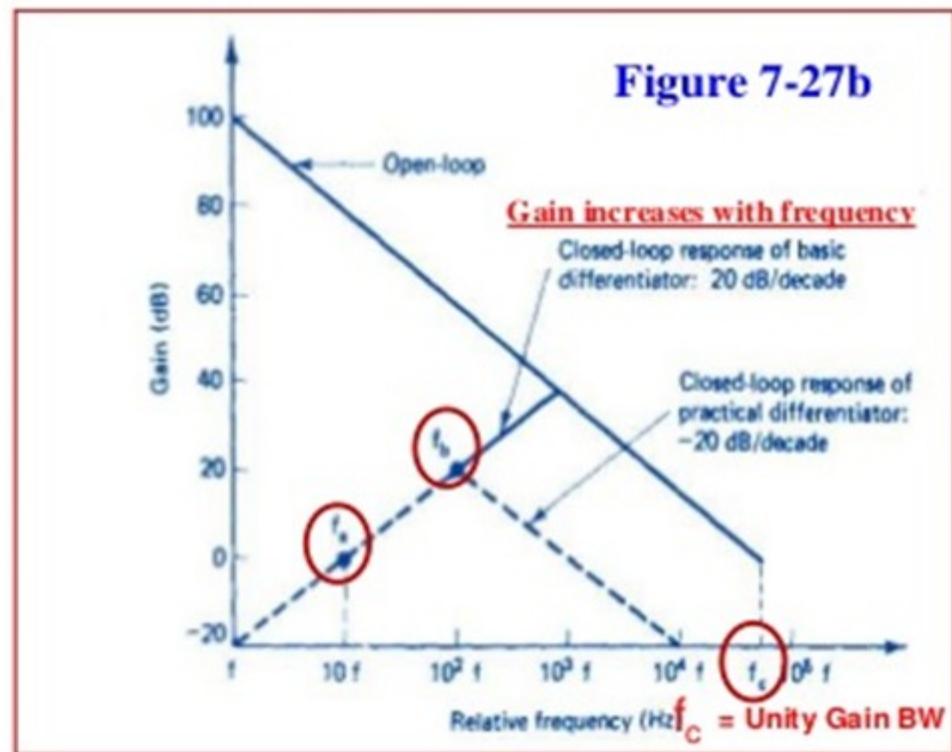
$$f_b = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_F C_F}$$

**f<sub>c</sub> = Unity Gain BW**

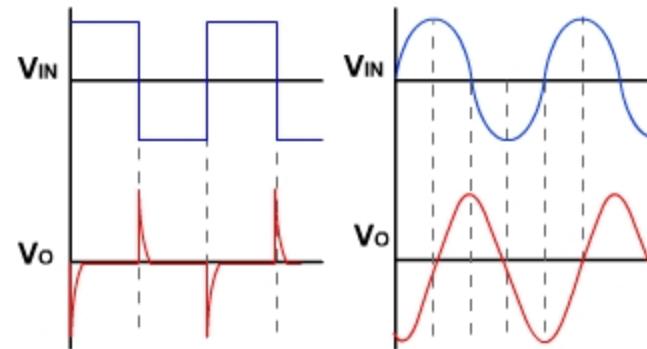
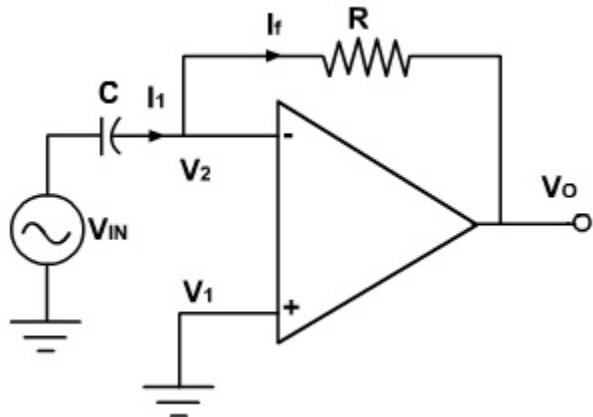
**Figure 7-27** Basic differentiator, (a) Circuit, (b) Frequency response.



**Figure 7-28**



# Ideal Differentiator



The expression for the output voltage can be obtained from the Kirchoff's current equation written at node  $v_2$ .

Since,

$$i_{in} = i_f$$

Therefore,  $C \frac{d}{dt}(V_{in} - 0) = \frac{0 - V}{R}$

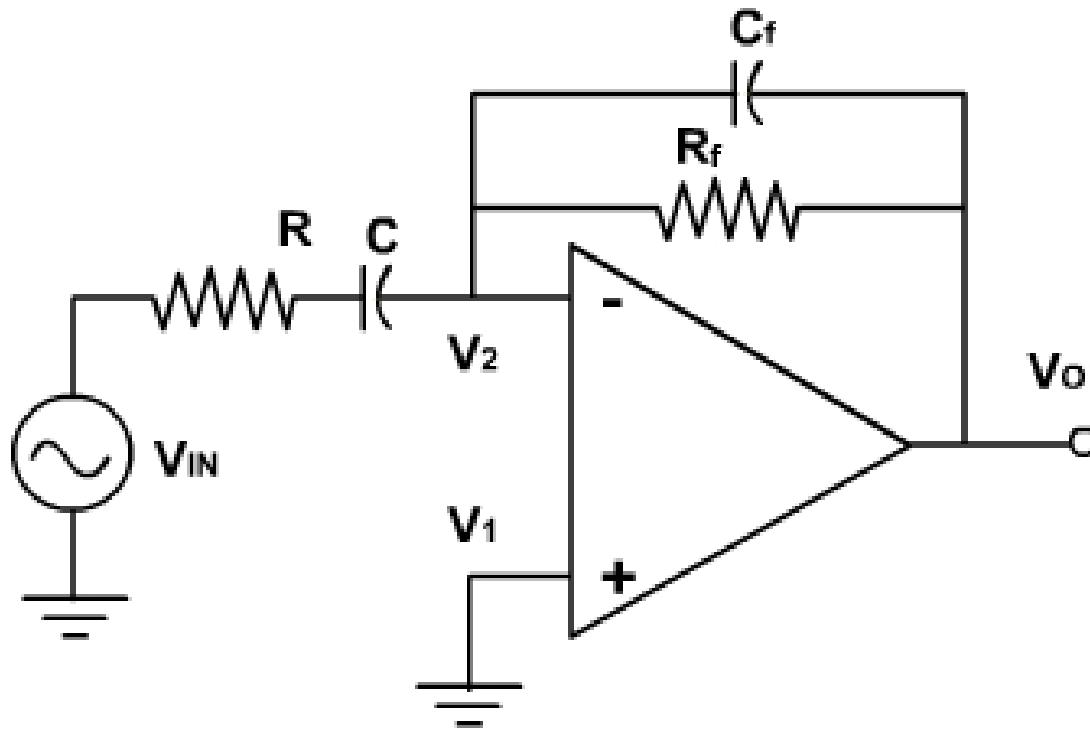
$$V_o = -RC \frac{dV_{in}}{dt}$$

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to  $R_f C$ .

$$T \geq R_f C$$

As the frequency changes, the gain changes. Also at higher frequencies the circuit is highly susceptible at high frequency noise and noise gets amplified. Both the high frequency noise and stability problem can be corrected by adding, few components.

# Practical Differentiator



# Limitations of Differentiator

- Limitations are due to noise, stability and input impedance.
- In order to minimize noise and aid in stability, a small capacitor is placed in parallel with feedback resistor which will reduce high frequency gain.
- In order to place lower limit on the input impedance, a resistor may be connected in series with a differentiating capacitor
- The gain of practical differentiator circuit is reduced significantly and this avoids the high frequency noise and results in better stability.

# Applications of Differentiators

- In wave shaping circuits to detect high frequency components in an input signal
- As a rate of change detector in FM modulators.

# Design Steps of differentiators

- Select  $F_a = \text{highest freq of the input signal to be differentiated}$ , choose  $C_1 < 1\text{ microfarad}$ , calculate RF
- Choose  $f_b = 20f_a$ , calculate  $R_1$  and  $C_F$  so that  $R_1C_1 = R_1C_F$

- Design a differentiator to differentiate an input signal that varies in the frequency from 10Hz to about 1 KHz
- Sol:

1.  $F_a = 1\text{KHZ}$

$$f_a = \frac{1}{2\pi R_F C_1}$$

• Let  $C_1 = 0.1\text{microF}$ ,  $R_F = 1.59\text{Kohm} = 1.5\text{kohm}$

2.  $F_b = 20\text{kHz}$

$$f_b = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_F C_F}$$

$R_1 = 79.5\text{ohm} = 82\text{ ohm}$ .  $R_1 C_1 = R_F C_F$

$C_F = 0.0055\text{microfarad}$

$R_{out} = R_F = 1.5\text{kohm}$

## Calculating Gain and Design Questions

### INVERTING

$$\text{Voltage gain, } A_v = \frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

### NON - INVERTING

$$\text{Voltage gain, } A_v = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$$

## Calculating Output and Design Questions

### SUMMING AMPLIFIER

Output voltage

$$V_o = -R_F \left( \frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} + \frac{V_{i3}}{R_3} \right)$$

### INTEGRATOR AMPLIFIER

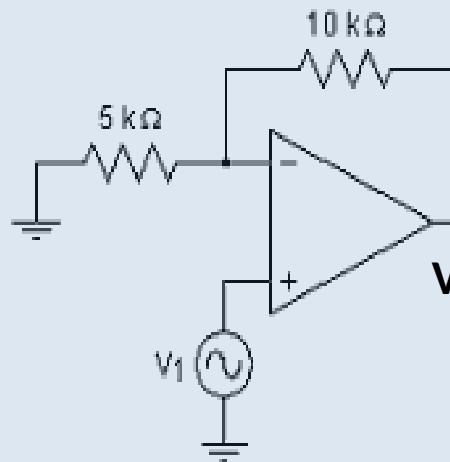
### DIFFERENTIATOR AMPLIFIER

$$\text{Output voltage, } v_o = -R_2 C_1 \frac{dv_I}{dt}$$

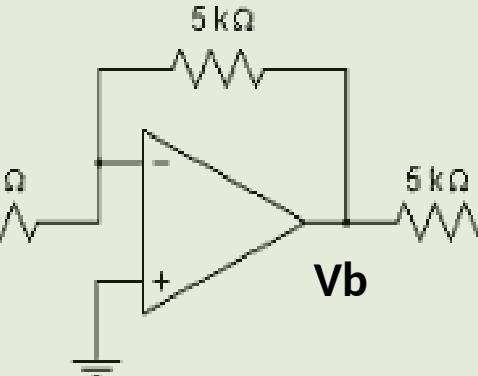
$$\text{Output voltage, } v_o = -\frac{1}{R_1 C_2} \int v_I dt$$

If the capacitor has some initially voltage,  $V_C$

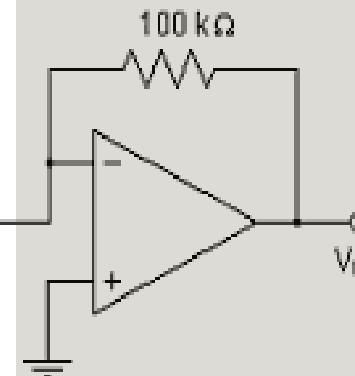
$$v_o = V_C - \frac{1}{R_1 C_2} \int v_I dt$$



NON - INVERTING



INVERTING



INVERTING

Calculate the input voltage if the final output,  $V_o$  is 10.08 V.

**Finally:**

$$V_a = (1 + 10/5) V_1$$

$$0.504 = 3V_1$$

$$\underline{V_1 = 0.168 \text{ V}}$$



**Then:**

$$V_b = -(5/5) V_a$$

$$-0.504 = -V_a$$

$$V_a = 0.504 \text{ V}$$

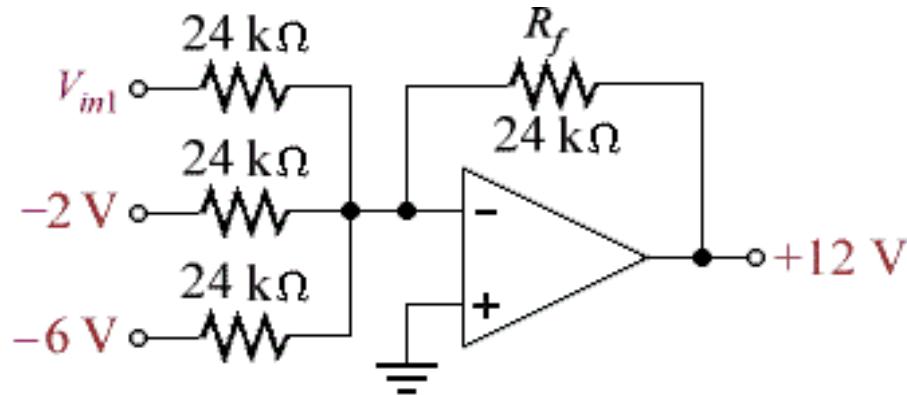


**Have to work backwards:**

$$V_o = -(100/5) V_b$$

$$10.08 = -20 V_b$$

$$V_b = -0.504 \text{ V}$$



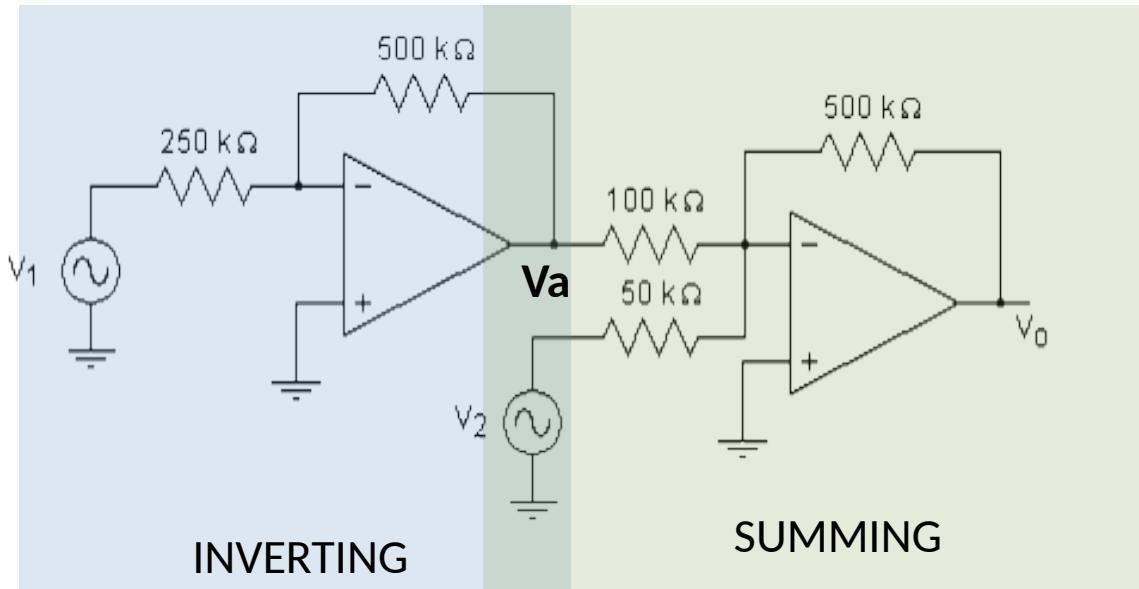
What is the value of  $V_{in1}$  from the figure above?

$$12 = -24 [ V_{in1} / 24 + (-2) / 24 + (-6) / 24 ]$$

$$12 = - [ V_{in1} - 2 - 6 ]$$

$$12 = - V_{in1} + 2 + 6$$

$$\underline{V_{in1} = -4 \text{ V}}$$



Calculate the output voltage,  $V_o$  if  $V_1 = V_2 = 700 \text{ mV}$

$$Va = -(500/250) 0.7$$

$$V_a = -1.4 \text{ V}$$

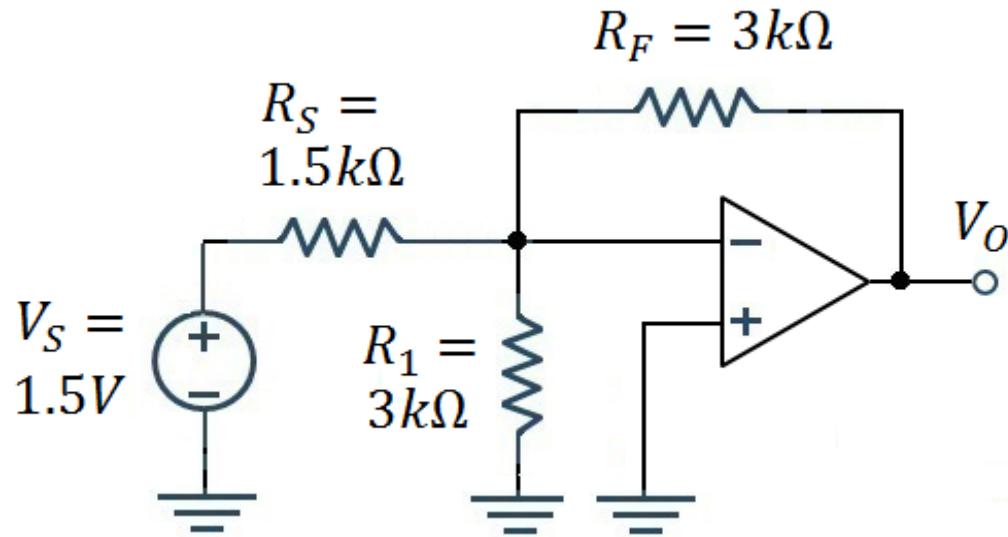


**Then:**

$$V_o = -500 [ V_a / 100 + V_2 / 50 ]$$

$$V_o = -500 \left[ -1.4 / 100 + 0.7 / 50 \right]$$

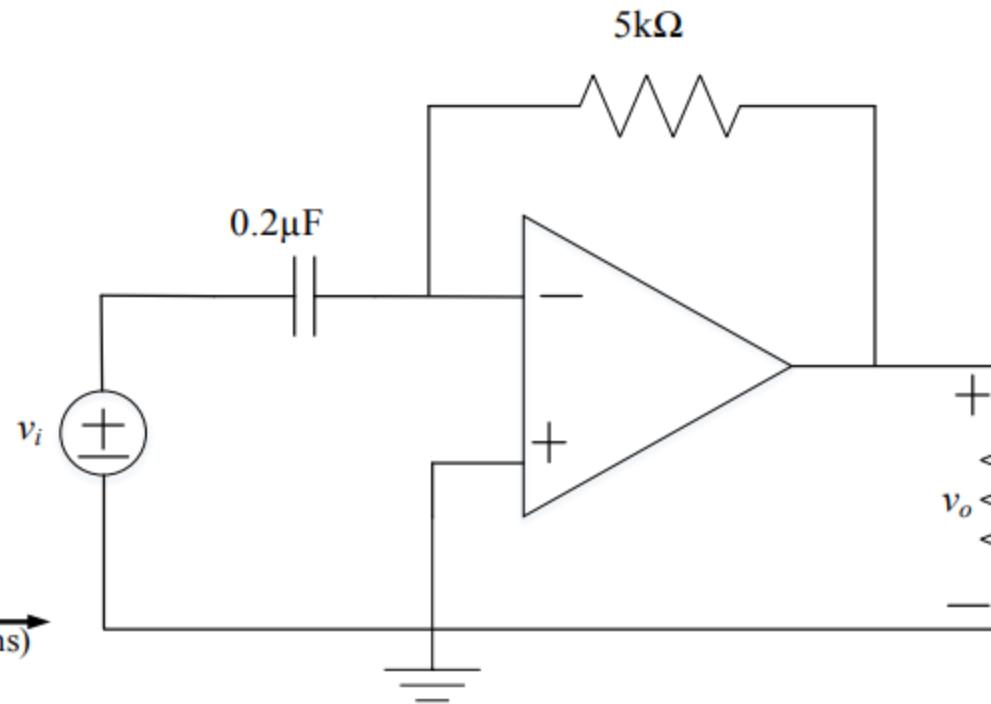
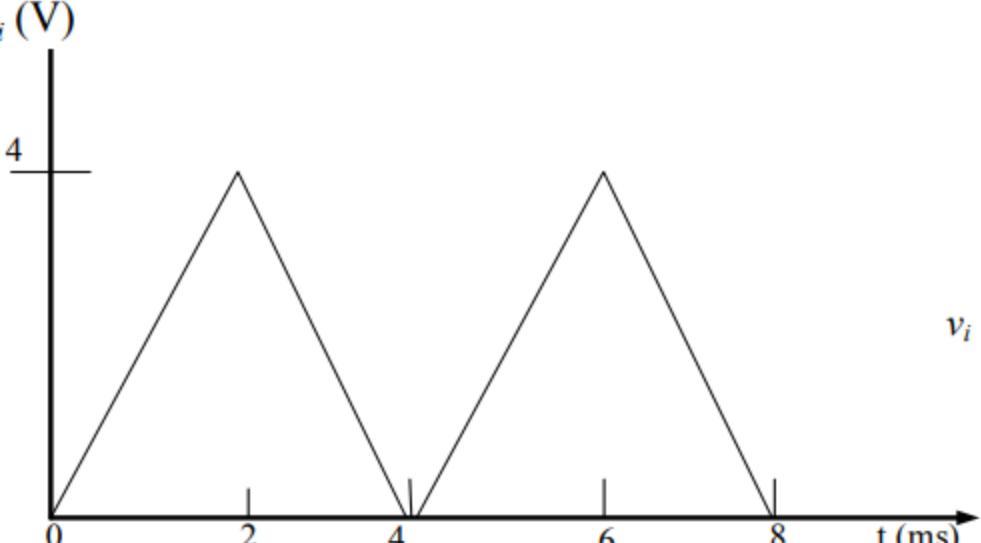
$$V_o = 0 \text{ V}$$



Calculate the output voltage  $V_o$  of the operational amplifier circuit as shown in the figure.

**week 10 assignment**  
[https://nptel.ac.in/courses/108108111/W10A1  
.pdf](https://nptel.ac.in/courses/108108111/W10A1.pdf)

- Sketch the output voltage waveform  $v_o(t)$  for the circuit shown, given the input voltage waveform below



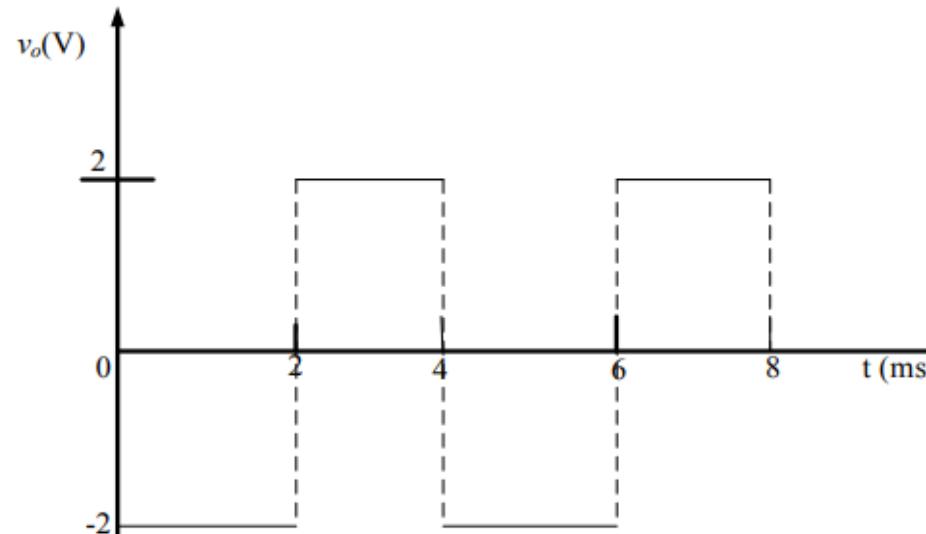
**Soln:** The time constant is  $RC = 5 \times 10^3 \times 0.2 \times 10^{-6} = 10^{-3} s$

Input voltage is given by,

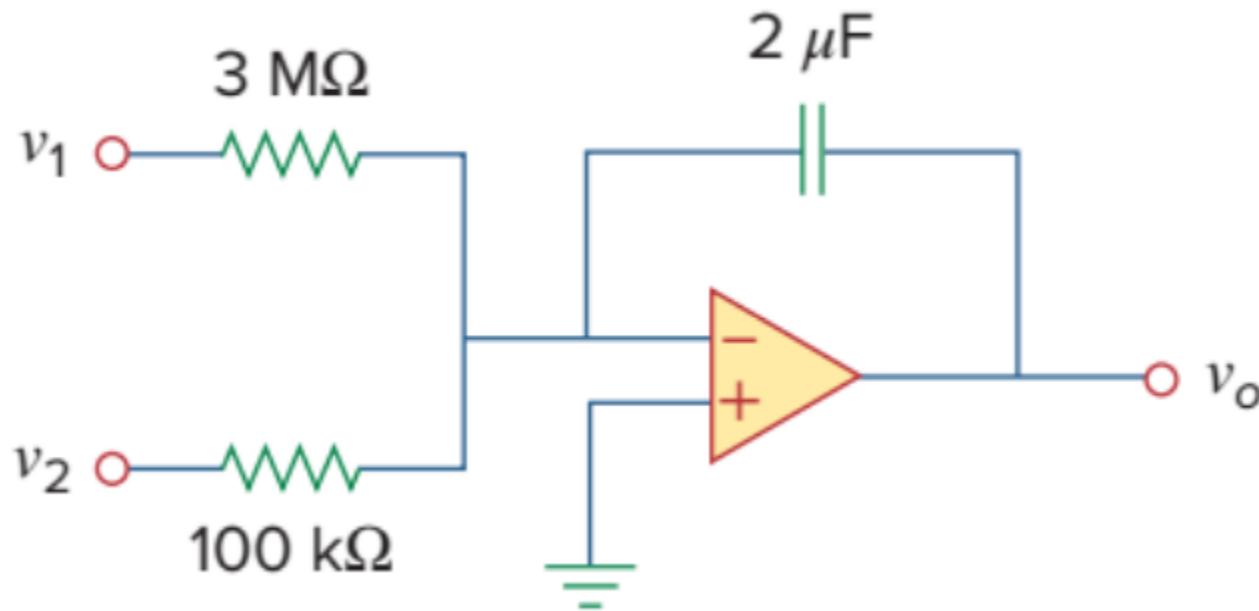
$$v_i = \begin{cases} 2000t & ; \quad 0 < t < 2 \text{ ms} \\ 8 - 2000t & ; \quad 2 < t < 4 \text{ ms} \end{cases}$$

Thus, the output voltage is given as,

$$v_o = -RC \frac{dv_i}{dt} = \begin{cases} -2V & ; \quad 0 < t < 2\text{ms} \\ 2V & ; \quad 2 < t < 4\text{ms} \end{cases}$$



If  $v_1(t) = 10\cos(2t)$  mV and  $v_2(t) = 0.5t$  mV below, find  $v_o(t)$  for  $t > 0$ . Assume that the voltage across the capacitor is zero at  $t = 0$ .



- the output voltage is

$$v_o = -\frac{1}{R_1 C} \int v_1 dt - \frac{1}{R_2 C} \int v_2 dt$$

$$\Rightarrow v_o = \frac{1}{3*10^6 * 2*10^{-6}} \int_0^t 10 \cos(2\tau) d\tau - \frac{1}{100*10^3 * 2*10^{-6}} \int_0^t 0.5\tau d\tau$$

$$v_o = -\frac{1}{6} \frac{10}{2} \sin 2t - \frac{1}{0.2} \frac{0.5t^2}{2}$$

$$v_o = -0.833 \sin 2t - 1.25t^2 mV$$

# *Analog and Digital Integrated Circuits*

**EE- ECE2011A**



# Unit III

# Non-Linear Applications

# Lesson Plan

Topic	Sub points	Book-Page Nos.
Voltage Comparator	Inverting,Non inverting ,Characteristics,Voltage Limiters	T1-315
Schmitt Trigger-Inverting	Working,transfer curve	T1-317 , R1-218
Schmitt Trigger-Non-Inverting	Just explaination	R1-317
Voltage Limiters	Working	T1-351
Precision Rectifier,Half wave	Saturating and non saturating working ,waveforms,	T1-240, R1-163
Precision Full wave Rectifiers	Working ,waveforms	R1-167
Square Wave Generator,Triangular Wave	Working	T1-287

# Non Linear Applications

- High gain Amplifier with positive feedback or without feedback- it operates in  $\pm V_{sat}$
- This is called as bistable behavior of Op-Amp and it is highly non linear.

# Important Concepts

Comparator

Schmitt  
Triggers

Waveform  
Generators

With help of  
Diode

Precision  
Rectifiers

Clippers /  
Clampers

Peak Detector /  
Sample and Hold

# What is a Comparator??

- Its input is analog and its output is digital (1/0 or high/low).
- It is a one-bit Analog-to-Digital Converter (ADC) .
- The output changes its state when the input voltage crosses a reference value.

# Types of Comparators

- Inverting Type
  - +ve reference or -ve reference
- Non-Inverting Type
  - +ve reference or -ve reference
- Zero Crossing Detector
  - Zero Reference. Switching will happen when input crosses zero level.

## Comparator

An analog comparator has two inputs one is usually a constant reference voltage  $V_R$  and other is a time varying signal  $v_i$  and one output  $V_o$ .

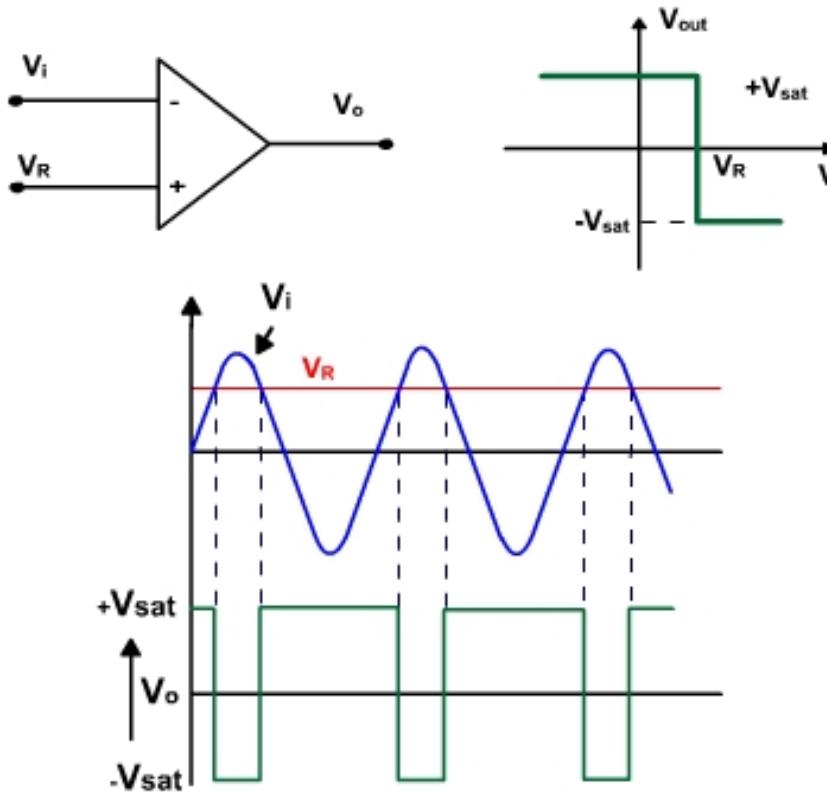
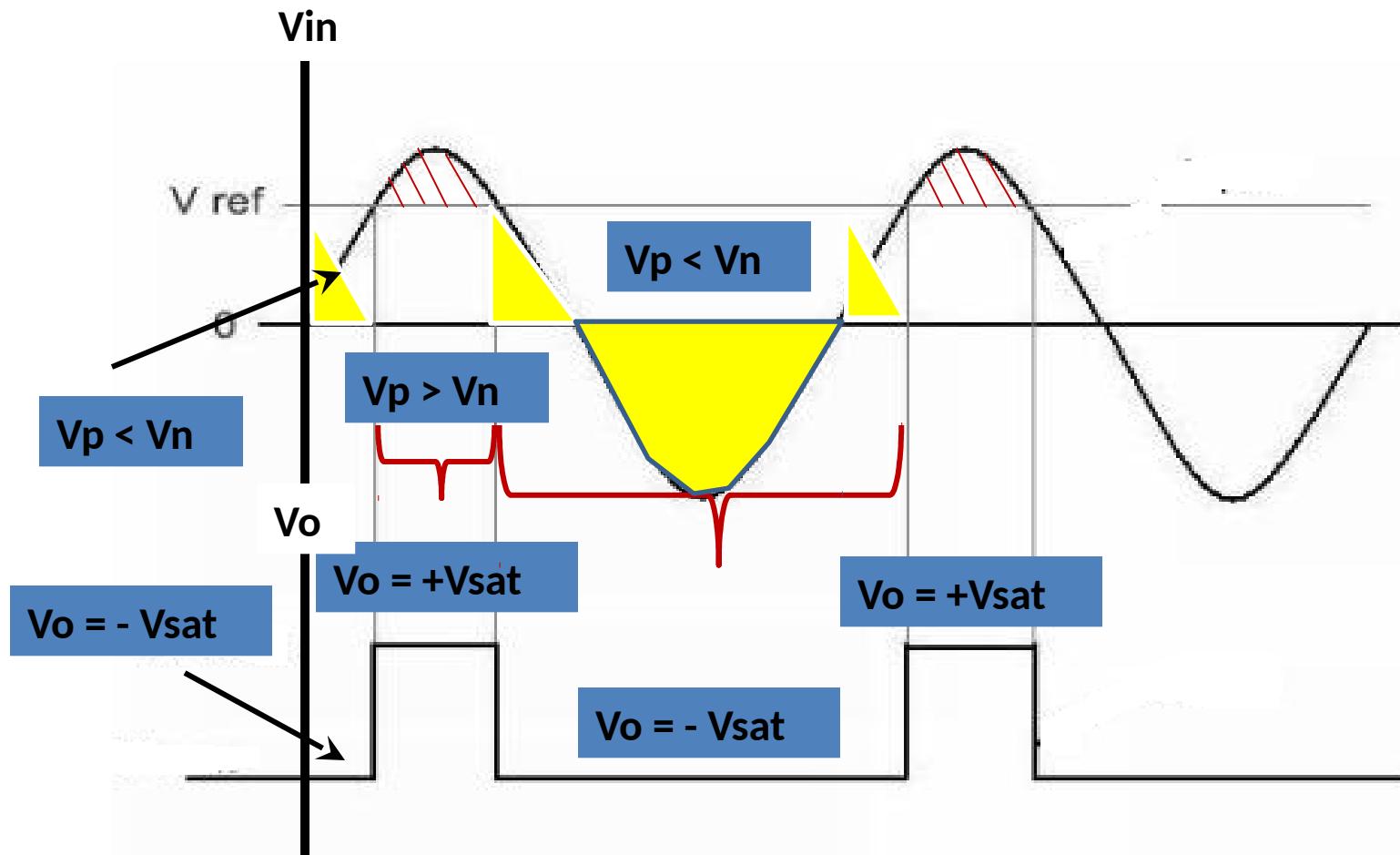


Figure 1

# Comparator Waveforms



# Working

When the noninverting voltage is larger than the inverting voltage the comparator produces a high output voltage ( $+V_{sat}$ ). When the non-inverting output is less than the inverting input the output is low ( $-V_{sat}$ ).

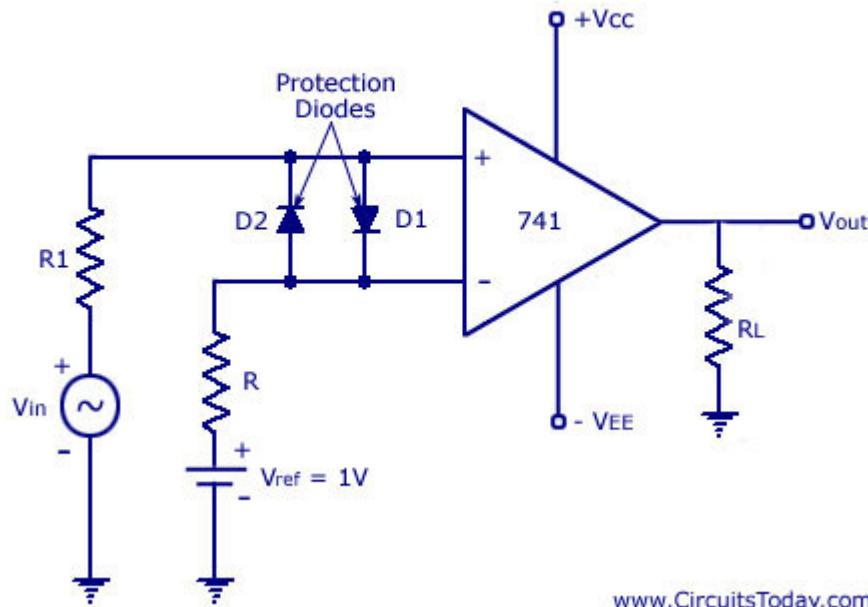
**Fig 1,** also shows the output of a comparator for a sinusoidal input is

- $V_o = -V_{sat}$  if  $v_i > V_r$
- $V_o = +V_{sat}$  if  $v_i < V_r$

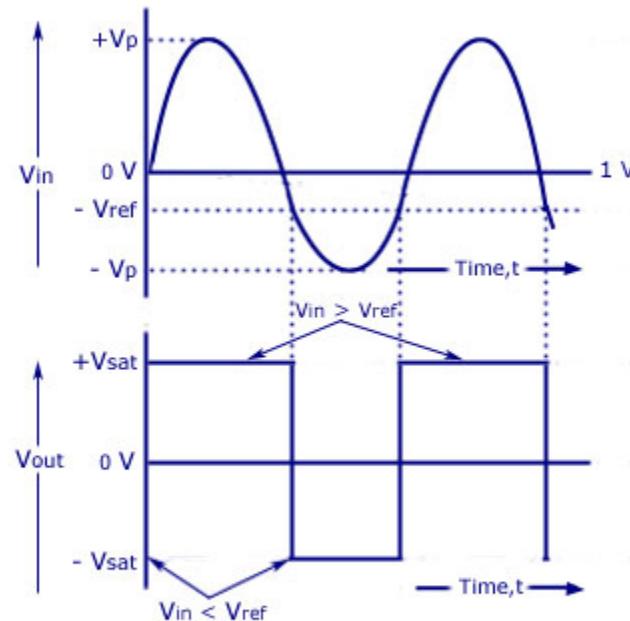
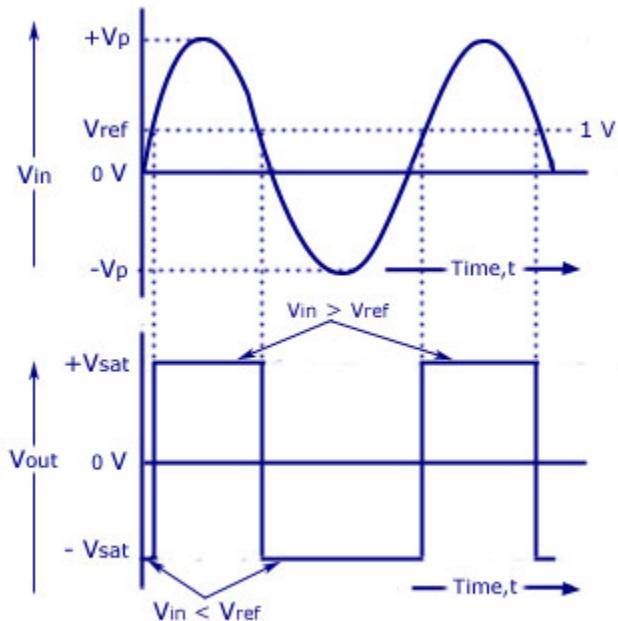
# Non-Inverting Type

- +Reference
- -reference
- Waveforms
- Transfer characteristics
- Diodes D1 and D2 protect the Op-Amp from damage due to excessive input voltage Vin- Clamp diodes
- R in series with vin is used to limit the current through the diodes
- $R_{out} \approx R$  is connected to inverting terminal to reduce the offset

## Non-Inverting Comparator Circuit



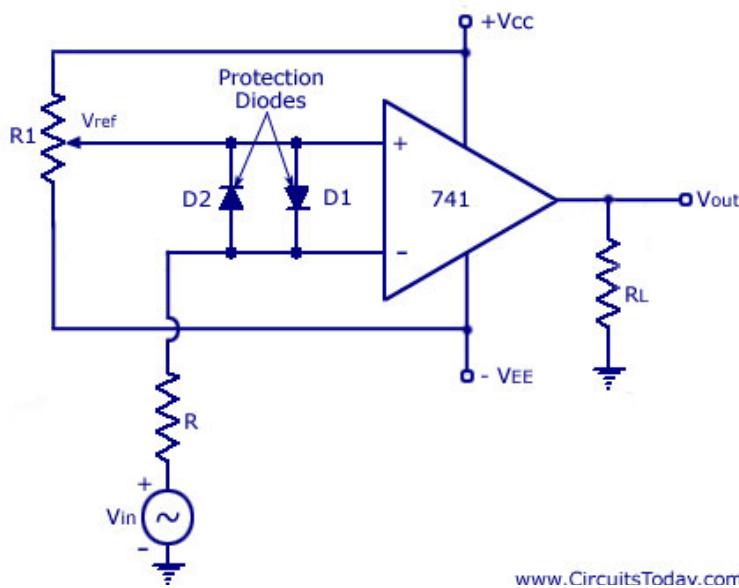
[www.CircuitsToday.com](http://www.CircuitsToday.com)



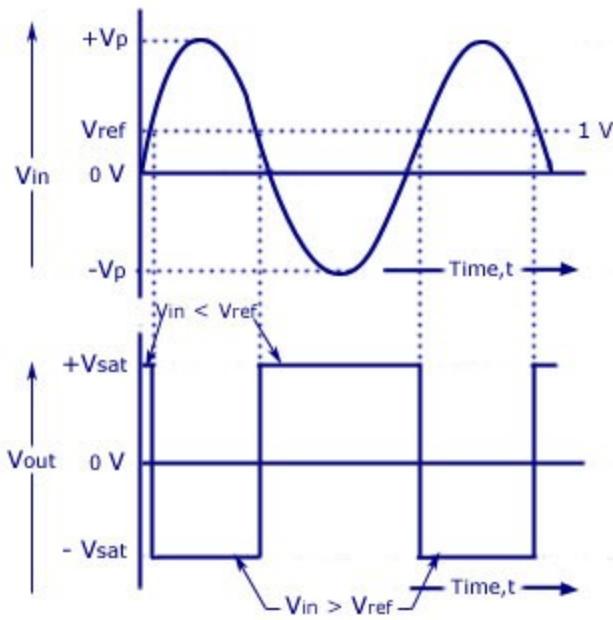
# Inverting Type

- +Reference
- -reference
- Waveforms
- Transfer characteristics

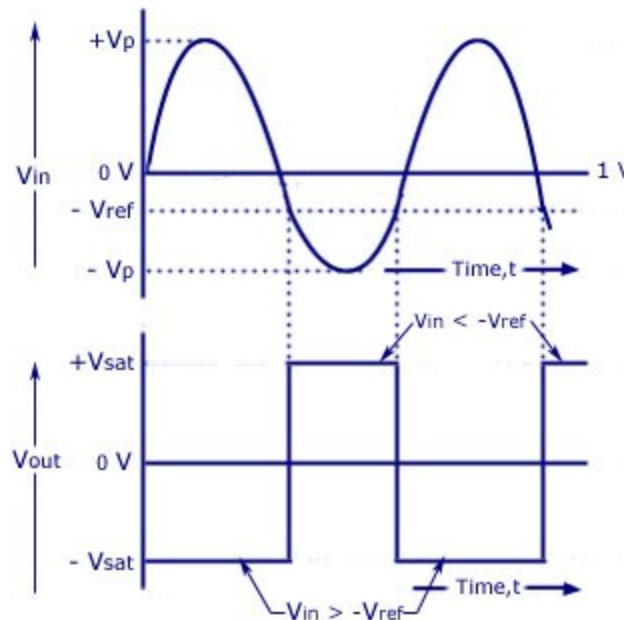
## Inverting Comparator Circuit



[www.CircuitsToday.com](http://www.CircuitsToday.com)



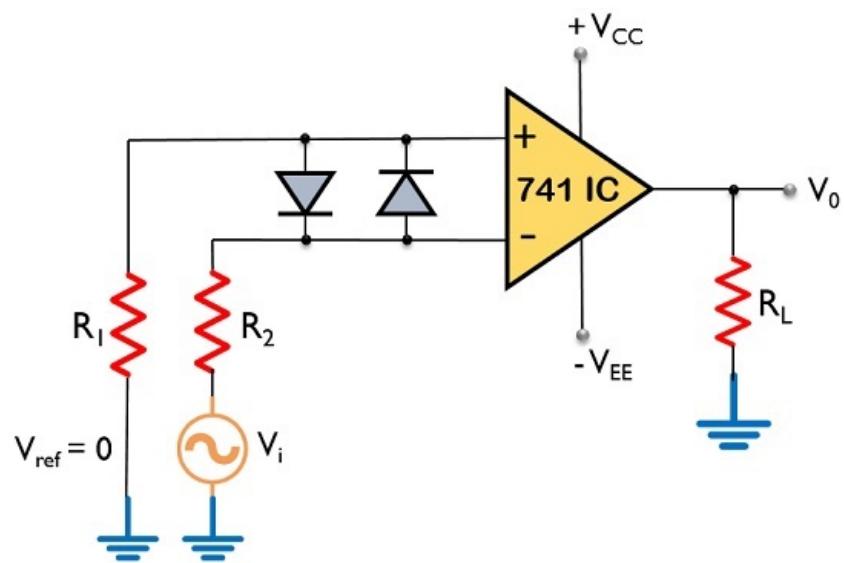
**Input and Output Waveforms  
For Positive Vref**



**Input and Output Waveforms  
For Negative Vref**

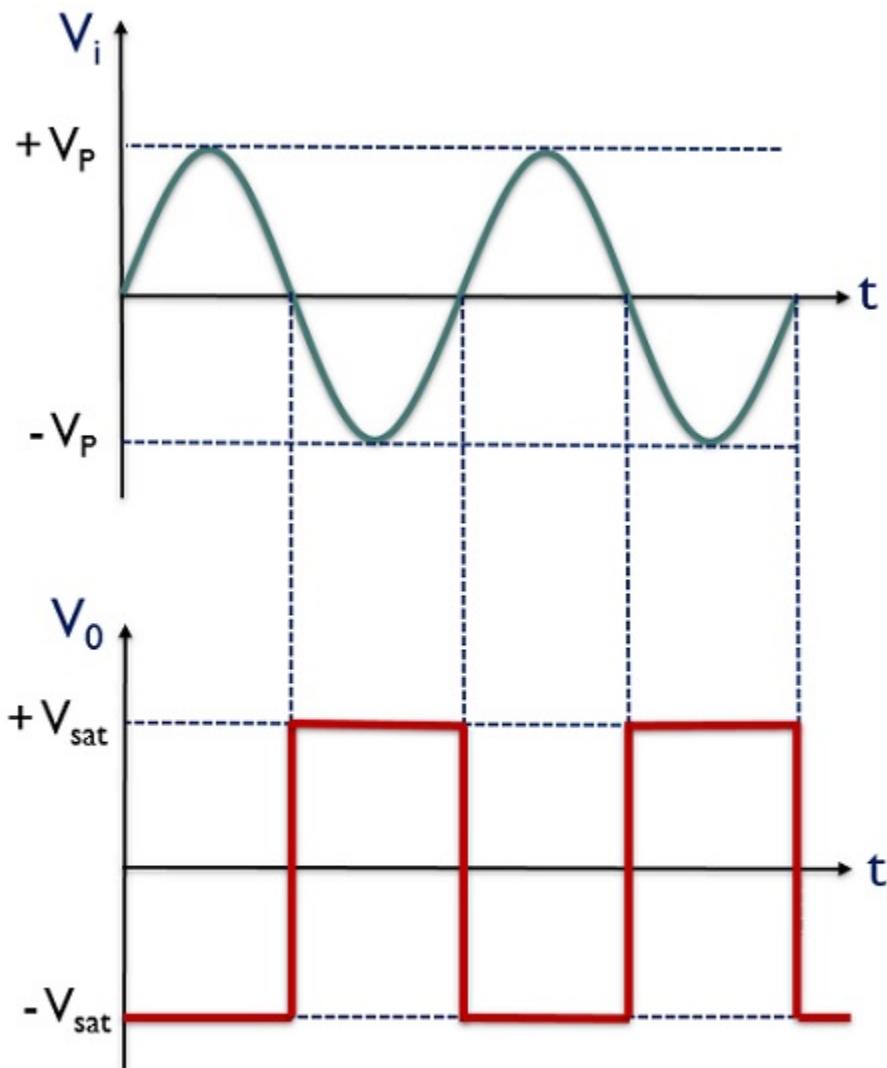
# Zero Crossing Detector

- Reference voltage is zero
- Waveforms



**Circuit Diagram of Zero-Crossing Detector**

Electronics Coach



**Input and Output Waveforms**

Electronics Coach

# Comparator Characteristics

- Speed of Operation: switching speed, high slew rate is required
- Accuracy: it depends on voltage gain, CMRR, input offset, thermal drift
- Compatibility of output with any digital family

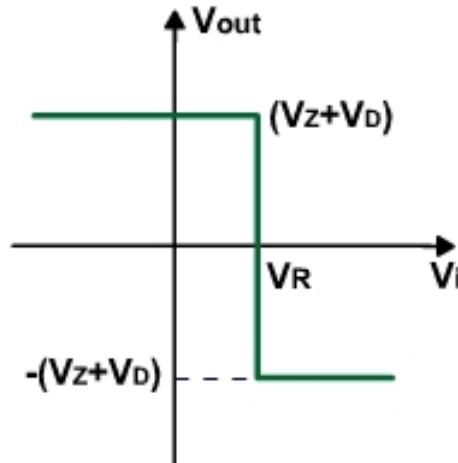
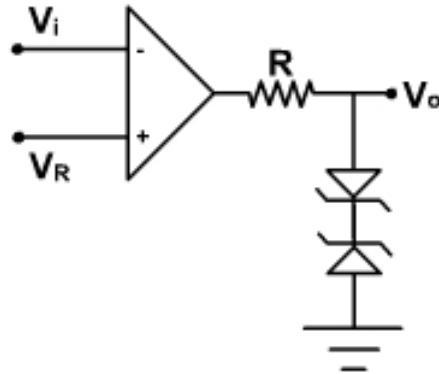
\*\*Compensated Op-Amp (IC 741): Internal capacitor for stabilization, capacitor slows down rate of change of output

Un compensated Op-Amp(IC 301): Don't have internal capacitor , so output rises at a much faster speed as compared with compensated Op-amp

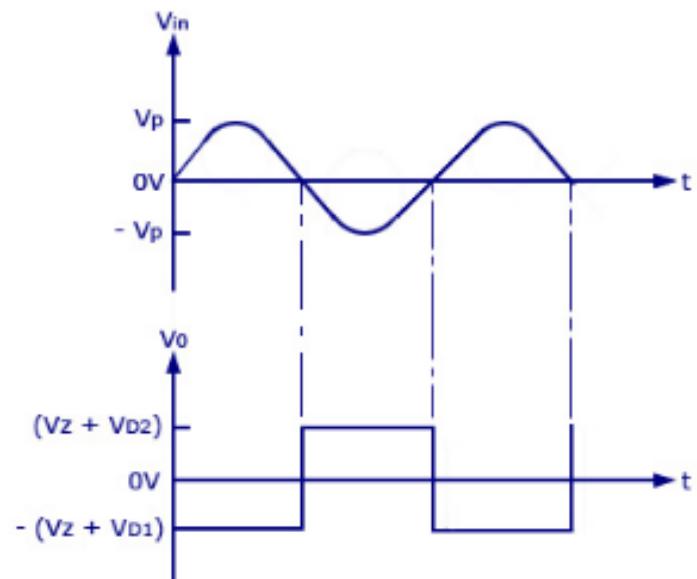
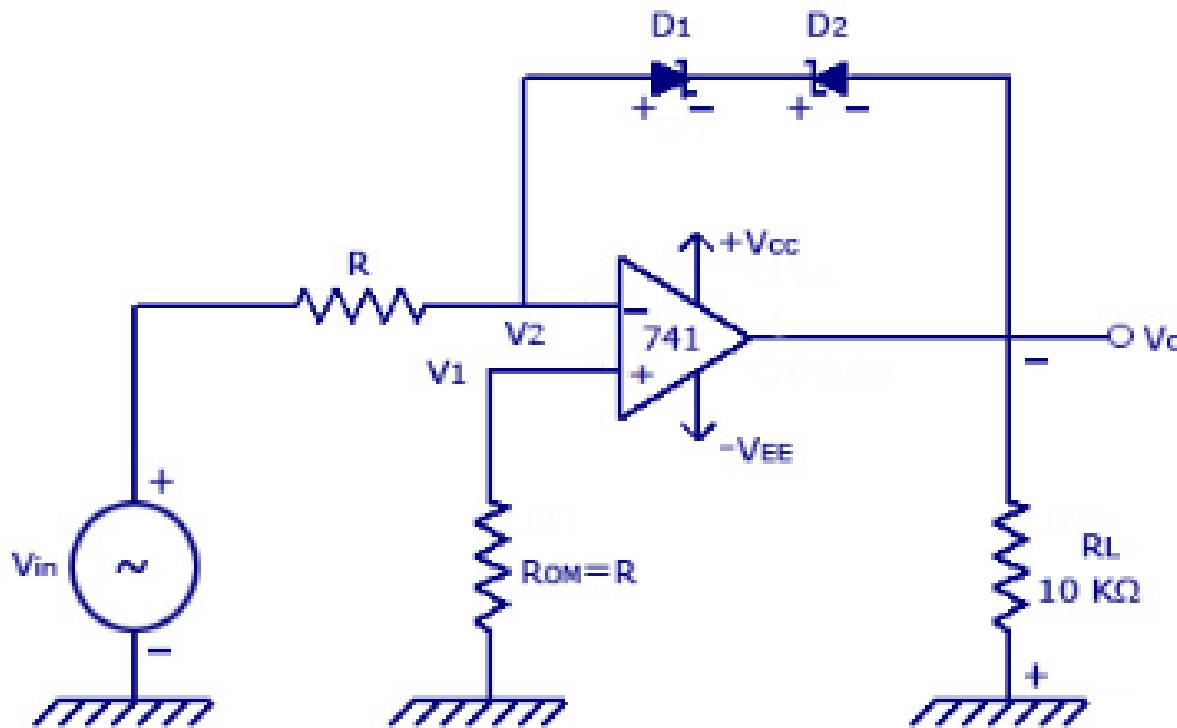
Comparator Ics: LM 339, LM 311

# Voltage Limiters

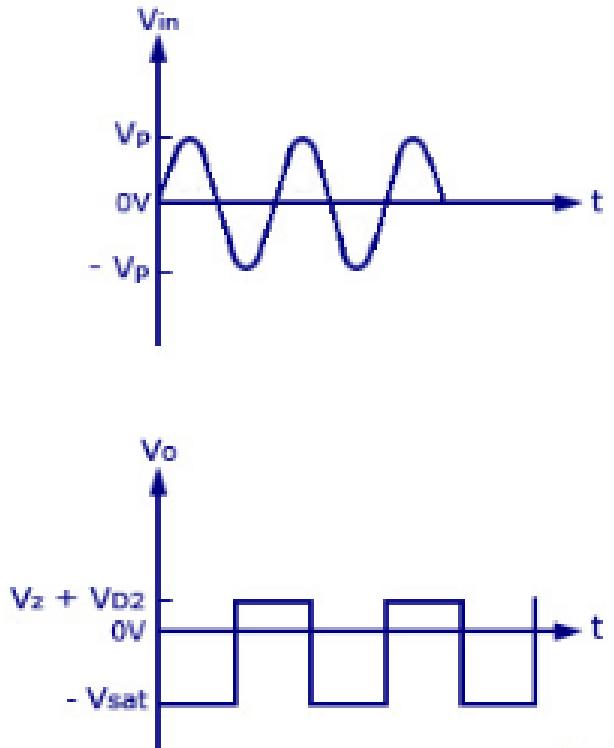
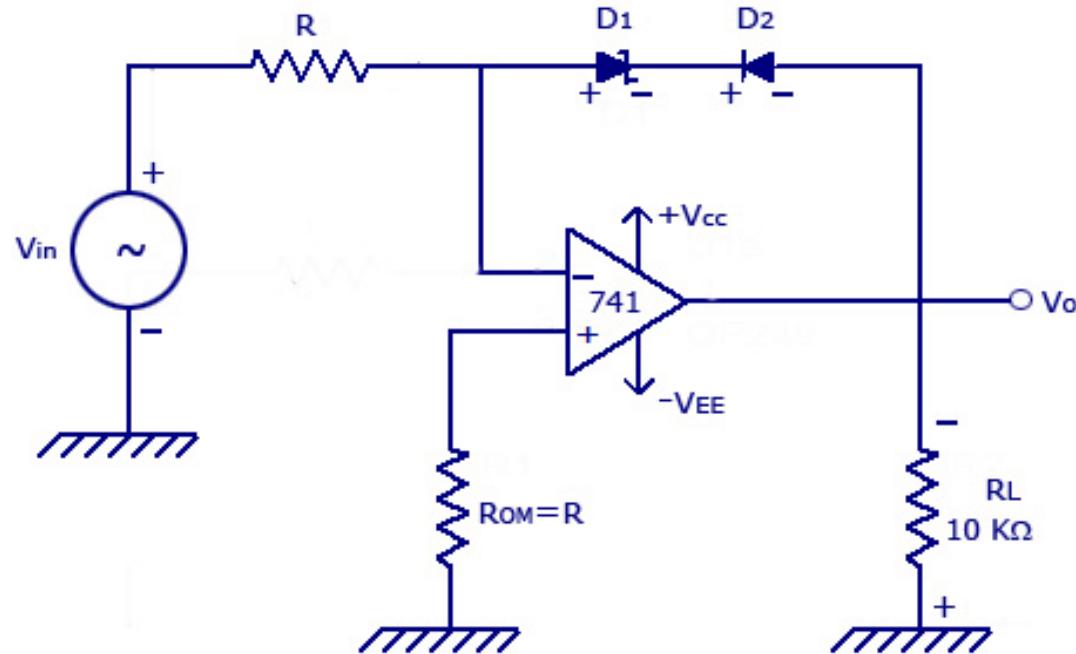
If we want to limit the output voltage of the comparator two voltages (one positive and other negative)then a resistor R and two zener diodes are added to clamp the output of the comparator. The circuit of such comparator is shown in Fig, The transfer characteristics of the circuit is also shown below



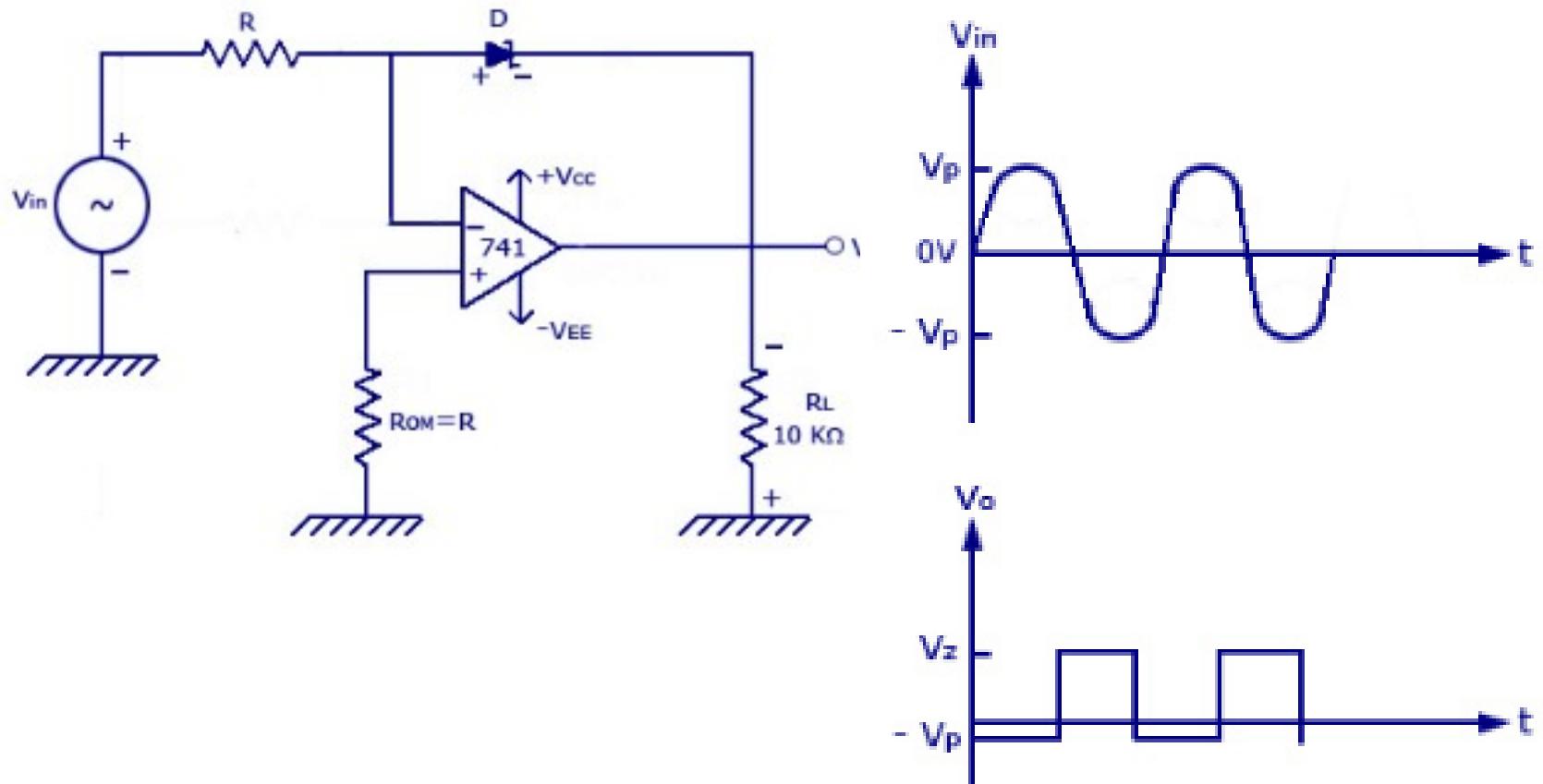
# Voltage Limiters with zener diodes



The figure below shows a combination of zener diode and rectifier diodes: Positive output voltage Limiting



# Voltage Limiter with single zener diode



# Comparator Applications

1. Level detectors / Window Detectors
  - Automatic Measurement of physical signals and control – Biomedical, Agriculture, Industrial Process Plants etc.
  - Musical Instruments
2. Zero -Crossing Detectors
  - frequency / phase measurement.
3. One bit ADC / PWM generator / Signal generators
  - Communication Systems
4. Switching Regulators
  - Power Supplies

# Comparator ICs

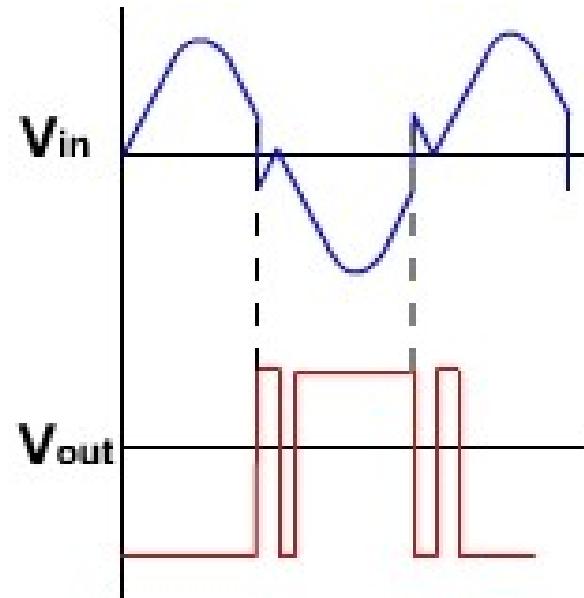
- LM311 / LM339.
- Open collector output:- Pull up resistor is necessary.
- Can work on Single Power Supply.

- \*\***741**- compensated- internal C- it slows down the rate of change of output
  - Slew rate is 0.5V/microsec
- \*\***301**-uncompensated- no C- output rises much faster
  - Slew rate is higher than compensated op amp

**Uncompensated Ics are used as comparator**

## Noise in Zero Crossing Detector

If Noise exists near ground level it can create false triggering and cause chattering of relay.



So give positive feedback to comparator and improve noise immunity. Such a regenerative comparator is called **Schmitt Trigger**.

# Noise Immunity

- Inherent but very small ‘*hysteresis!*’
- False triggering due to noise!
- Use offset minimizing techniques.
- Select op-amp with very small offset voltage.
- Use Positive feedback.

# Schmitt Trigger

- If the input to a comparator contains noise, the output may be erratic when  $v_{in}$  is near a trip point.
- For instance, with a zero crossing, the output is low when  $v_{in}$  is positive and high when  $v_{in}$  is negative.
- If the input contains a noise voltage with a peak of 1mV or more, then the comparator will detect the zero crossing produced by the noise.
- Figure 2 shows the output of zero crossing detection if the input contains noise.

# Schmitt Triggers

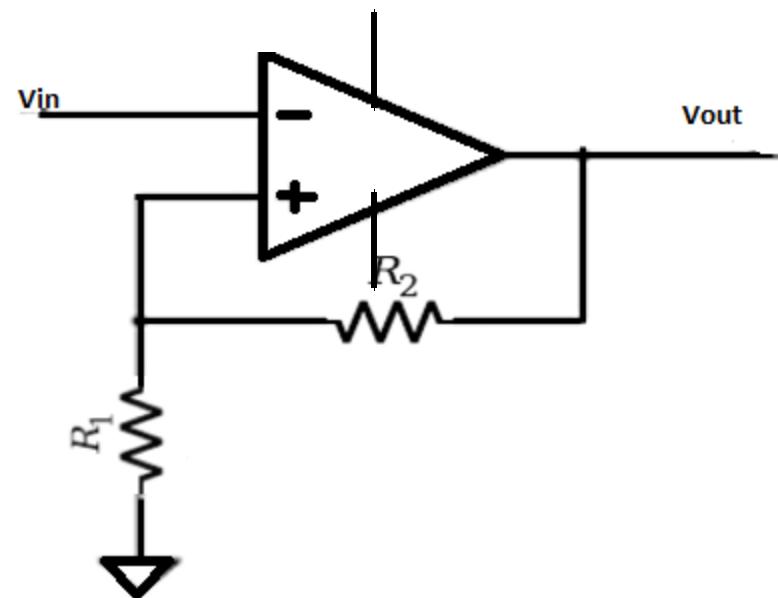


Figure 2

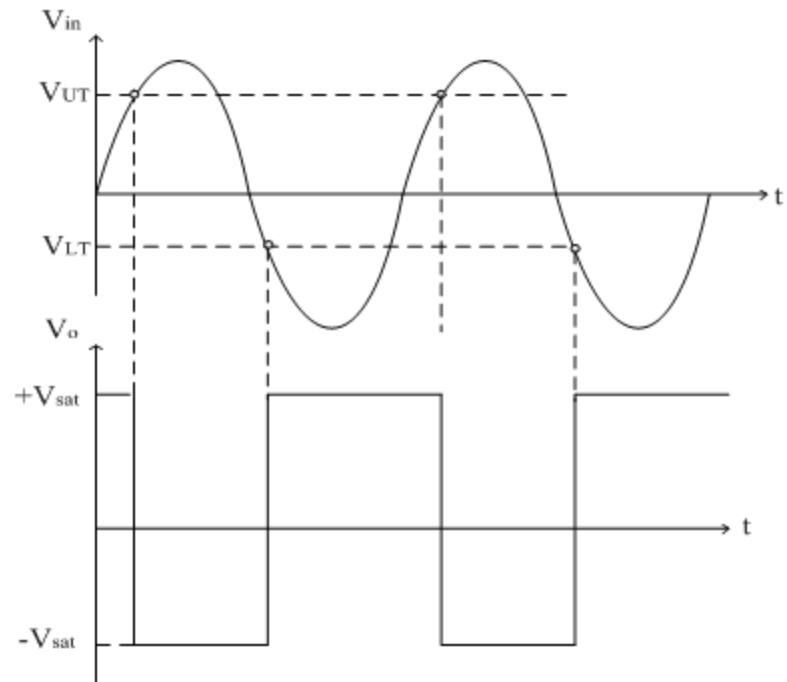


Figure 3

circuit is insensitive to the  
changes in the i/p in this region  
**Hysteresis Width**

## Hysteresis Loop (Transfer Characteristics)

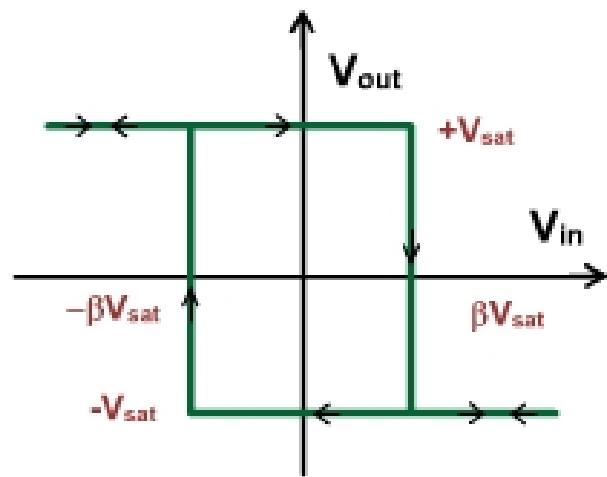


Figure 4

# Noise Immunity

- Inherent but very small ‘*hysteresis!*’
- False triggering due to noise!
- Use offset minimizing techniques.
- Select op-amp with very small offset voltage.
- Use Positive feedback.

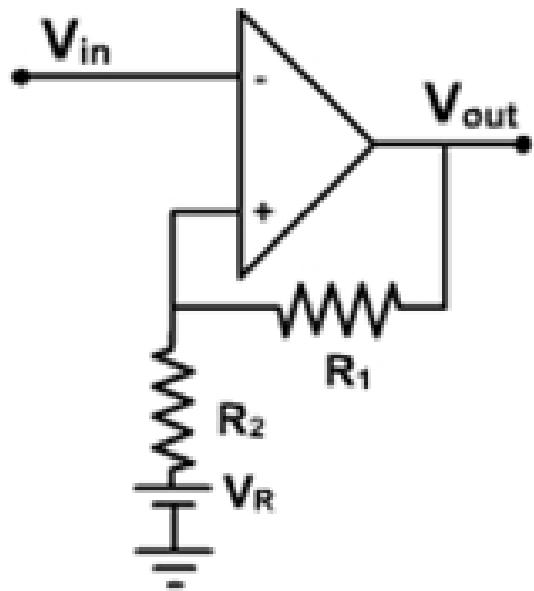
# How to decide threshold voltages?

- $V_{lt}$  and  $V_{ut}$  should be greater than Noise Voltages.
- $R_1$  and  $R_2$  can be selected according to the values of  $V_{lt}$  and  $V_{ut}$ .

# Schmitt Trigger - Types

- **Inverting** and Non-inverting
- Symmetric ( $| V_{lt} | = | V_{ut} |$ )
- Asymmetric ( $| V_{lt} | \neq | V_{ut} |$ )

# Asymmetric ST Using additional Vdc



Applying KVL

$$V_o = I R_1 + I R_2 + V_R$$

$$\therefore I = (V_o - V_R) / (R_1 + R_2)$$

The threshold point

$$V_T = I R_2 + V_R$$

$$V_T = [(V_o - V_R) / (R_1 + R_2)] R_2 + V_R$$

.....(1)

$$V_T = R_2 / (R_1 + R_2) V_o - R_2 / (R_1 + R_2) V_R + V_R$$

$$V_T = R_2 / (R_1 + R_2) V_o + R_1 / (R_1 + R_2) V_R$$

When  $V_{out} = +V_{sat}$ ,  $V_T = +ve$

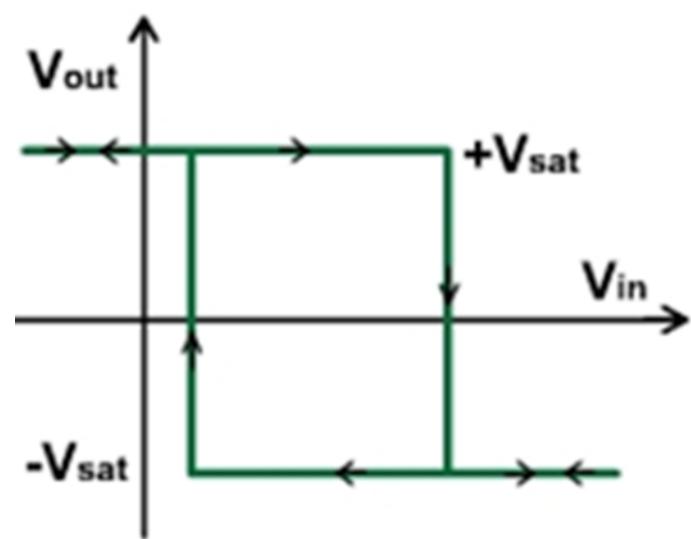
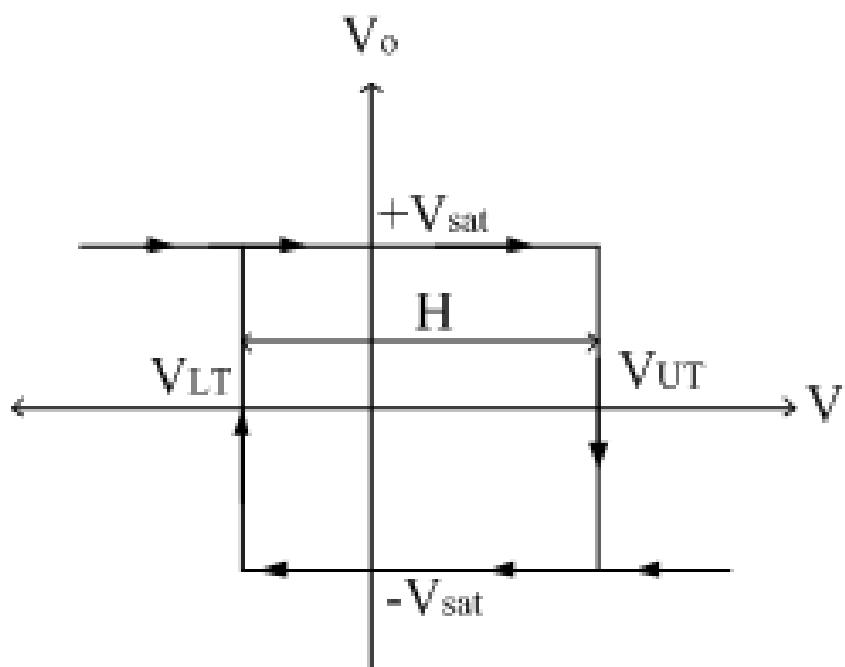
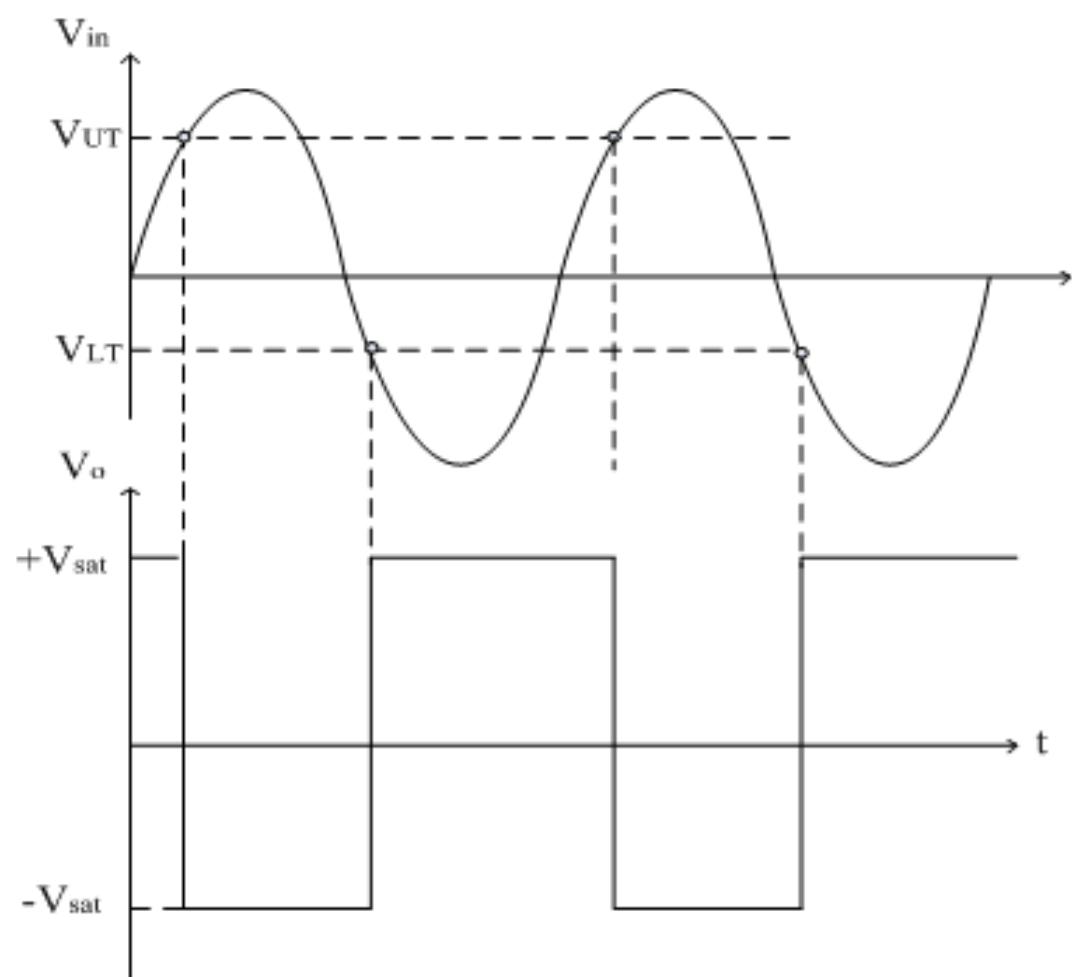
When  $V_{out} = -V_{sat}$ ,  $V_T = -ve$

Using Eq 1,

When  $V_O = +V_{sat}$ , the reference. Voltage (UTP) is given by

$$\begin{aligned} UTP &= \frac{(V_{sat} - V_R)R_2}{R_1 + R_2} + V_R \\ &= \beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2} \end{aligned}$$

$$\begin{aligned} LTP &= \frac{(-V_{sat} - V_R)R_2}{R_1 + R_2} + V_R \\ &= -\beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2} \end{aligned}$$



If  $V_R$  is positive the loop is shifted to right side; if  $V_R$  is negative, the loop is shifted to left side. The hysteresis voltage  $V_{hys}$  remains the same.

# Asymmetric inverting ST using diode

# Non Inverting Schmitt Trigger

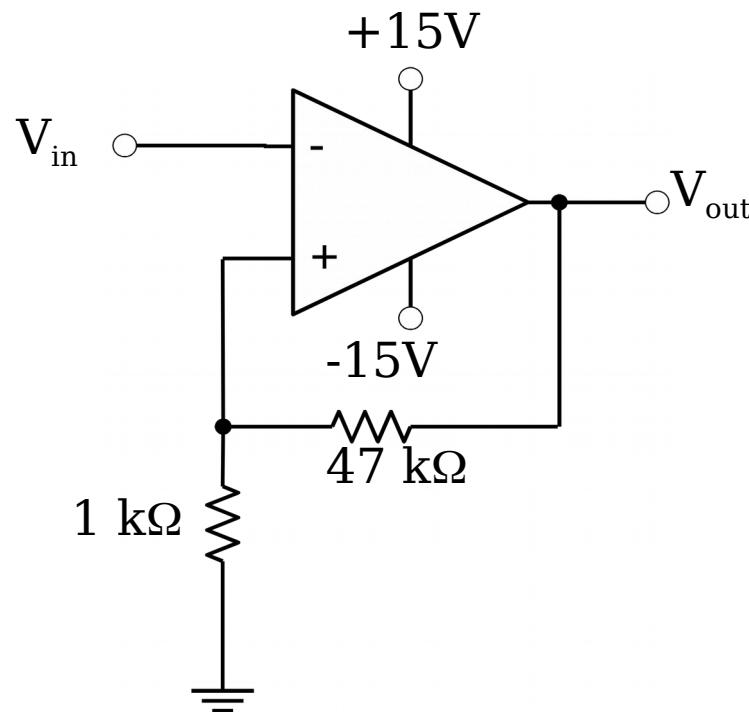
# Design Schmitt Trigger

- Given:
    - $V_{lt}$ ,  $V_{ut}$
    - $V_{supply}$
    - $R1.$
  - Find:
    - $R2$
    - $V_{DC}$
  - To Draw:
    - Hysteresis
    - Waveforms
- Two Ways to design Asymmetric Schmitt Trigger:

  1. Using additional VDC
  2. Using diodes & Resistors in series in feedback path.

# Example 1

- If  $V_{\text{sat}} = 13.5 \text{ V}$ , what are the trip points and hysteresis in Figure below?

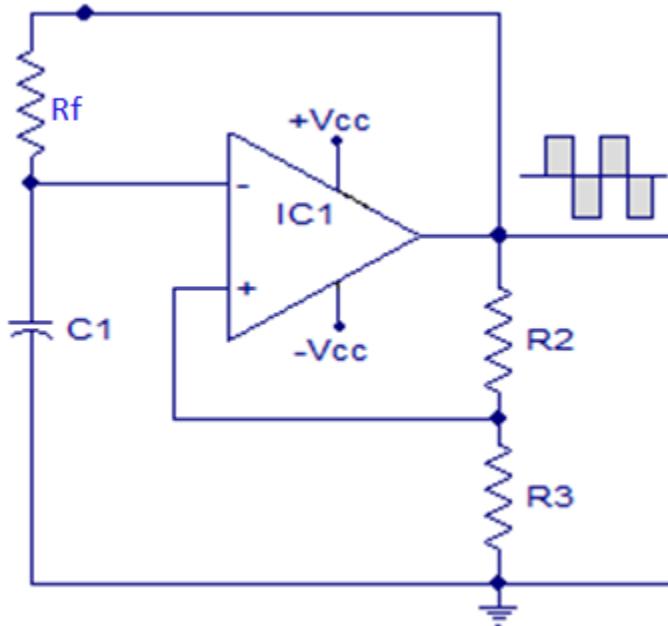


$$V_{UTP} = \frac{1k\Omega}{48k\Omega}(+13.5V) = 0.281V$$

$$V_{LTP} = \frac{1k\Omega}{48k\Omega}(-13.5V) = -0.281V$$

$$V_{HYS} = V_{UTP} - V_{LTP} = 0.281V - (-0.281V) = 0.562V$$

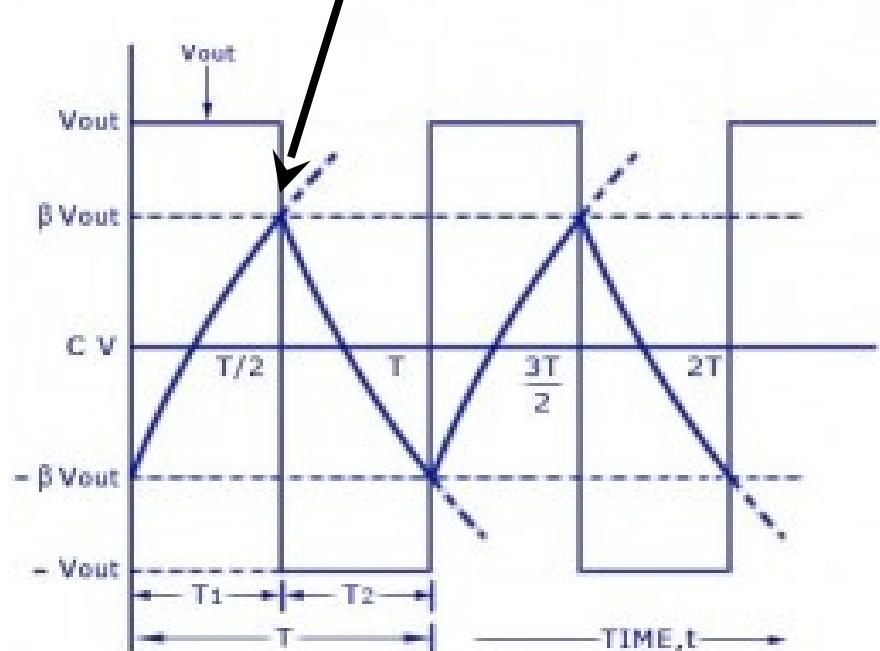
# Waveform Generators



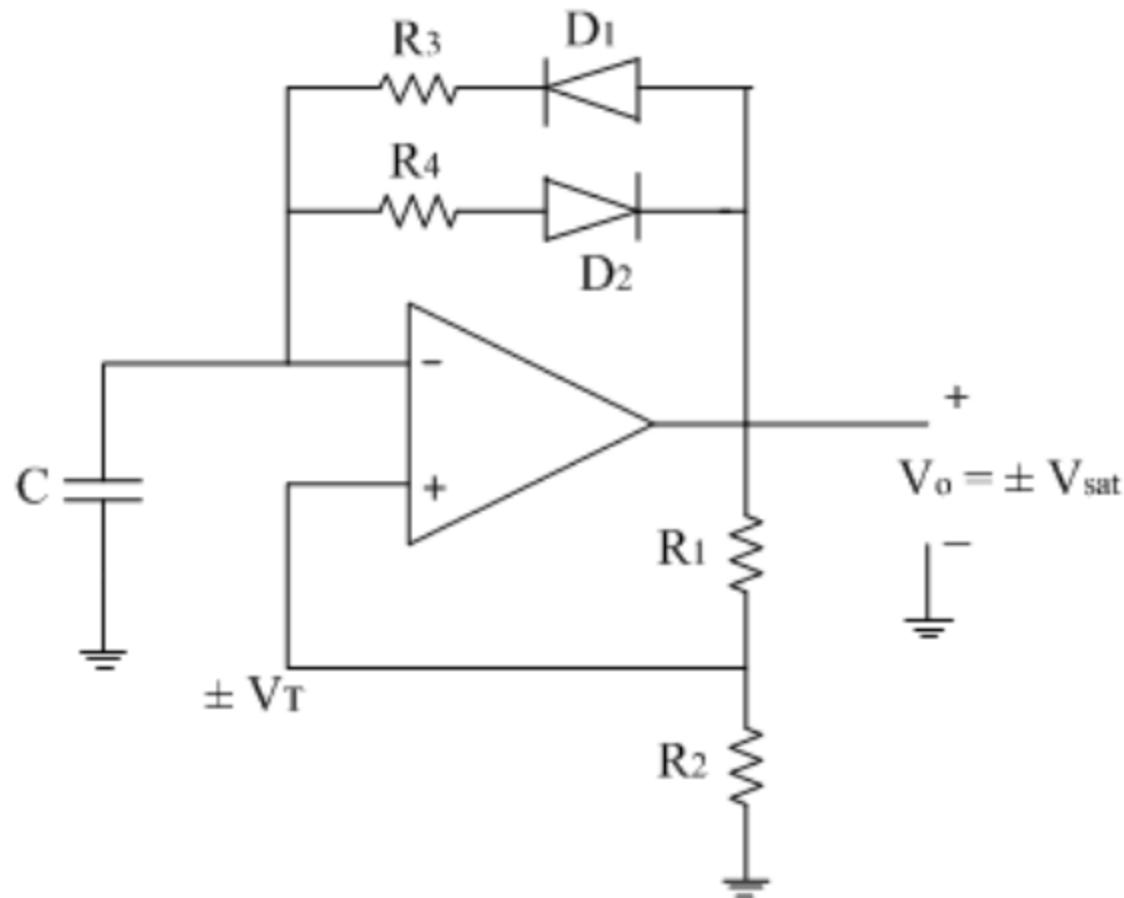
Duty Cycle variation by using diodes in series with Rf in feedback path.

## Astable Multivibrator

C not allowed to charge more as Vout trips to -ve level.



# Asymmetrical Square wave generator



<https://www.electronics-tutorial.net/analog-integrated-circuits/multivibrators/asymmetrical-square-wave-generator/>

- When output is high (i.e.  $+V_{sat}$ ), diode D1 is forward biased and capacitor C starts charging through resistance  $R_3$  towards  $+V_{sat}$  and diode D2 is reversed biased.  
Therefore the charging time constant of the capacitor is  $\tau_c = R_3 C$   
When output is low (i.e.  $-V_{sat}$ ), diode D2 is forward biased and capacitor C starts charging through resistance  $R_3$  towards  $-V_{sat}$  (i.e. discharging in negative direction) and diode D1 is reversed biased.  
Therefore the discharging time constant of the capacitor is  $\tau_d = R_4 C$
- As in both the cases time constant is different, we get different ON and OFF time for output square wave and hence asymmetrical square wave.

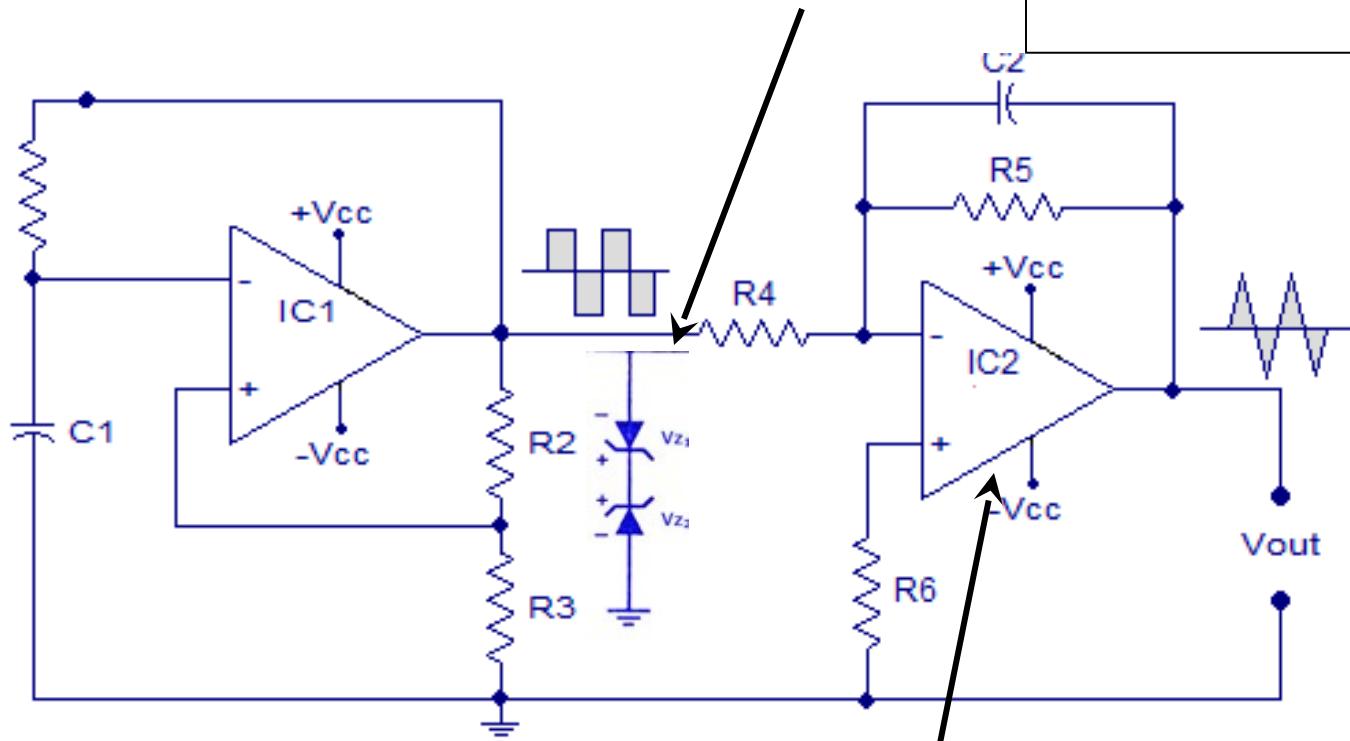
# Important Equations

$$T = 2R_fC \times \ln\left(\frac{1 + \beta}{1 - \beta}\right)$$

$$\beta = \frac{R_3}{R_2 + R_3}$$

$$f = \frac{1}{T}$$

# Triangular Wave Generator-1

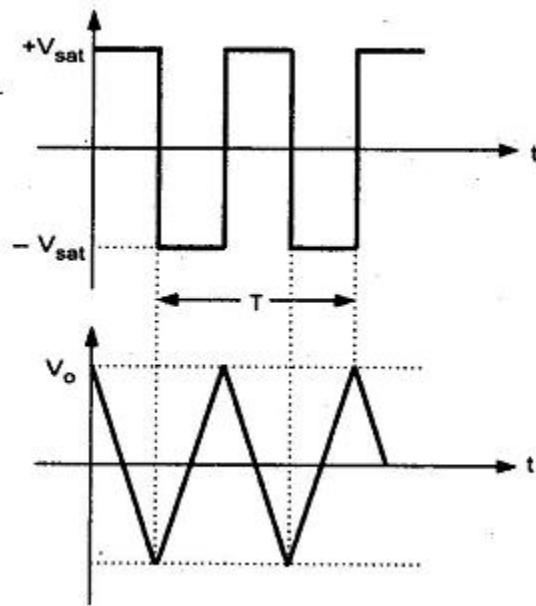


Input voltage of IC2 is closer to Vsat levels. To avoid this use zener diodes.

Design this Integrator with  $f_b = f_{out}$ .

$5 \cdot R_4 \cdot C_2 \gg T/2$ , T of square waveform  
For stable output,  $R_5 = 10R_4$ ,  $R_6 = R_{out}$

- Although the amplitude of the square wave is constant ( $\pm V_{sat}$ ), the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa. This is because the reactance of capacitor decreases at high frequencies and increases at low frequencies.

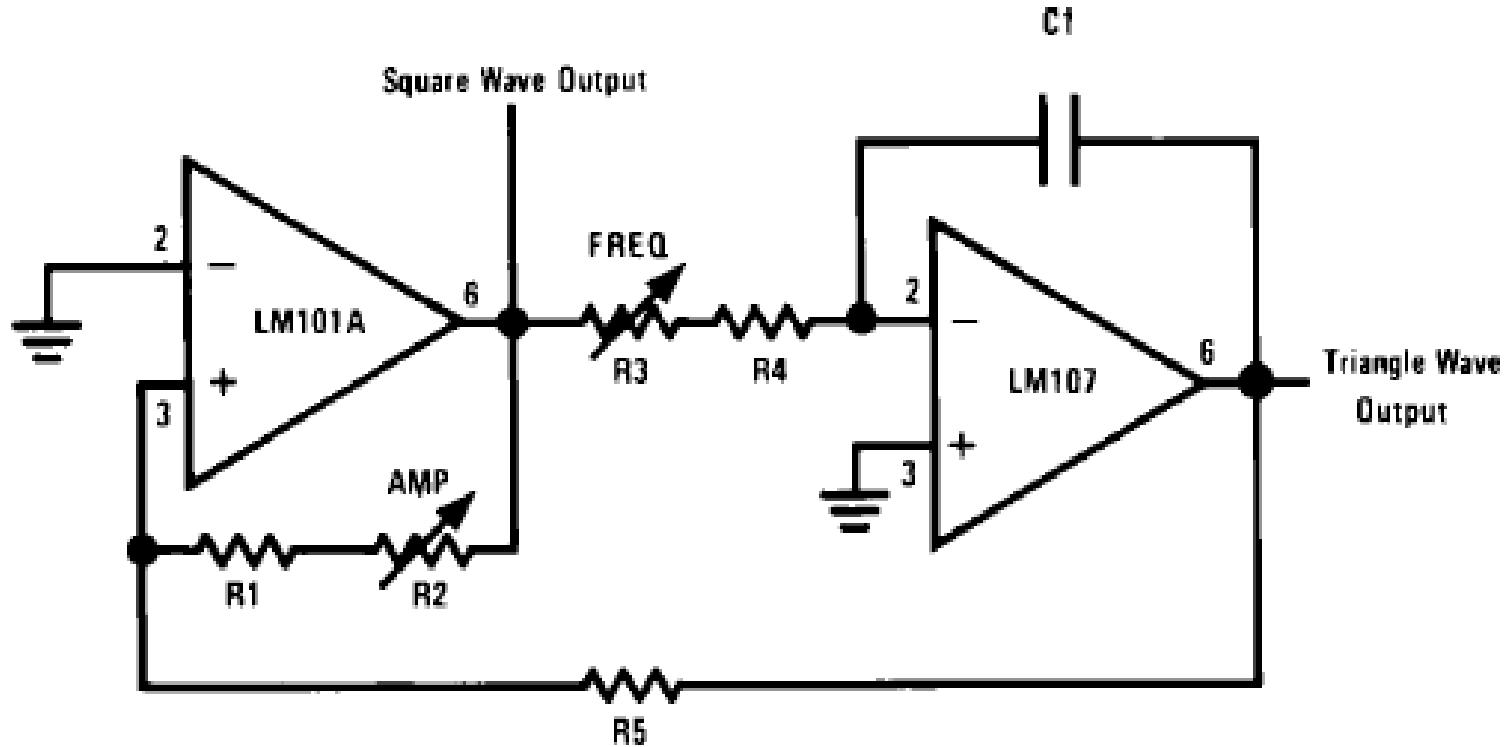


# Design Waveform Generator

- Given:
  - $V_{opp}$ ,  $f_o$ , Duty Cycle,  $\beta$ ,  $C$
- Find:
  - $R_3$ ,  $R_2$ ,  $R_f$  and components related to integrator circuit.
- To draw:
  - Waveforms across timing capacitor, output of IC1 and IC2.

# using Comparator and Integrator with fewer components

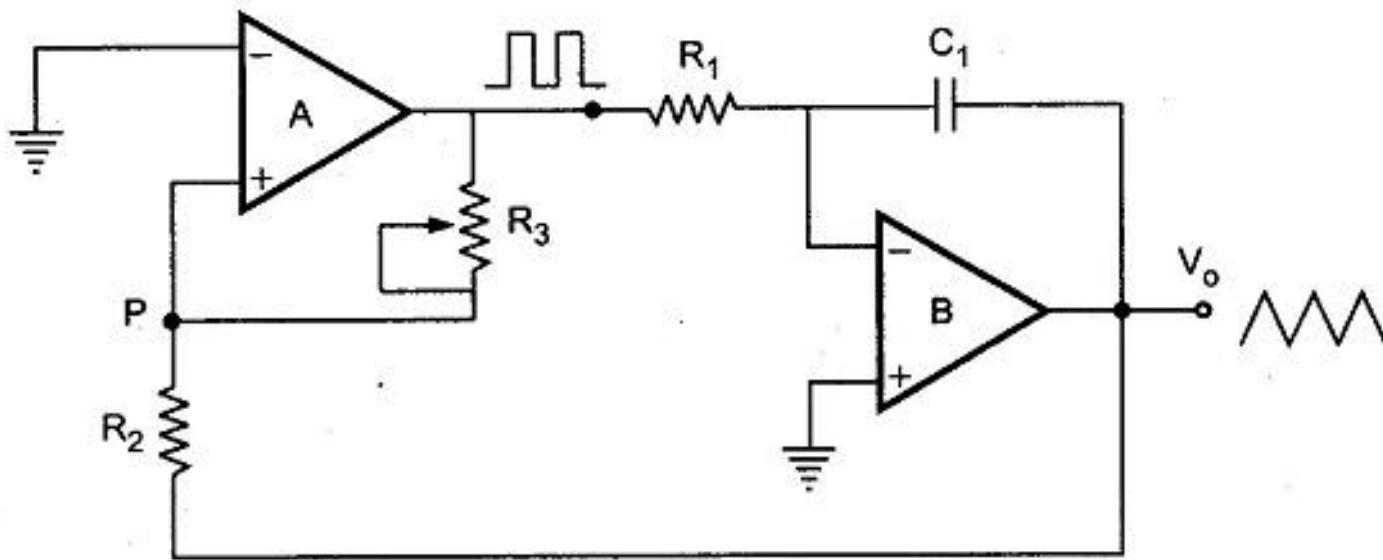
---



$$V_{O_{pp}} = 2 \frac{R_5 V_{sat}}{R_1 + R_2}$$

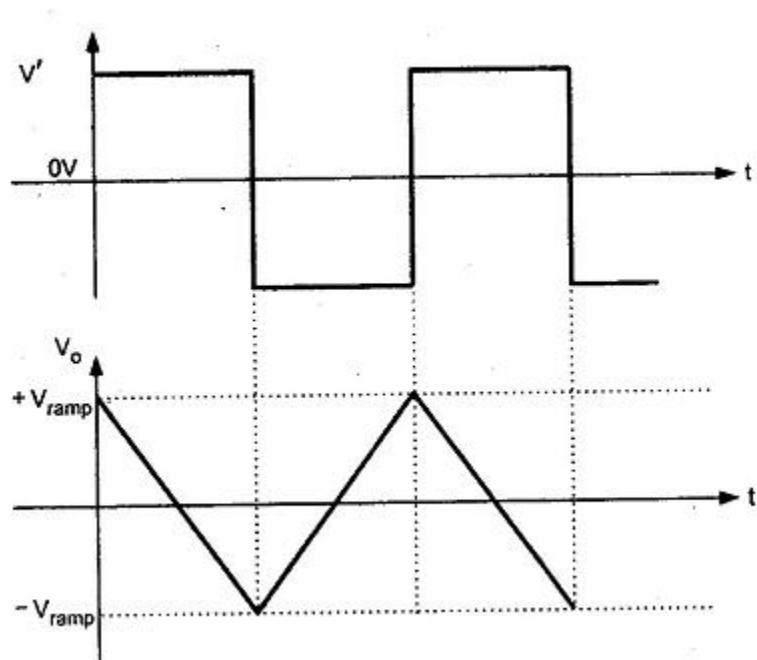
$$T = \frac{4C_1 R_5 (R_3 + R_4)}{R_1 + R_2}$$

# Triangular Wave Generator-2



It consists of a comparator (A) and an integrator (B). The output of comparator A is a square wave of amplitude  $\pm V_{sat}$  and is applied to the inverting (−) input terminal of the integrator B. The output of integrator is a triangular wave and it is feedback as input to the comparator A through a voltage divider R<sub>2</sub> R<sub>3</sub>.

# Waveforms of triangular waveform generator



Assume that the output of comparator A is at  $+V_{sat}$ . This forces a constant current through C to give a negative going ramp at the output of the integrator, as shown in the Fig. Therefore, one end of voltage divider is at a voltage  $+V_{sat}$  and the other at the negative going ramp. When the negative going ramp reaches a certain value  $-V_{ramp}$ , the effective voltage at point

As a result, the output of comparator A switches from positive saturation to negative saturation ( $-V_{sat}$ ). This forces a reverse constant current (right to left) through C to give a positive going ramp at the output of the integrator, as shown in the Fig. 2.89. When positive going ramp reaches  $+V_{ramp}$ , the effective voltage at point p becomes slightly above OV. As a result, the output of comparator A switches from negative saturation to positive saturation ( $+V_{sat}$ ). The sequence then repeats to give triangular wave at the output of integrator B.

When comparator output is at  $+V_{sat}$ , the effective voltage at point P is given by

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} [ +V_{sat} - (-V_{ramp}) ] \quad \dots (1)$$

When effective voltage at P becomes equal to zero, we can write above equation

$$\begin{aligned} -V_{ramp} + \frac{R_2}{R_2 + R_3} [ +V_{sat} - (-V_{ramp}) ] &= 0 \\ -V_{ramp} + \frac{R_2}{R_2 + R_3} (V_{ramp}) + \frac{R_2}{R_2 + R_3} (+V_{sat}) &= 0 \\ \frac{-R_3}{R_2 + R_3} (V_{ramp}) &= -\frac{R_2}{R_2 + R_3} (+V_{sat}) \\ -V_{ramp} &= \frac{-R_2}{R_3} (+V_{sat}) \end{aligned} \quad \dots (2)$$

Similarly, when comparator output is at  $-V_{sat}$ , we

$$V_{ramp} = \frac{-R_2}{R_3} (-V_{sat}) \quad \dots (3)$$

The peak to peak amplitude of the triangular wave can be given

$$\begin{aligned} V_{o(pp)} &= +V_{ramp} - (-V_{ramp}) \\ &= \frac{-R_2}{R_3} (-V_{sat}) - \left( \frac{-R_2}{R_3} \right) (+V_{sat}) \end{aligned} \quad \dots (4)$$

If  $|+V_{sat}| = |-V_{sat}|$  then, we can write

$$V_{o(pp)} = \frac{R_2}{R_3} V_{sat} + \frac{R_2}{R_3} V_{sat} = \frac{2R_2}{R_3} V_{sat} \quad \dots (5)$$

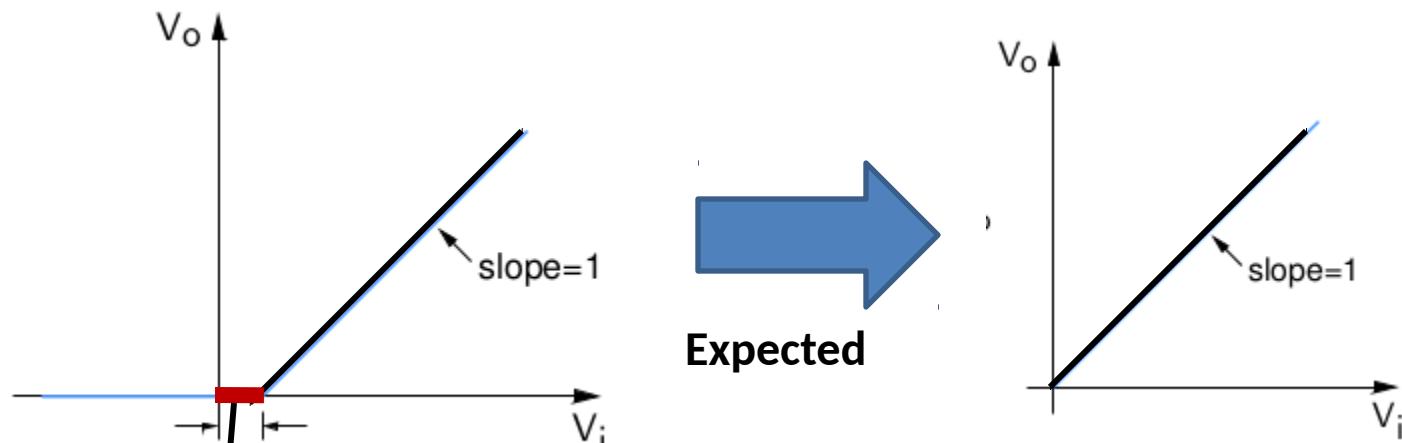
$$f_0 = \frac{R_3}{4R_1 C_1 R_2}$$

# Precision Rectifier

- Ordinary diodes cannot rectify voltages below cut-in voltage of the diode.
- A circuit which act as an ideal diode or precision signal processing rectifier for rectifying voltages which are below the level of cut-in voltage can be designed by placing the diode in the feedback loop of an opamp

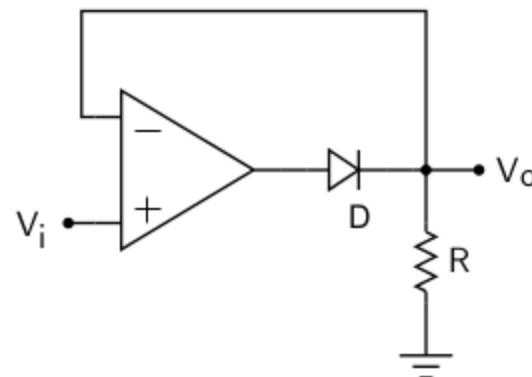
# Precision Rectifier

- Simple Diode Rectifier:



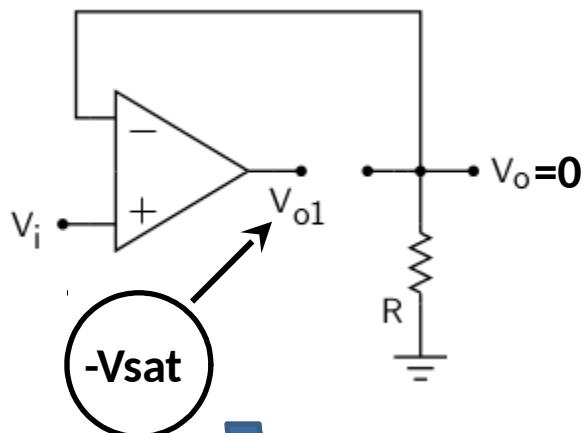
**Not useful for small  
signal applications!**

# Basic Half Wave Precision Rectifier



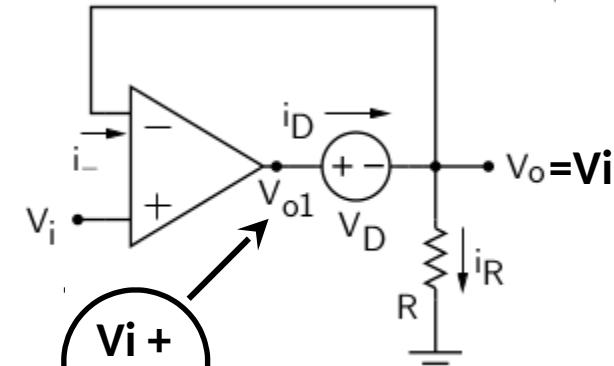
Limitation on  
Switching Speed !

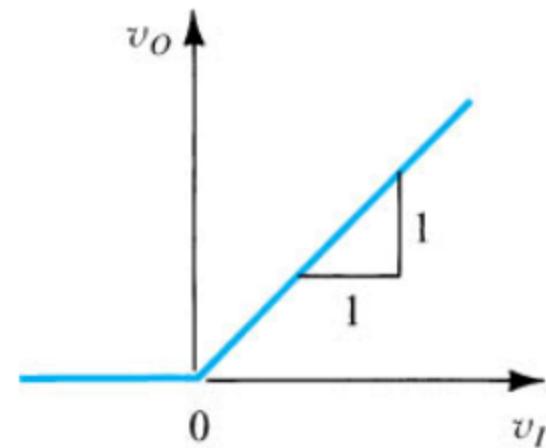
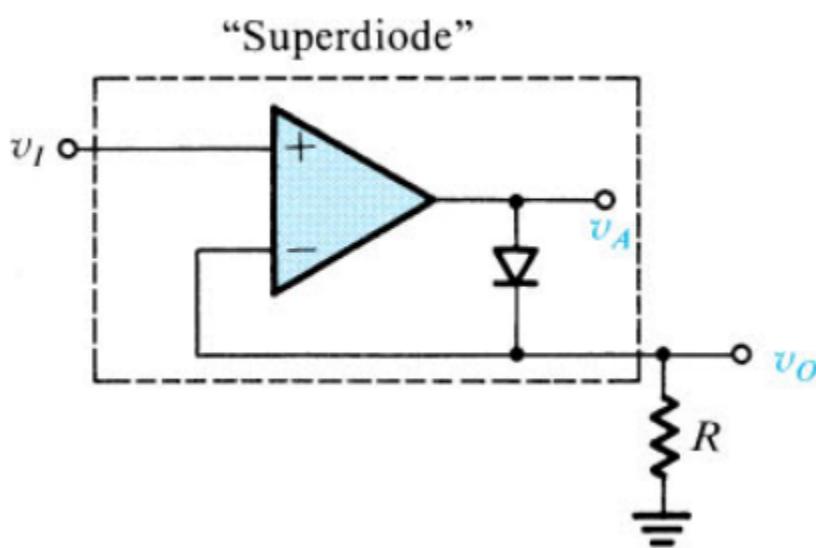
(I)  $V_i < 0V$



(II)  
 $V_i$  very small but Positive: D still OFF,  $V_{o1}$  goes to  $+V_{sat}$ , Immediately D turns ON.

(III)  $V_i > 0V$





# Limitations

The circuit has some serious limitations.

- **The main one is speed. It will not work well with high frequency signals.**
- For a low frequency positive input signal, 100% negative feedback is applied when the diode conducts. The forward voltage is effectively removed by the feedback, and the inverting input follows the positive half of the input signal almost perfectly.
- When the input signal becomes negative, the op amp has no feedback at all, so the output pin of the op amp swings negative as far as it can.
- When the input signal becomes positive again, the op amp's output voltage will take a finite time to swing back to zero, then to forward bias the diode and produce an output. This time is determined by the op amp's slew rate, and even a very fast op amp will be limited to low frequencies.

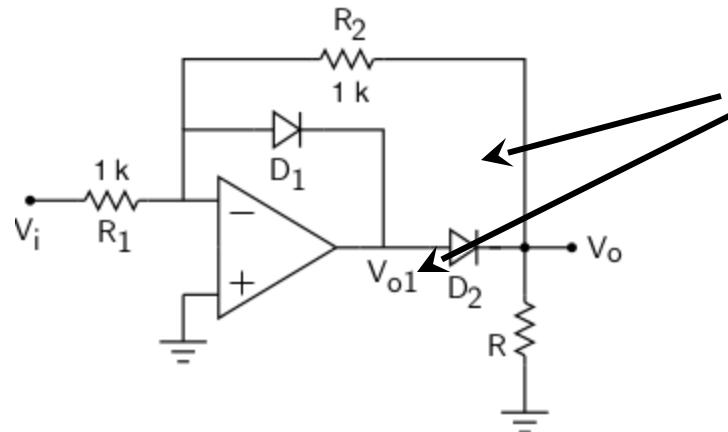
# Advantages

- No diode voltage drop between input and output
- The ability to rectify very small voltages
- Amplification if required
- Low output impedance

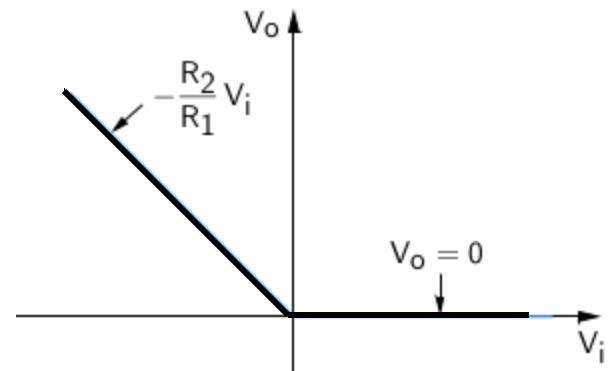
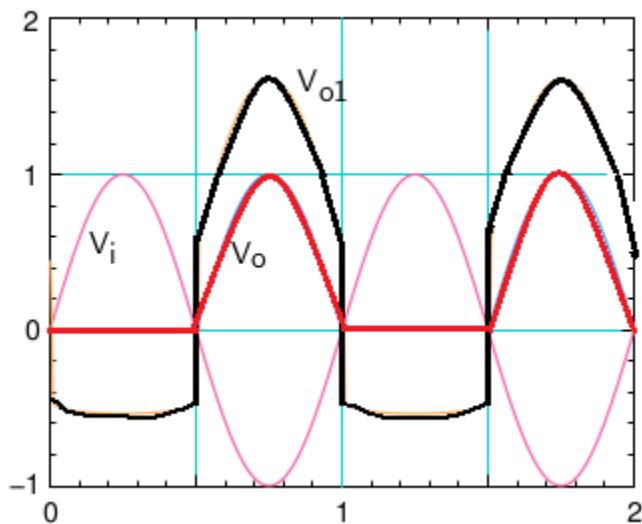
\*\*While the input waveform is in its negative half cycle, the output of the Op-Amp is saturated in a negative direction. Some time is required to get the Op-Amp out of saturation and this will limit the frequency response of the circuit.

So for high frequency performance, a nonsaturating precision rectifier circuit must be used

# Improved Half Wave Precision Rectifier

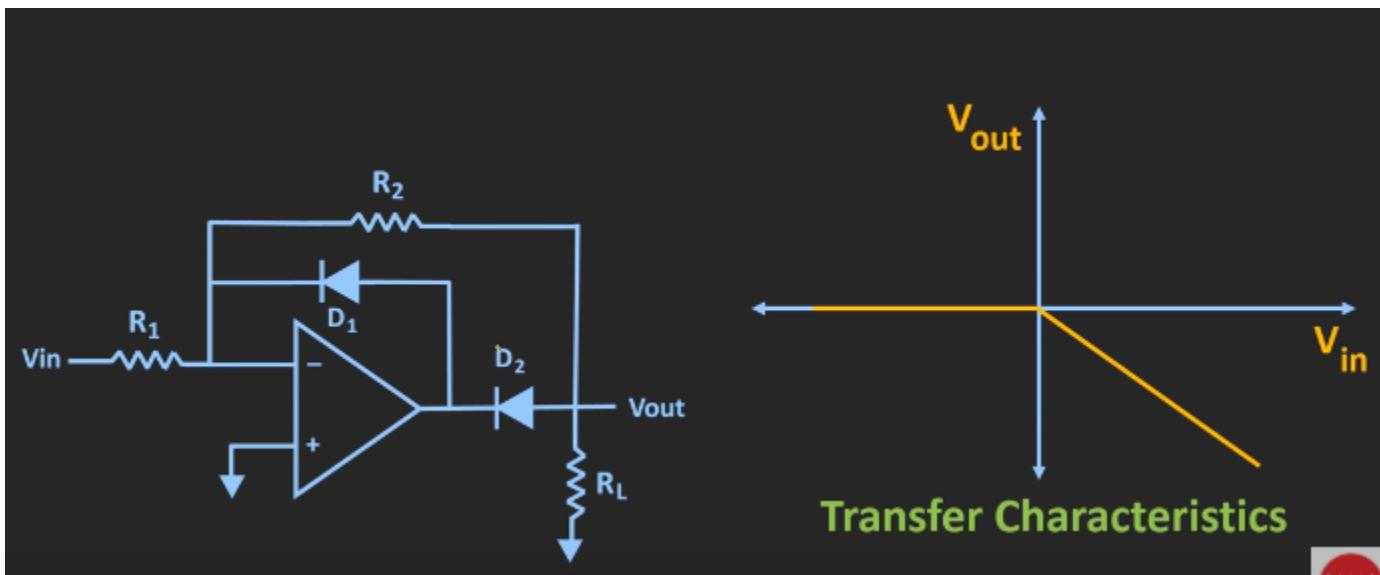


Op-amp doesn't enter into saturation!  
Switching speed improves.

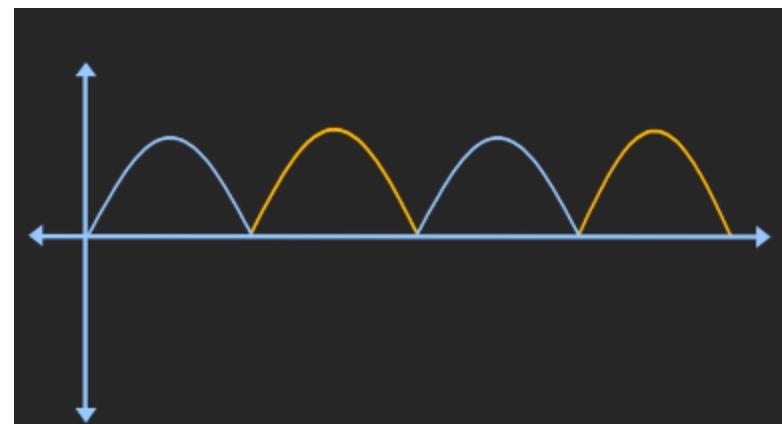
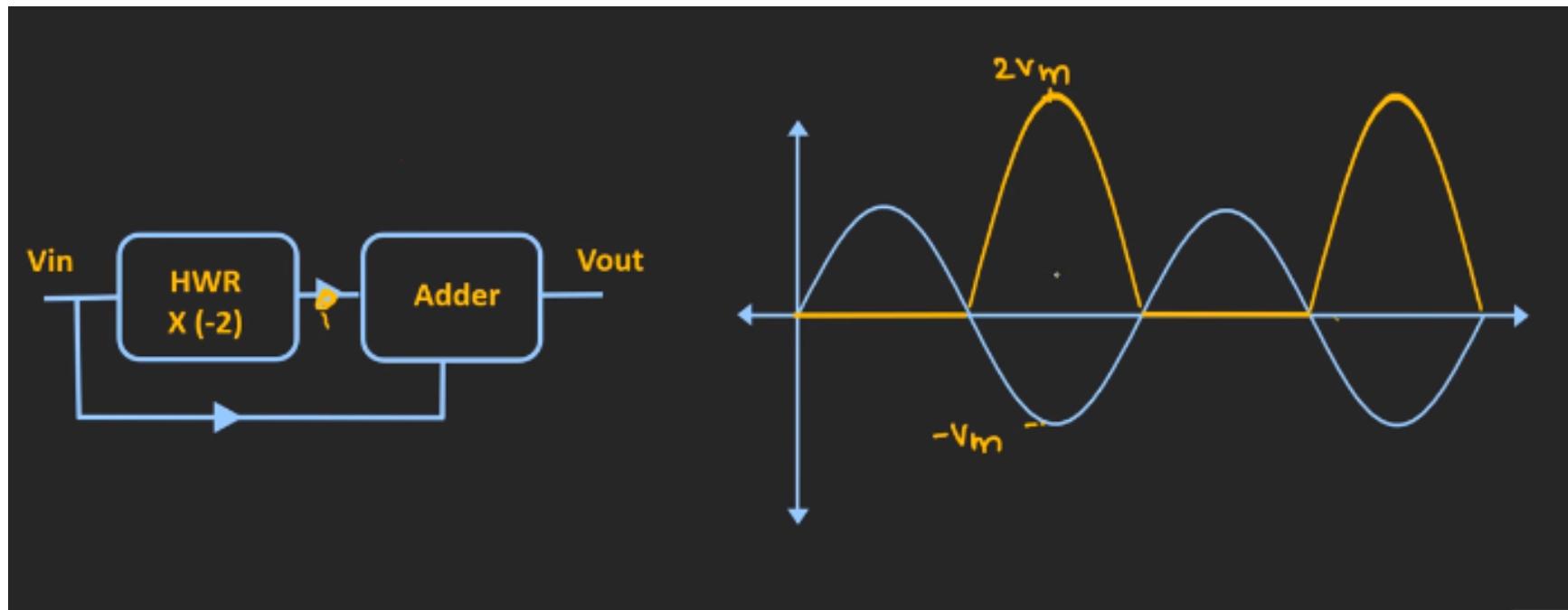




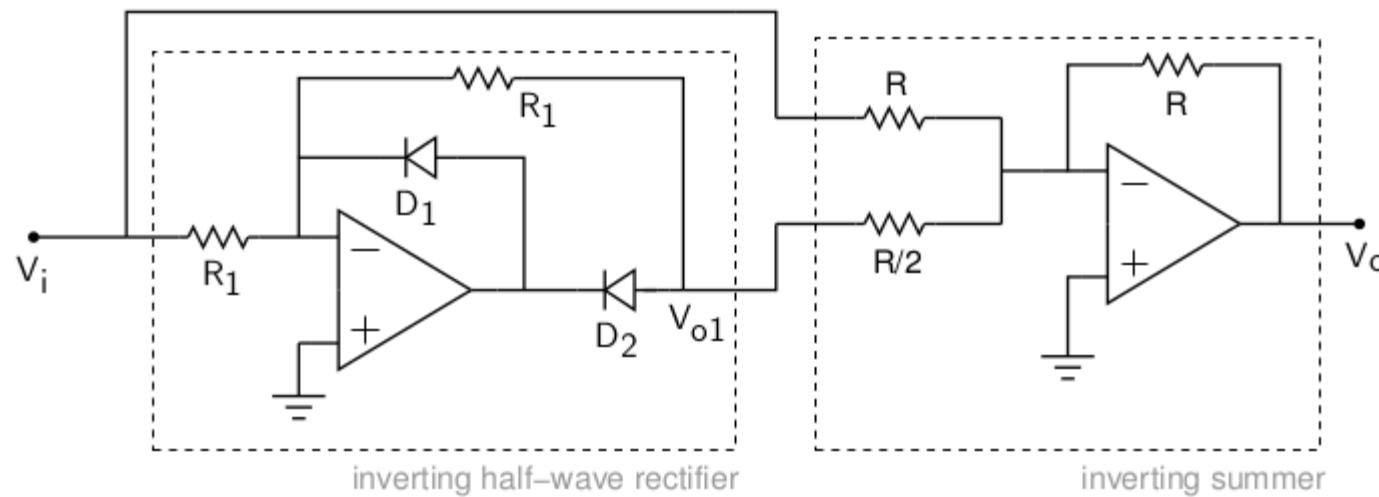
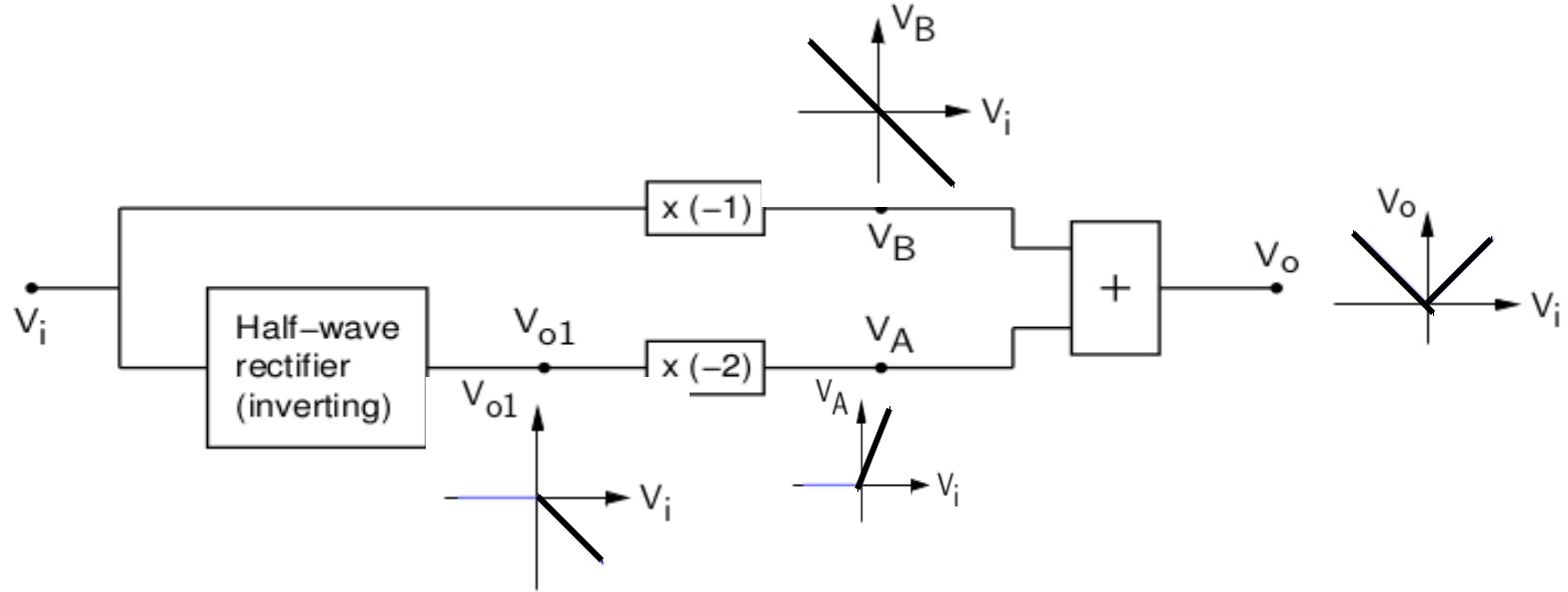
# HWR



# Precision FWR

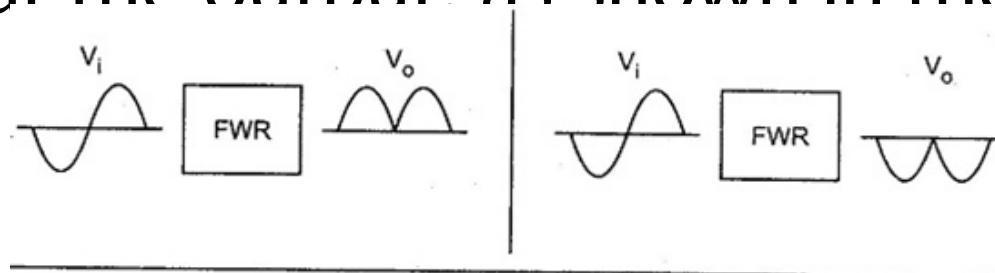


# Full Wave Precision Rectifier

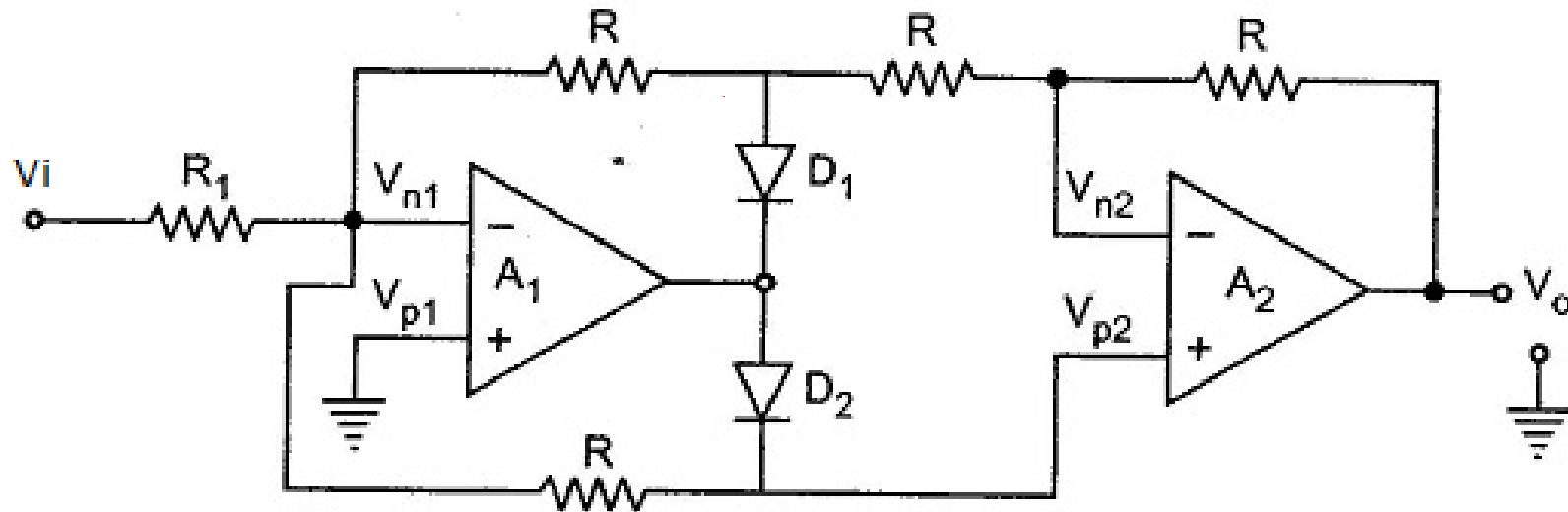


# Full Wave Precision Rectifier

- The Precision Full Wave Rectifiers circuits accept an ac signal at the input, inverts either the negative or the positive half, and delivers both the inverted and non inverted halves at the output as shown in the Fig.

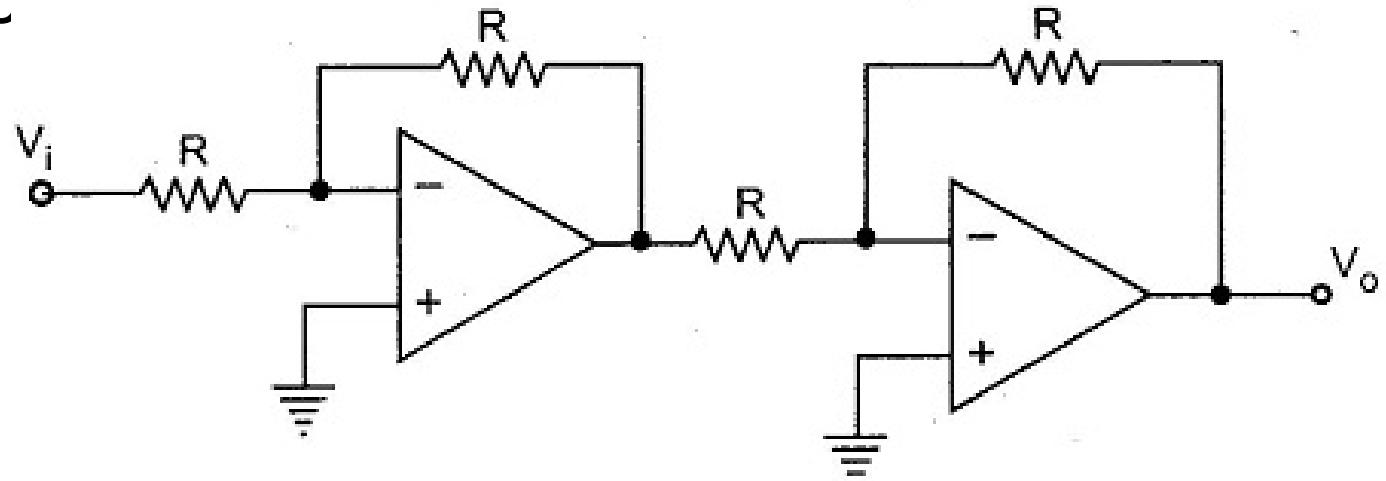


# Precision Full Wave Rectifier



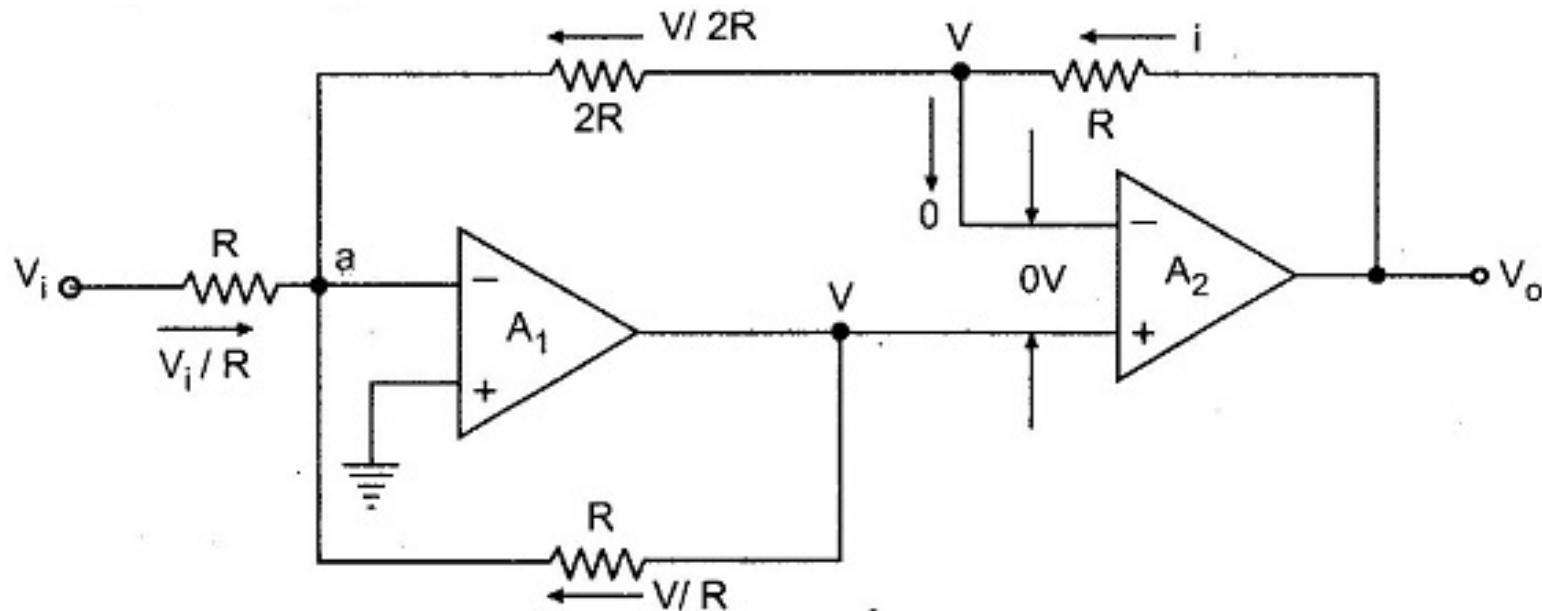
# Working

- **CASE 1 :  $V_i > 0$  :** When  $V_i > 0$ , inverting side of  $A_1$  will force its output to swing negative, thus forward biasing  $D_1$  and reverse biasing  $D_2$ . Since no current flows through resistance  $R$  connected between  $V_{n1}$  and  $V_{p2}$ , both are equipotential

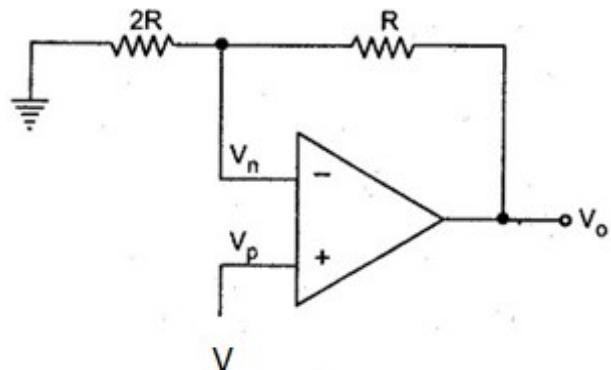


# Working

- **CASE 2 :  $V_i < 0$**  : When  $V_i < 0$ , negative, the output voltage of  $A_1$  swings to positive, making diode D1 reverse biased and diode D2 forward biased.



# Working



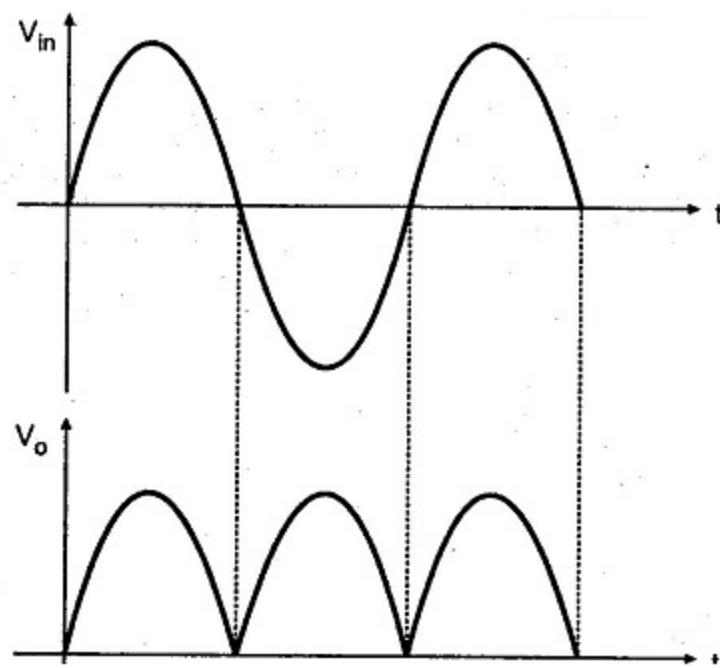
To find  $V_o$  in terms of  $V$  we concentrate on the equivalent circuit of  $A_2$ , as shown

$$\therefore V_o = \left(1 + \frac{R}{2R}\right)V$$

$$= \left(\frac{2R+R}{2R}\right)V = \frac{3}{2}V$$

$$V_o = \frac{3}{2} \left(\frac{-2}{3}V_i\right) = -V_i$$

# Full Wave Rectifier Waveforms



# Criteria for Selecting Components

- High Slew Rate Op-amps (LF351)
- High GBWP ( $> 10 * \text{Gain} * f_{\text{input}}$ )
- Fast switching diodes (1N4148)
- Low values of R (typically  $1k\Omega$ )

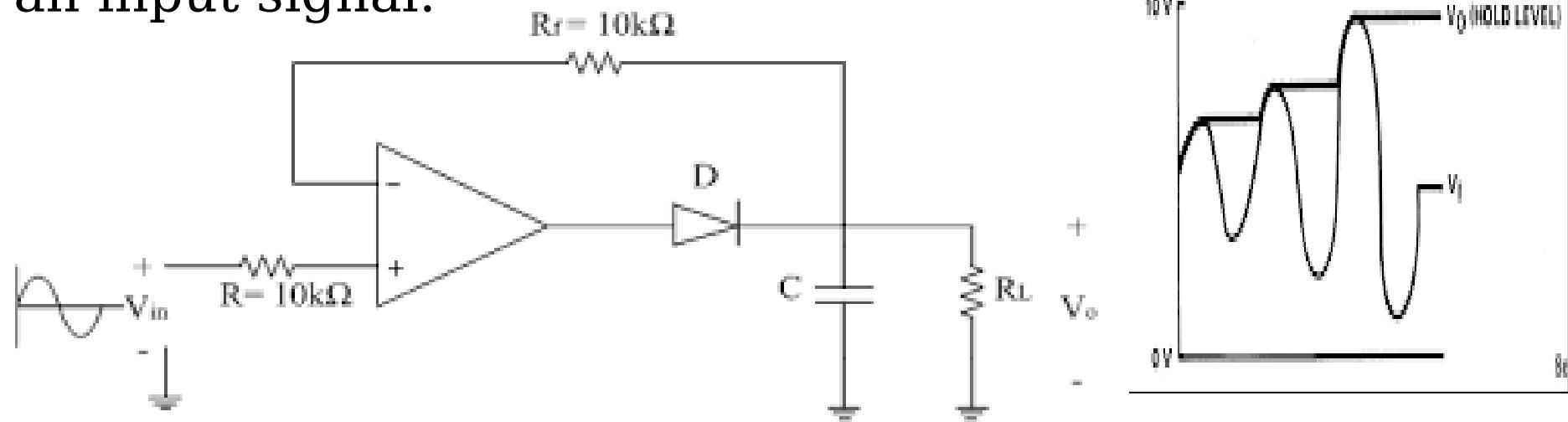
# Precision Rectifiers-Applications

- Small Signal – High Frequency Applications.
  1. Waveshaping Circuits
  2. AC-DC converters.

- Extra Slides 72 to 90

# Peak Detectors

A peak detector is simply a circuit that traces the peaks in an input signal.



**Leakage current must be less !**

✗ Electrolytic , Tantalum

✓ Polypropylene or Polysterene

$$CR_d \leq \frac{T}{10}$$

proper operation of the circuit, the charging time constant (margin time constant) must satisfy above equation. 74

For proper operation of the circuit, the charging time constant ( $CR_d$ ) and discharging time constant

( $CR_L$ ) must satisfy the following condition.

$$CR_d \leq T/10$$

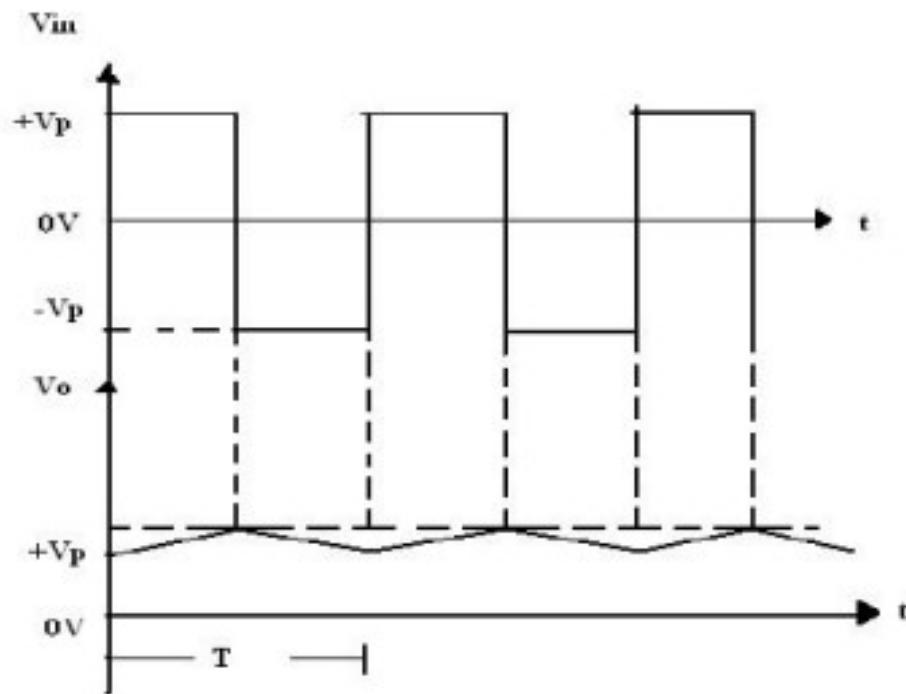
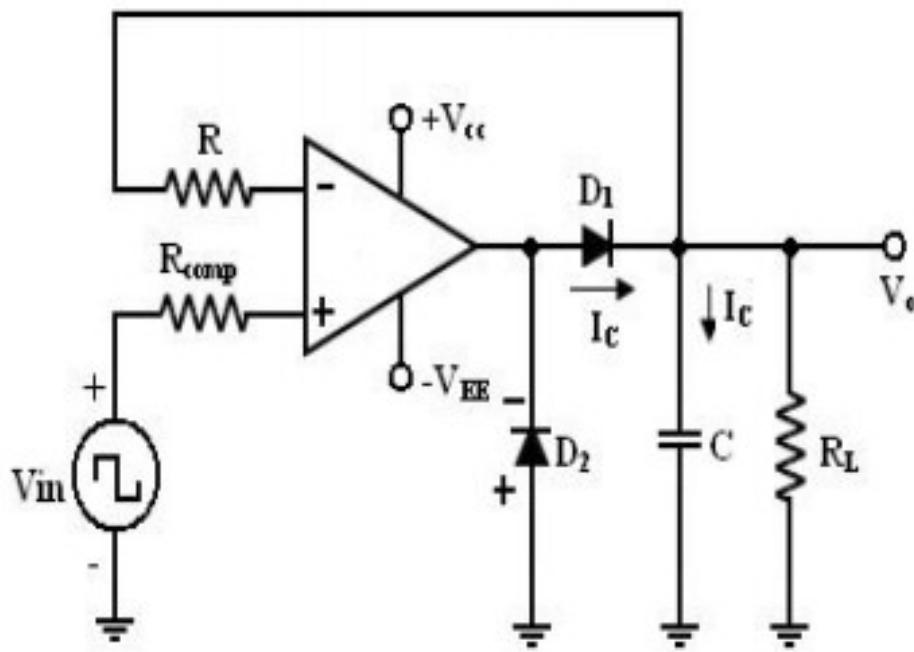
Where  $R_d$  = Resistance of the forward-biased diode.

$T$  = time period of the input waveform.

$$CRL \geq 10T \quad (2)$$

Where  $R_L$  = load resistor.

If  $R_L$  is very small so that eqn. (2) cannot be satisfied.



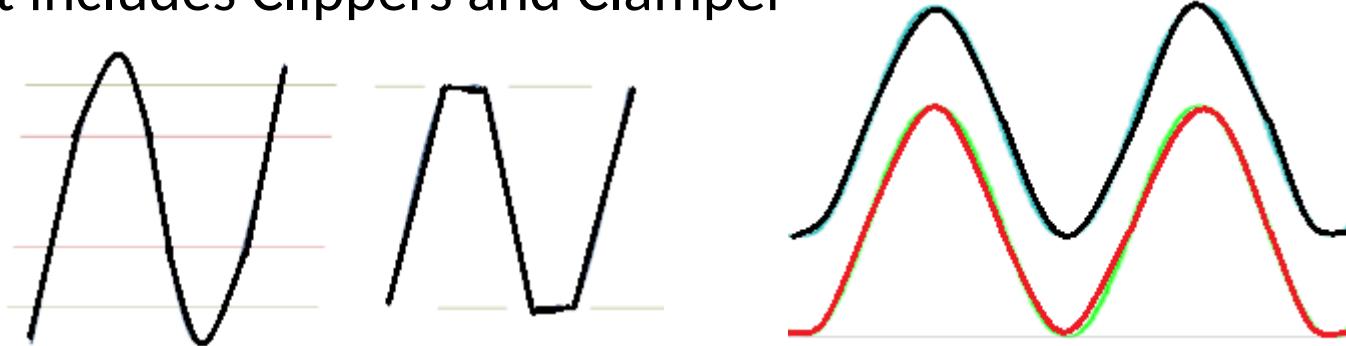
**Fig. Peak detector circuit and input and output waveforms**

R is used to protect op-amp against the excessive discharge currents when the power supply is switched off.

Rcomp minimizes the offset problems. D2 conducts during negative half cycle and hence prevents the op-amp from going into negative saturation

# Waveshaping Circuits

- Waveshaping circuits are commonly used in digital computers and communications such as TV and FM receivers.
- It includes Clippers and Clampers

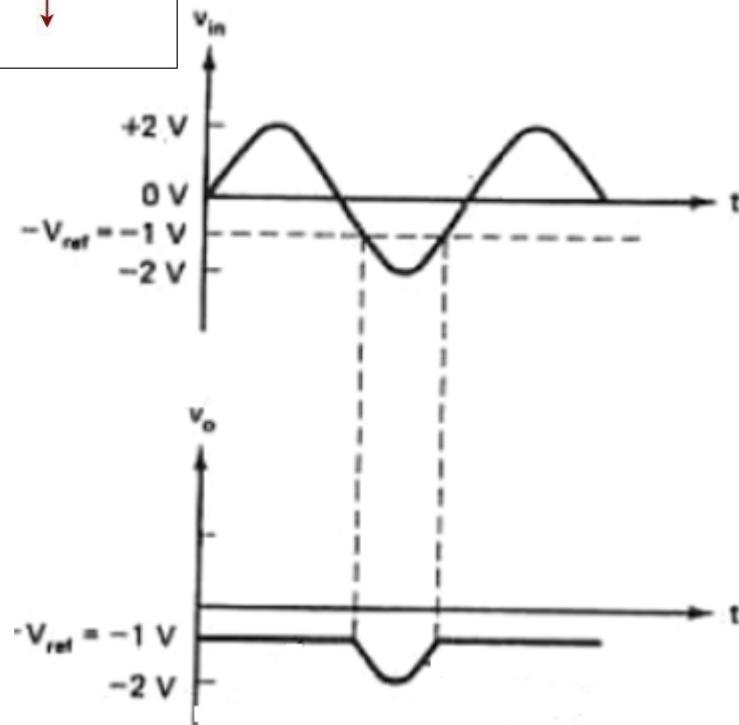
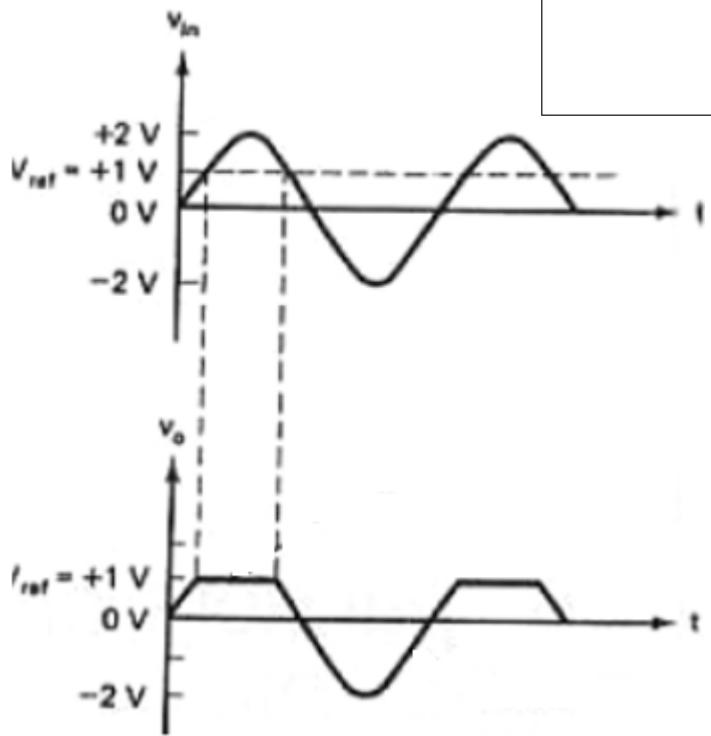
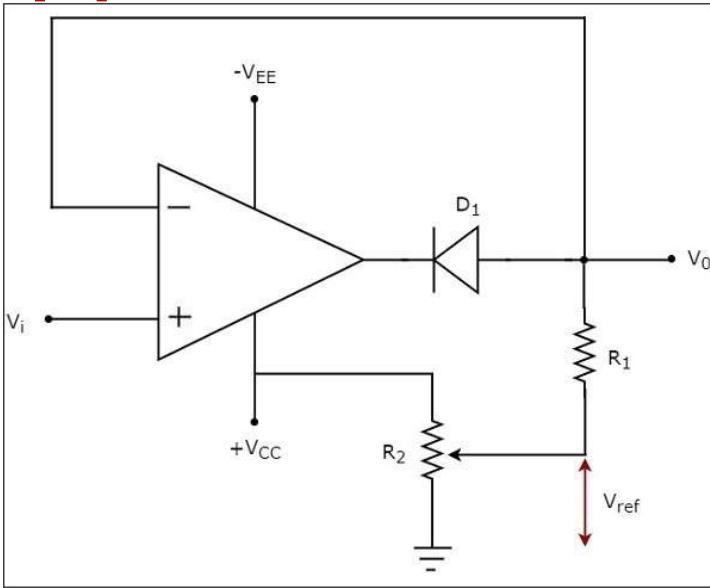


- Circuit Protection by Amplitude Limitation.
- Removing distortions by level shifting.

- **Wave shaping circuits** are the electronic circuits, which produce the desired shape at the output from the applied input wave form. These circuits perform two functions –
  - Attenuate the applied wave
  - Alter the dc level of the applied wave.
  - There are two types of wave shaping circuits: **Clippers** and **Clampers**.

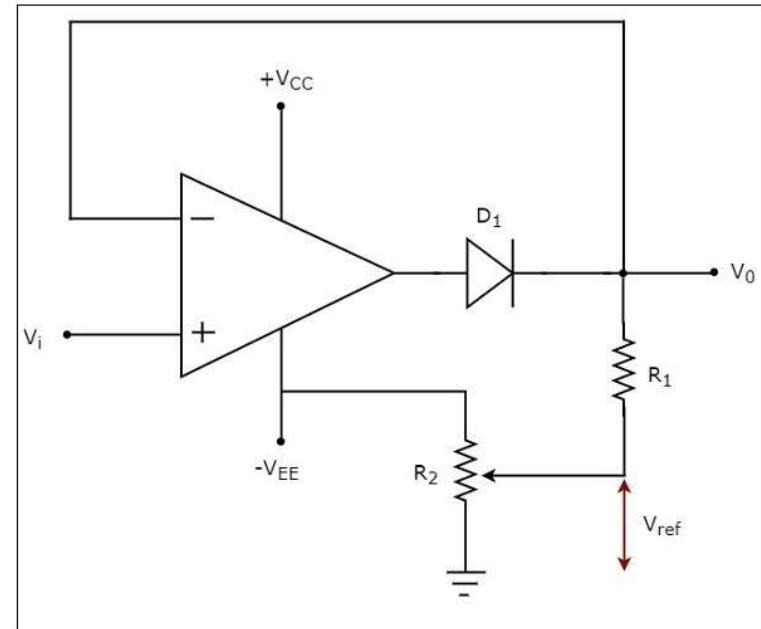
- The main advantage of clippers is that they eliminate the unwanted noise present in the amplitude of an ac signal.
- Clippers can be classified into the following two types based on the clipping portion of the input.
  - Positive Clipper
  - Negative Clipper

# Positive Clippers(Removes +ve peaks)



# Negative Clipper

Draw the waveforms



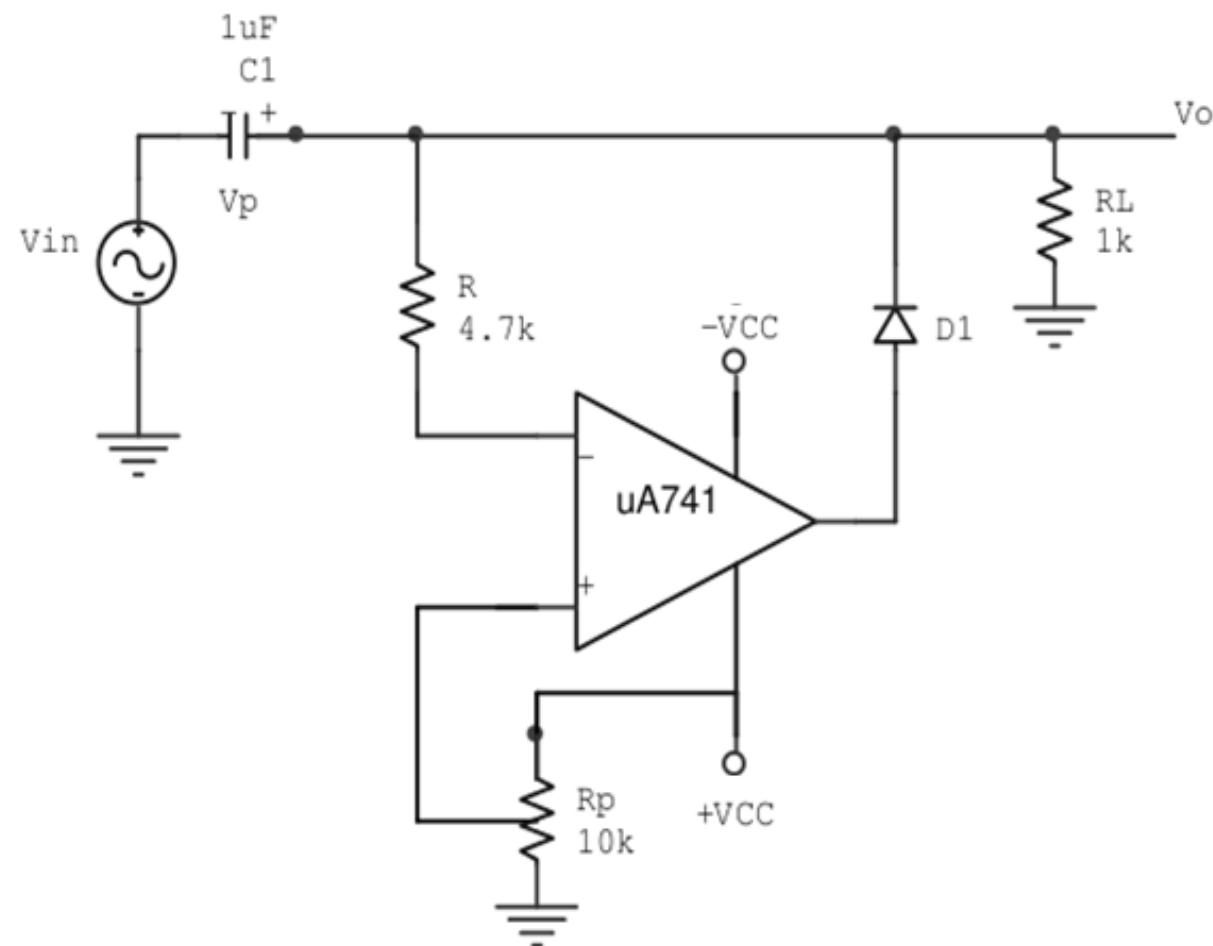
# Clampers

adds a desired DC level to

the ac input signal

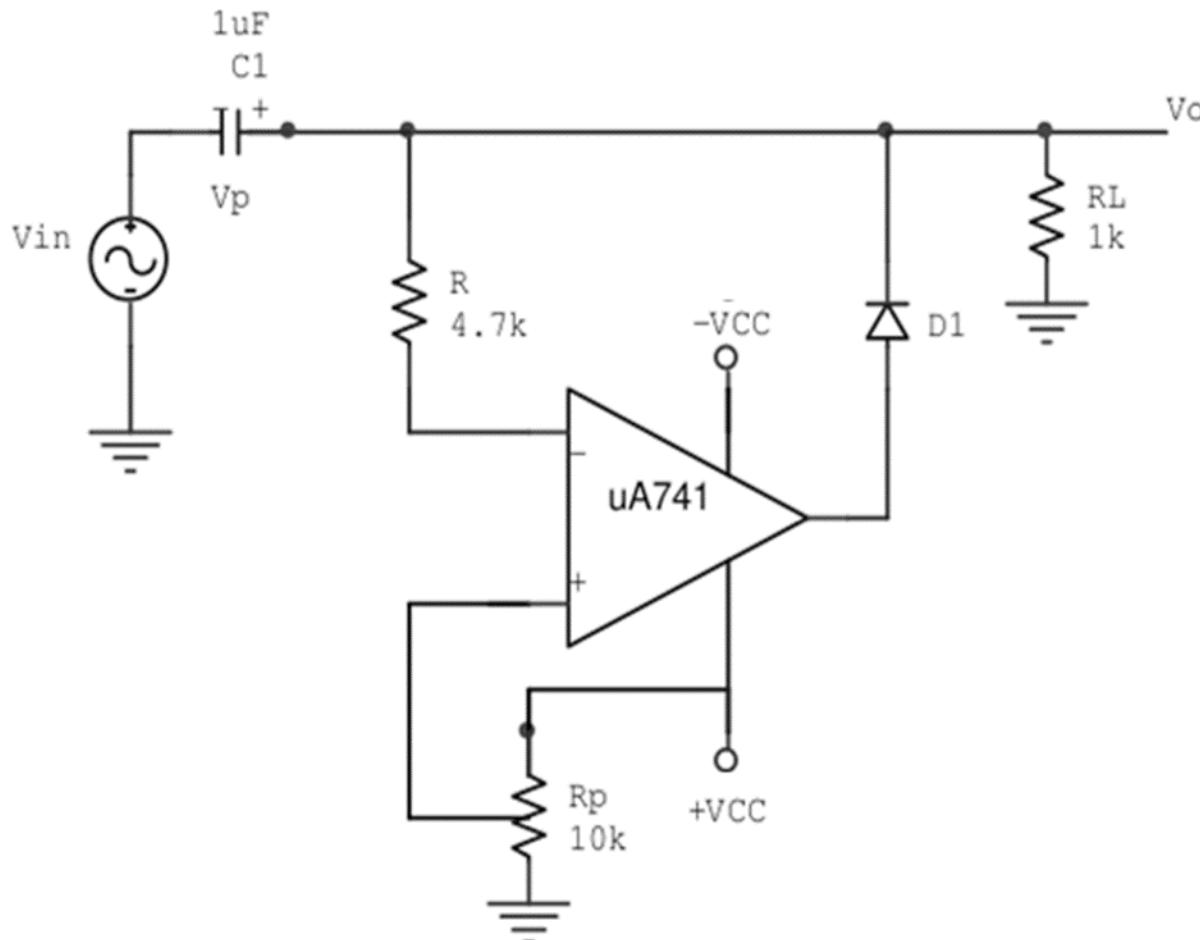
Positive Clamper

Negative Clamper

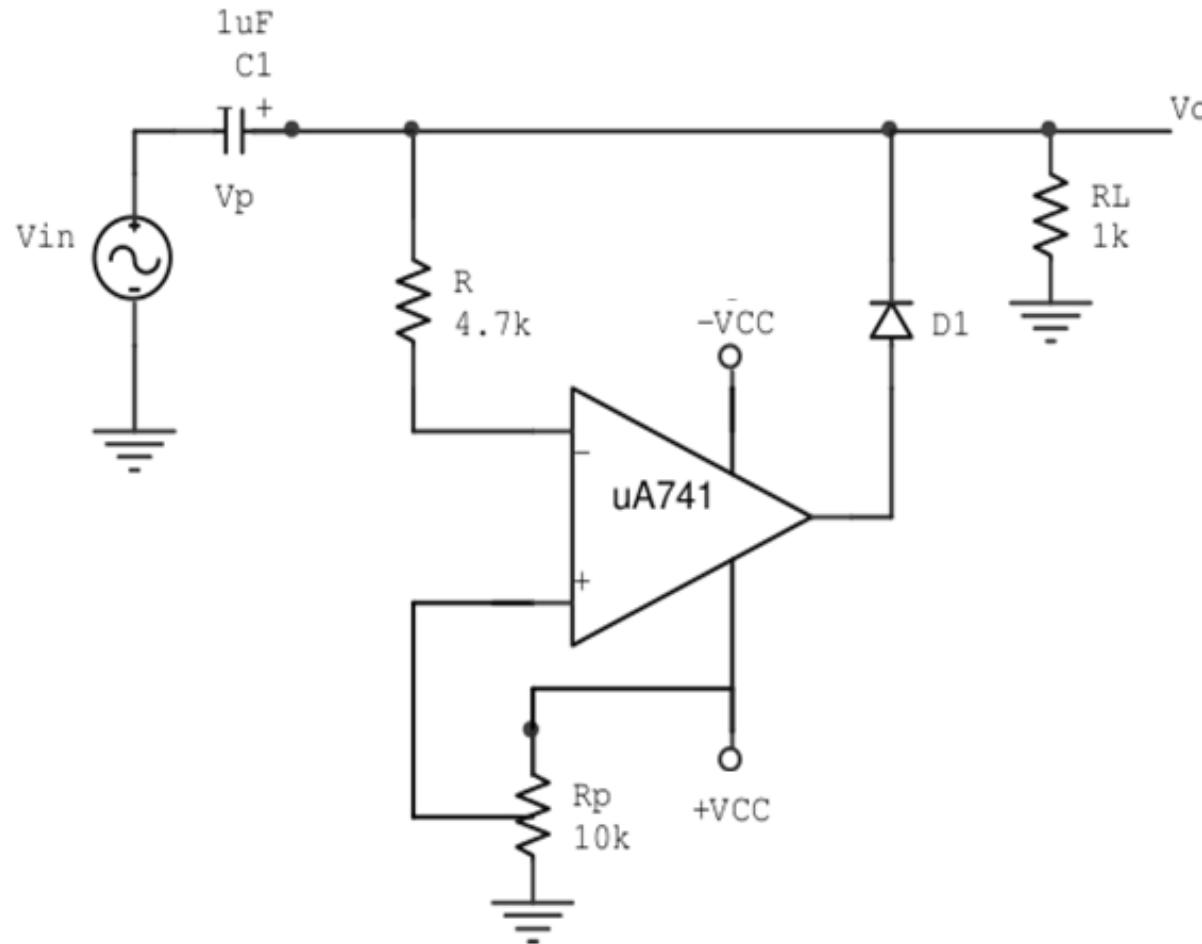


## Peak Clammer

Assuming  $V_{in} > 0$ , OpAmp output is positive, diode D is forward biased, Circuit works as voltage follower,  $V_o' = V_{in}$ ,  $C_1$  is open circuit for DC voltage



Assuming  $V_{ref} = 0$ , when  $V_{in}$  is negative output is positive, D is forward biased, C charges towards the Diode through the Diode.

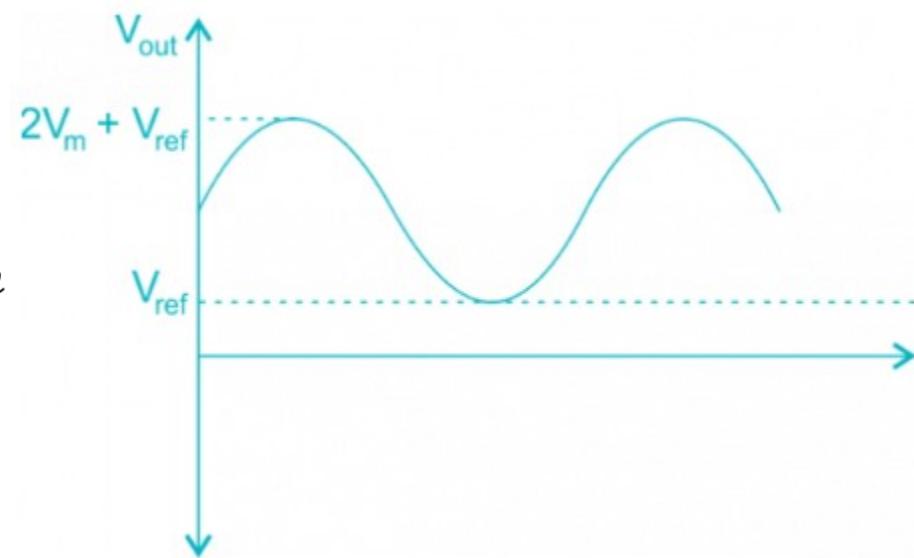
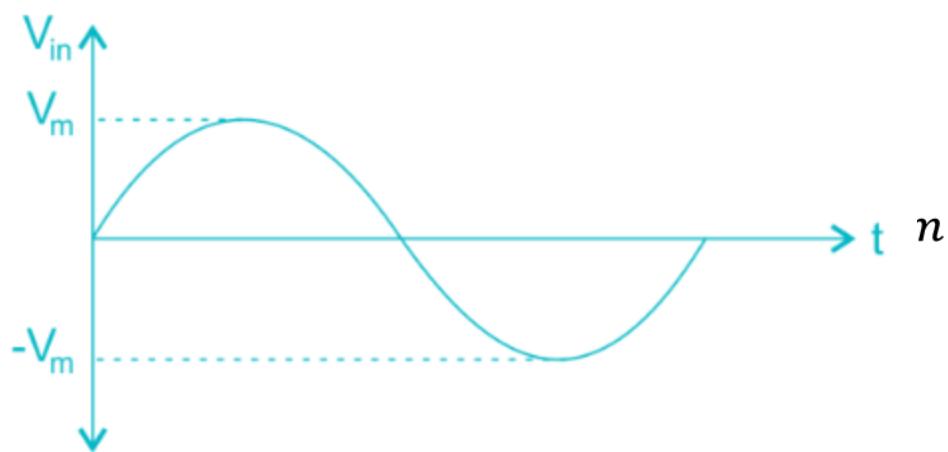


When  $V_{in}$  is positive op amp output is negative, D is reverse biased, there is no discharge path for C,  $V_o'' = V_m + V_{in}$

When  $V_{in}$  is positive op amp output is negative, D is reverse

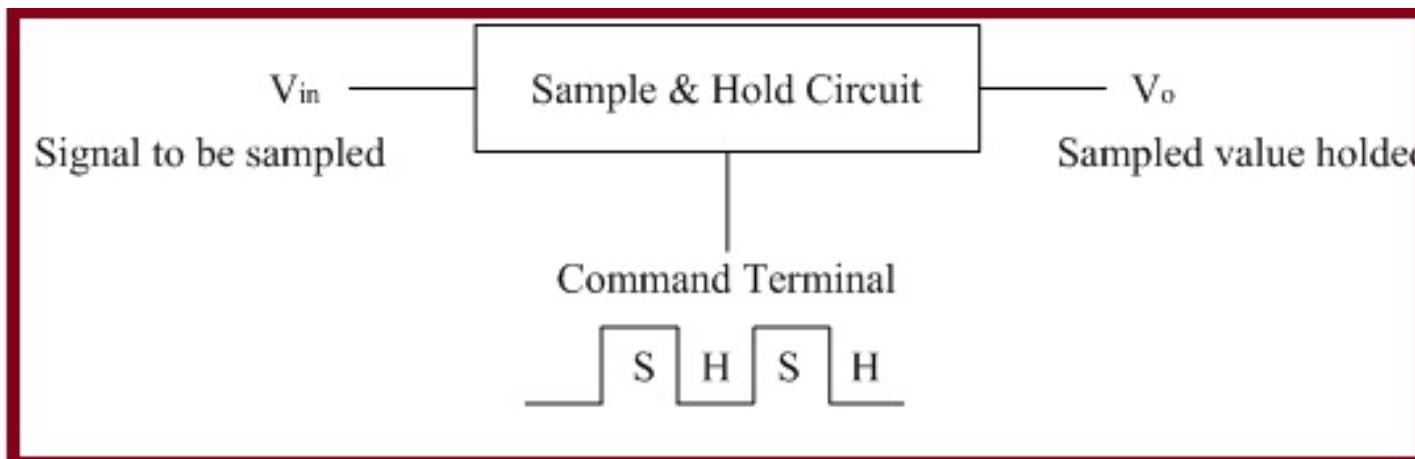
biased, there is no discharge path for C,  $V_o'' = V_m + V_{in}$

- $V_O =$

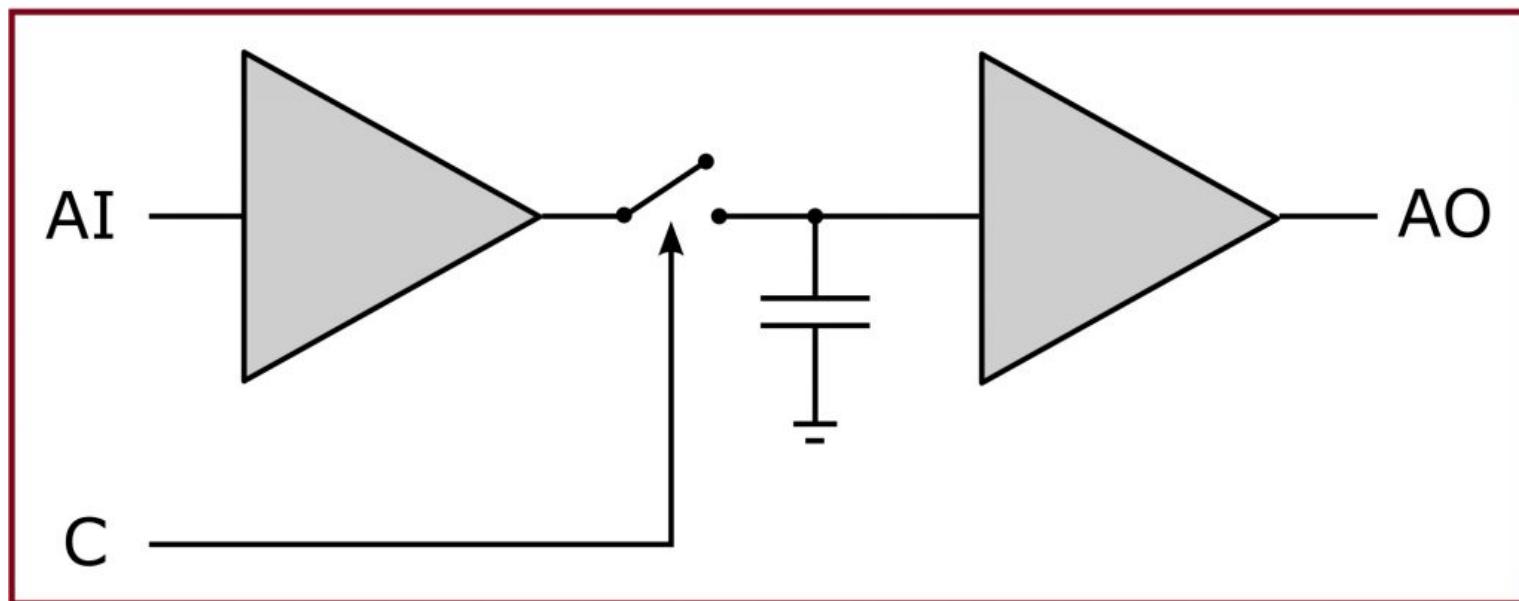


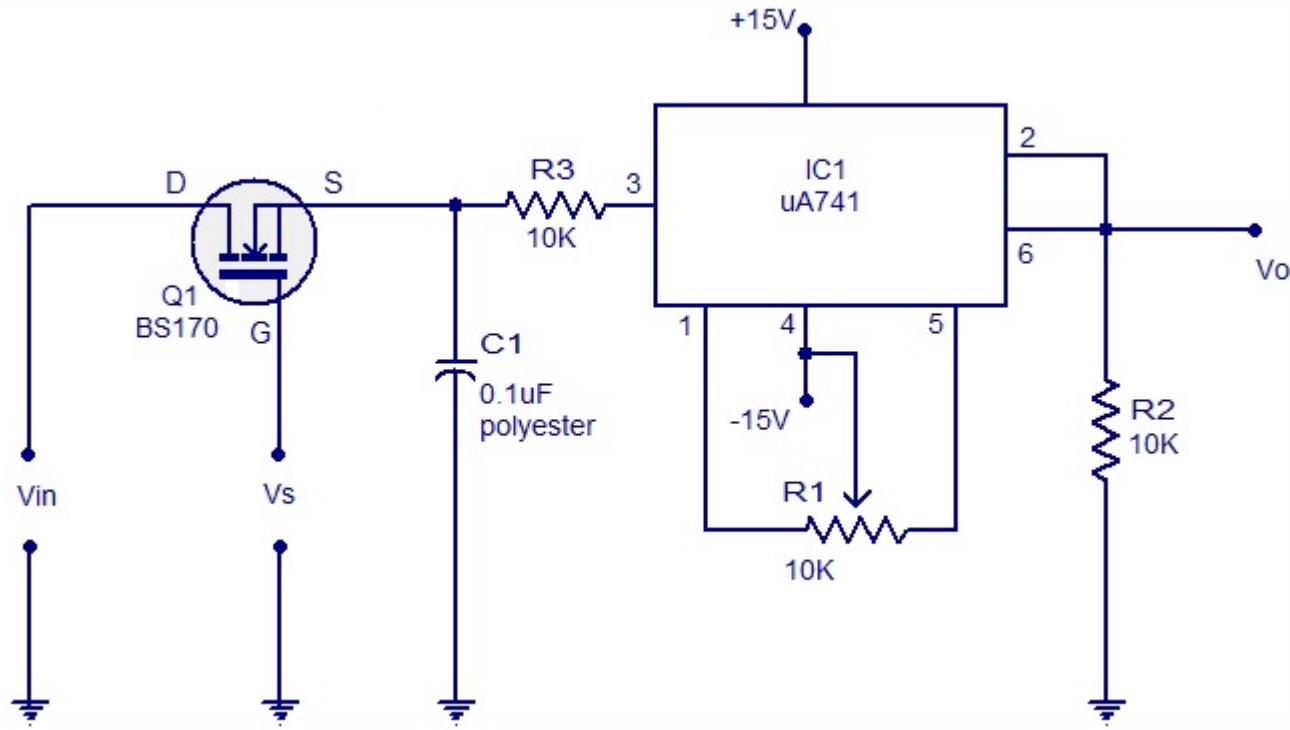
# Sample and Hold

- As the name indicates , a sample and hold circuit is a circuit which samples an input signal and holds onto its last sampled value until the input is sampled again.
- Sample and hold circuits are commonly used in analogue to digital converts, communication circuits, PWM circuits etc.

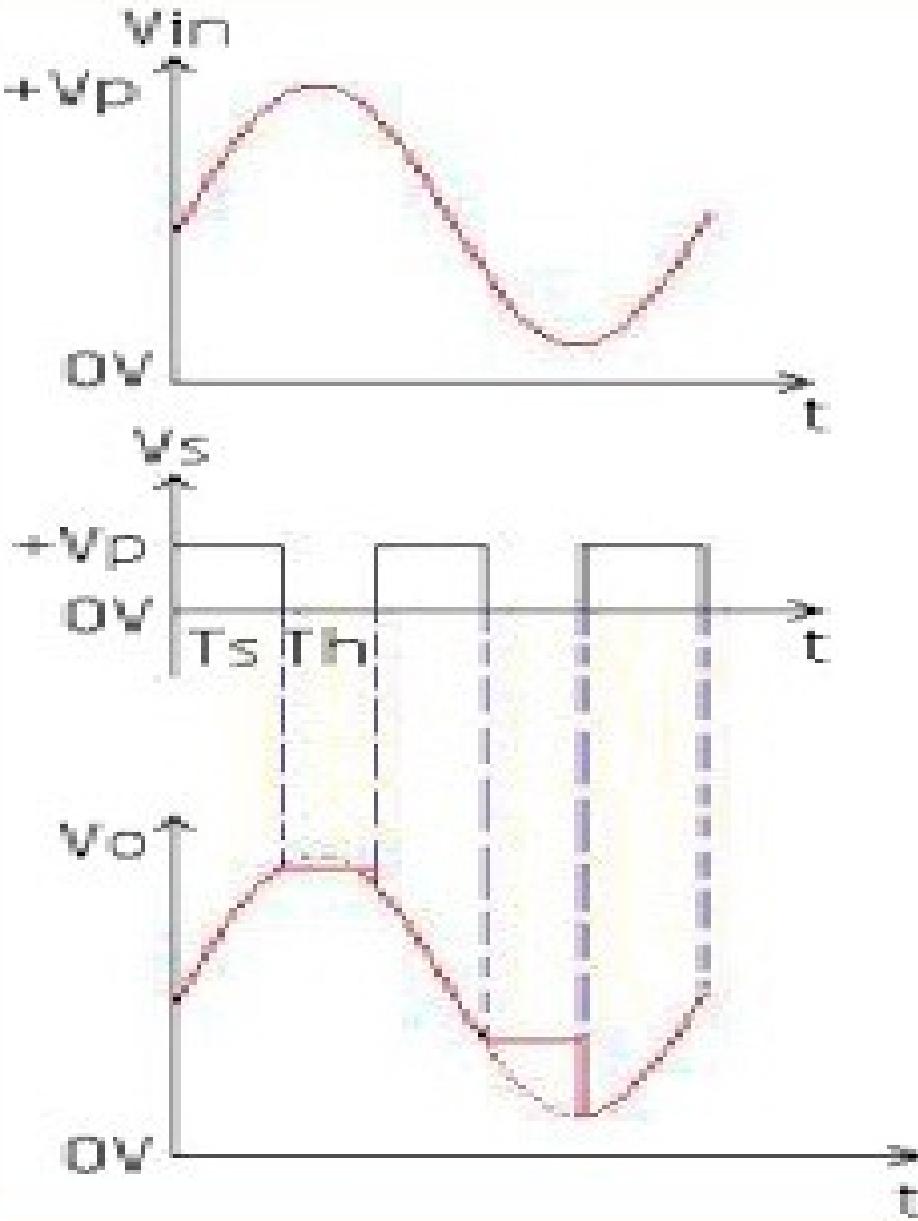


- When the switch is locked sampling method will come into the image and when the switch is unlocked holding outcome will be there. The capacitor allied to the second op-amp is nothing but a holding capacitor.





As a switching element, the N-channel Enhancement MOSFET is used. The input voltage is given via its drain terminal and control voltage is also given through its gate terminal. When the +ve pulse of the control voltage is applied, the MOSFET will be activated state. And it performs as a closed switch. On the opposing, when the control voltage is nothing then the MOSFET will be deactivated state and works as the open switch.

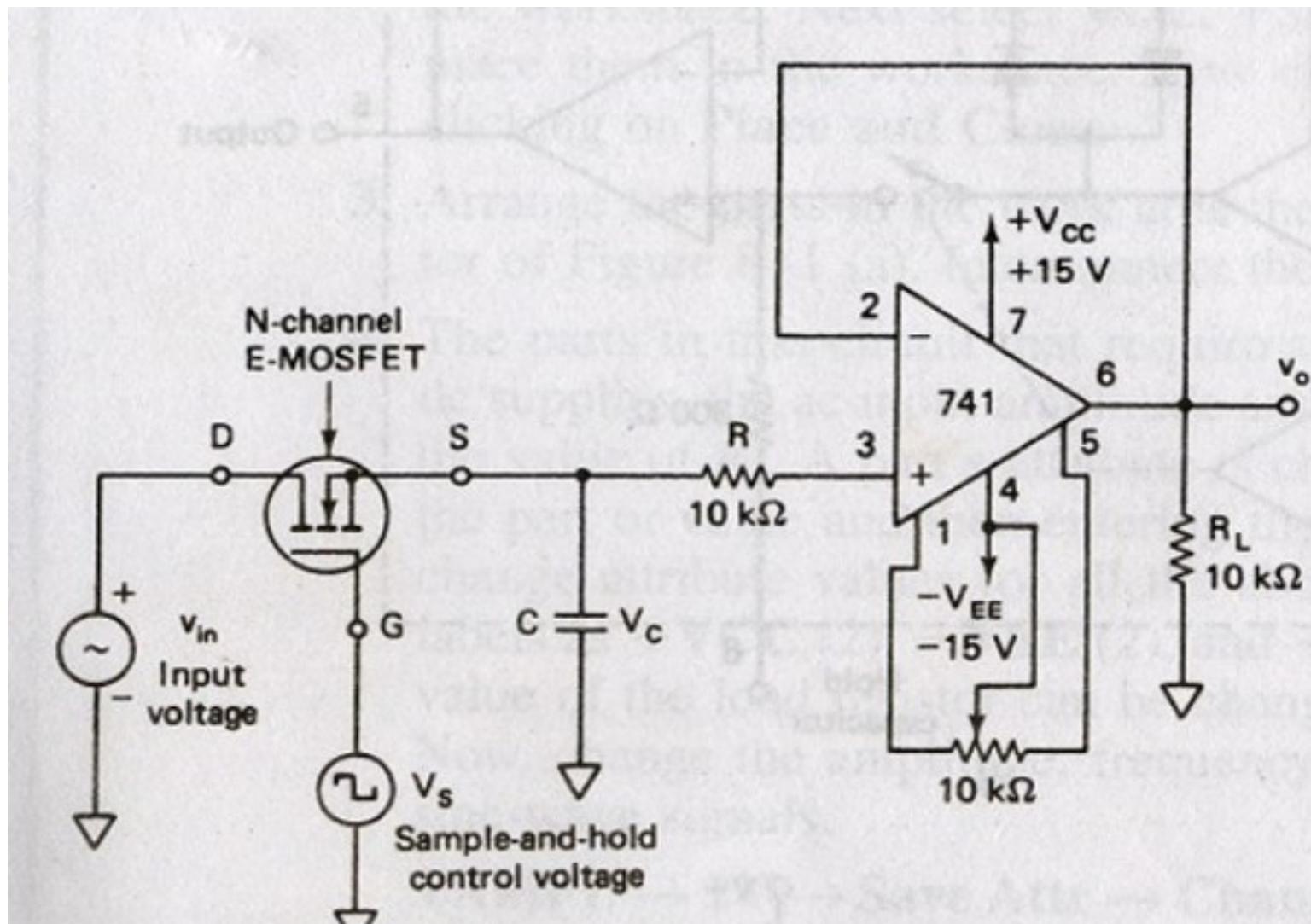


When the MOSFET works as a closed switch, the analog signal given to it through the drain terminal will be fed to the capacitor. Then the capacitor will charge to its peak value. When the switch is released, then the capacitor discontinues charging. Due to the high impedance op-amp connected at the circuit end, the capacitor will knowledge high impedance due to this it cannot get discharged

This directs to the holding of the charge by the capacitor for the exact amount of time. This can be referred as **holding period**. And the time in which samples of i/p voltage is produced is named **sampling period**. The o/p processed by op-amp throughout the holding period. So, holding period holds implication for Op-Amps.

Low leakage capacitors: Teflon, polyethylene

# Sample & Hold Circuit



# References

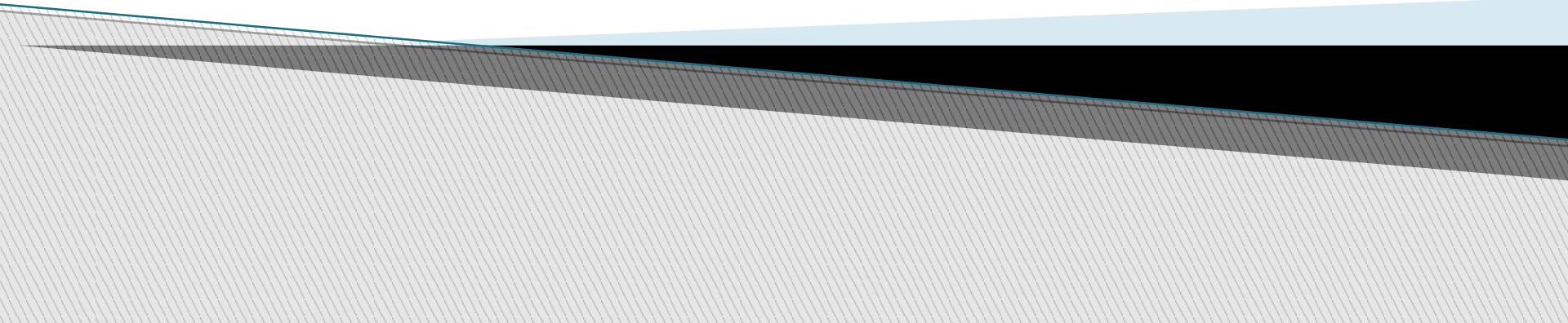
1. Ramakant Gayakwad, "Op-amps and Linear Circuits", Pearson Education, 2000.
2. Salivahanan and Kanchana Bhaskaran, "Linear Integrated Circuits", Tata McGraw Hill.
3. George Clayton and Steve Winder, "Operational Amplifiers", 5<sup>th</sup> Edition, Newness.
4. Sergio Franco, "Design with Operational Amplifiers and Analog Integrated Circuits", Tata McGraw Hill.
5. William Stanley, "Operational Amplifiers with Linear Integrated Circuits," 4<sup>th</sup> Edition, Pearson Education.
6. <http://nptel.ac.in/courses/117107094>
7. [https://www.youtube.com/watch?v=NVj\\_Eu3sJL4](https://www.youtube.com/watch?v=NVj_Eu3sJL4) (Lecture Series by Prof. T. S. Natarajan, Dept. of Physics, IIT Madras).

# References:

- [https://nptel.ac.in/courses/117107094/lecturers/lecture\\_17/lecture17\\_page3.htm](https://nptel.ac.in/courses/117107094/lecturers/lecture_17/lecture17_page3.htm)
- [https://nptel.ac.in/courses/117107094/lecturers/lecture\\_18/lecture18\\_page2.htm](https://nptel.ac.in/courses/117107094/lecturers/lecture_18/lecture18_page2.htm)

# **Unit-4**

## **ACTIVE FILTERS**



# Objectives

- ▶ To understand basics of active filter using op-amp
- ▶ To analyze different types of filters
- ▶ To design first order & second order LPF,HPF,BPF & BRF for different cutoff frequencies.

# Introduction

- Filters are circuits that are capable of *passing signals within a band* of frequencies while *rejecting or blocking* signals of frequencies *outside this band*. This property of filters is also called “frequency selectivity”.
- Filter can be passive or active filter.

**Passive filters:** The circuits built using RC, RL, or RLC circuits.

**Active filters :** The circuits that employ one or more op-amps in the design in addition to resistors and capacitors

# Advantages of Active Filters over Passive Filters

- Active filters can be designed to provide required gain, and hence no attenuation as in the case of passive filters
- No loading problem, because of high input resistance and low output resistance of op-amp.
- Active Filters are cost effective as a wide variety of economical op-amps are available.

# Applications

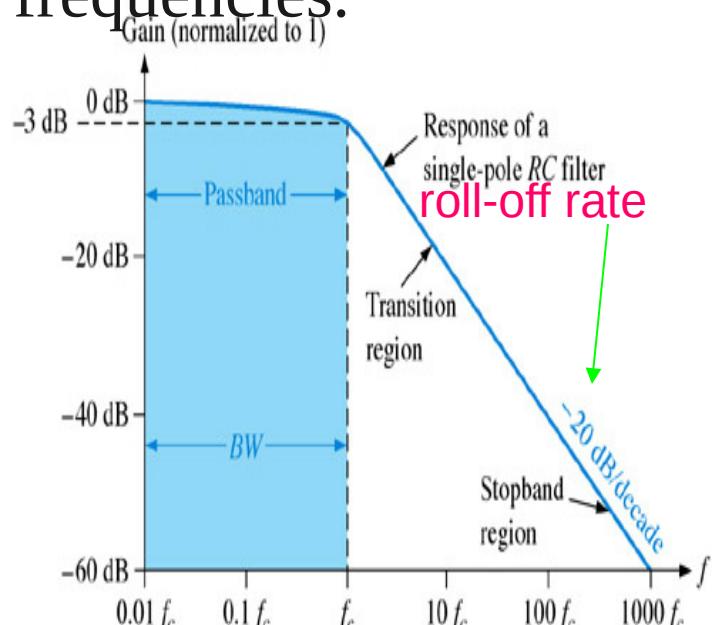
- Active filters are mainly used in communication and signal processing circuits.
- They are also employed in a wide range of applications such as entertainment, medical electronics, etc.

# Active Filters

- There are 5 basic categories of active filters:
  - 1. Low-pass filters**
  - 2. High-pass filters**
  - 3. Band-pass filters**
  - 4. Band-reject filters**
  - 5. All pass filters**
- Each of these filters can be built by using op-amp as the active element combined with RC, RL or RLC circuit as the passive elements.

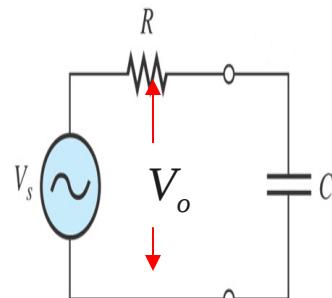
# Low Pass Filter Responses

- A low-pass filter is a filter that passes frequencies from 0Hz to critical frequency,  $f_c$  and significantly attenuates all other frequencies.

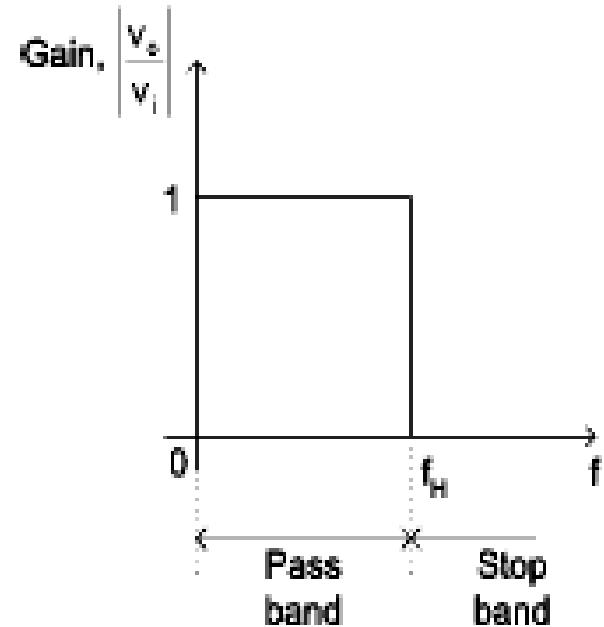


(a) Comparison of an ideal low-pass filter response with actual response

Actual response



(b) Basic low-pass circuit



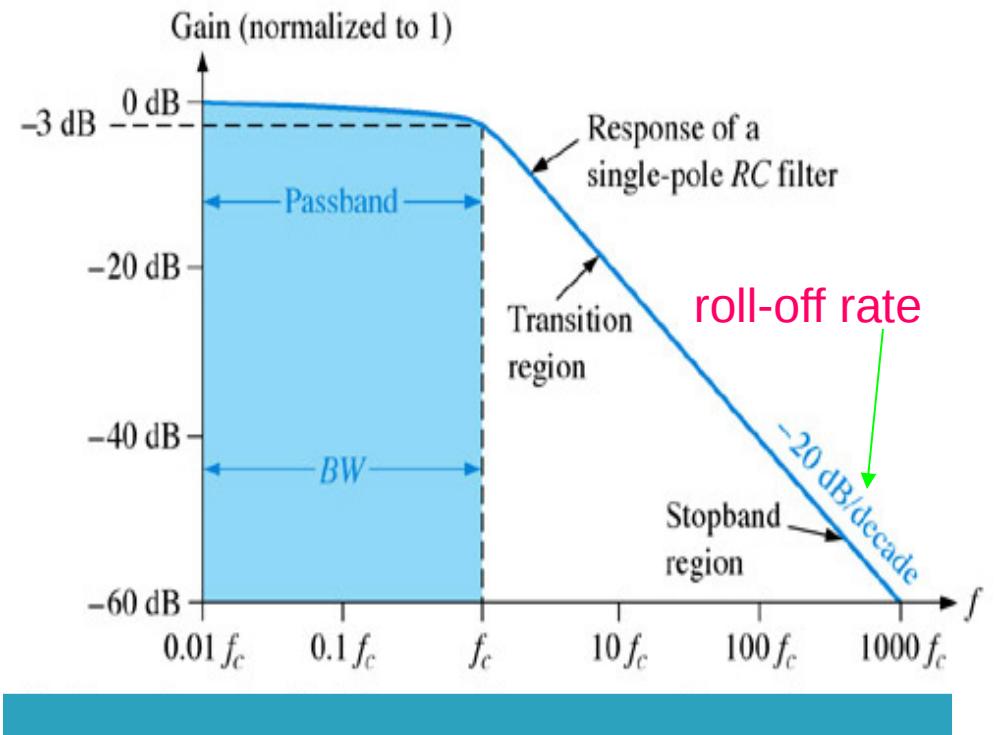
Ideal response

**Passband** of a filter is the range of frequencies that are allowed to pass through the filter with minimum attenuation (usually defined as less than -3 dB of attenuation).

**Transition region** shows the area where the fall-off occurs.

**Stopband** is the range of frequencies that have the most attenuation.

**Critical frequency,  $f_c$** , (also called the cutoff frequency) defines the end of the passband and normally specified at the point where the response drops – 3 dB (70.7%) from the passband response.



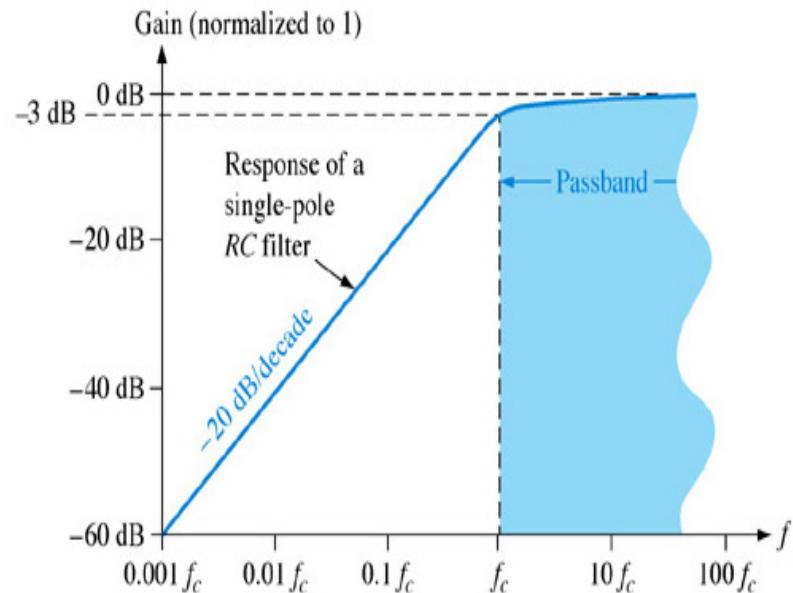
- At low frequencies,  $X_C$  is very high and the capacitor circuit can be considered as open circuit. Under this condition,  $V_o = V_{in}$  or  $A_V = 1$  (unity).
- At very high frequencies,  $X_C$  is very low and the  $V_o$  is small as compared with  $V_{in}$ . Hence the gain falls and drops off gradually as the frequency is increased.

- The bandwidth of an ideal low-pass filter is equal to  $f_c$
- The critical frequency of a low-pass RC filter occurs when  $X_C = R$  and can be calculated using the formula below:

$$f_c = \frac{1}{2\pi RC}$$

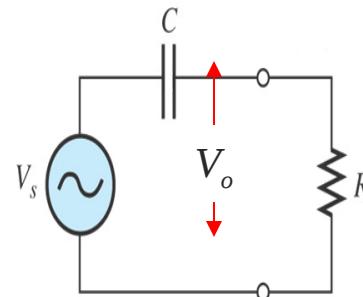
# High Pass Filter Response

- A high-pass filter is a filter that significantly attenuates or rejects all frequencies **below**  $f_c$  and passes all frequencies **above**  $f_c$ .
- The passband of a high-pass filter is all frequencies above the  $f_c$

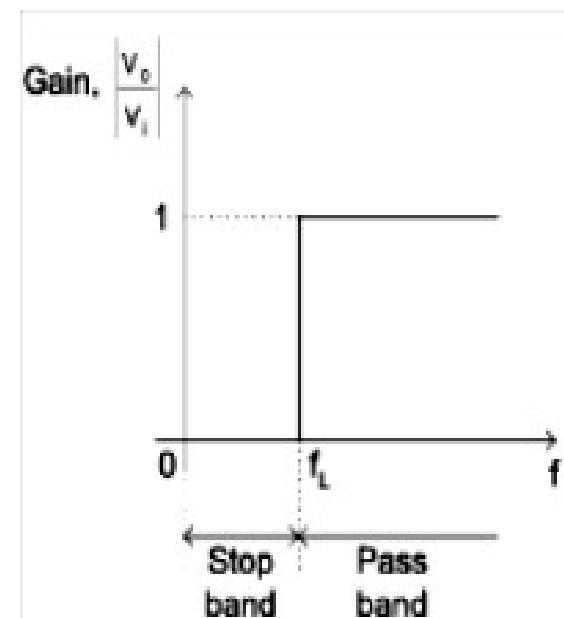


(a) Comparison of an ideal high-pass filter response with actual response

Actual response



(b) Basic high-pass circuit



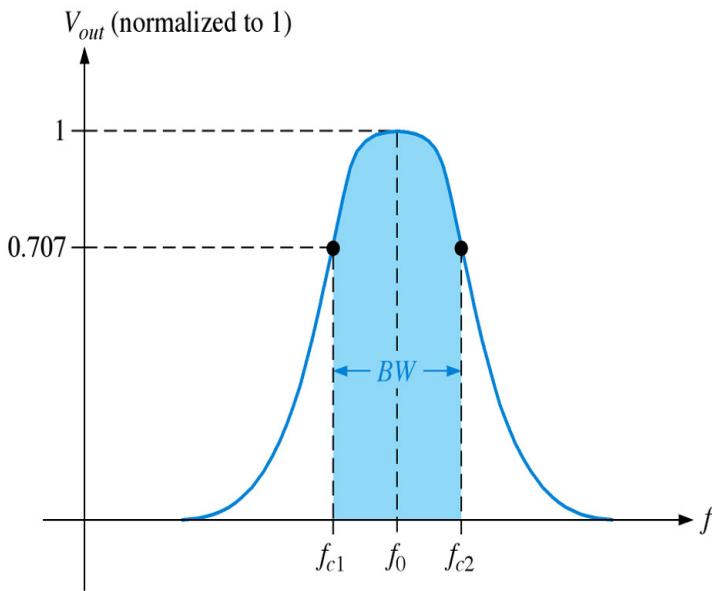
Ideal response

- The critical frequency of a high-pass RC filter occurs when  $X_C = R$  and can be calculated using the formula below:

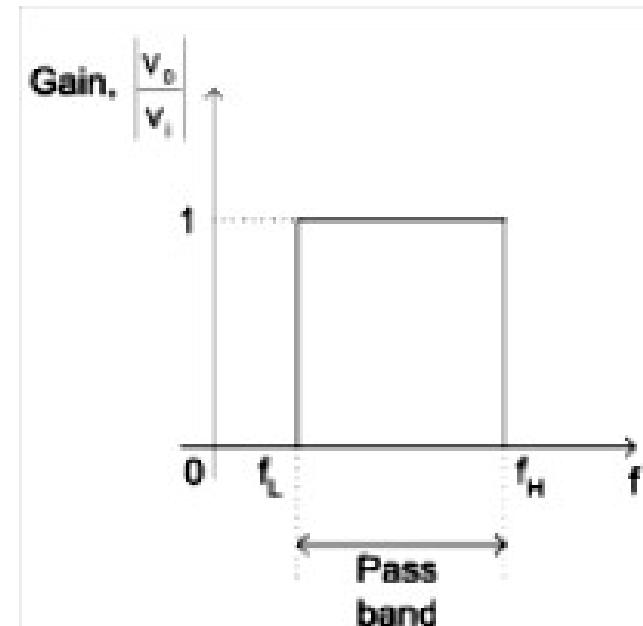
$$f_c = \frac{1}{2\pi RC}$$

# Band Pass Filter Response

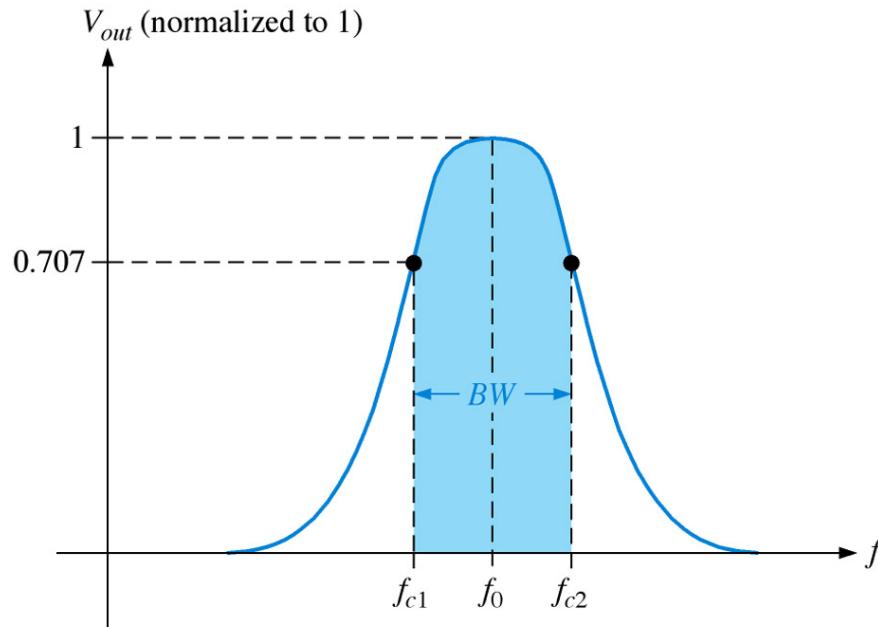
- A band-pass filter passes all signals lying within a band between a lower-frequency limit and upper-frequency limit and essentially rejects all other frequencies that are outside this specified band.



Actual response



Ideal response



- The bandwidth (BW) is defined as the difference between the upper critical frequency ( $f_{c2}$ ) and the lower critical frequency ( $f_{c1}$ ).

$$BW = f_{c2} - f_{c1}$$

- The frequency about which the pass band is centered is called the *center frequency*,  $f_o$  and defined as the geometric mean of the critical frequencies.

$$f_o = \sqrt{f_{c1} f_{c2}}$$

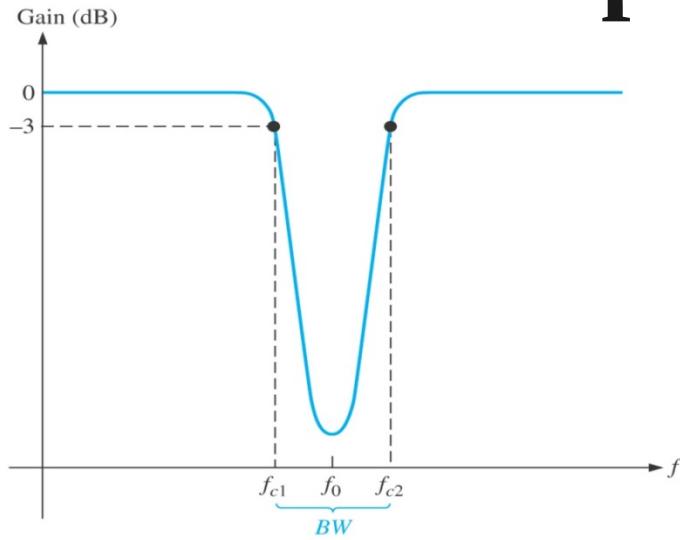
- The ***quality factor (Q)*** of a band-pass filter is the ratio of the center frequency to the bandwidth.

$$Q = \frac{f_o}{BW}$$

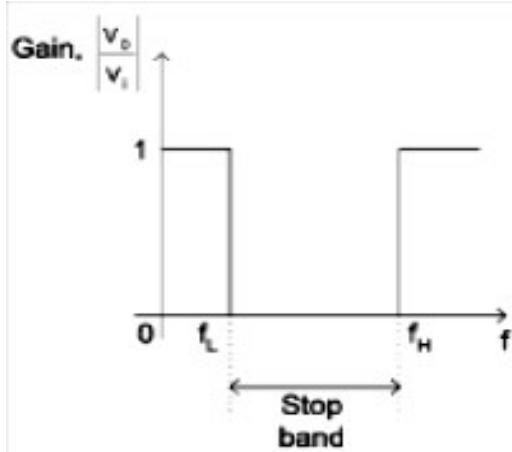
- The higher value of Q, the narrower the bandwidth and the better the selectivity for a given value of  $f_o$ .
- ( $Q > 10$ ) as a narrow-band or ( $Q < 10$ ) as a wide-band
- The quality factor (Q) can also be expressed in terms of the damping factor (DF) of the filter as :

$$Q = \frac{1}{DF}$$

# Band Stop Filter Response



Actual response



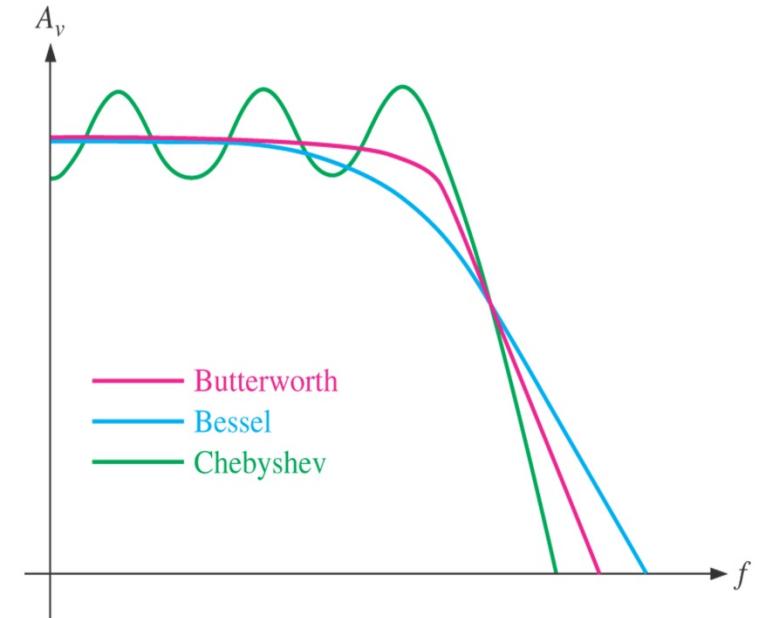
Ideal response

Band-stop filter is a filter which its operation is opposite to that of the band-pass filter because the frequencies within the bandwidth are rejected, and the frequencies above  $f_{c1}$  and  $f_{c2}$  are passed.

- For the band-stop filter, the bandwidth is a band of frequencies between the 3 dB points, just as in the case of the band-pass filter response.

# Filter Approximation

- There are **3** characteristics of filter response :
  - i) **Butterworth** characteristic
  - ii) **Chebyshev** characteristic
  - iii) **Bessel** characteristic.
- Each of the characteristics is identified by the shape of the response curve



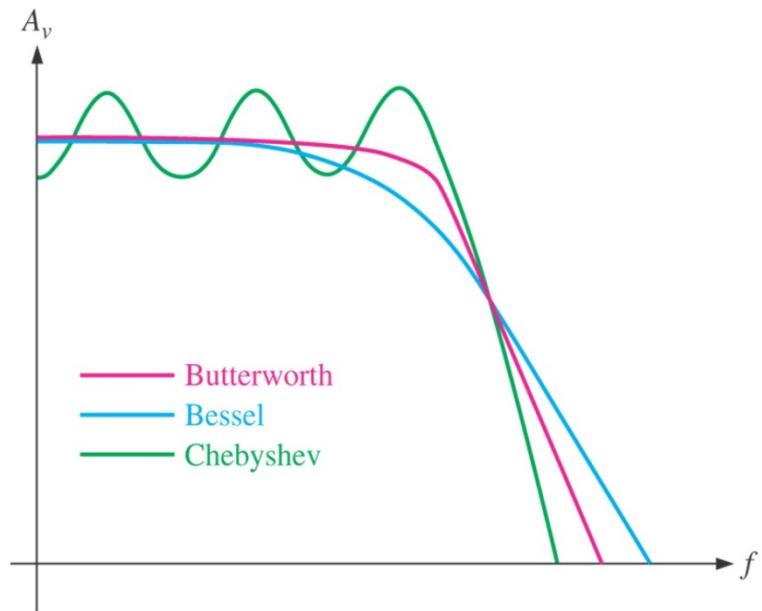
**Comparative plots of three types of filter response characteristics.**

# Butterworth Characteristics

Filter response is characterized by flat amplitude response in the passband.

Provides a roll-off rate of -20 dB/decade/pole.

Filters with the Butterworth response are normally used when all frequencies in the passband must have the *same gain*.



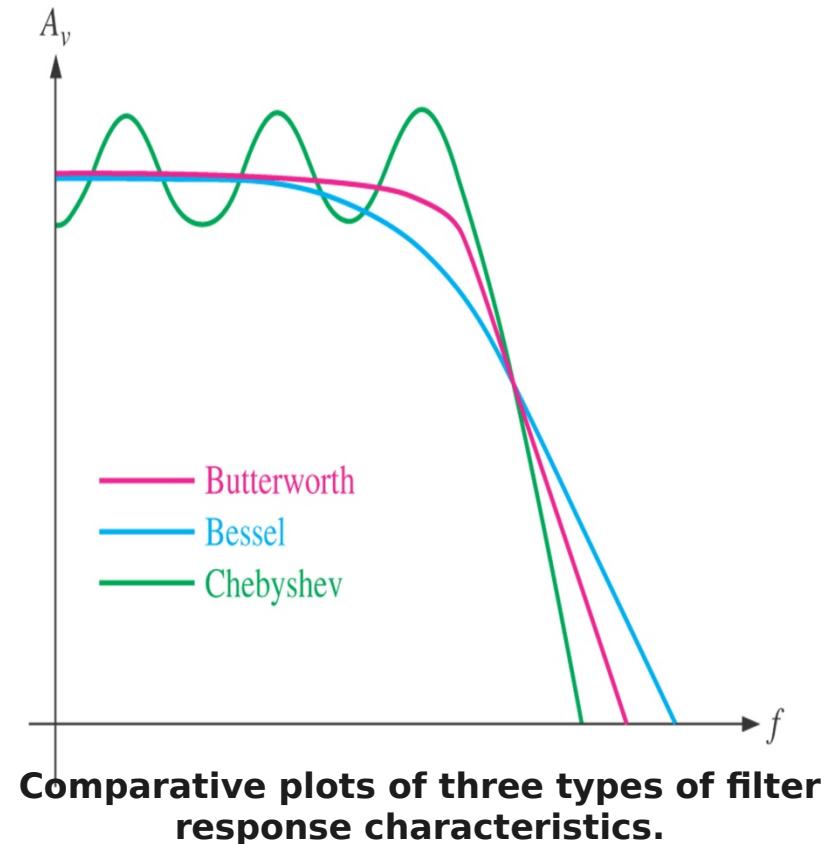
Comparative plots of three types of filter response characteristics.

# Chebyshev Characteristics

Filter response is characterized by overshoot or ripples in the passband.

Provides a roll-off rate greater than -20 dB/decade/pole.

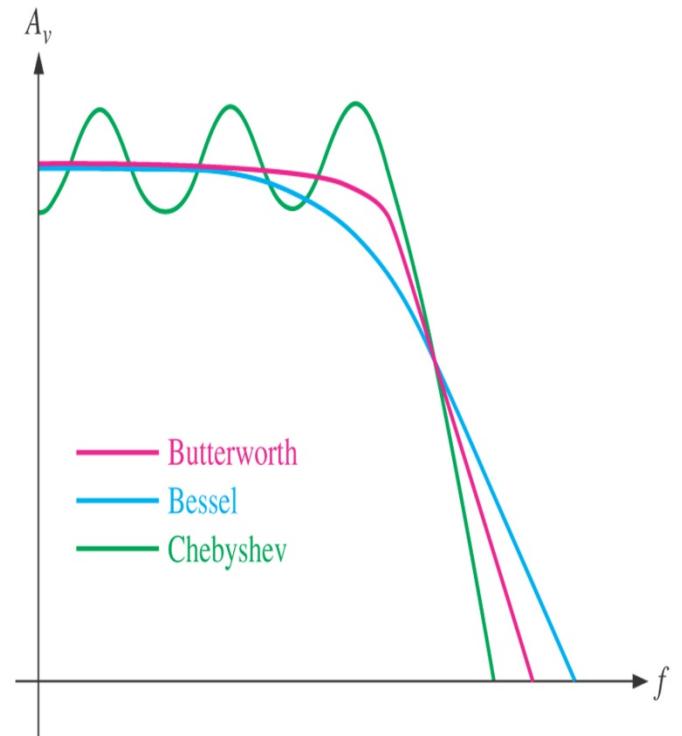
Filters with the Chebyshev response can be implemented with fewer poles and less complex circuitry for a given roll-off rate



# Bessel Characteristics

Filter response is characterized by a linear characteristic, meaning that the phase shift increases linearly with frequency.

Filters with the Bessel response are used for filtering pulse waveforms without distorting the shape of waveform.



**Comparative plots of three types of filter response characteristics.**

# Damping Factor

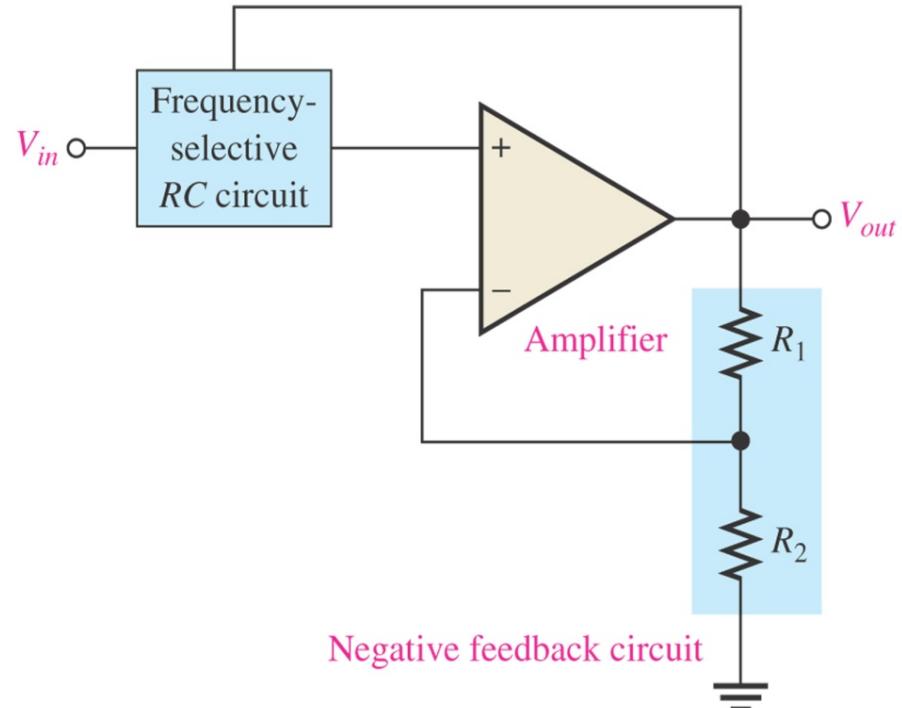
The damping factor (DF) of an active filter determines which response characteristic the filter exhibits.

This active filter consists of an amplifier, a negative feedback circuit and RC circuit.

The amplifier and feedback are connected in a non-inverting configuration.

DF is determined by the negative feedback and defined as :

$$DF = 2 - \frac{R_1}{R_2}$$



**General diagram of active filter**

- The value of DF required to produce a desired response characteristics depends on order (number of poles) of the filter.
- A pole (single pole) is simply one resistor and one capacitor.
- The more poles filter has, the faster its roll-off rate

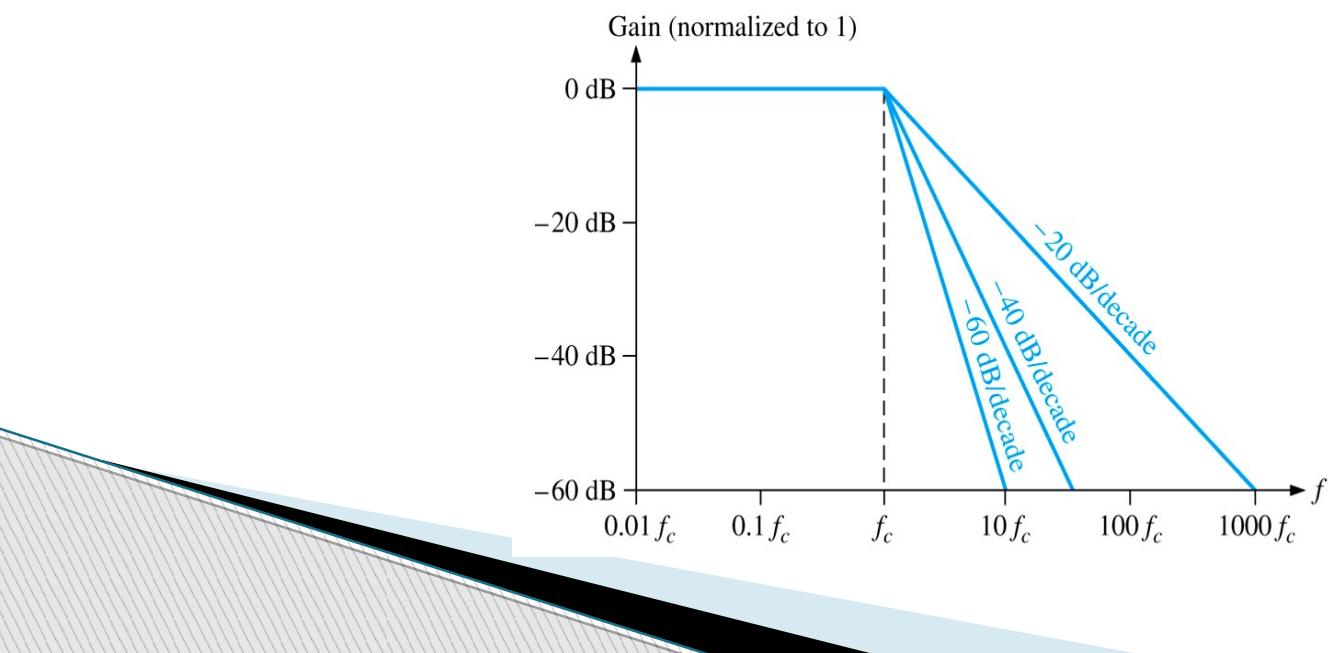
For a single-pole (first-order) filter, the critical frequency is :

$$f_c = \frac{1}{2\pi RC}$$

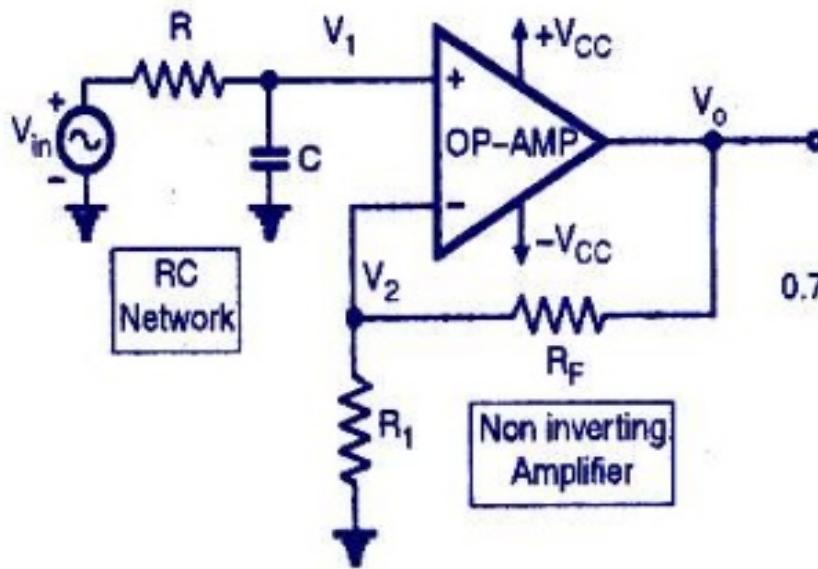
The above formula can be used for both low-pass and high-pass filters.

The number of poles determines the roll-off rate of the filter. For example, a Butterworth response produces -20dB/decade/pole. This means that:

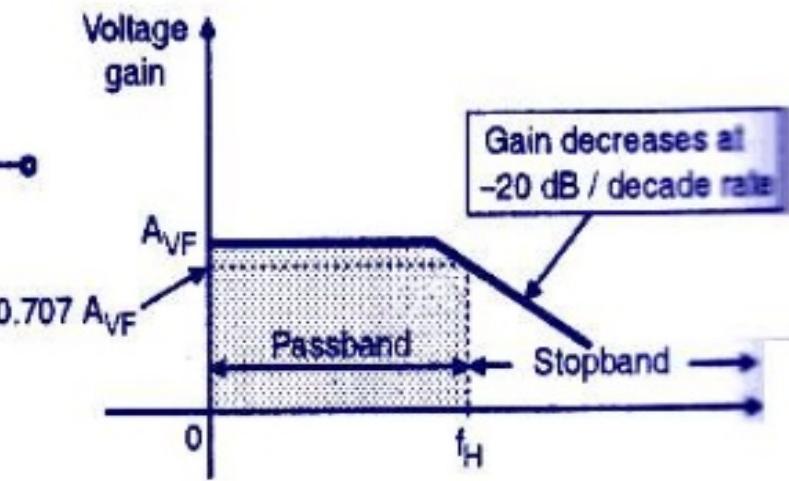
- One-pole (first-order) filter has a roll-off of -20 dB/decade
- Two-pole (second-order) filter has a roll-off of -40 dB/decade
- Three-pole (third-order) filter has a roll-off of -60 dB/decade



# First order lowpass butterworth Filter



(a) First order low-pass filter



(b) Frequency response characteristics

According to the voltage-divider rule, the voltage at the noninverting terminal (across capacitor  $C$ ) is

$$v_1 = \frac{-jX_C}{R - jX_C} v_{in}$$

where

$$j = \sqrt{-1} \quad \text{and} \quad -jX_C = \frac{1}{j2\pi f C}$$

$$v_1 = \frac{v_{in}}{1 + j2\pi f RC}$$

and the output voltage

$$v_o = \left( 1 + \frac{R_F}{R_I} \right) v_1$$

That is,

$$v_o = \left(1 + \frac{R_F}{R_1}\right) \frac{v_{in}}{1 + j2\pi f RC}$$

or

$$\frac{v_o}{v_{in}} = \frac{A_F}{1 + j(f/f_H)}$$

where  $\frac{v_o}{v_{in}}$  = gain of the filter as a function of frequency

$$A_F = 1 + \frac{R_F}{R_1} = \text{passband gain of the filter}$$

$f$  = frequency of the input signal

$$f_H = \frac{1}{2\pi RC} = \text{high cutoff frequency of the filter}$$

The gain magnitude and phase angle equations of the low-pass filter can be obtained by converting Equation (7-1b) into its equivalent polar form, as follows:

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$$
$$\phi = -\tan^{-1} \left( \frac{f}{f_H} \right)$$

where  $\phi$  is the phase angle in degrees.

The operation of the low-pass filter can be verified from the gain magnitude equation, (7-2a):

1. At very low frequencies, that is,  $f < f_H$ ,

$$\left| \frac{v_o}{v_{in}} \right| \approx A_F$$

2. At  $f = f_H$ ,

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{2}} = 0.707A_F$$

3. At  $f > f_H$ ,

$$\left| \frac{v_o}{v_{in}} \right| < A_F$$

# Low pass Filter Design

**Low-pass filter design** The following steps are used for the design of active low-pass filter.

1. Choose the value of high cut-off frequency  $f_H$ .
2. Select the value of capacitor  $C$  such that its value is  $\leq 1 \mu\text{F}$ .
3. When the values  $f_H$  and  $C$  are known, the value of  $R$  can be calculated by using,  $f_H = \frac{1}{2\pi RC}$ .
4. Finally, select the values of  $R_i$  and  $R_f$  depending on the desired passband gain by using,  $A = 1 + \left( \frac{R_f}{R_i} \right)$ .

**Example —** Design a first order low-pass filter at a cut-off frequency of 2kHz with a passband gain of 2.

Solution

Given  $f_H = 2\text{kHz}$  and  $A = 2$

Let  $C = 0.01\mu\text{F}$

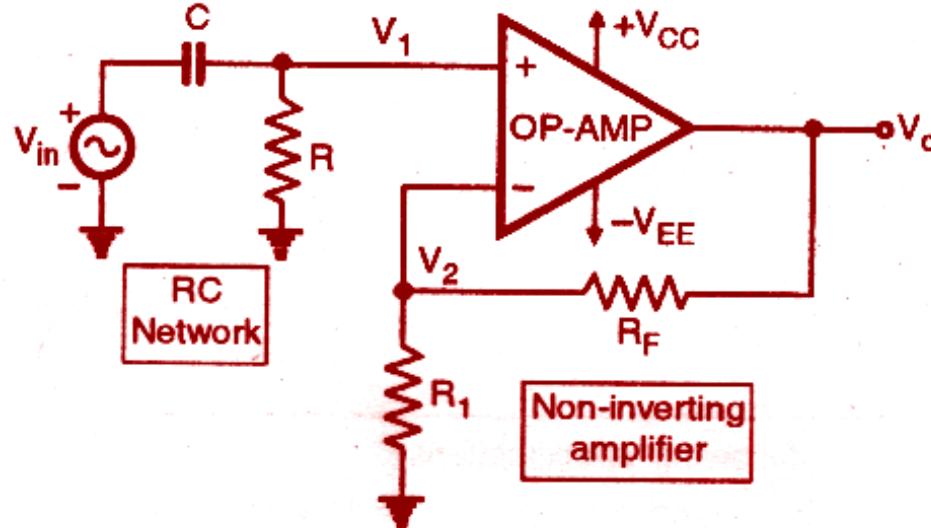
We know that  $f = \frac{1}{2\pi RC}$

$$\text{Therefore, } R = \frac{1}{2\pi fC} = \frac{1}{2\pi(2 \times 10^3) \times 10^{-8}} = 7.95\text{k}\Omega$$

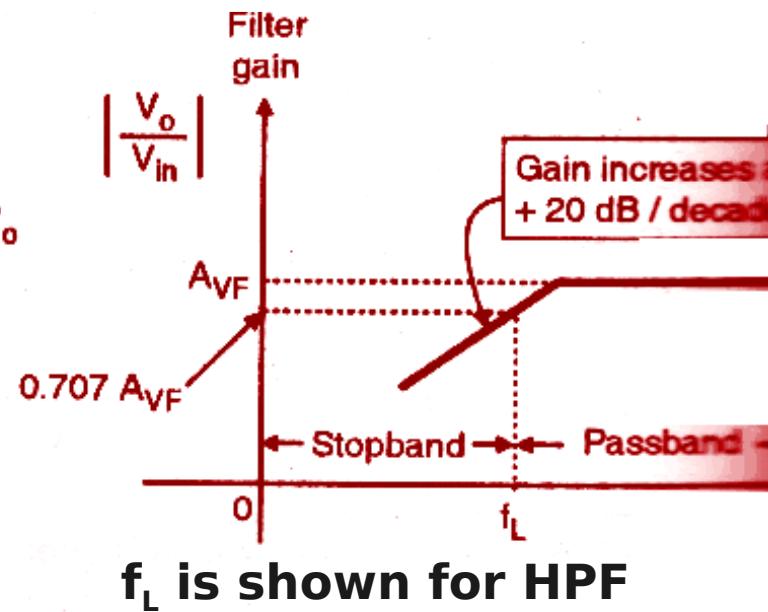
$$A = 1 + \frac{R_f}{R_i} = 2$$

Therefore,  $R_f = R_i = 10\text{k}\Omega$  (say)

# First Order High Pass Filter



(a) First order high-pass filter



(b) Frequency response characteristics

RC components decide the cut off frequency of the HPF where as  $R_F$  &  $R_1$  decide the closed loop gain.

# Expression For The Gain:

**Voltage**  $V_1 = \frac{R}{R - jX_C} V_{in}$

Where  $X_C = \frac{1}{2\pi f C}$

$$f_L = \frac{1}{2\pi R C}$$

$$V_1 = \frac{R}{R - \frac{j}{2\pi f C}} V_{in} = \frac{R}{R + \frac{1}{j 2\pi f C}} = \frac{(R \times j 2\pi f C)}{1 + j 2\pi f R C} V_{in}$$

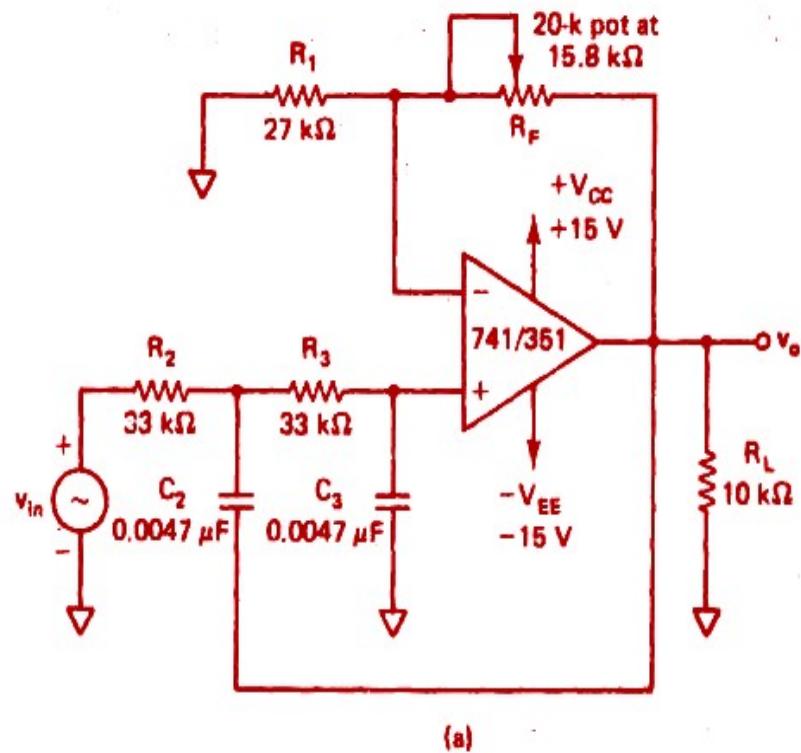
$$\frac{j \left[ \frac{f}{f_L} \right]}{1 + j \left[ \frac{f}{f_L} \right]} V_{in}$$

$$V_0 = A_{VF} \cdot V_1 = \frac{A_{VF} \left[ \frac{j f}{f_L} \right]}{1 + j \frac{f}{f_L}} V_{in}$$

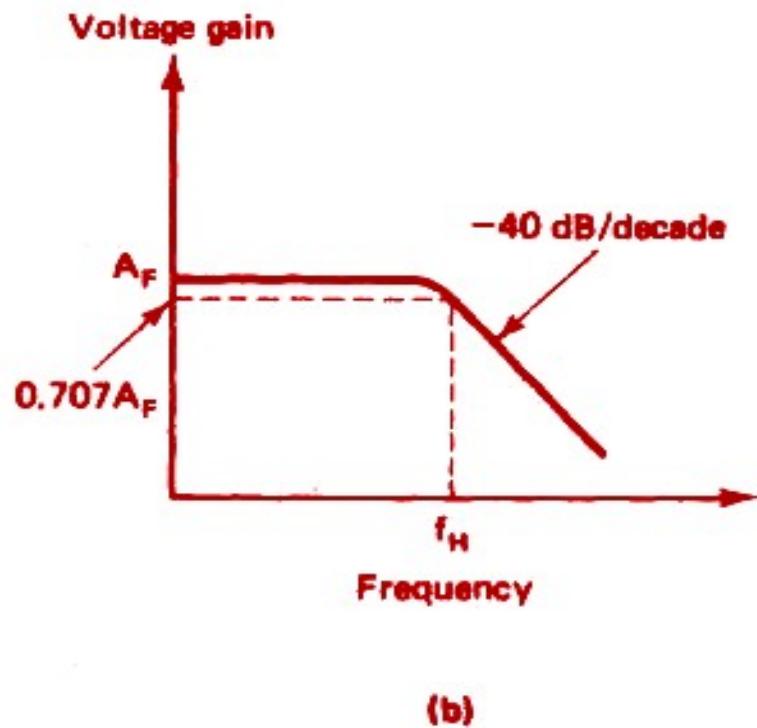
$$\frac{V_0}{V_{in}} = \frac{A_{VF} \left[ \frac{j f}{f_L} \right]}{1 + j \left( \frac{f}{f_L} \right)}$$

**Magnitude** =  $\left| \frac{v_o}{v_{in}} \right| = \frac{A_F(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$

# Second-order Low-pass Butterworth Filter



(a)



(b)

The gain of the second-order filter is set by  $R_1$ , and  $R_F$ , while the high cutoff frequency  $f_H$  is determined by  $R_2$ ,  $C_2$ ,  $R_3$ , and  $C_3$ , as follows:

**High Cutoff frequency,**

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_f}{\sqrt{1 + \left( \frac{f}{f_H} \right)^4}}$$

$$A_F = 1 + \frac{R_F}{R_1}$$

**A<sub>F</sub> = 1.586 for 2<sup>nd</sup> order Butterworth Filter**

# Second order low pass filter design

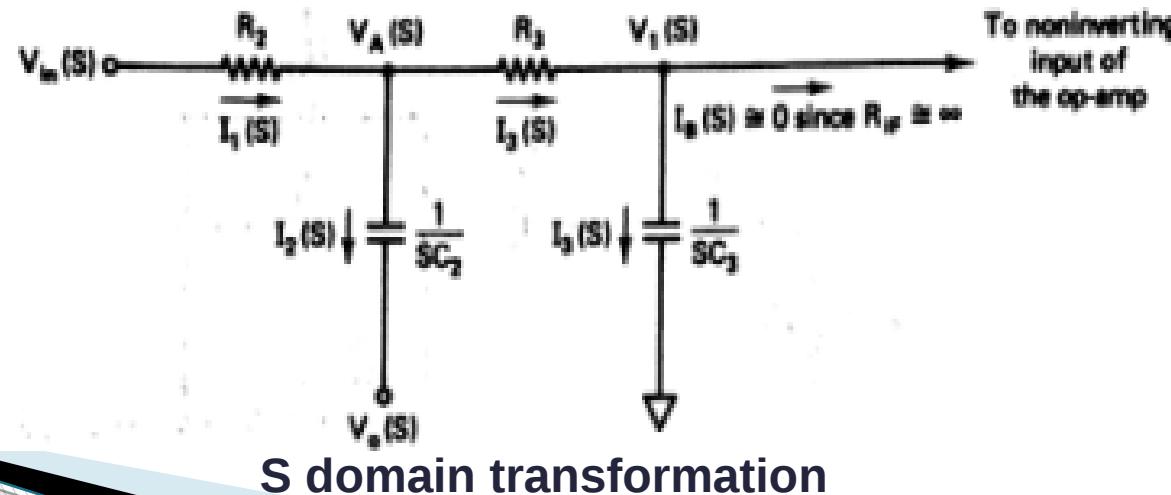
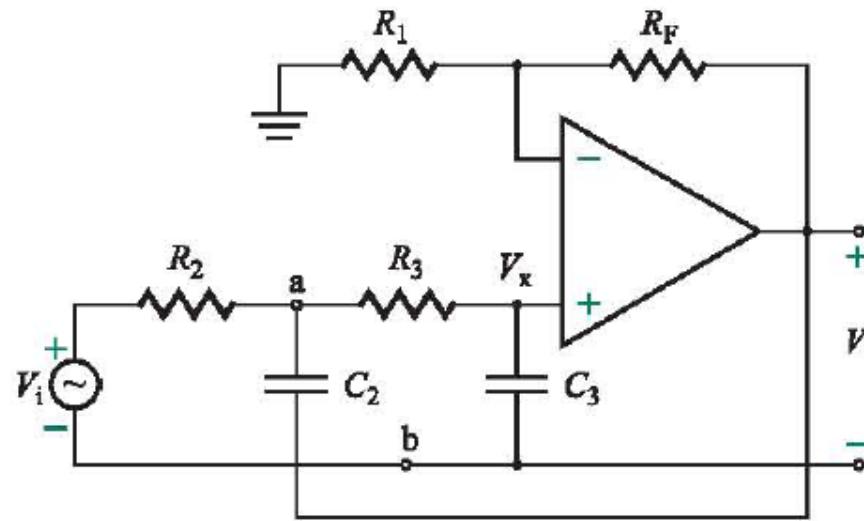
1. Choose a value for the high cutoff frequency  $f_H$
2. To simplify the design calculations, set

$$R_2 = R_3 = R \text{ and } C_2 = C_3 = C.$$

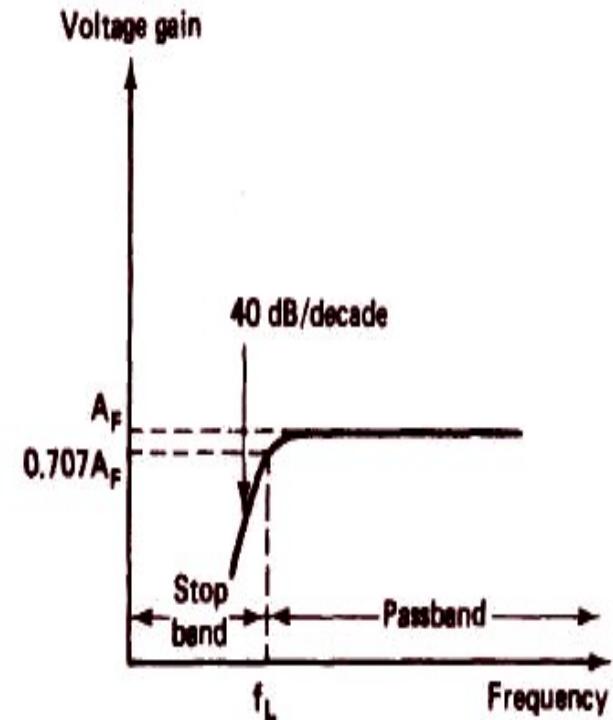
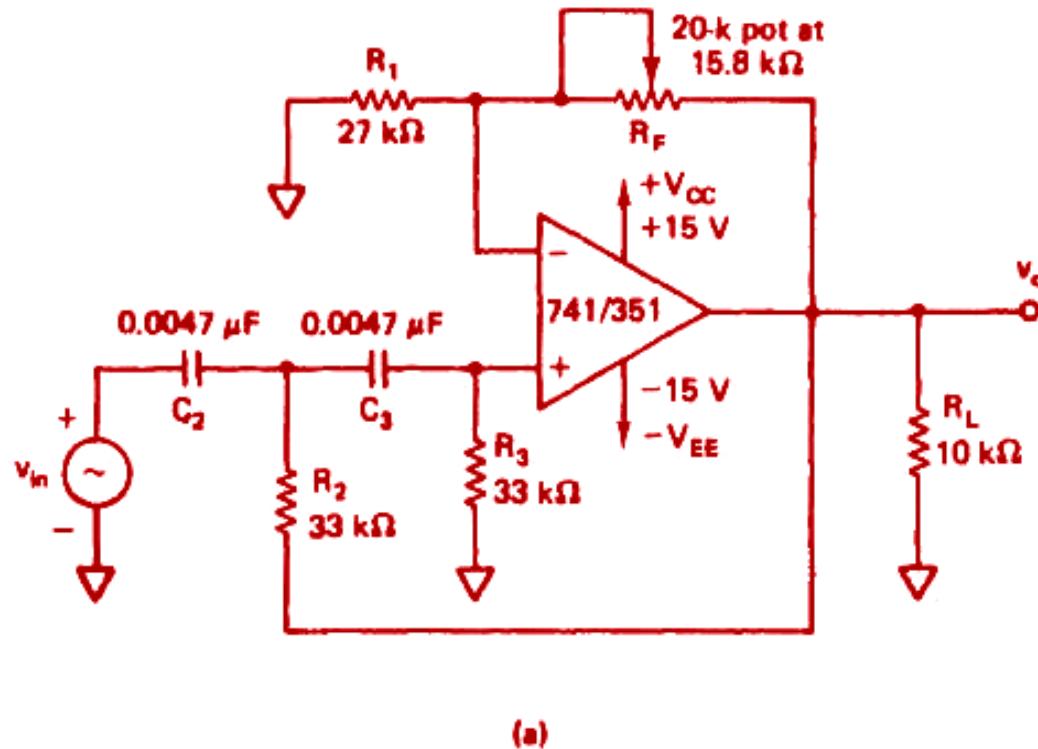
Then choose a value of  $C \leq 1\mu\text{F}$

3. Calculate the value of  $R$  using Equation for  $f_H$ :  $\frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$
4. Finally, because of the equal resistor ( $R_2 = R_3$ ) and capacitor ( $C_2 = C_3$ ) values, the pass band voltage gain  $A_F = (1 + R_F/R_1)$  of the second-order low-pass filter has to be equal to 1.586.  
That is,  $R_F = 0.586/R_1$
5. This gain is necessary to guarantee Butterworth response.  
Hence choose a value of  $R_1 < 100 \text{ k}\Omega$  and calculate the value of  $R_F$ .

# Second- Order Low-Pass Butterworth Filter



# Second-order High-pass Butterworth Filter



# Second-order High-pass Butterworth Filter

As in the case of the first-order filter, a second-order high-pass filter can be formed from a second-order low-pass filter simply by interchanging the frequency determining resistors and capacitors.

$$f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{1 + \left( \frac{f_L}{f} \right)^4}}$$

**A<sub>F</sub> = 1.586 for 2<sup>nd</sup> order  
Butterworth Filter**

# Band Pass Filter

A bandpass filter has pass band between two cut off frequencies  $f_H$  and  $f_L$ . Such that  $f_H > f_L$ .

Any input frequency outside this is attenuated

Two types of band pass filter

- 1) Wide bandpass whose quality factor  $Q < 10$
- 2) Narrow bandpass filter whose quality factor  $Q > 10$

Thus  $Q$  is measure of selectivity that means if  $Q$  is higher then the filer is more selective and its bandwidth is narrow.

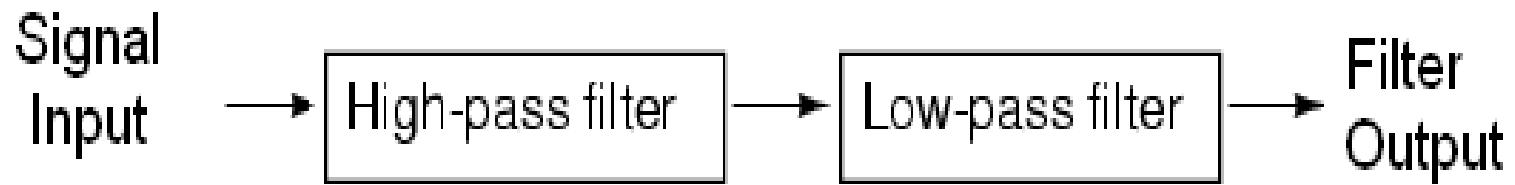
The relationship between  $Q$ , the 3-dB BW and center frequency  $f_C$  is given by ,

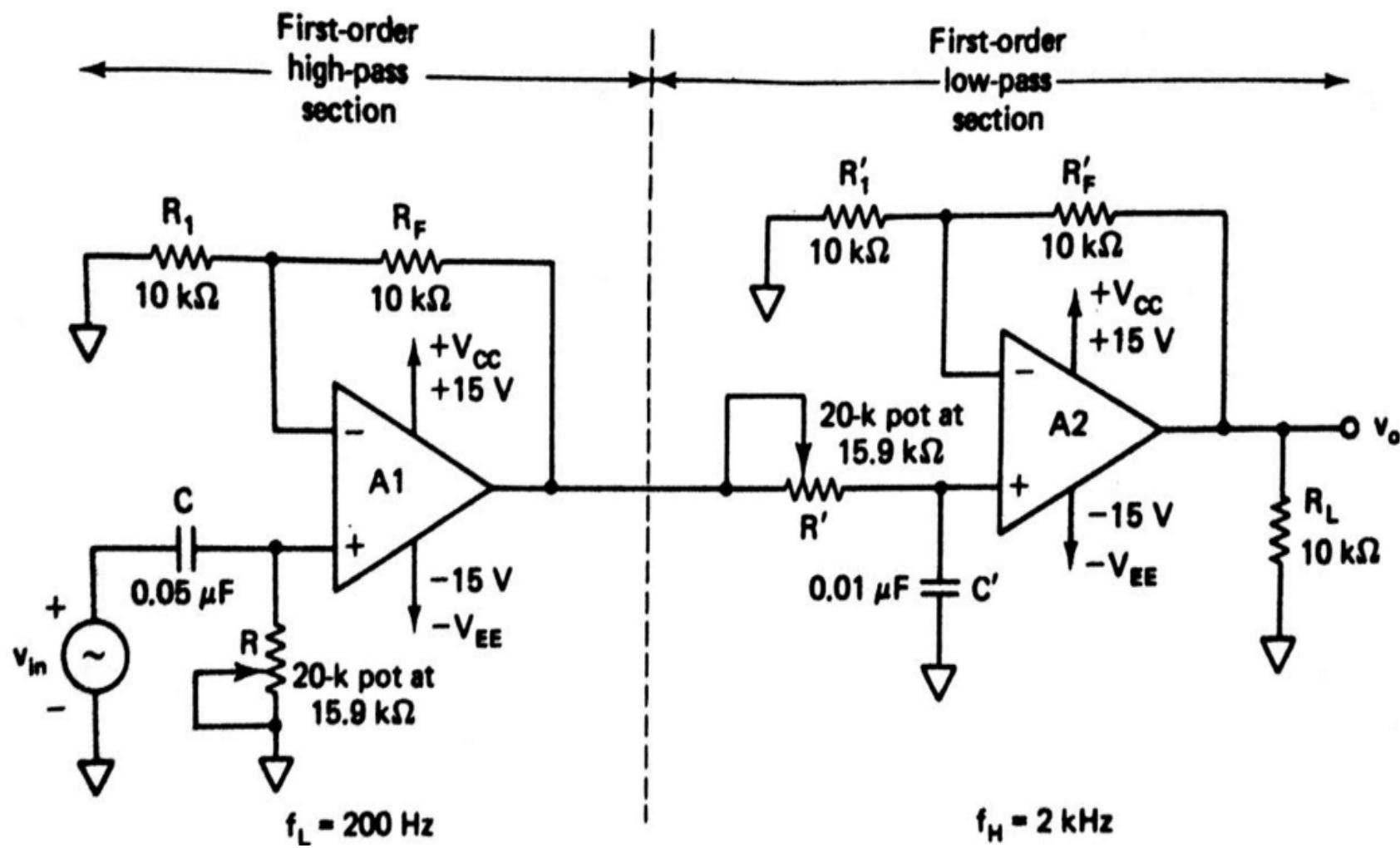
$$Q = \frac{f_C}{\text{BW}} = \frac{f_C}{f_H - f_L}$$

For wide bandpass filter the center frequency  $f_C$  can be defined as,

$$f_C = \sqrt{f_H f_L}$$

# Block Diagram Of Band pass Filter





**Example 1 :Design a wide bandpass filter with  $f_L=200\text{hz}$  and  $f_H$  is  $1 \text{ kHz}$  and passband gain=4.**

a. Draw the frequency response plot of this filter .

B. Calculate the value of Q for filter.

(a) A low-pass filter with  $f_H = 1 \text{ kHz}$  was designed in Example 7-1; therefore, the same values of resistors and capacitors can be used here, that is,  $R' = 15.9 \text{ k}\Omega$  and  $C' = 0.01 \mu\text{F}$ . As in the case of the high-pass filter, it can be designed by following the steps of section 7-3-1:

1.  $f_L = 200 \text{ Hz}$ .
2. Let  $C = 0.05 \mu\text{F}$ .
3. Then

$$R = \frac{1}{2\pi f_L C} = \frac{1}{(2\pi)(200)(5)(10^{-8})}$$
$$= 15.9 \text{ k}\Omega$$

Since the band-pass gain is 4, the gain of the high-pass as well as low-pass sections could be set equal to 2. That is, input and feedback resistors must be equal in value. say  $10 \text{ k}\Omega$  each.

- (b) The voltage gain magnitude of the band-pass filter is equal to the product of the voltage gain magnitudes of the high-pass and low-pass filters. Therefore, from Equations

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_{PT}(f/f_L)}{\sqrt{[1 + (f/f_L)^2][1 + (f/f_H)^2]}}$$

where  $A_{PT}$  = total passband gain

$f$  = frequency of the input signal (Hz)

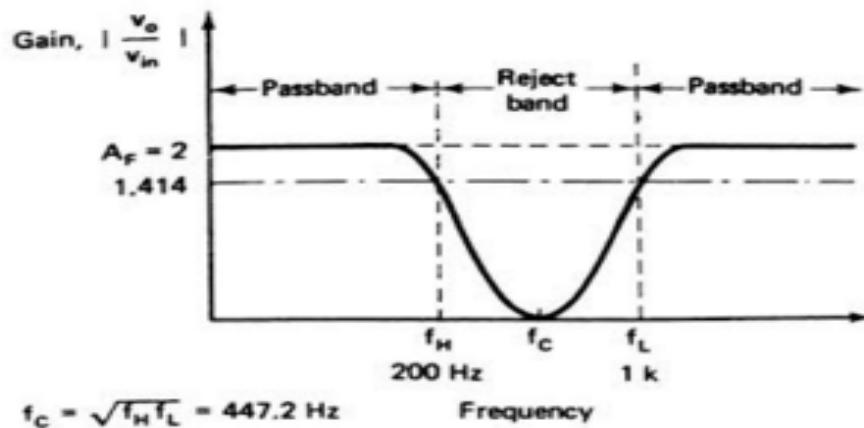
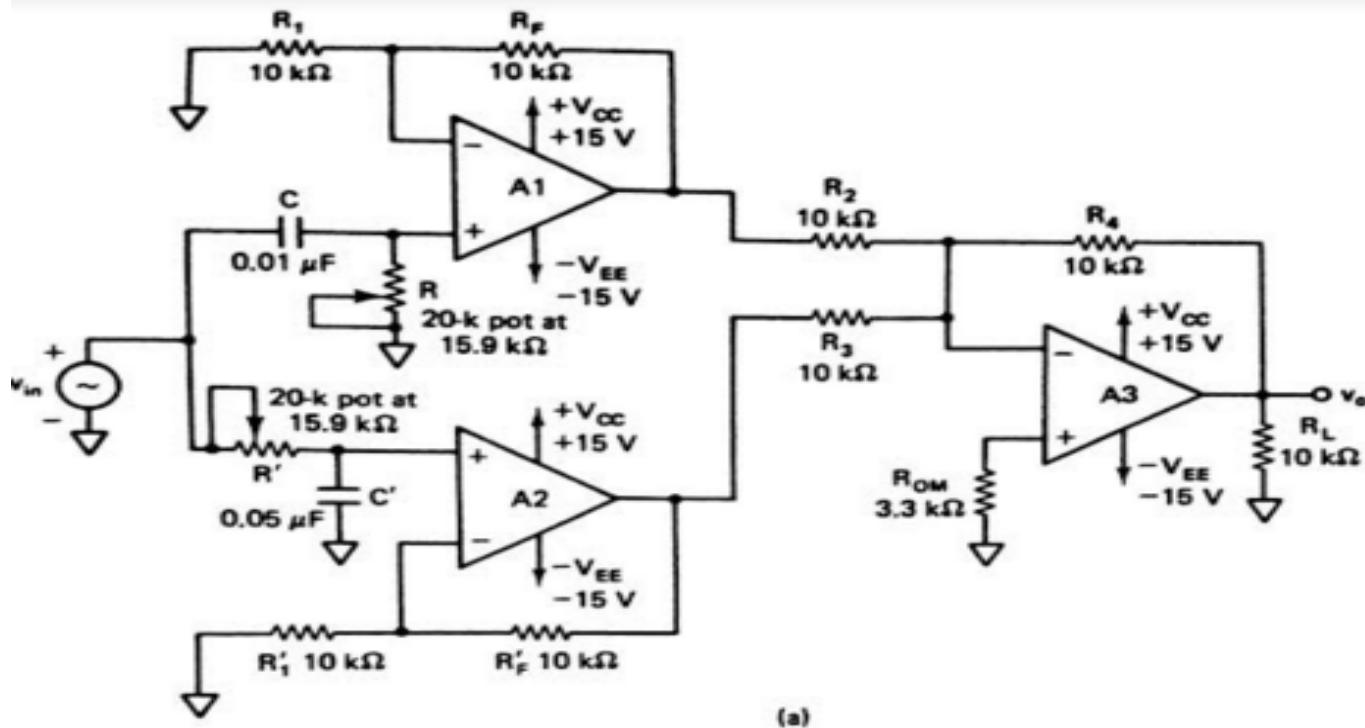
$f_L$  = low cutoff frequency (Hz)

$f_H$  = high cutoff frequency (Hz)

Here  $A_{PT} = 4$ ,  $f_L = 200$  Hz, and  $f_H = 1$  kHz. The frequency response data in Table 7-5 are obtained by substituting into Equation (7-10) the values of  $f$  from 10 Hz to 10 kHz.

$$f_C = \sqrt{(1000)(200)} = 447.2 \text{ Hz}$$

# Band stop filter



# Band Reject filter

- It is also called as bandstop or band elimination filter
- In this filter frequencies are attenuated in the stopband while they are passed outside this band
- It can be classified as 1)wide band reject 2)narrow band reject
- The narrow band reject filter is also known as notch filter which has  $Q > 10$  and its bandwidth is much smaller than wideband reject filter
- wideband reject filter consist of LPF, HPF and summing amplifier.
- To realize this  $f_L$  of HPL must be greater than  $f_H$  of LPF and the passband gain of both the filters must be equal

## Example: Design the wide band reject filter so that a. $f_L = 1 \text{ kHz}$ , $f_H = 200 \text{ Hz}$

a wide band-pass filter was designed with  $f_L = 200 \text{ Hz}$  and  $f_H = 1 \text{ kHz}$ . In this example these band frequencies are interchanged, that is,  $f_L = 1 \text{ kHz}$  and  $f_H = 200 \text{ Hz}$ . This means that we can use the same components as in Example 1, but interchanged between high-pass and low-pass sections. Therefore, for the low-pass section,  $R' = 15.9 \text{ k}\Omega$  and  $C' = 0.05 \mu\text{F}$ , while for the high-pass section

$$R = 15.9 \text{ k}\Omega \text{ and } C = 0.01 \mu\text{F}$$

Since there is no restriction on the passband gain, use a gain of 2 for each section. Hence let

$$R_1 = R_F = R'_1 = R'_F = 10 \text{ k}\Omega$$

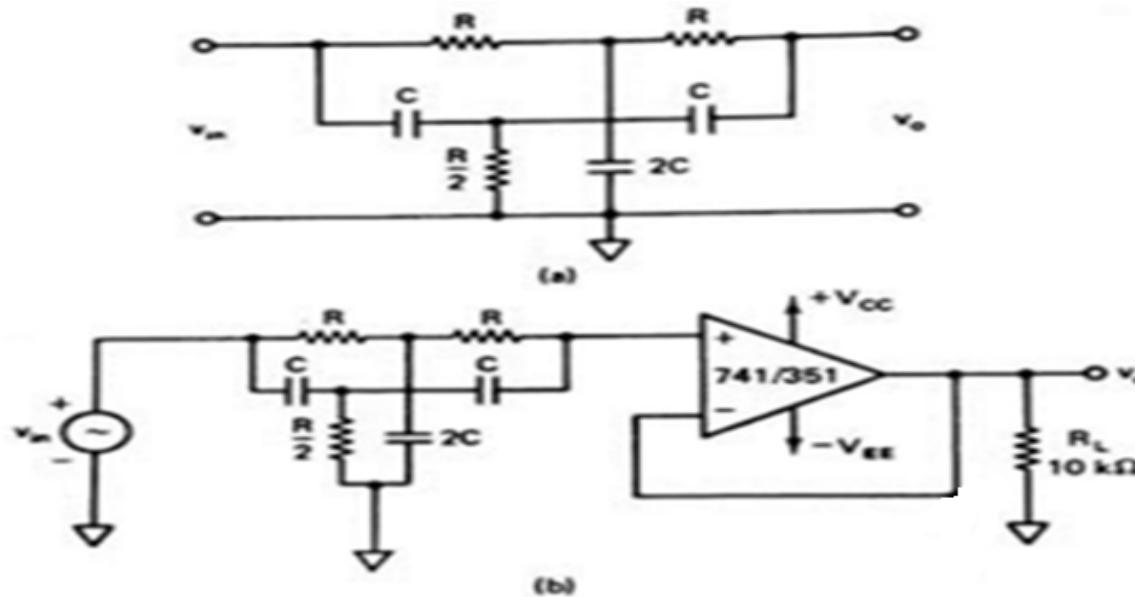
Furthermore, the gain of the summing amplifier is set at 1; therefore,

$$R_2 = R_3 = R_4 = 10 \text{ k}\Omega$$

Finally, the value of  $R_{OM} = R_2 \parallel R_3 \parallel R_4 \cong 3.3 \text{ k}\Omega$ .

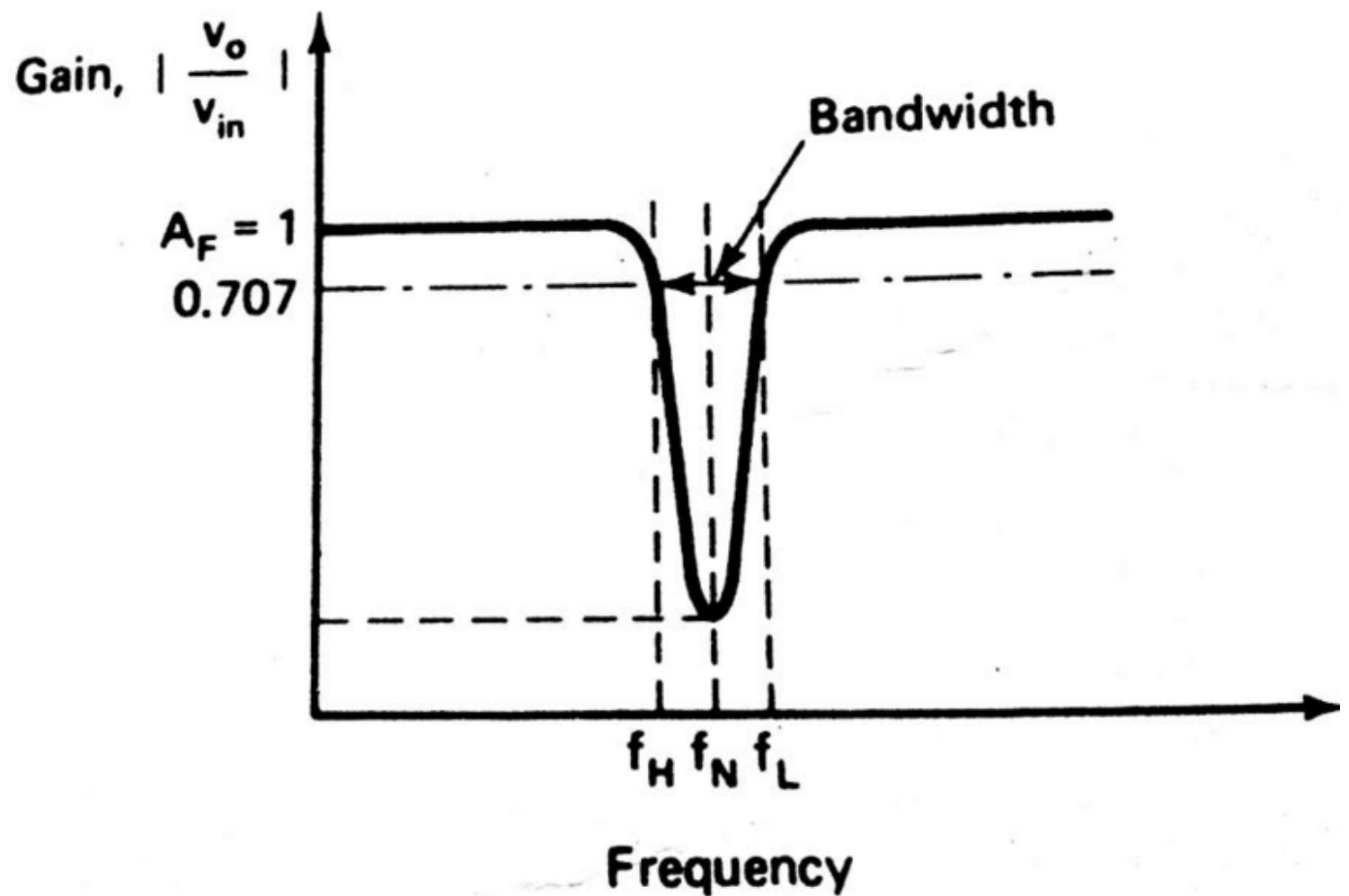
The complete circuit is shown in Figure 7–14(a), and its response is shown in Figure 7–14(b). The voltage gain changes at the rate of 20 dB/decade above  $f_H$  and below  $f_L$ , with a maximum attenuation occurring at  $f_C$ .

# Narrow Band pass filter



It is also known as notch filter , is commonly used for the rejection of single frequency such as 60Hz power line frequency hum. The most commonly used notch filter is the twin-T network .

# Frequency Response



The notch-out frequency is the frequency  $f_N$  at which the maximum attenuation occurs and it is given by

$$f_N = \frac{1}{2\pi RC}$$

The passive twin-T network has a relatively low figure of merit Q. The Q of the network can be increased significantly if it is used with the voltage follower.

It is mostly used in communication and biomedical instruments for eliminating undesired frequency

# Example : Design a 60 Hz active notch filter

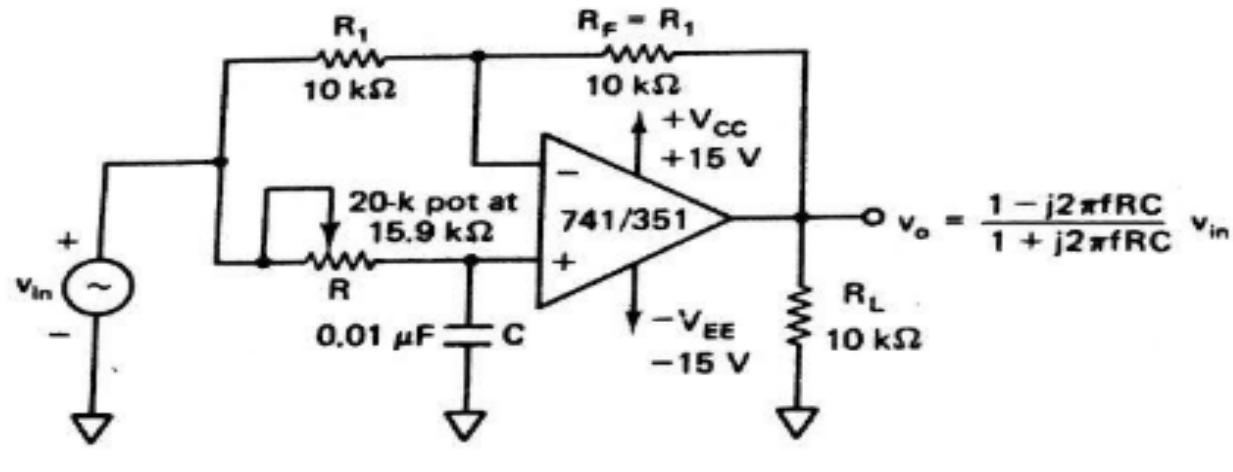
Let  $C = 0.068 \mu\text{F}$ . Then, from Equation  $f_N = \frac{1}{2\pi RC}$

the value of  $R$  is

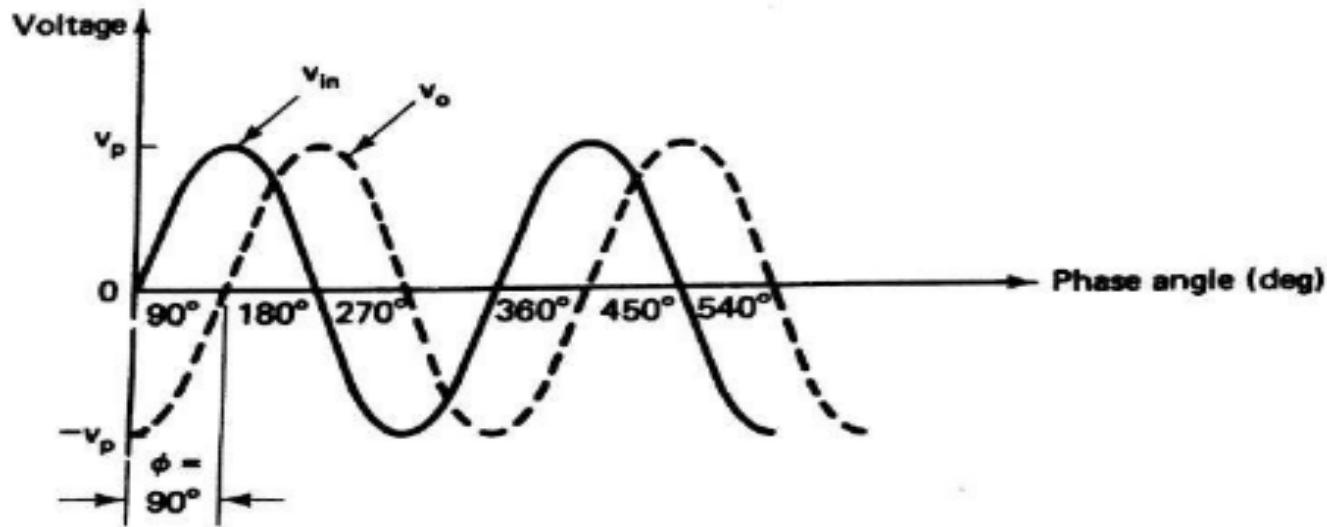
$$R = \frac{1}{2\pi f_N C} = \frac{1}{(2\pi)(60)(68)(10^{-9})} = 39.01 \text{ k}\Omega$$

(Use 39 k $\Omega$ .) For  $R/2$ , parallel two 39-k $\Omega$  resistors; for the  $2C$  component, parallel two 0.068- $\mu\text{F}$  capacitors.

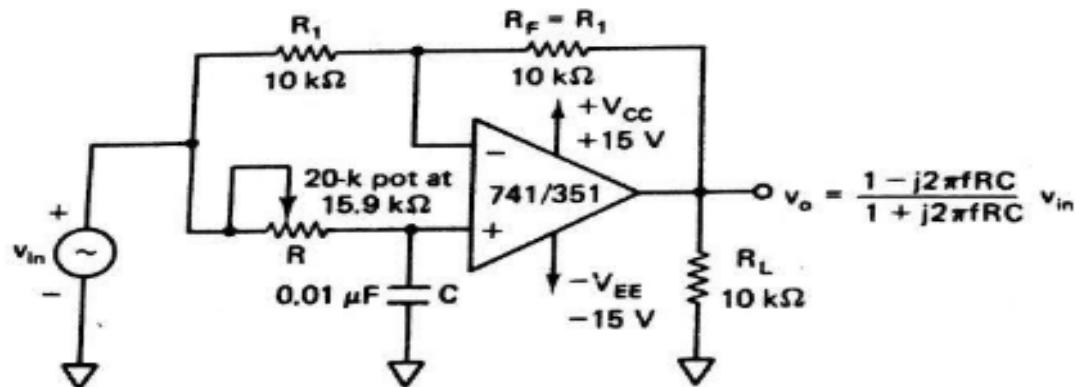
# All Pass Filter



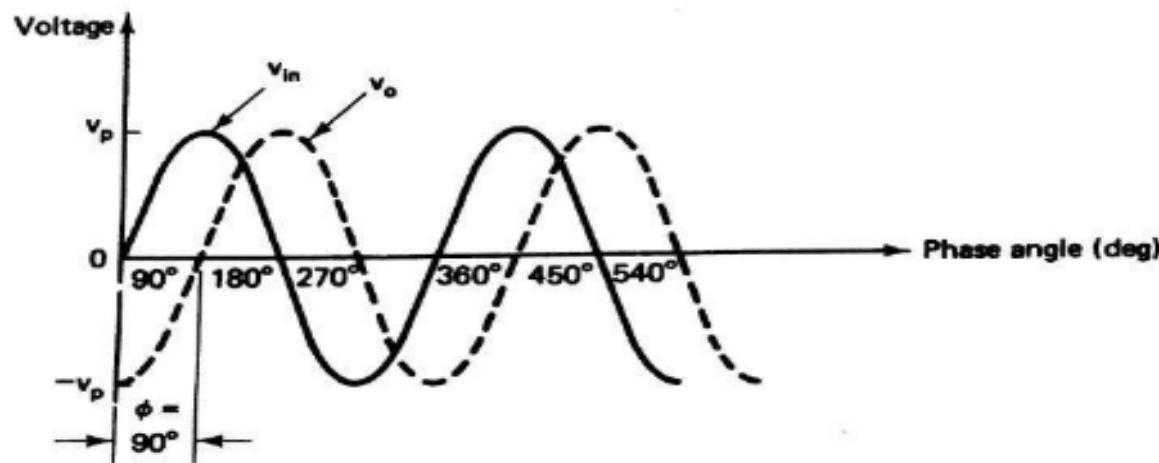
(a)



# ALL PASS FILTER



(a)



# All Pass Filter

- It passes all frequency components of the input signal without attenuation, while providing predictable phase shifts for different frequencies of the input signal.
- When signals are transmitted over transmission lines, such as telephone wires, they undergo change in phase.
- To compensate for these phase changes, all pass filters are required . It is also known as delay equalizers or phase correctors.

➤ In all pass filter  $R_F = R_1$  and the output voltage  $V_o$  can be obtained by using the superposition theorem .

$$V_o = -V_{in} + \frac{-jXc}{R - jXc} V_{in} \quad (2)$$

Substituting  $X_c = 1/2\pi f C$  and simplifying above equation we get,

$$\frac{v_o}{v_{in}} = \frac{1 - j2\pi f RC}{1 + j2\pi f RC}$$

where, f is the input signal frequency

The amplitude of  $\frac{v_o}{v_{in}}$  is unity throughout the useful frequency range and the phase shift between  $V_o$  and  $V_{in}$  is a function of input frequency f.

The phase angle  $\phi$  is given by,

$$\phi = -2\tan^{-1}\left(\frac{2\pi f RC}{1}\right)$$

The  $V_o$  lags  $V_{in}$  by  $90^\circ$

For fixed values of R and C the phase angle changes from  $0$  to  $-180^\circ$  as the frequency  $f$  is varied from zero to infinity.

If the positions of R and C are interchanged, the phase shift between input and output becomes positive i.e  $V_o$  leads  $V_{in}$  by  $90^\circ$ .

Example: For the Allpass filter find phase angle if the frequency of  $V_{in}$  is 1 kHz.

$$\phi = -2 \tan^{-1} \left( \frac{2\pi f RC}{1} \right)$$

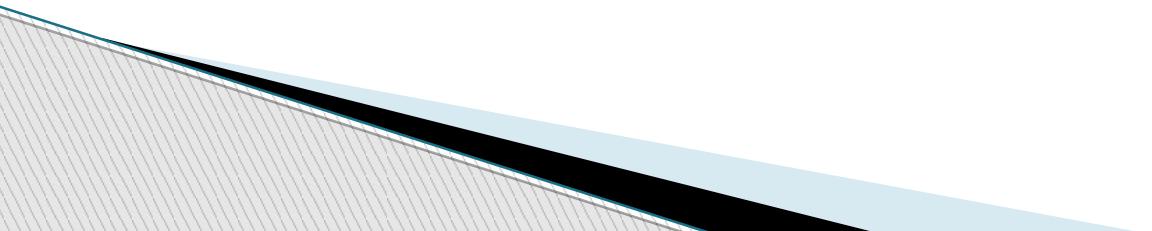
$$\begin{aligned}\phi &= -2 \tan^{-1} \left[ \frac{(2\pi)(10^3)(15.9)(10^3)(10^{-8})}{1} \right] \\ &= -90^\circ\end{aligned}$$

This means that the output voltage  $v_o$  has the same frequency and amplitude but lags  $v_{in}$  by  $90^\circ$

# Reference

- 1.Ramakant A. Gaikwad, “Op Amps and Linear Integrated Circuits”, Pearson Education 2000.
- 2.Salivahanan and KanchanaBhaskaran, “Linear Integrated Circuits”, Tata McGraw Hill,India 2008

# Thank You.



# ADC

## Analog to Digital Converter

# Conversion process

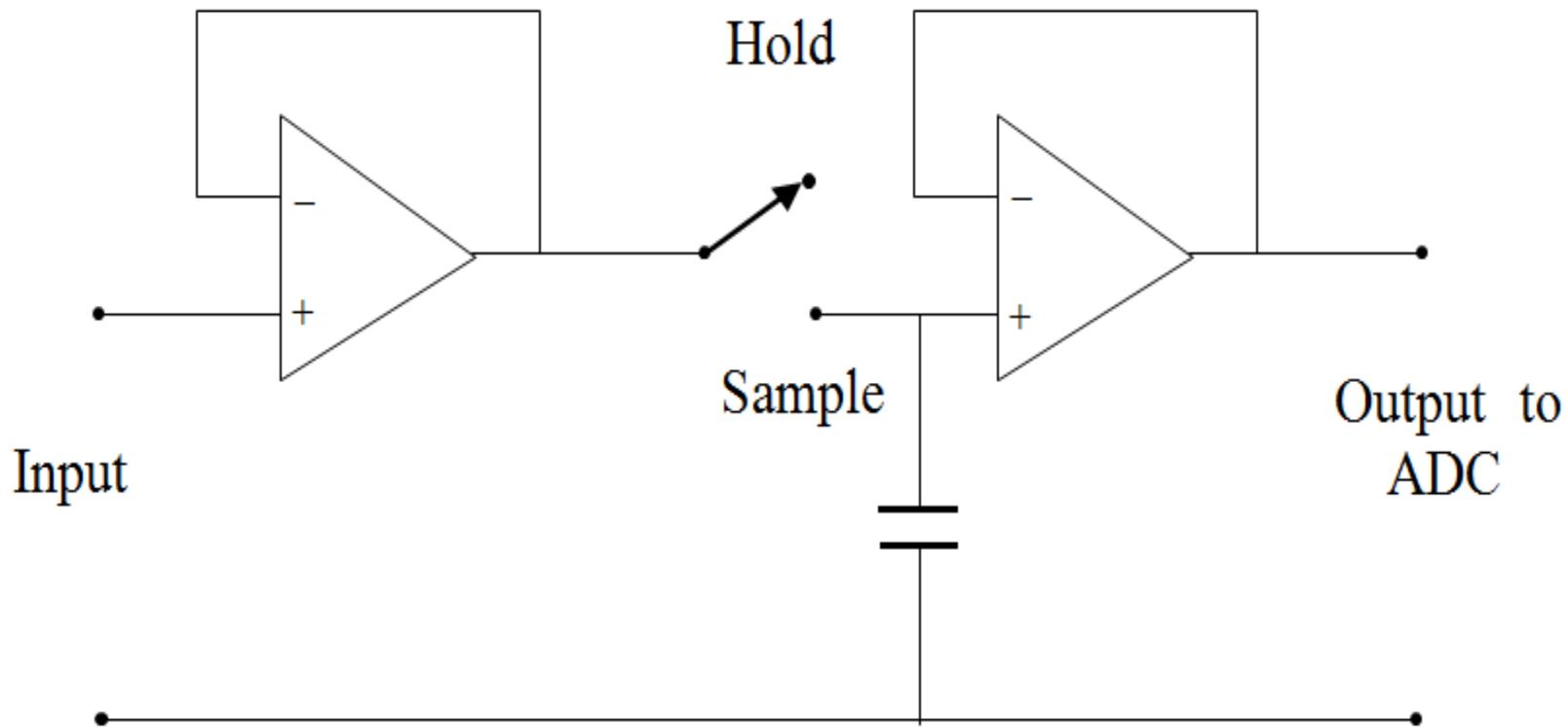
3 steps:

- Sampling
- Quantification
- Coding

These operations are all performed in a same element  
called **the A to D Converter**

# Conversion process: Sampling

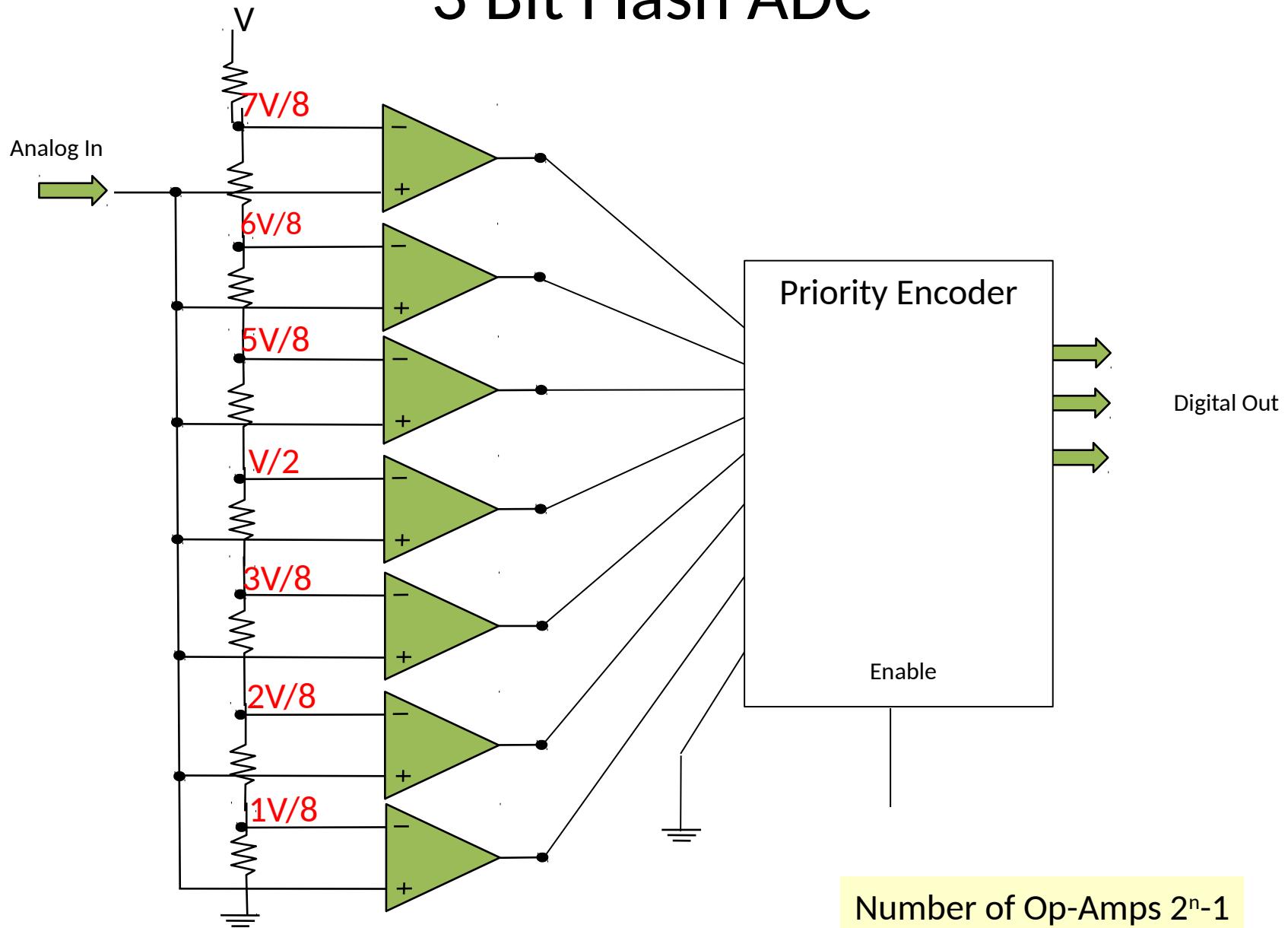
To measure an AC voltage at a particular instant in time, it is necessary to sample the waveform with a 'sample and hold' (S/H) circuit.



# Types of ADCs

- Flash ADC
- Dual slope converter
- Successive approximation converter
- Sigma-delta ADC

# 3 Bit Flash ADC



# Flash ADC

- Let's start design of a 2-bit flash ADC for resolution of 0.25V
- Number of OP-Amp Required :  $2^n - 1$
- The reference voltage required:

$$V_{ref} = \text{Resolution} * 2^n$$

$$\text{Reference voltage} = 0.25 * 4 = 1V$$

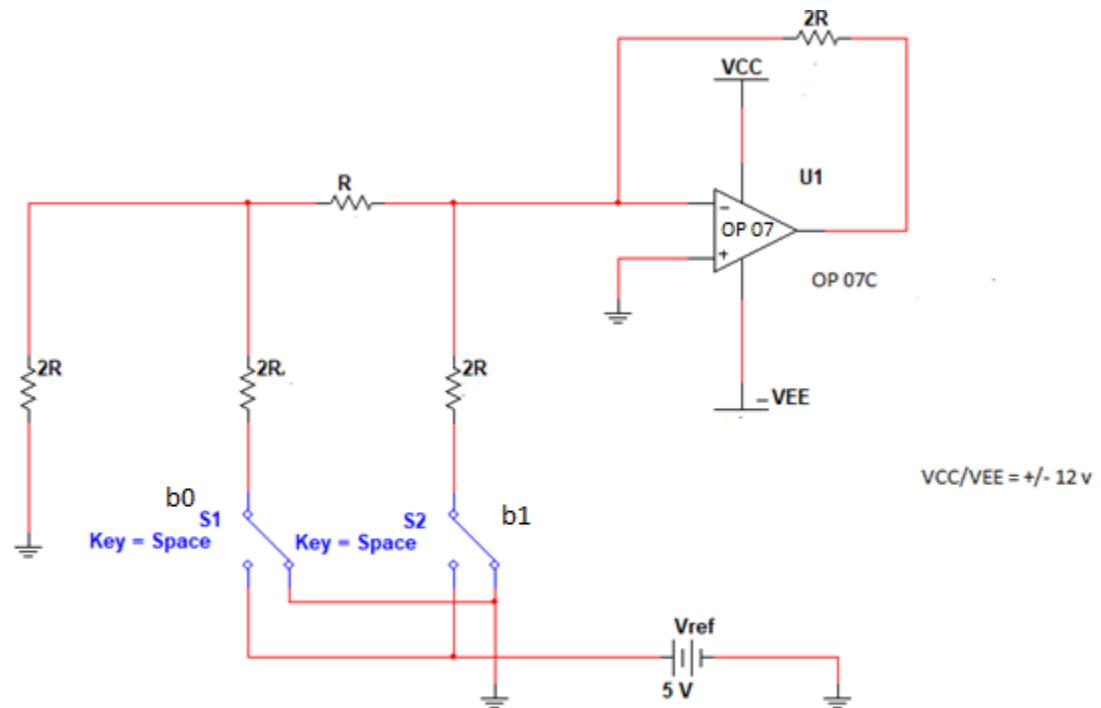
# Flash ADC

Analog input Voltage ( $V_i$ )	Comparator outputs			Digital Outputs	
	C1	C2	C3	B1	B0
$0 \leq V_i \leq V/4$	0	0	0	0	0
$V/4 \leq V_i \leq V/2$	1	0	0	0	1
$V/2 \leq V_i \leq 3V/4$	1	1	0	1	0

Logic expression for b0 and b1.

$$b_1 = C_1 C_2 \overline{C_3} + C_1 C_2 C_3 = C_1 C_2 (\overline{C_3} + C_3) = C_1 C_2$$

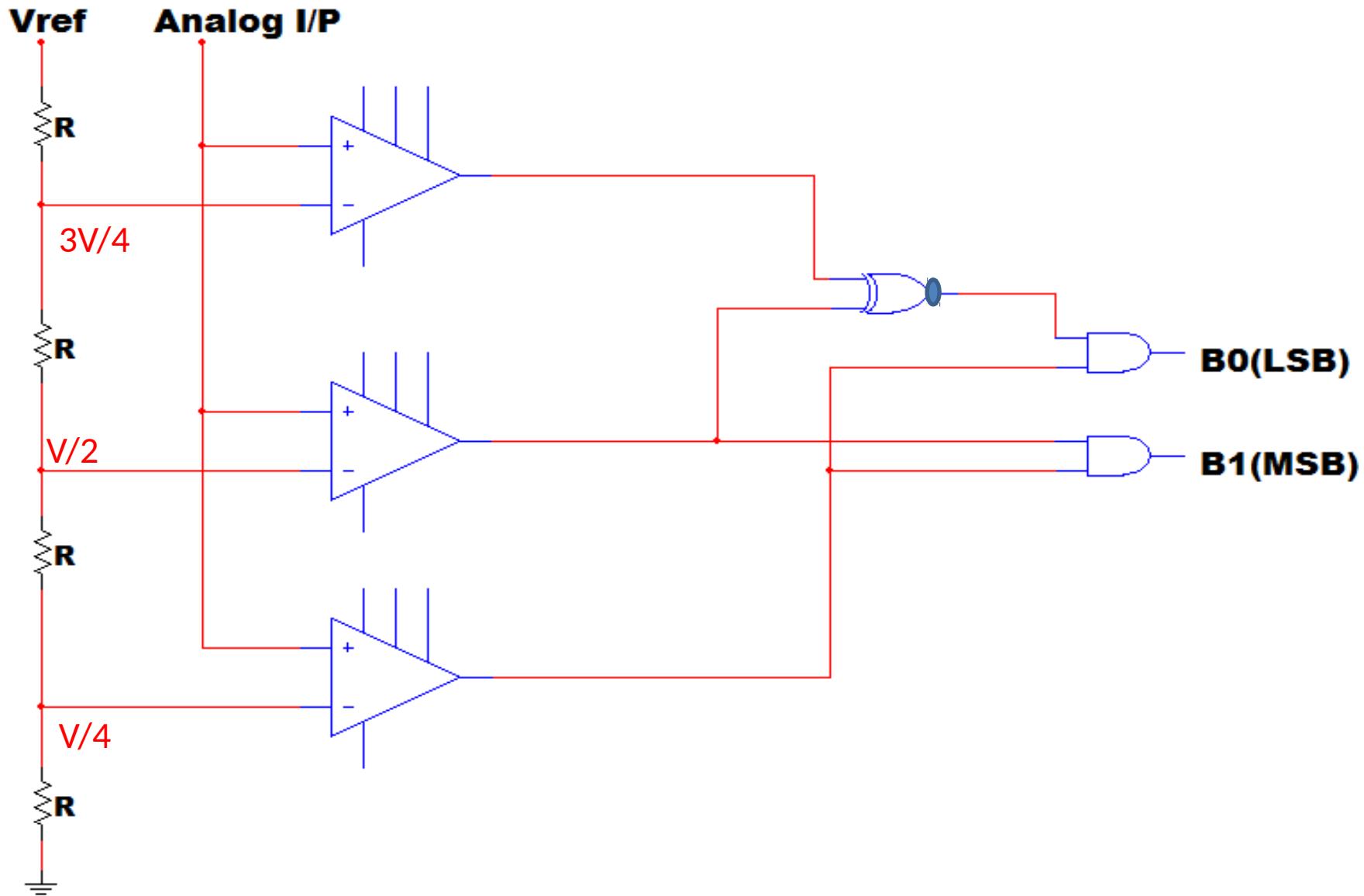
$$b_0 = C_1 \overline{C_2 C_3} + C_1 C_2 C_3 = C_1 (\overline{C_2 \oplus C_3})$$



$$V_o = V_{ref} * (b_1 * 2^{-1} + b_0 * 2^{-2})$$



# Flash ADC



# Flash ADC

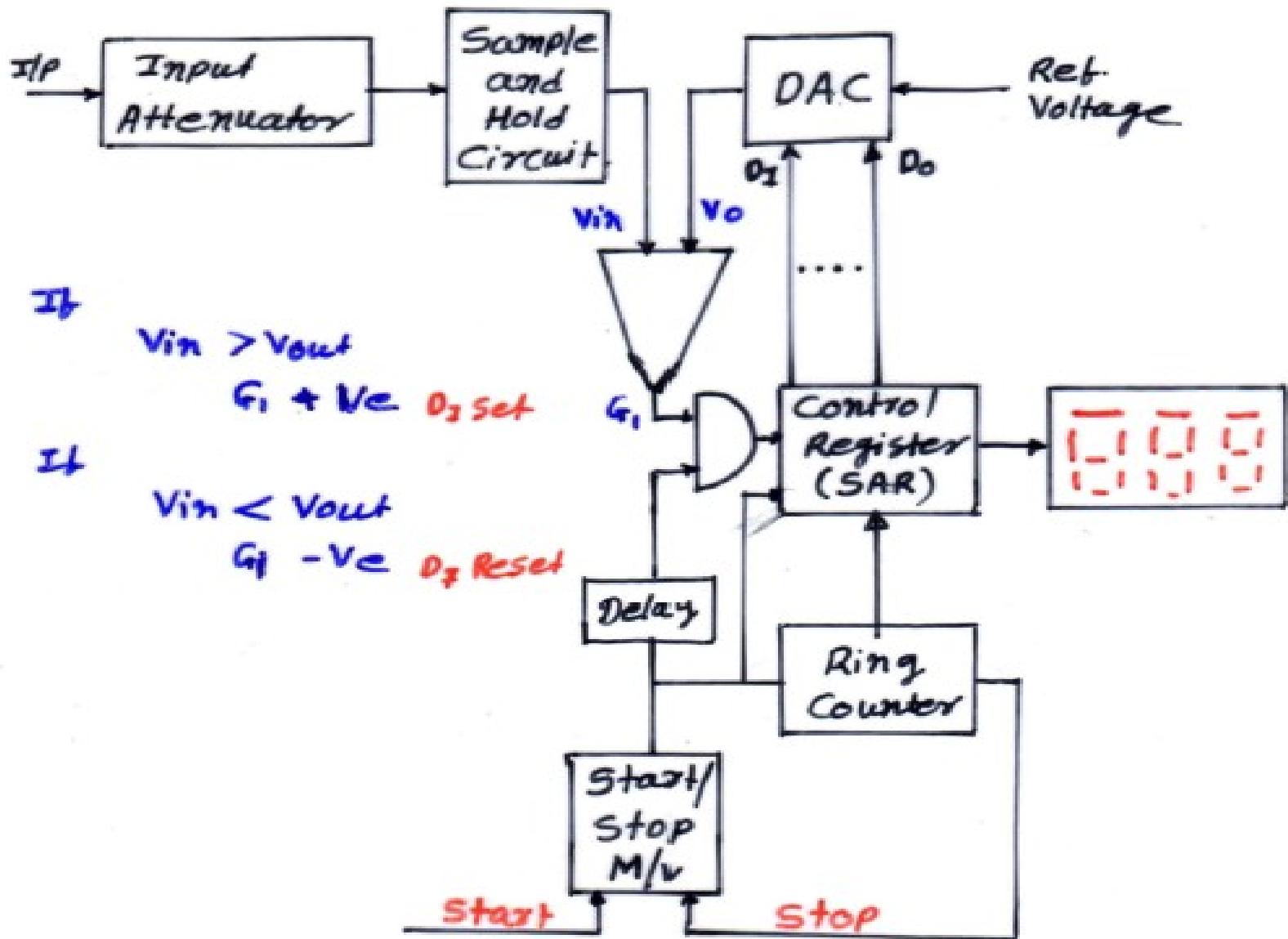
## Advantages

- Flash ADCs are very fast and can convert data at high frequencies.

## Disadvantages

- The major disadvantage to flash ADCs is the complexity of the circuits.
  - an 8-bit Flash ADC requires 255 op amps
  - a 12-bit Flash ADC requires 4095 op amps
  - a 16-bit flash ADC requires 65,535 op amp
- High Cost (Major factor over 6 bits)

# Successive Approximation



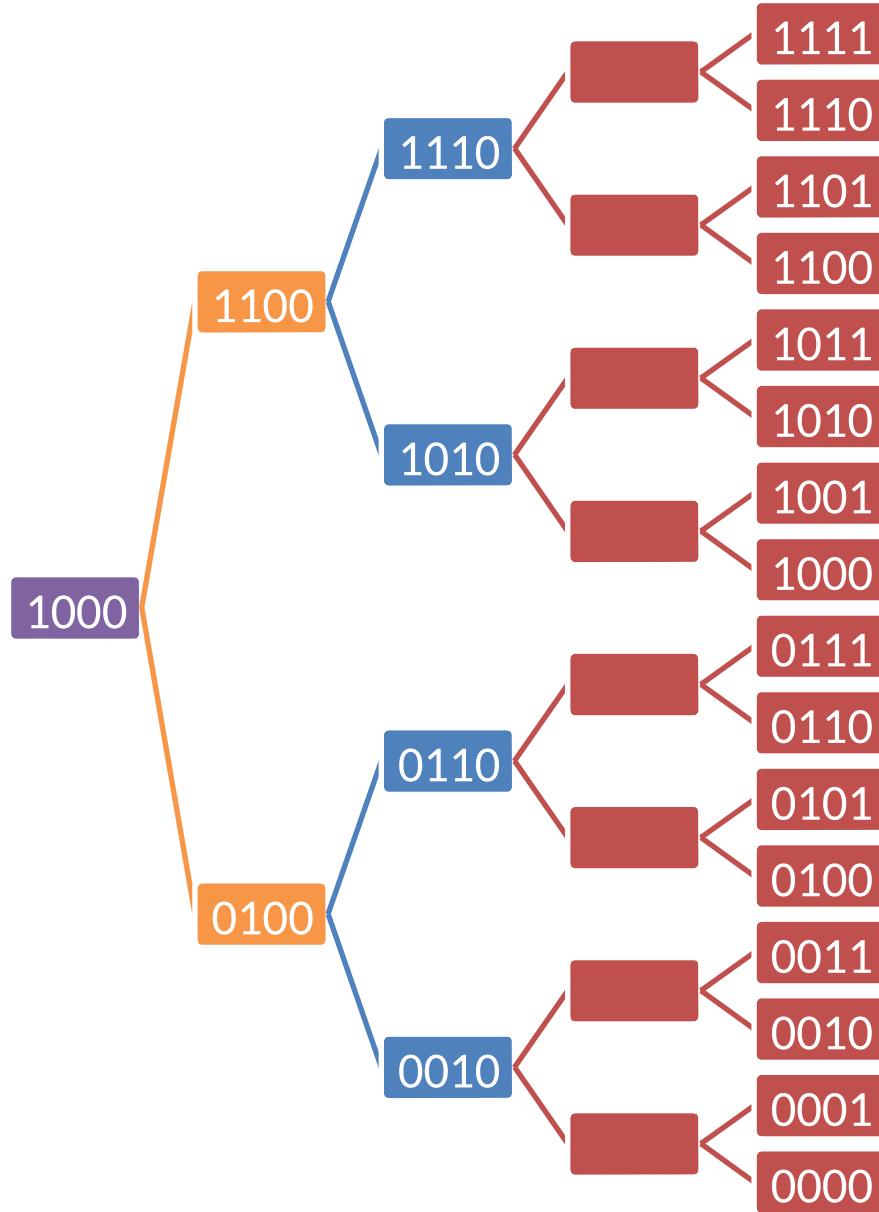
# Successive Approximation ADC

If  $V_{in} = 1V$

SET	D3	D2	D1	D0	Voltage	Compare	Bit Set/Reset
	2.5	1.25	0.625	0.312			
D3	1	0	0	0	2.5V	$V_{in} < V_{out}$	D3 Reset
D2	0	1	0	0	1.25	$V_{in} < V_{out}$	D2 Reset
D1	0	0	1	0	0.625	$V_{in} > V_{out}$	D1 Set
D0	0	0	1	1	0.9375	$V_{in} > V_{out}$	D0 Set

Final conversion of 1V is 0011

# Successive Approximation



# Successive Approximation

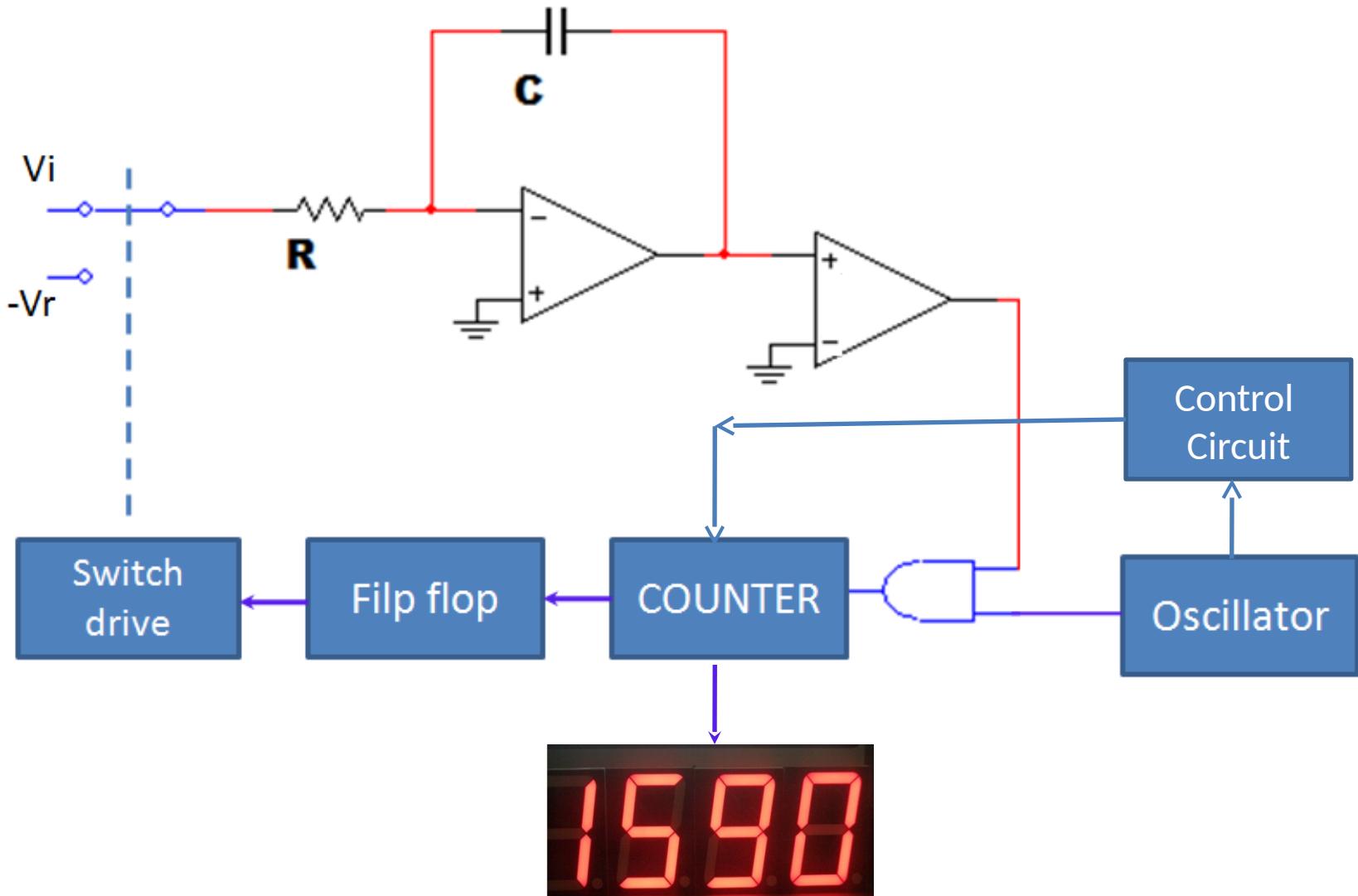
## Advantages

- Capable of high speed
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost

## Disadvantages

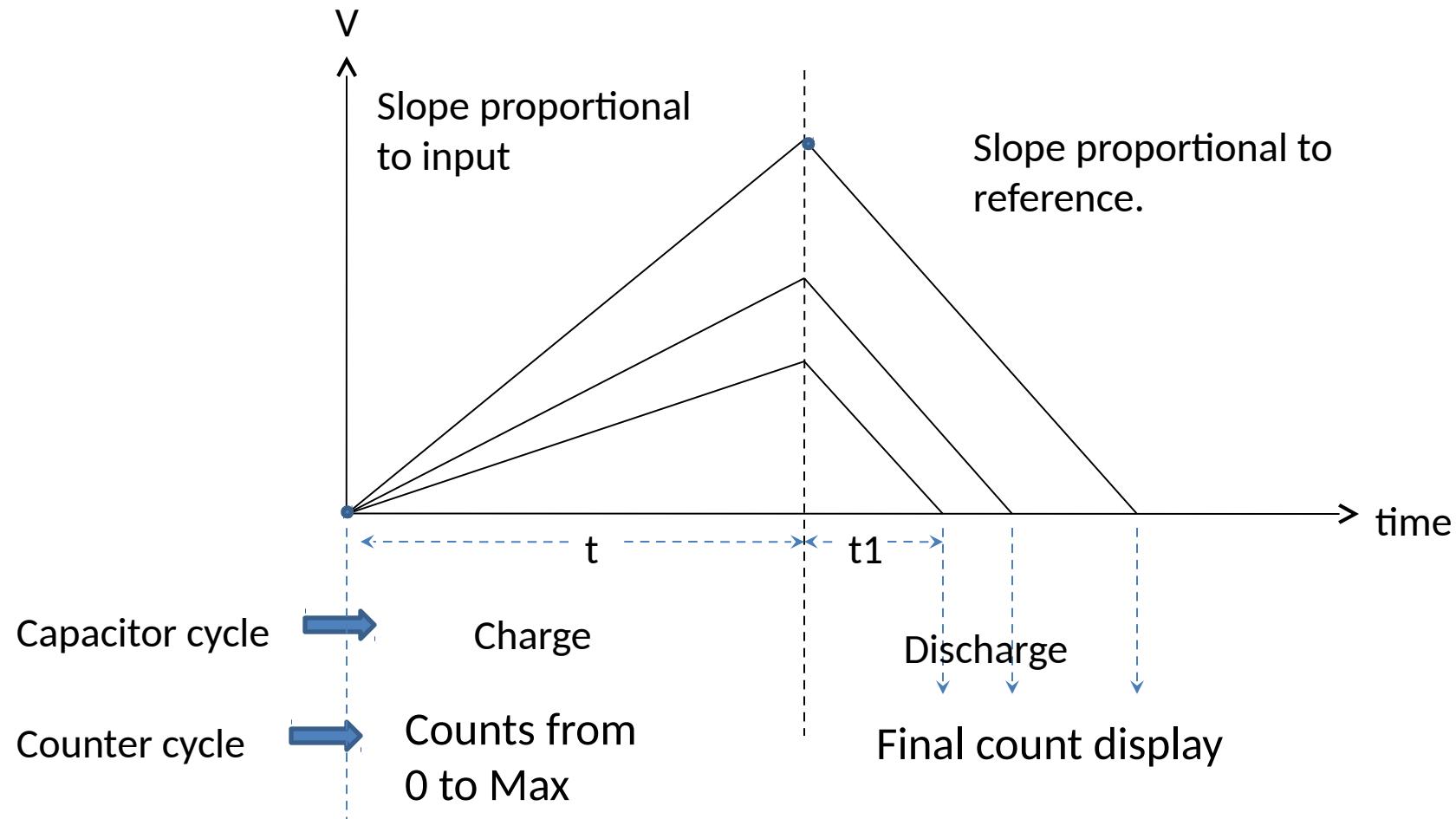
- Higher resolution
- Relatively slower than Flash ADC
- Speed limited ~5Msps

# Dual Slope converter



# Dual Slope converter (Voltage to time conversion)

Principle: Measure the time of positive slope of integrator output proportional to test input voltage and negative slope of integrator output proportional to negative reference voltage.



# Dual Slope converter

During Charging

$$V_o = - \frac{1}{RC} \int_0^t V_i dt$$

$$V_o = - \frac{V_i t}{RC}$$

During Discharging

$$V_o = - \frac{1}{RC} \int_0^{t_1} V_r dt$$

$$V_o = - \frac{V_r t_1}{RC}$$

$$- \frac{V_i t}{RC} = - \frac{V_r t_1}{RC}$$

$$V_i = V_r \frac{t_1}{t}$$

T=Time period of oscillator

$$t = n_1 T \quad \text{constant}$$

$$t_1 = n_2 T$$

$$V_i = V_r \frac{n_2 T}{n_1 T}$$

$$V_i = V_r \frac{n_2}{n_1} = k n_2$$

# Dual Slope converter

- Consider clock frequency : 1MHz
- Reference voltage : - 1V
- The fixed time period (t) : 1mS
- Unknown input voltage : 5V
- During the fixed time period (t)

$$V_i = V_r \frac{n_2}{n_1}$$

$$V_i = 1 \frac{n_2}{1000} = 0.001n_2$$

$$5 = 0.001n_2$$

$$n_2 = 5000$$

# Dual Slope converter

## Advantages

- Greater noise immunity by process of integration
- High resolution [8-10bits]
- Excellent accuracy (input voltage is independent of the integrator time constant)
- Low cost

## Disadvantages

- Slow speed
- High precision external components required to achieve accuracy

# Comparison

Type of ADC	Speed	Price	Noise Immunity	Conversion Time
Dual slope	□□□	□□	□□□	Vary $(2*2^n)$ tclk
Successive approximation	□□□	□	□	Constant No. of bits * tclk
Parallel / flash	□□□□□	□□□□□	□	Constant Single tclk

- Calculate the maximum conversion time of a 8-bit successive approximation ADC, if the clock rate is 2MHz.

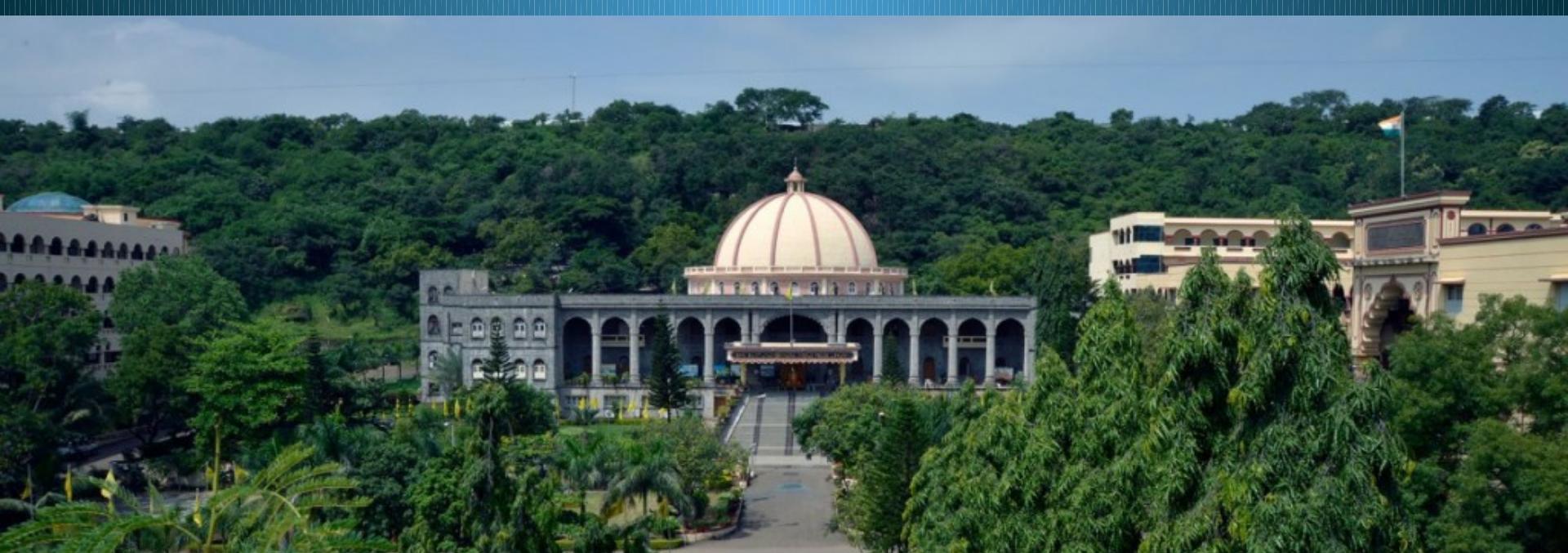
Solution:

- For a 8-bit successive approximation ADC, the conversion time is constant and equal to

$$T_c = \frac{n}{f} = \frac{8}{2 \times 10^6} = 4 \times 10^{-6} s = 4 \mu s$$



# *Analog and Digital Integrated Circuits*



# Unit IV

# Converters

# Lesson Plan

Topic	Sub points	Book-Page Nos.
DAC -specs	Definitions	Salivahanan
Types of DAC ,Advantages & Disadvantages	Binary Weighted, R to R Ladder	Salivahanan
ADC-specs	Definitions	Salivahanan
Types of ADC- Advantages & Disadvantages	Flash, SAR	Salivahanan
Numericals		



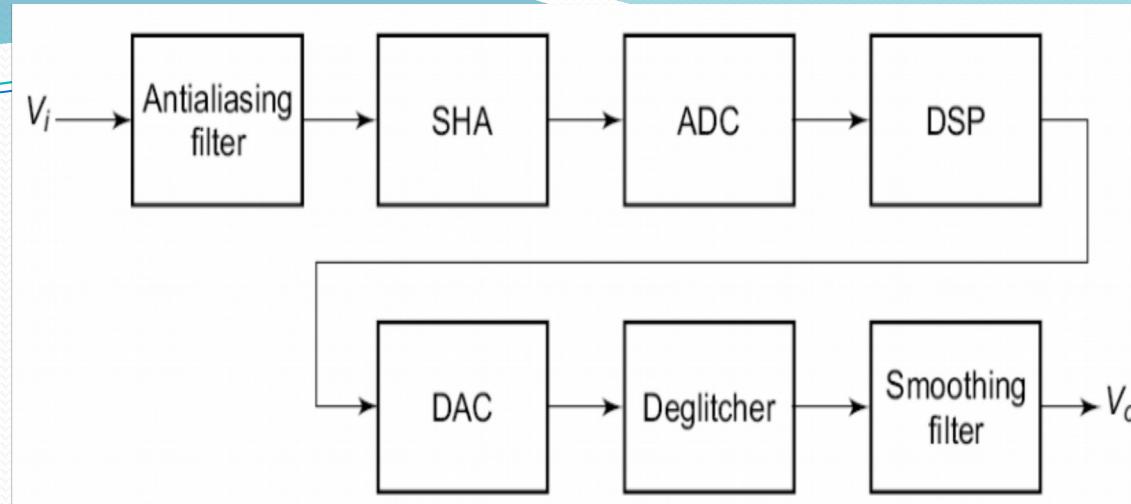
## D/A AND A/D CONVERTERS

- The data converters convert one form of data into another form.
- Used to convert analog signals into equivalent digital data, which in turn act as input for digital systems, and back to analog signals when needed.

## ANALOG AND DIGITAL DATA CONVERSIONS

- The most common technique of acquiring signals is by *sampling*.
- **Sampling a signal - the process of acquiring its values at discrete points in time.**
- The definitions related analog and digital conversion processes are
  - i) *Analog signal* - Signal defined over a continuous period - Amplitude assume a continuous range of values.
  - ii) *Quantization* - Process of denoting a variable by a finite set of discrete values.
  - iii) *Quantized variable* - Signal variable that can assume only finite values.
  - iv) *Discrete time signal* - Defined at particular points of time - time variable is quantized - The function is called a *sampled-data* signal - Sampled data signal result from sampling an analog signal at discrete points of time.

a *digital signal* is a function, in which the time and amplitude are quantized. A digital signal is always represented by a sequence of words, where each word can contain a finite number of *bits* (binary digits).



## Sampled data system using A/D and D/A converters

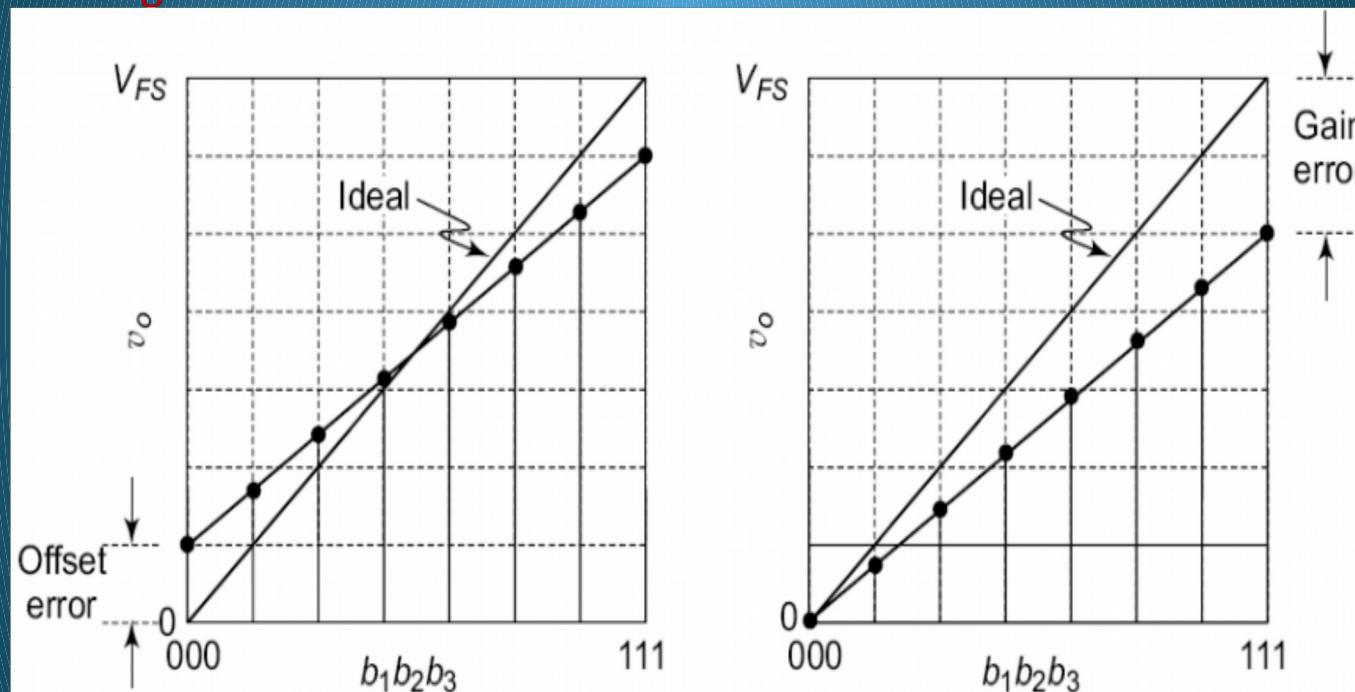
- Analog input signal from transducer is band-limited by *anti-aliasing* filter.
- Signal - Sampled at frequency > twice max frequency of band-limited input signal.
- ADCs require input to be held constant during conversion. Hence, *Sample-and-Hold Amplifier (SHA)* is introduced
- The SHA freezes the band-limited signal just before the start of each conversion.
- The digital signal from A/D converter may be processed, transmitted and recorded in digital form by the digital signal processor (DSP) block.
- Then, the digital signal is converted into analog signal by D/A converter for use in analog form.
- *Deglitcher* introduced in loop before smoothing process, to remove any output glitches generated during input code variations.

# DAC Specifications

## Accuracy

Absolute accuracy defines the maximum deviation of the output from the ideal value and it is expressed in fractions of 1 LSB.

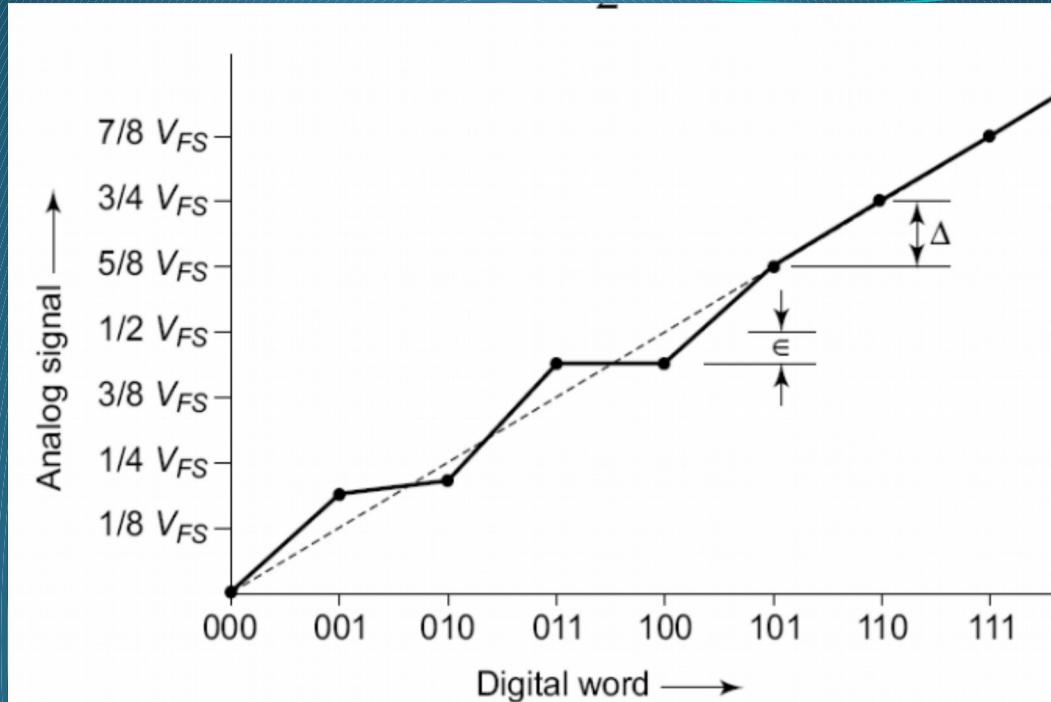
## Offset Voltage



D/A converter offset and gain errors and (b) Nullifying the errors

# DAC Specifications

## Linearity



- The most common dynamic errors are *full-scale error* and *linearity error*.
- *Full-scale error* is the maximum deviation of the output value from its expected or *ideal* value, expressed in percentage of full-scale.
- *Linearity error* is the maximum deviation in step size from the ideal step size.

## Differential Nonlinearity (DNL) Error

For a D/A converter, the DNL error is the difference between the ideal and the measured output responses for successive D/A converter codes.

# DAC Specifications

## Integral Nonlinearity (INL) Error

For data converters, INL is deviation of an actual transfer function from a straight line.

## Monotonicity

- A D/A converter is monotonic if its output value increases as the binary inputs are incremented from one value to the next. That is, the staircase output can have no downward step as the binary input is incremented.

## Resolution (Step Size)

- Resolution of D/A converter is defined as the smallest change that can occur in the analog output as a result of a change in the digital input. The resolution is always equal to the weight of the LSB and is also known as the step size, since it is the amount of  $V_o$  that will change when the digital input data goes from one step to the next.

$$\text{Percentageresolution} = \frac{\text{step size}}{\text{full scale}} \times 100$$

## Settling time

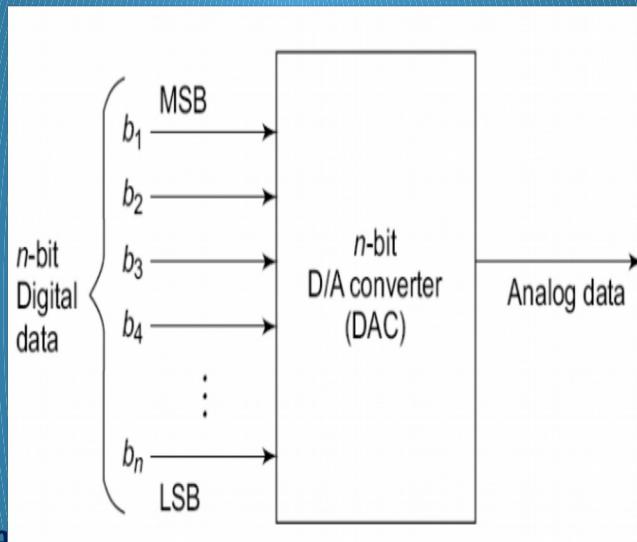
The time required for the output of a D/A converter to settle down to within  $\pm(1/2)$  LSB of the final value for a given digital input is known as *settling time*.

## Temperature sensitivity

For a fixed digital input, the analog input varies with temperature, normally from  $\pm 50\text{ppm}/^\circ\text{C}$  to  $\pm 1.5\text{ppm}/^\circ\text{C}$ . This factor determines the stability of D/A converter.

## BASIC D/A CONVERSION TECHNIQUES

$$V_o = KV_{FS} = KV_{FS} \left( b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n} \right)$$



$V_o$  = output voltage

$V_{FS}$  = full-scale range of voltage

$K$  = scaling factor, usually unity

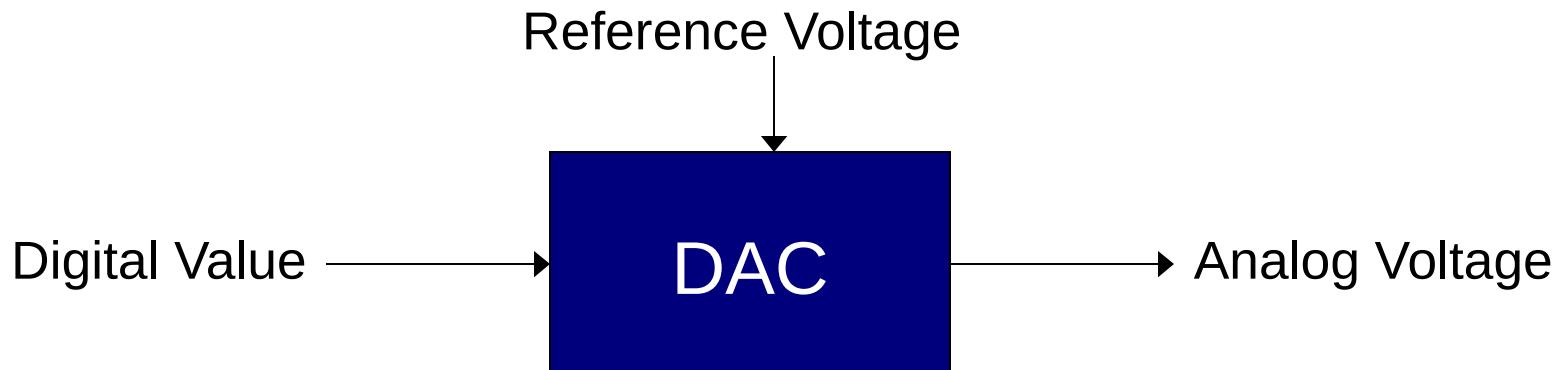
$b_1 \dots b_n$  = n-bit word with binary point at left

$b_1$  = most significant bit (MSB) of weight  $V_{FS}/2$

$b_n$  = least significant bit (LSB) of weight  $V_{FS}/2^n$

# Purpose

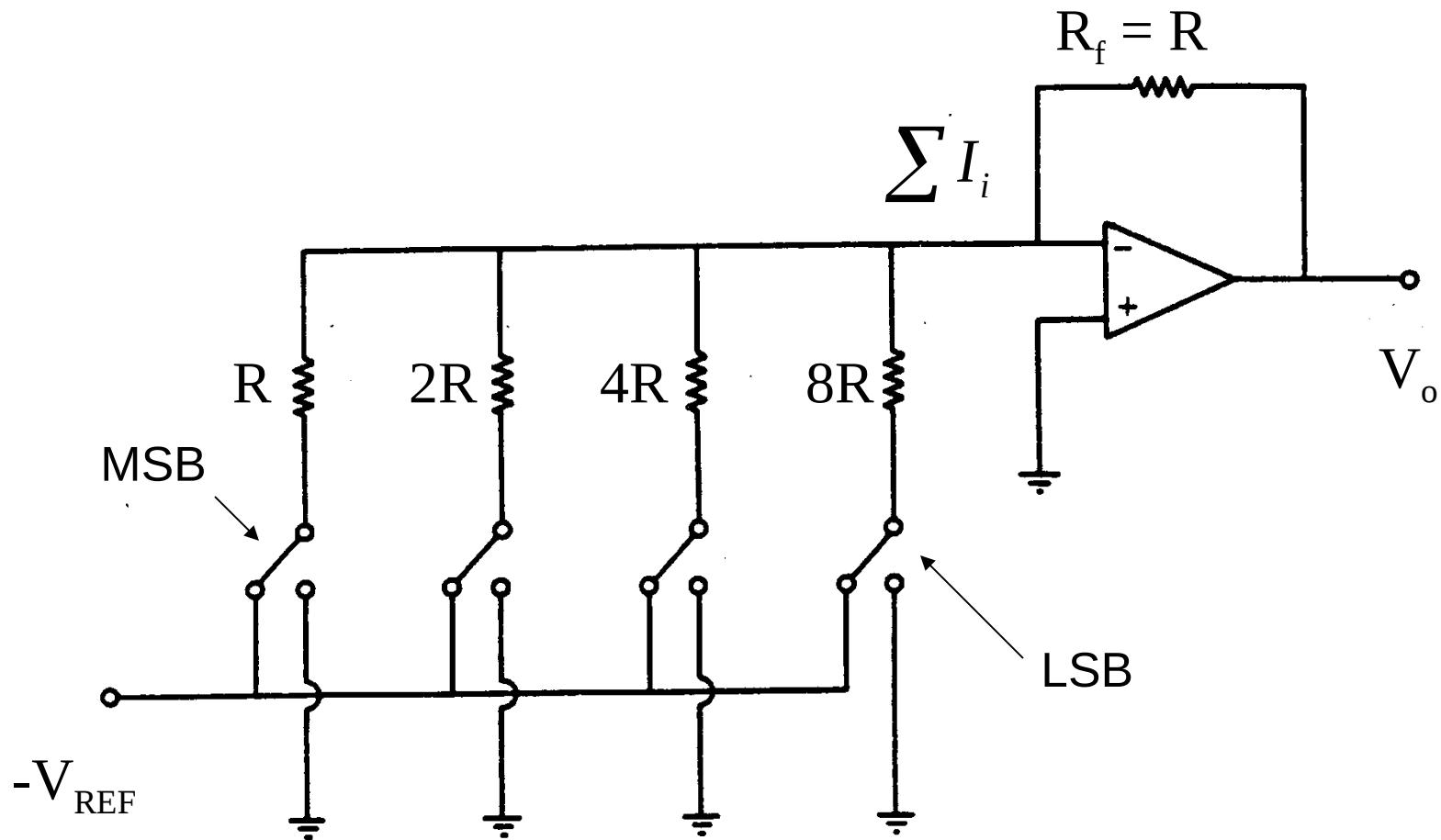
- To convert digital values to analog voltages
- Performs inverse operation of the Analog-to-Digital Converter (ADC)
- $V_{OUT} \propto$  Digital Value



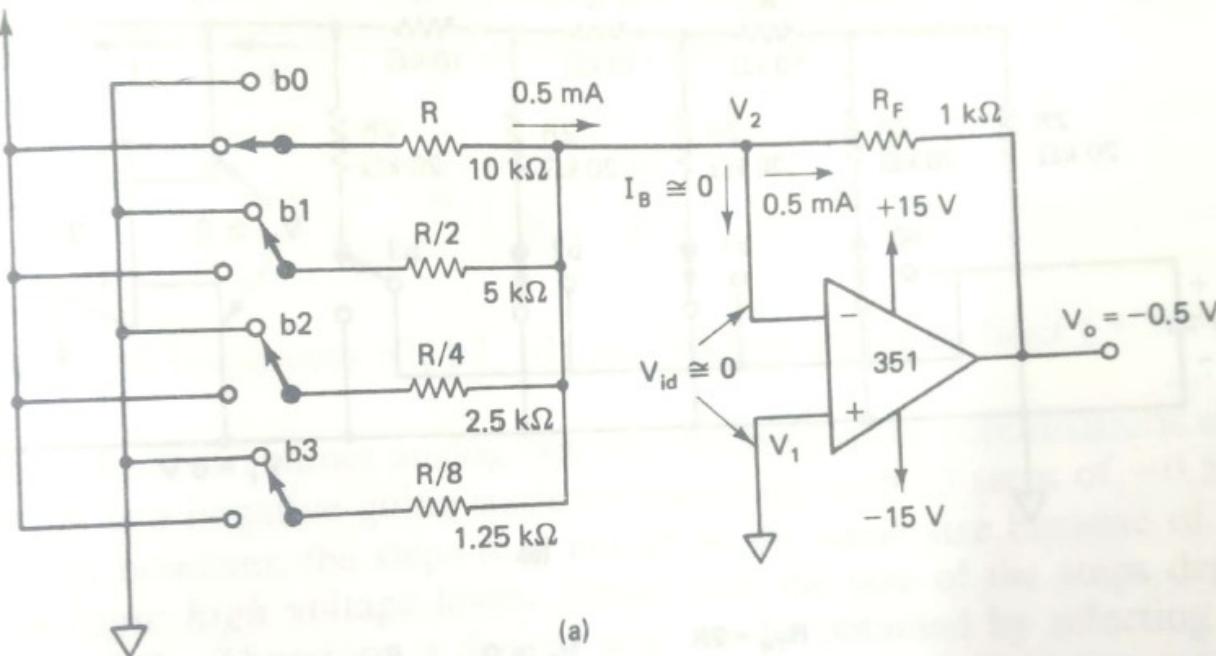
# DACs

- **Types**
  - Binary Weighted Resistor
  - R-2R Ladder
  - Multiplier DAC
    - The reference voltage is constant and is set by the manufacturer.
  - Non-Multiplier DAC
    - The reference voltage can be changed during operation.
- **Characteristics**
  - Comprised of switches, op-amps, and resistors
  - Provides resistance inversely proportion to significance of bit

# Binary Weighted Resistor



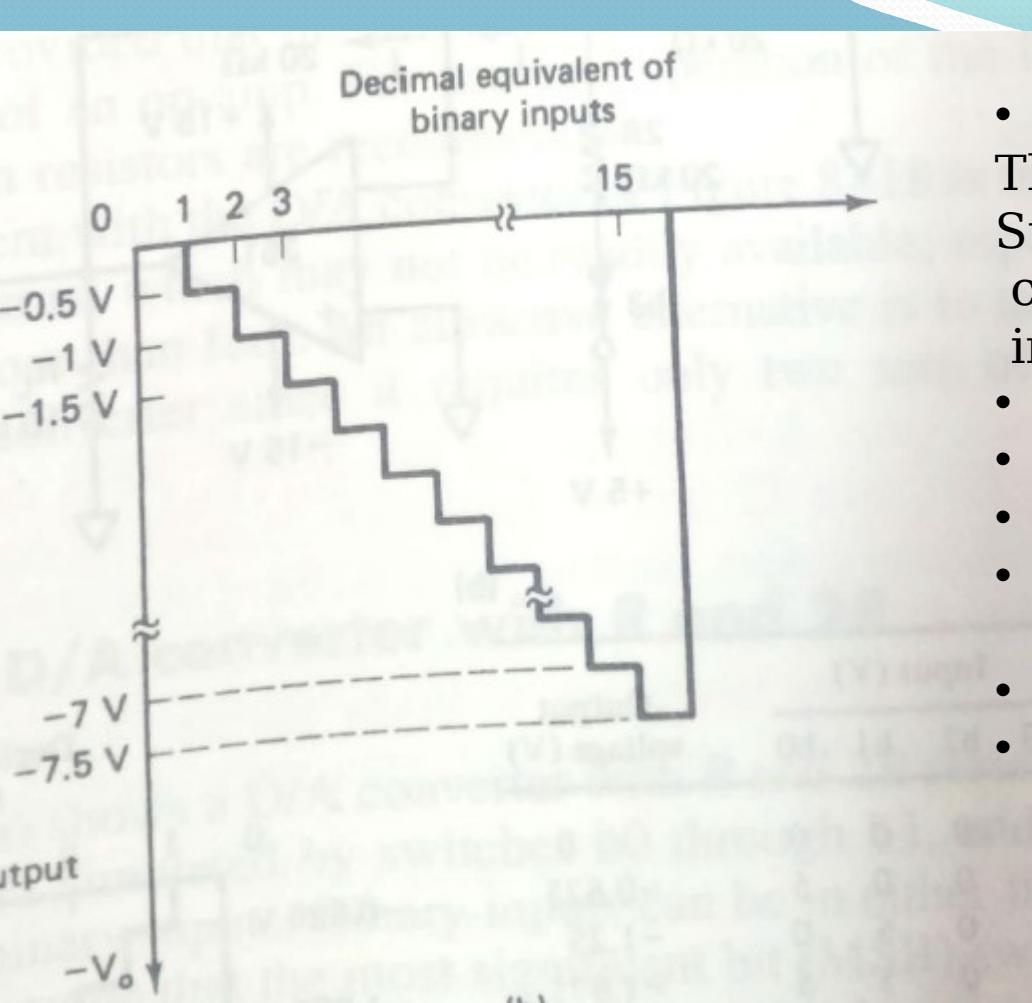
# D/A Converter with binary -weighted resistors EXAMPLE CIRCUIT FR Gayakwad WITH VALUES



this figure the opamp is connected in the inverting mode. It can also be connected in non-inverting mode since the number of binary inputs is the same as the number of bits in the converter.

There are 16 possible combinations of binary inputs for b0 through b3. Therefore there will be 16 possible analog output values.

When switch b0 is closed (connected to +5V), the voltage across  $R_1$  is 5V. Therefore current through  $R_1$  is  $\frac{5V}{10k\Omega} = 0.5mA$ . Hence the current through feedback resistor  $R_f$  is also 0.5 mA. Which produces output voltage of  $-(1K)(0.5mA) = -0.5 V$ .



- If  $b_1$  is closed and  $b_0$  is opened  
This action connects  $R_f/2$  to the positive Supply of  $+5V$ . Causing twice as much current ( $1\text{ mA}$ ) to flow through  $R_f$ , which in turn doubles output voltage.  
Thus output voltage  $V_o$  is  $-1\text{ V}$ .
- Thus output voltage  $V_o$  is  $-1\text{ V}$
- When  $b_0$  and  $b_1$  are closed, the current through  $R_f$  will be  $0.5\text{ mA}$
- current through  $R_f$  will be  $0.5\text{ mA}$
- which will generate output voltage  $-1.5\text{ V}$
- The output voltage equation is given By  $V_o = R_f \frac{b_0}{R_1} + \frac{b_1}{R_2} + \frac{b_3}{R_4} + \frac{b_3}{R_8}$
- The output voltage equation is given By  $= -+++$

Disadvantage: Requires weighted resistors

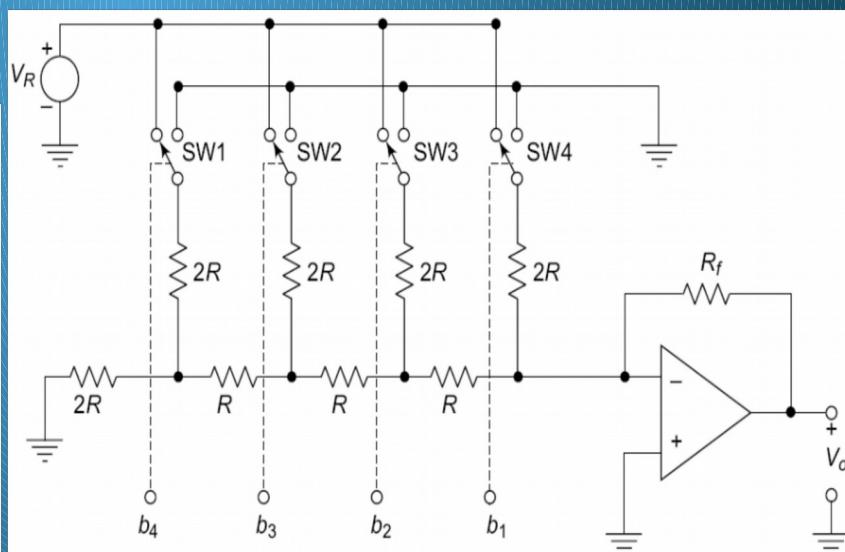
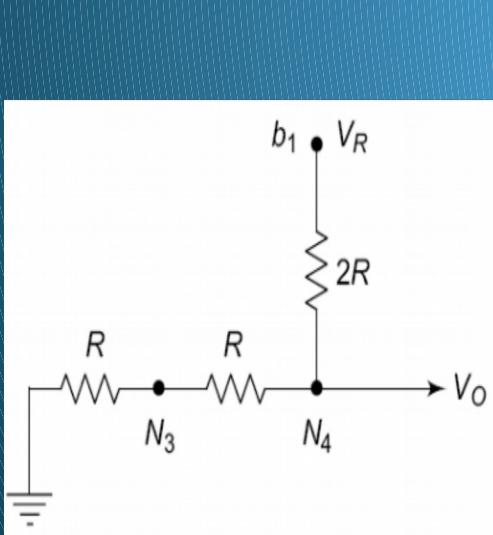
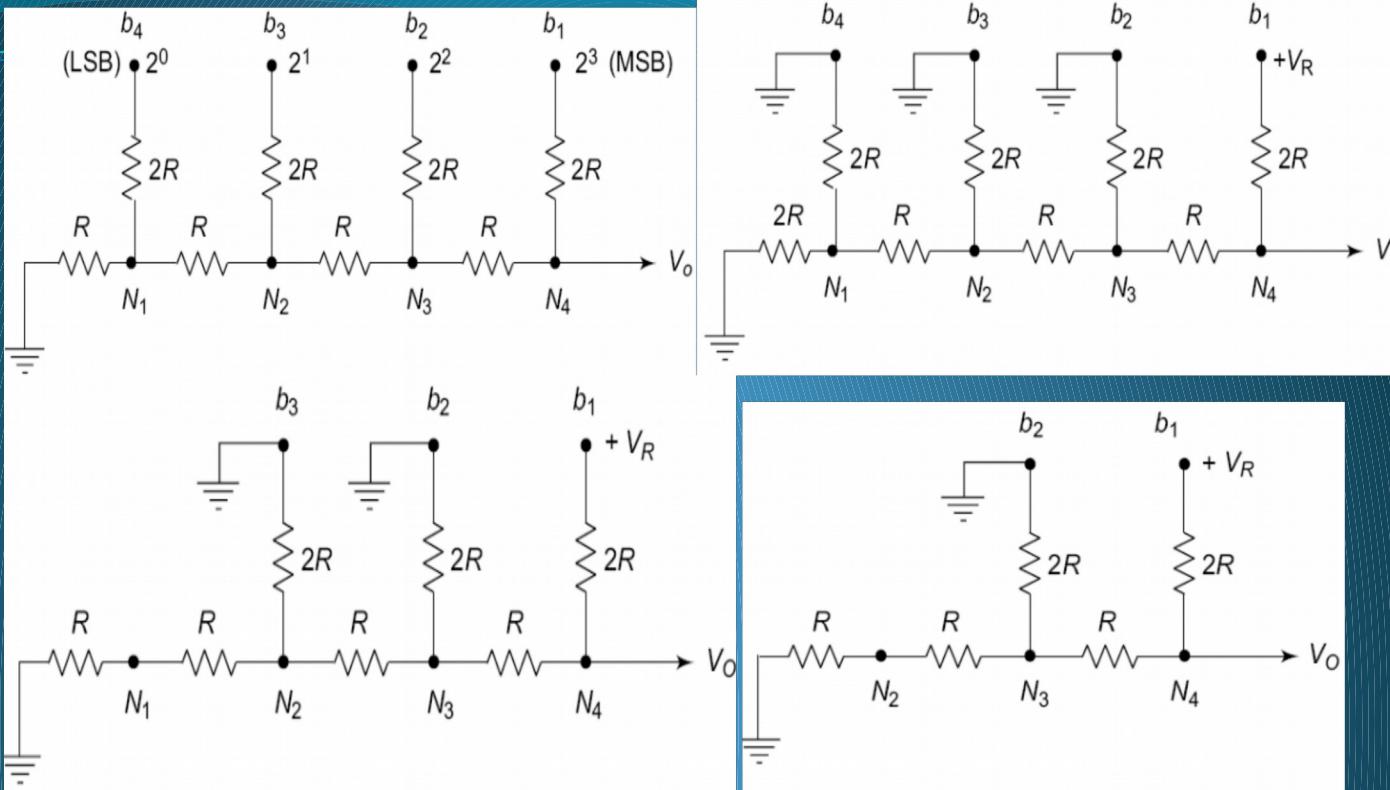
**Example** A system uses a 12-bit word to represent input signal. If the maximum peak-to-peak voltage at output is set for 4V, find the resolution of system and dynamic range.

## Solution

The 12-bit word can represent  $2^{12}$  or 4096 levels, which are equally spaced across the 4V range. Then, the step size  $= \frac{4V}{4096} = 976\mu V$ . Therefore the system can identify input changes as low as  $976\mu V$ .

The *dynamic range* gives the ratio of the largest value to the smallest value which can be converted. Therefore, the dynamic range  $= \frac{4V}{976\mu V} = 4096$ . The dynamic range in dB is given by  $20 \log_{10} 4096 = 72 \text{ dB}$ .

# R-2R Ladder D/A Converter



- R-2R Ladder D/A converter uses only two values i.e.,  $R$  and  $2R$ .
- Hence, it is suited well for IC fabrication. Typical  $R$  values -  $2.5k\Omega$  to  $10k\Omega$ .  
The output voltage is a weighted sum of digital inputs.
- Eg. for 4-bit  $b_1 b_2 b_3 b_4 = 1000$ , the circuit can be modified as shown.

- The analog output voltage  $V_o = \frac{V_R \times 2R}{R + R + 2R} = \frac{V_R}{2}$

$$V_o = \frac{V_R}{2^1} + \frac{V_R}{2^2} + \frac{V_R}{2^3} + \dots + \frac{V_R}{2^n} \text{ where } n \text{ is the total number of bits at the input.}$$

$$V_o = V_R \frac{R_f}{R} \left( \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4} \right) = V_R \frac{R_f}{R \times 2^4} (b_1 2^3 + b_2 2^2 + b_3 2^1 + b_4 2^0)$$

Or, assuming  $R_f = R_1$ ,  $V_o = \frac{V_R}{2^n} (b_1 2^{n-1} + b_2 2^{n-2} + \dots + b_n 2^0)$

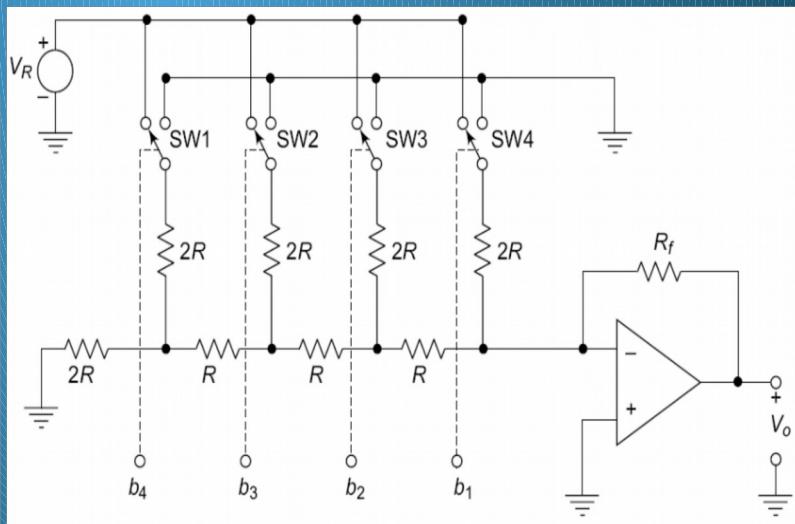
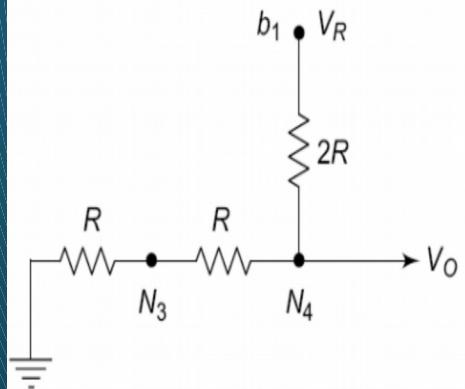
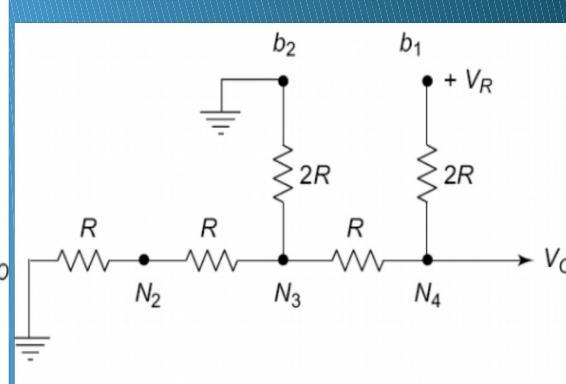
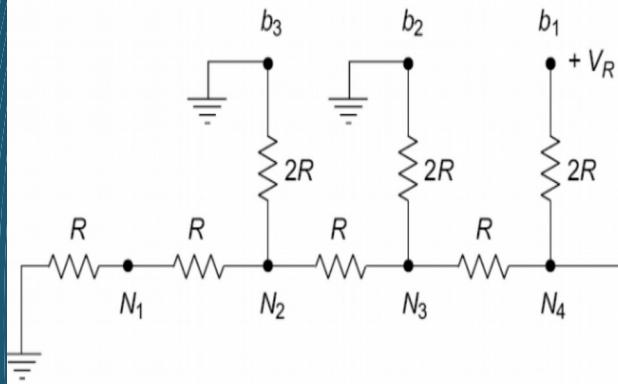
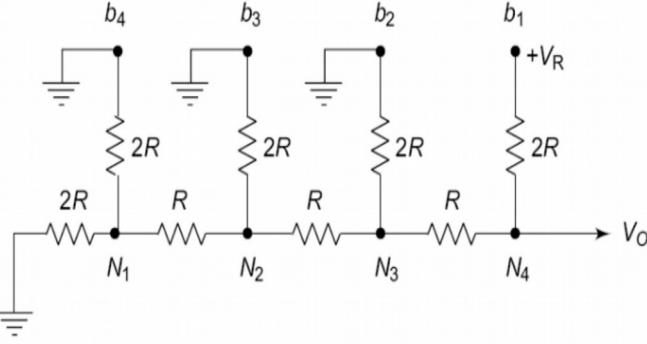
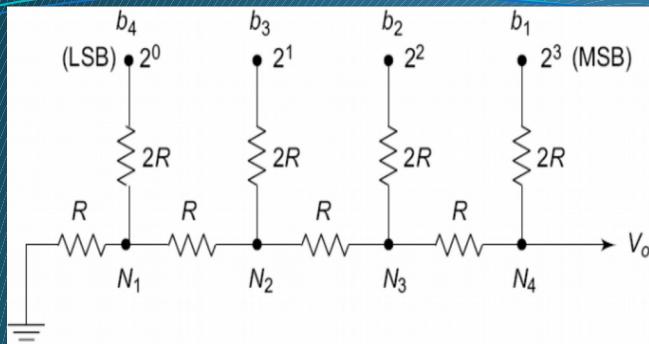
- The resolution of the  $R/2R$  ladder type DAC with current output is

$$\text{Resolution } I = \frac{1}{2^n} \times \frac{V_R}{R}$$

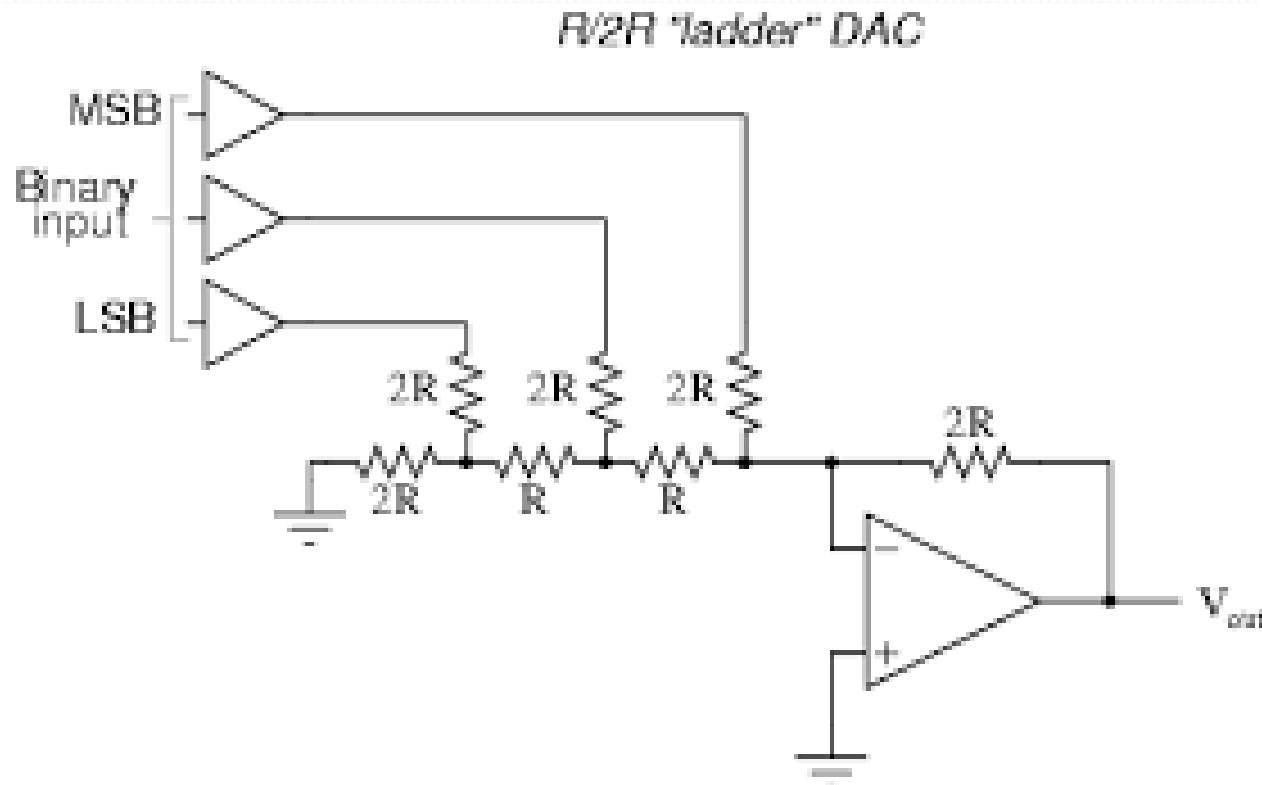
- The resolution of the  $R/2R$  ladder type D/A converter with voltage output is

$$\text{Resolution } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f$$

# R-2R Ladder D/A Converter



# R-2R 3 bit DAC



- R-2R Ladder D/A converter uses only two values i.e.,  $R$  and  $2R$ .
- Hence, it is suited well for IC fabrication. Typical  $R$  values -  $2.5k\Omega$  to  $10k\Omega$ .  
The output voltage is a weighted sum of digital inputs.
- Eg. for 4-bit  $b_1 b_2 b_3 b_4 = 1000$ , the circuit can be modified as shown.

- The analog output voltage  $V_o = \frac{V_R \times 2R}{R + R + 2R} = \frac{V_R}{2}$

$$V_o = \frac{V_R}{2^1} + \frac{V_R}{2^2} + \frac{V_R}{2^3} + \dots + \frac{V_R}{2^n} \text{ where } n \text{ is the total number of bits at the input.}$$

$$V_o = V_R \frac{R_f}{R} \left( \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4} \right) = V_R \frac{R_f}{R \times 2^4} (b_1 2^3 + b_2 2^2 + b_3 2^1 + b_4 2^0)$$

Or, assuming  $R_f = R_1$ ,  $V_o = \frac{V_R}{2^n} (b_1 2^{n-1} + b_2 2^{n-2} + \dots + b_n 2^0)$

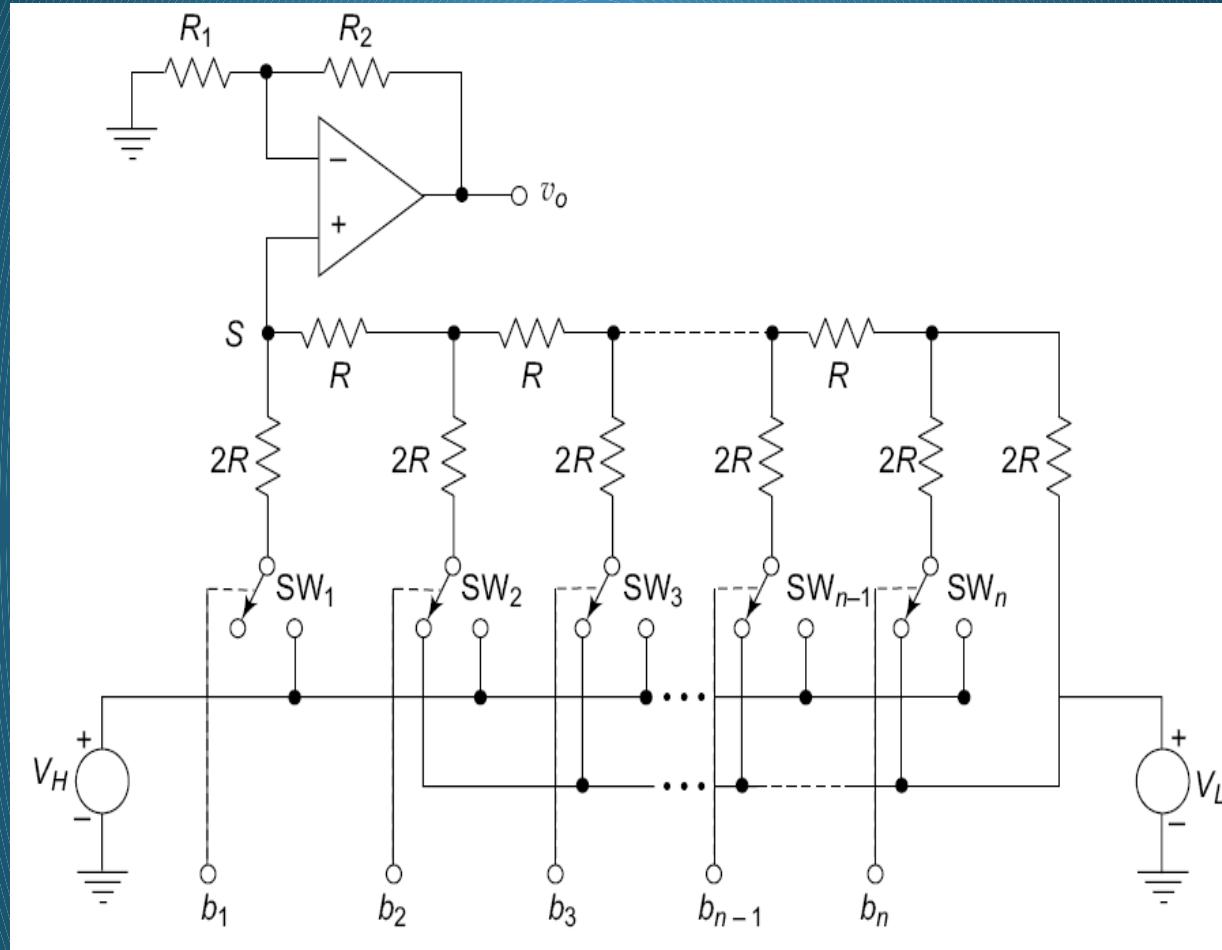
- The resolution of the  $R / 2R$  ladder type DAC with current output is

$$\text{Resolution } I = \frac{1}{2^n} \times \frac{V_R}{R}$$

- The resolution of the  $R / 2R$  ladder type D/A converter with voltage output is

$$\text{Resolution } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f$$

## Voltage Mode R-2R Ladder



# Pros & Cons

	Binary Weighted	R-2R
Pros	Easily understood	Only 2 resistor values Easier implementation Easier to manufacture Faster response time
Cons	Limited to ~ 8 bits Large # of resistors Susceptible to noise Expensive Greater Error	More confusing analysis

# A/D Converters

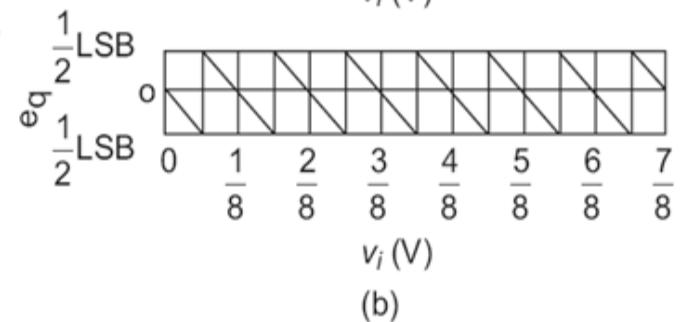
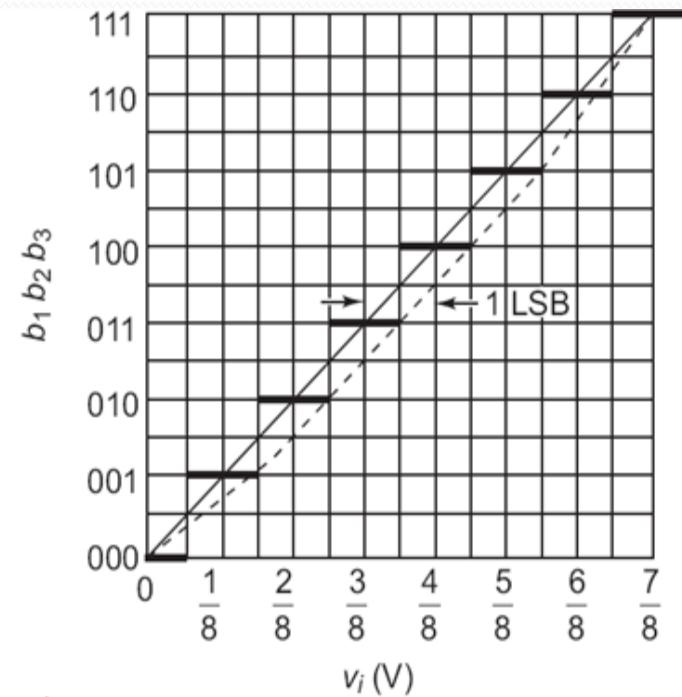
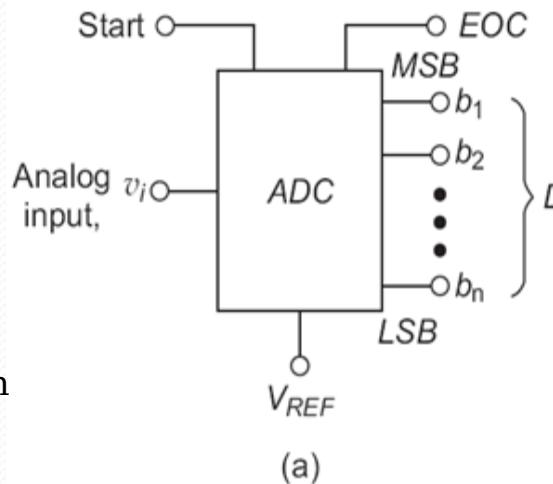
- It converts an analog signal into its equivalent n-bit binary coded digital output signal.
- The analog input is sampled at a frequency much higher than the maximum frequency component of the input signal.
- ADC accepts an analog input  $V_i$  and produces an output binary word  $b_1, b_2, \dots, b_n$  of fractional value  $D$

$$D = b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}$$

where,  $b_1$  is the MSB and  $b_n$  is the LSB.

# A/D Converters contd....

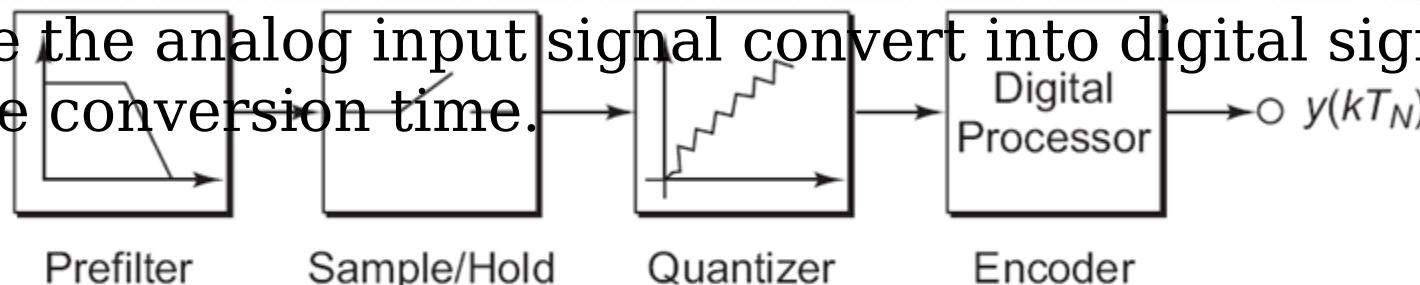
- Fig a shows symbolic representation of ADC
- Fig b shows the ideal characteristics of 3bit A/D converter with full-scale analog voltage  $V_{FS} = 1V$
- ADC process divides the analog input signal into  $2^n$  intervals called **Code Ranges.**
- The values  $V_i$



A/D converter (a) Symbolic representation and (b) Ideal transfer characteristics and quantization noise for a 3-bit A/D converter

# Block Diagram of ADC

- It consists of antialiasing filter or prefilter, Sample-and-Hold amplifier , a Quantizer and an Encoder.
- **Prefilter:** avoids the aliasing (misidentification of high frequency signals).
- **Sample-and-Hold:** It holds the input analog signal into the ADC at a constant value during the conversion time.
- **Quantizer:** it segments the reference voltage into the subranges, typically for an n-bit digital output code , there are  $2^n$  subranges.
- **Encoder:** The digital processor forms the encoder circuit which encodes the subrange into the corresponding digital bits.
- Therefore the analog input signal converts into digital signal within the conversion time.



General block diagram of an A/D converter

# A/D Converter Applications

- Digital Audio: Digital audio workstations, sound recording, pulse-code modulation
- Digital signal processing: TV tuner cards, microcontrollers, digital storage oscilloscopes
- Scientific instruments: Digital imaging systems, radar systems, temperature sensors

# Specifications of Analog to digital Convereter

**Resolution:** It refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits.

- The resolution of the converter indicates the number of discrete values it can produce over the range of analog values.
- Resolution =  $\frac{V_{FS}}{2^n}$ , where n is the number of digital output word bits.  
$$\Delta V_i \text{ for } 1 \text{ LSB} = \frac{V_{FS}}{2^n}$$
- The digital output starts at 0 for the ADC, therefore the maximum full scale input voltage which will cause the output to be all logic 1s is 1LSB less than  $V_{FS} - 1 \text{ LSB}$  voltage range .

An 8-bit A/D converter accepts an input voltage signal of range 0 to 10 V. (a) What is the minimum value of the input voltage required to generate a change of 1 LSB? (b) What input voltage will generate all 1s at the A/D converter output? (c) What is the digital output for an input voltage of 4.8 V?

- Solution:

(a)

$$1 \text{ LSB} = \frac{10 \text{ V}}{2^8} = 39.1 \text{ mV}$$

(b)

$$v_{iFS} = V_{FS} - 1 \text{ LSB}$$

$$v_{iFS} = 10 \text{ V} - 39.1 \text{ mV} = 9.961 \text{ V.}$$

(c) The digital output for an applied input voltage of 4.8V is given by

$$D = \frac{4.8 \text{ V}}{39.1 \text{ mV}} = 122.76 = 123$$

Converting this to binary gives the digital output for an 8-bit A/D converter to be  
01111011

# Specification of ADC Converter contd...

## Quantization Error

A digital error in an A/D converter is based on resolution of digital system. When an analog signal converted to digital form is converted back to analog, output is a staircase waveform, which is a discontinuous signal composed of a number of discrete steps. The smallest step is the LSB - can be made smaller by increasing the number of digital bits. The possible error is called *quantization error*, or *digitizing error* and it is commonly the bit. Higher the number of bits of ADC finer the resolution and smaller the quantization error.

## Analog Error

Due to variations in dc switching point of comparator - Offset, gain and linearity error of op-amp and resistors, reference voltage, ripple and noise of components.

## Linearity Error

Defined as measure of variation in voltage step size - Indicates difference between transitions for a minimum step of input voltage change - specified as fraction of 1 LSB.

# Specification of ADC Converter contd...

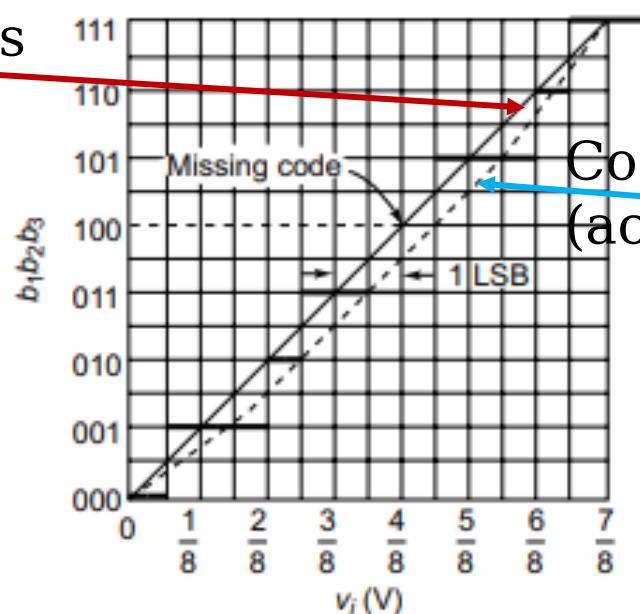
## Differential Nonlinearity (DNL) Error

The analog input levels that trigger any two successive output codes should differ by 1 LSB ( $DNL = 0$ ) for an A/D converter. Any deviation from 1 LSB  $\rightarrow$  DNL error.

## Integral Nonlinearity (INL) Error

The **maximum** deviation of the code center line from the straight line passing through the end points of the ideal characteristics after nulling the offset and gain errors is called *Integral Nonlinearity error (INL)*.

Ideal characteristics



Code centre line  
(actual input step voltage range)

Fig. 11.26 A/D converter characteristic with a missing code

**Dither** The performance of ADC can be improved using Dither.

Dither is a very small amount of random noise (white noise) added to input before conversion. Its amplitude is set to half of LSB.

### **Conversion Time**

The time required for an A/D converter to convert an analog input value into its equivalent digital data is called the *conversion time*.

### **Input voltage range**

It is the range of voltage that an A/D converter can accept as its input without causing any overflow in the digital output.

# **CLASSIFICATION OF A/D CONVERTERS**

The A/D converters (ADC) can be classified based on their operational features as follows.

**Type I:** The A/D converters can be classified into two groups:

- a) Programmed A/D converters
- b) Non-programmed A/D converters

**Type II :** The A/D converters are classified into two groups:

- a) Closed-loop or feedback type A/D converters
- b) Open-loop type A/D converters

**Type III:** The A/D converters are classified into two groups:

- a) Capacitor – charging type A/D converters
- b) Discrete voltage comparison type A/D converters

**Type IV:** The A/D converters are classified into two groups based on their conversion techniques as

- a) Direct type A/D converters
- b) Integrating type A/D converters

# Based on operation of conversion

- Flash type/ Simultaneous (parallel)
- Successive approximation
- Dual Slope type(Integrator)
- Single slope type
- Counter type
- Tracking or Servo type

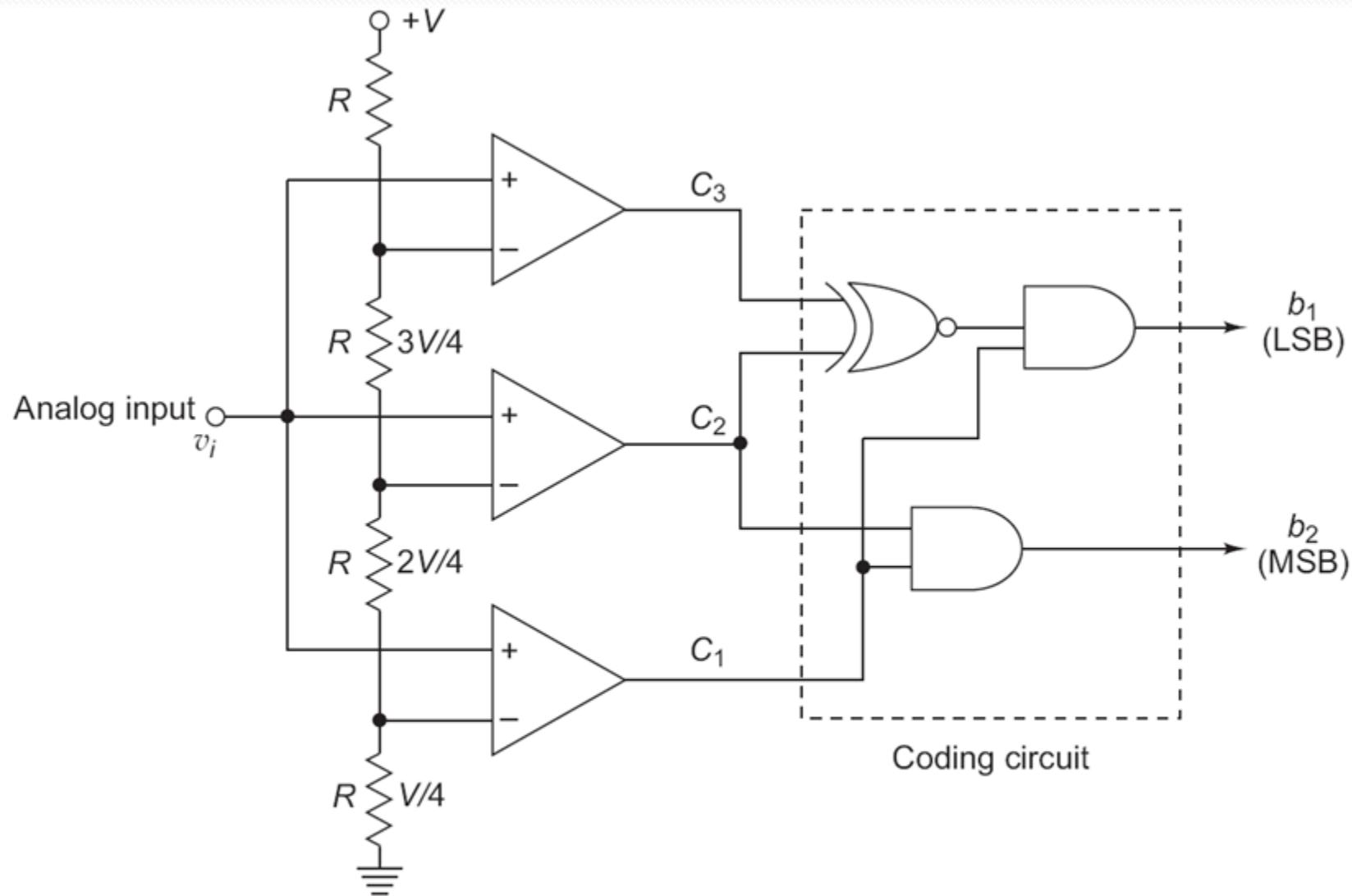
# Flash ADC

- Let's start design of a 2-bit flash ADC for resolution of 0.25V
- Number of OP-Amp Required :  $2^n - 1$
- The reference voltage required:

$$V_{ref} = \text{Resolution} * 2^n$$

$$\text{Reference voltage} = 0.25 * 4 = 1V$$

# Simultaneous Type (Flash Type) A/D Converter



*Block diagram of 2-bit simultaneous type A/D converter*

- Uses the  $2^N$  resistors to form a ladder voltage divider, which divides the reference voltage into  $2^N$  equal intervals.
- Uses the  $2^{(N)-1}$  comparators to determine in which of these  $2^N$  voltage intervals the input voltage  $V_{in}$  lies.
- The Combinational logic then translates the information provided by the output of the comparators
- This ADC does not require a clock so the conversion time is essentially set by the settling time of the comparators and the propagation time of the combinational logic.

# 2-bit Flash type ADC

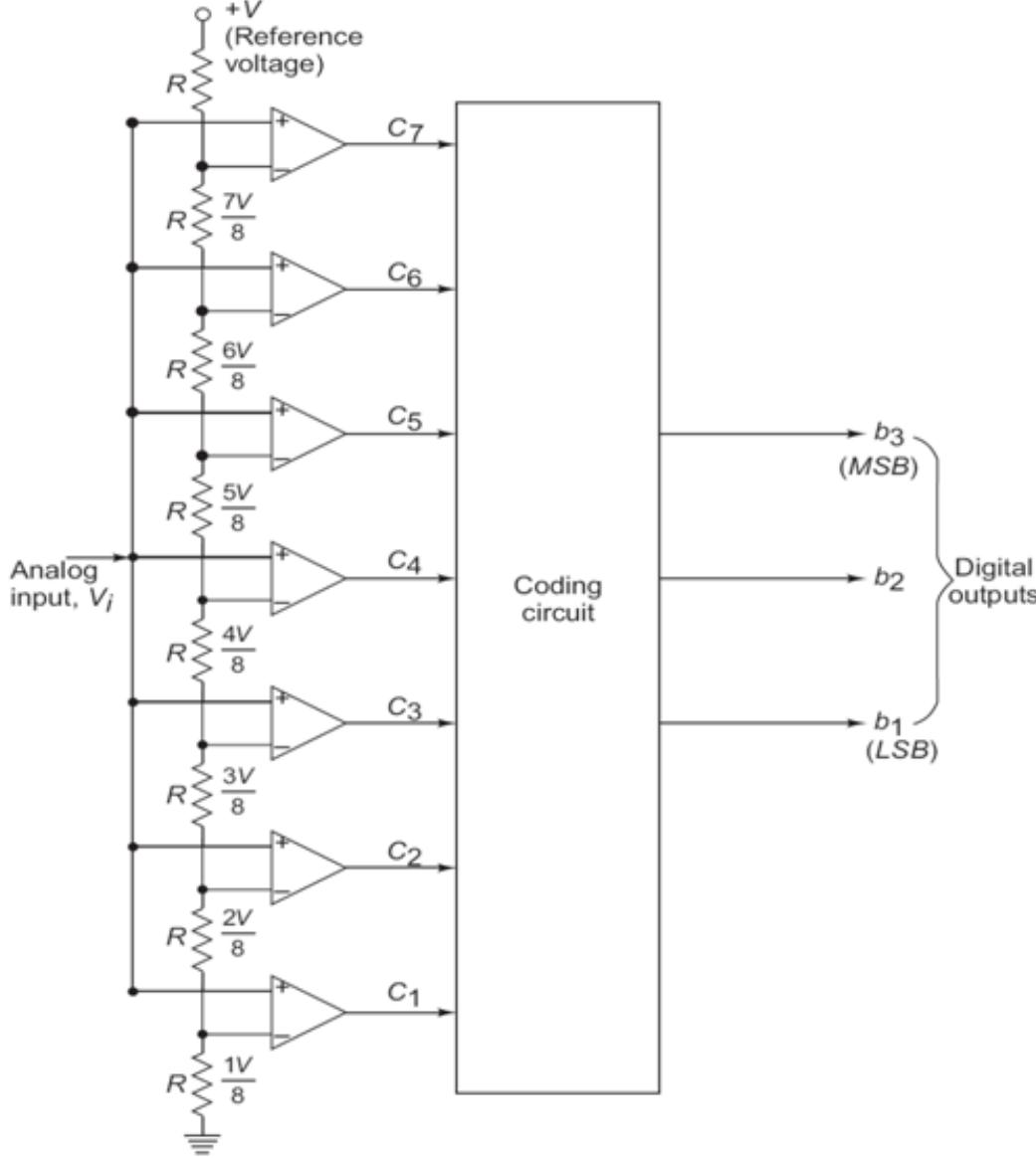
Comparator and digital outputs for a 2-bit simultaneous type A/D converter

Analog Input Voltage ( $V_i$ )	Comparator Outputs			Digital Outputs	
	$C_1$	$C_2$	$C_3$	$b_2$	$b_1$
$0 \leq V_i \leq V/4$	0	0	0	0	0
$V/4 \leq V_i \leq V/2$	1	0	0	0	1
$V/2 \leq V_i \leq 3V/4$	1	1	0	1	0
$3V/4 \leq V_i \leq V$	1	1	1	1	1

$$b_2 = C_1 C_2 \overline{C_3} + C_1 \overline{C_2} C_3 = C_1 C_2 \left( \overline{C_3} + C_3 \right) = C_1 C_2$$

$$b_1 = C_1 \overline{C_2 C_3} + C_1 C_2 C_3 = C_1 \left( \overline{C_2 \approx C_3} \right)$$

# 3-bit Flash type ADC



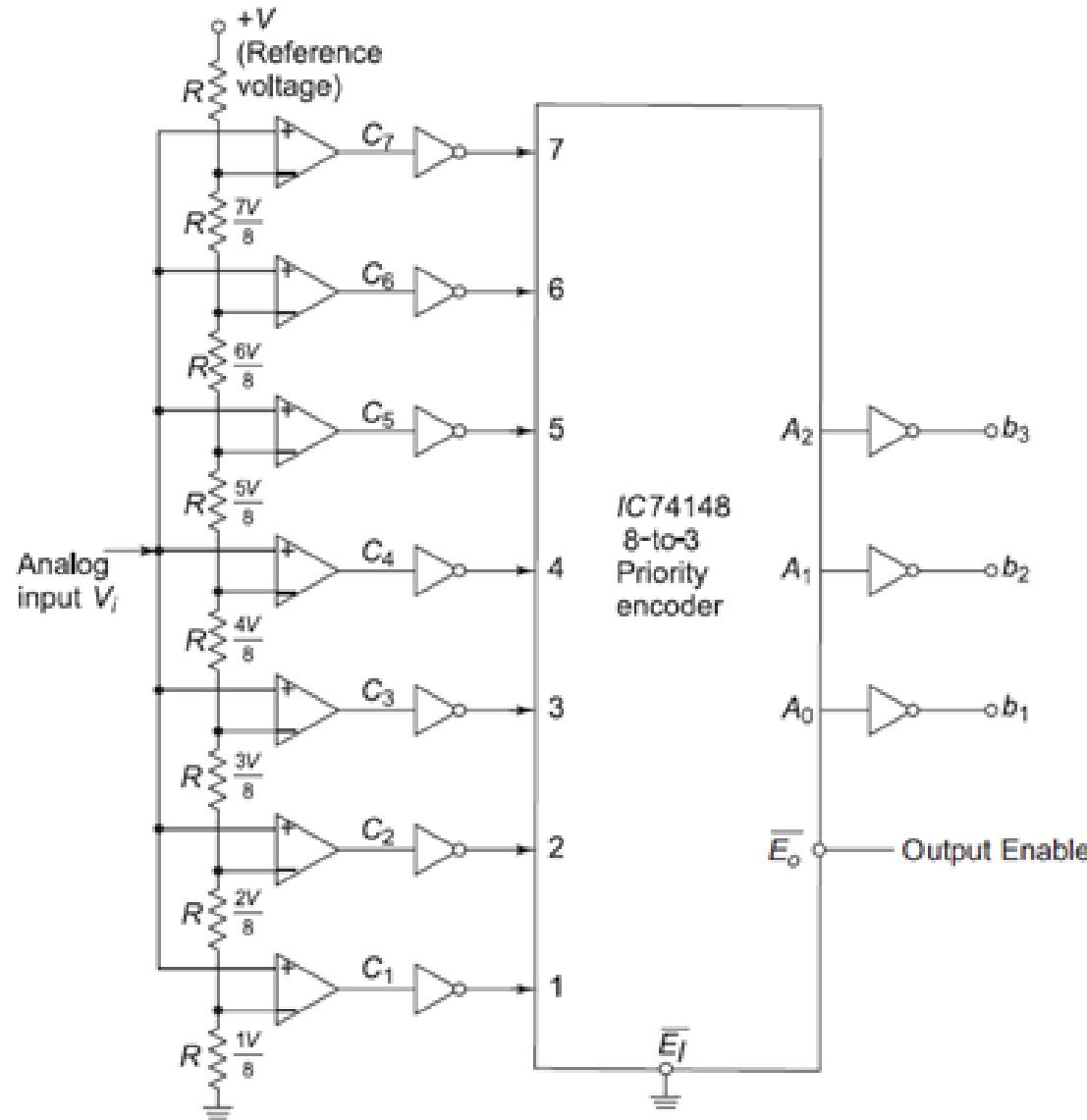
Block diagram of 3-bit simultaneous type A/D converter

# 3-bit Flash type ADC

Comparator and digital outputs for 3-bit simultaneous type A/D converter

Analog Input Voltage (V)	Comparator Outputs							Digital Outputs		
	$C_1$	$C_2$	$C_3$	$C_4$	$C_5$	$C_6$	$C_7$	$b_3$	$b_2$	$b_1$
$0 \leq V_i \leq V/8$	0	0	0	0	0	0	0	0	0	0
$V/8 \leq V_i \leq 2V/8$	1	0	0	0	0	0	0	0	0	1
$2V/8 \leq V_i \leq 3V/8$	1	1	0	0	0	0	0	0	1	0
$3V/8 \leq V_i \leq 4V/8$	1	1	1	0	0	0	0	0	1	1
$4V/8 \leq V_i \leq 5V/8$	1	1	1	1	0	0	0	1	0	0
$5V/8 \leq V_i \leq 6V/8$	1	1	1	1	1	0	0	1	0	1
$6V/8 \leq V_i \leq 7V/8$	1	1	1	1	1	1	0	1	1	0
$7V/8 \leq V_i \leq V$	1	1	1	1	1	1	1	1	1	1

# Logic Diagram of 3-bit Flash type ADC



Logic diagram of 3-bit simultaneous type A/D converter

# Flash ADC

## PROS

- Very Fast (Fastest)
- Very simple operational theory
- Speed is only limited by gate and comparator propagation delay

## CONS

- Expensive
- Prone to produce glitches in the output
- Each additional bit of resolution requires twice the comparators.

## Advantages

- Flash ADCs are very fast and can convert data at high frequencies.

## Disadvantages

- The major disadvantage to flash ADCs is the complexity of the circuits.
  - an 8-bit Flash ADC requires 255 op amps
  - a 12-bit Flash ADC requires 4095 op amps
  - a 16-bit flash ADC requires 65,535 op amp
- High Cost (Major factor over 6 bits)

# **Flash ADC**

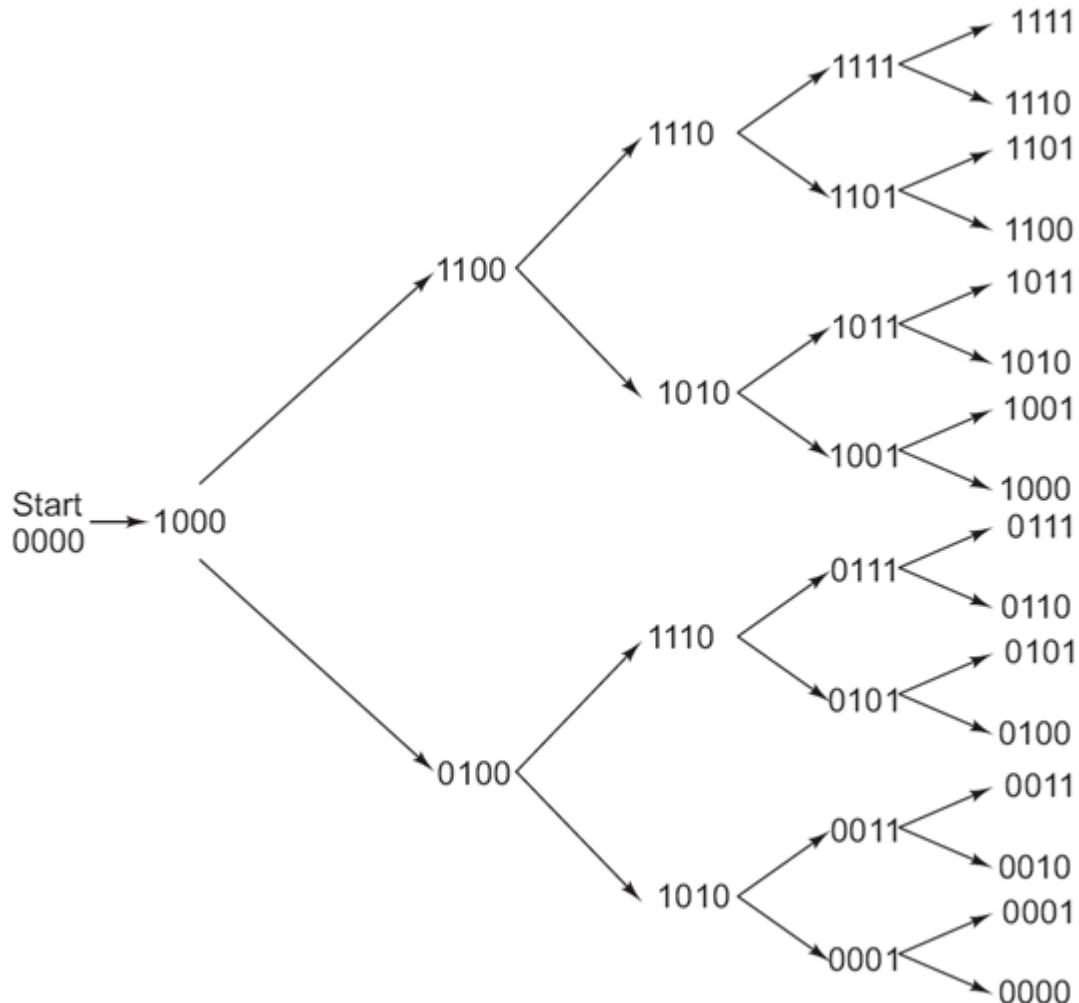
## **Advantages**

- (i) Fastest because A/D conversion is performed simultaneously through a set of comparators. Hence, it is also called flash type A/D converter. Typical conversion time is 100ns or less.**
- (ii) The construction is simple and easier to design.**

## **Disadvantages**

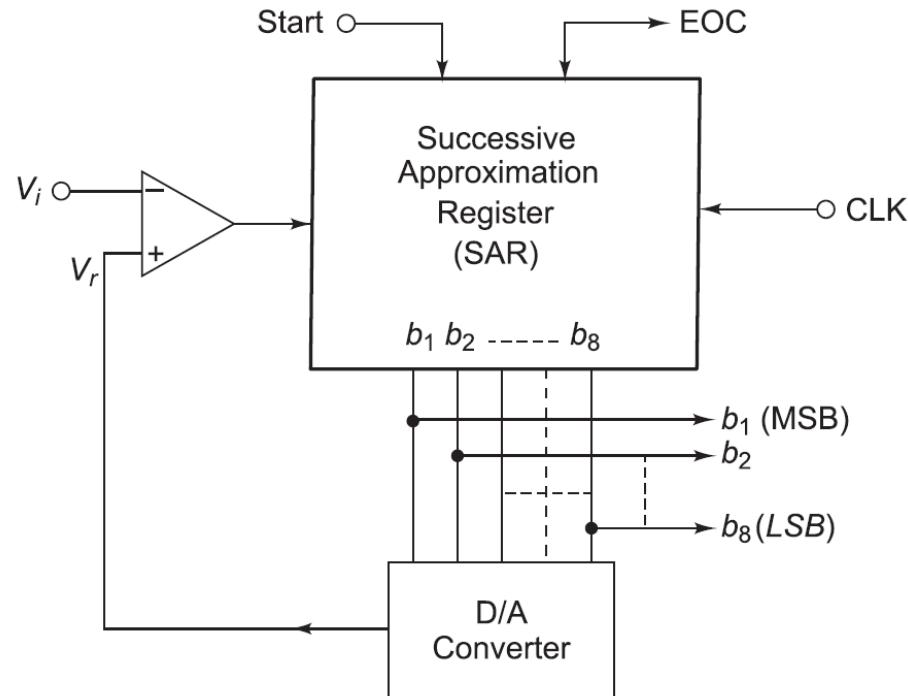
**Not suitable for A/D conversion with more than 3 or 4 digital output bits. Then  $2^{(N)-1}$  comparators are required for an n-bit A/D converter and the number of comparators required doubles for each added bit.**

# Successive Approximation Type A/D Converter



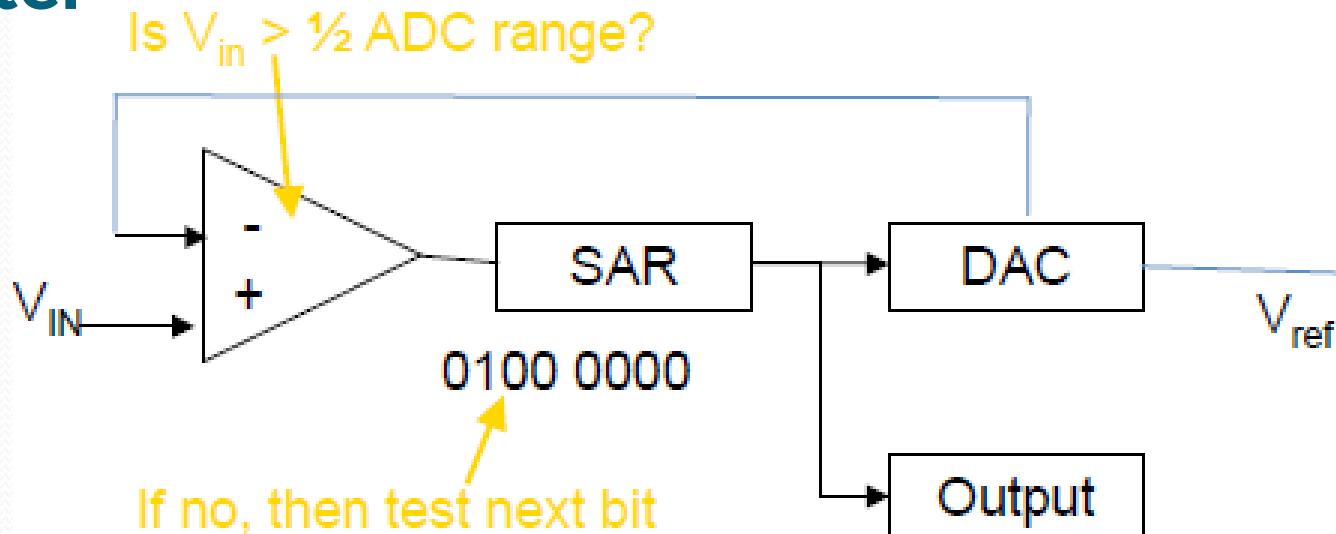
*Successive approximation principle for 4-bit digital output*

# Successive Approximation Type A/D Converter



- Uses a n-bit DAC to compare DAC and original analog results.
- Uses Successive Approximation Register (SAR) supplies an approximate digital code to DAC of  $V_{in}$ .
- Comparison changes digital output to bring it closer to the input value.

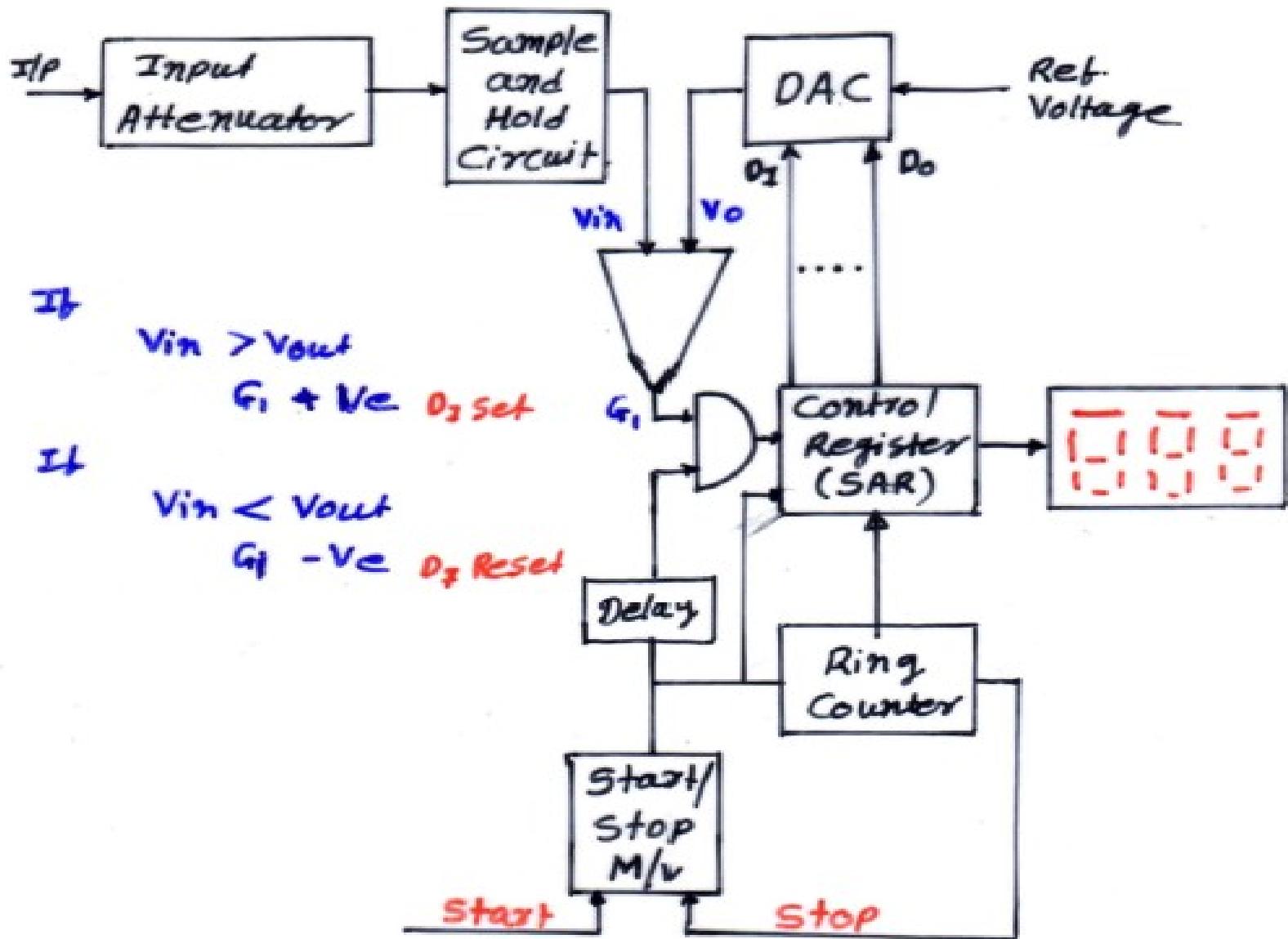
# Working of Successive Approximation Type A/D Converter



1. MSB initialized as 1
2. Convert digital value to analog using DAC
3. Compares guess to analog input
4. Is  $V_{in} > V_{DAC}$ 
  - Set bit 1
  - If no, bit is 0 and test next bit

Closed-Loop

# Successive Approximation



# Successive Approximation ADC

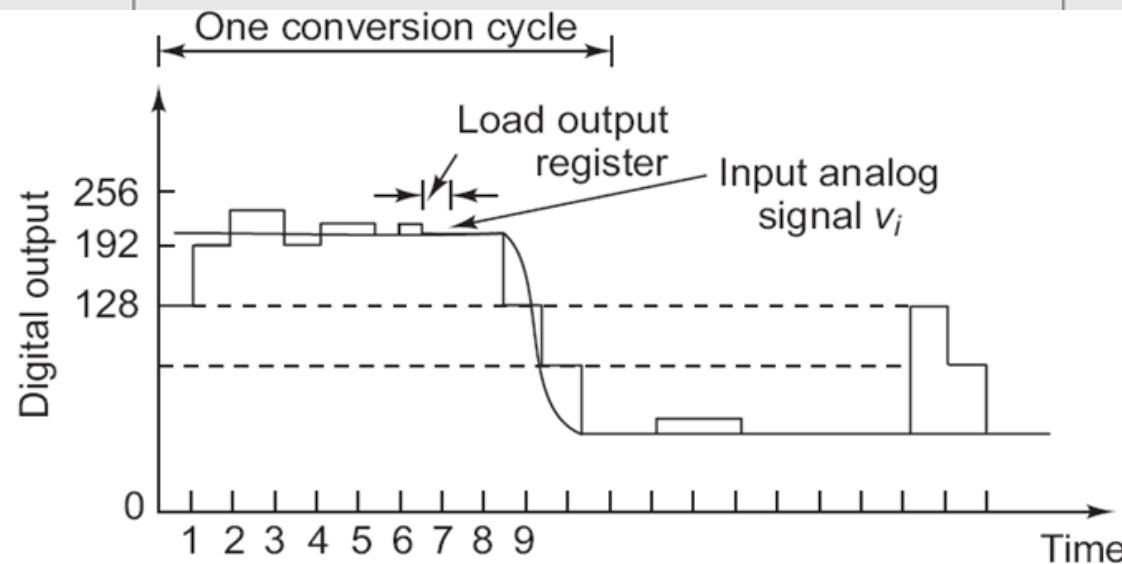
If  $V_{in} =$   
1V

SET	D3	D2	D1	D0	Voltage	Compare	Bit Set/Reset
	2.5	1.25	0.625	0.31 2			
D3	1	0	0	0	2.5V	$V_{in} < V_{out}$	D3 Reset
D2	0	1	0	0	1.25	$V_{in} < V_{out}$	D2 Reset
D1	0	0	1	0	0.625	$V_{in} > V_{out}$	D1 Set
D0	0	0	1	1	0.9375	$V_{in} > V_{out}$	D0 Set

**Final conversion of 1V  
is 0011**

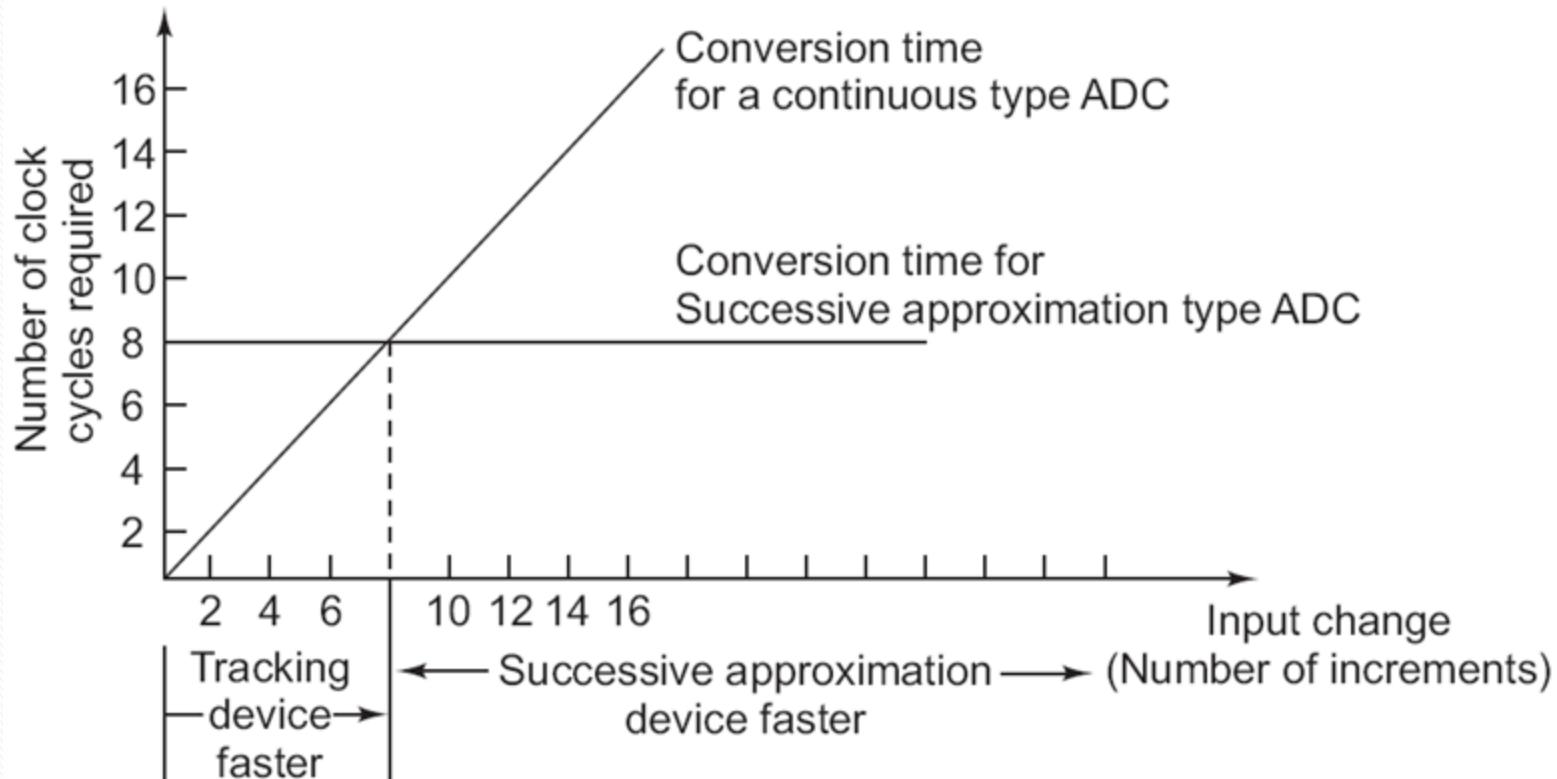
## Successive approximation conversion sequence

Correct Digital Representation	Successive Approximation Register (SAR) Output $V_i$ at Different Stages in the Conversion	Comparator Output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	



*Output response for an analog input*

# Successive Approximation Type A/D Converter



Speed comparison of successive approximation and tracking A/D converters

## **Advantages**

- For n bit ADC- Conversion time = n clock cycles
- Conversion time is independent of amplitude of input signal

## **Disadvantages**

- The circuit is complex
- The conversion time is longer than flash type of ADC

An 8-bit successive approximation A/D converter is driven by a 2 MHz clock signal. Find the conversion time required.

- The time for one clock pulse =  $1 / 2\text{MHz} = 0.5$  microsec.
- The time required to perform the calculation is the sum of (i) the time required for resetting SAR before performing the conversion, and (ii) the time required for performing the conversion. Therefore, the total number of clock pulses required for the conversion is given by ( $8 + 1 = 9$ ) clock cycles =  $9 * 0.5$  microsec = 4.5 microsec.

# Comparison

Type of ADC	Speed	Price	Noise Immunity	Conversion Time
Dual slope	□□□	□□	□□□	Vary $(2*2^n)$ tclk
Successive approximation	□□□	□	□	Constant No. of bits * tclk
Parallel / flash	□□□□□	□□□□□	□	Constant Single tclk

# **4. Digital Integrated Circuit Technology & Convertors**

# Lesson Plan

Introduction to Logic families ( <b>classification, parameters/characteristics</b> ). , Logic Gates using CMOS	1
Design of Synchronous sequential circuits(counter and shift register)	1
Concept of Moore and Mealy machines, Finite state machine design	1
Sequence detectors	1
DAC specs,types,Advantages and Disadvantages	1
weighted resistor type, R-2 Ladder type	1
ADC-specs ,types,Advantages and Disadvantages	1
Flash type ,Successive Approximation type ,ICs like MC1408(DAC) ,ADC0808	1

# Introduction to Logic families

- Using advance techniques, the complex circuits can be miniaturized and produced on a small piece of semiconductor material like silicon. Such a circuit is called integrated circuit (IC). Now-a-days, all the digital circuits are available in IC form. While producing digital ICs, different **circuit configurations and manufacturing technologies** are used. This results into a specific logic family.
- Each logic family designed in this way has identical electrical characteristics such as supply voltage range, speed of operation, power dissipation, noise margin etc.

# Significance of Logic Families

- For the sake of simplicity in design and compatibility in constructing any complex digital system, all digital circuits (ICs) used in the design process should be from same logic family.
- If the electrical IO characteristics of these logic circuits are not similar, there is a need to design an interfacing circuit to maintain the compatibility of digital logic ICs.

- This interfacing circuit will match the electrical characteristics of the logic circuits. This ensures the compatibility for proper operation of the circuit.
- In a logic family, the family members have similar electrical characteristics. Digital logic circuit has to be designed considering these compatibilities of different logic families in terms of different characteristics and parameters associated with the families.

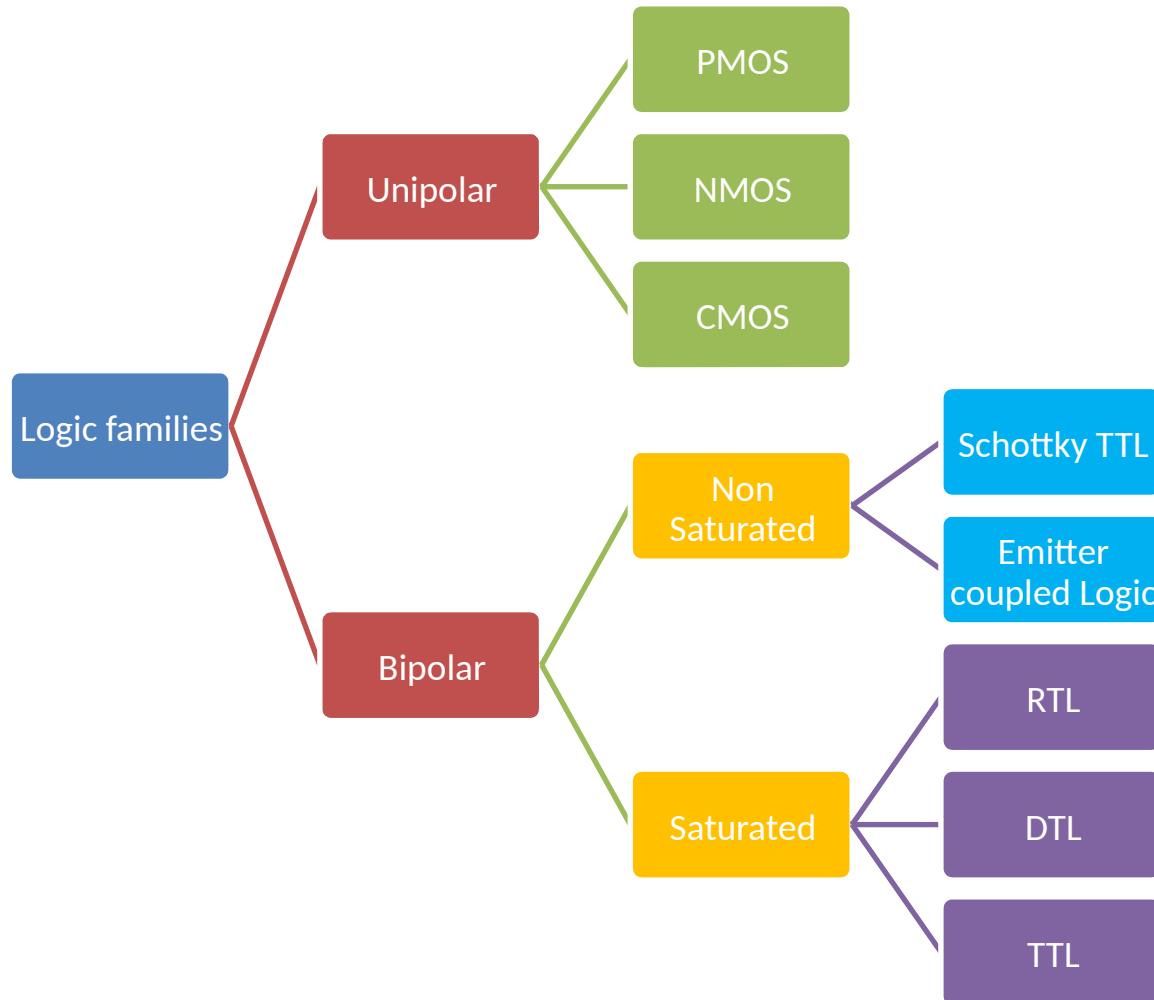
# Types of logic families

- The group of ICs are fabricated using a specific circuit configuration which is referred to as a Logic family. The circuit design of the basic gate of each logic family is the same.
- The logic family is designed by considering the basic electronic components such as resistors, diodes, transistors, and MOSFET; or combinations of any of these components

# Table 1. Logic families and the components used for construction of logic family

Name of logic family	Components used
DL(Diode Logic)	Diodes
RTL(Resistor Transistor Logic)	Resistors and transistors
DTL(Diode Transistor Logic)	Diodes, transistors and resistors
TTL(Transistor Transistor Logic)	Transistors and resistors
ECL(Emitter Coupled Logic)	Transistors and diodes
PMOS(P channel Metal Oxide Semiconductor Logic)	P- MOSFETs
NMOS(N channel Metal Oxide Semiconductor Logic)	N- MOSFETs
CMOS(Complementary Metal Oxide Semiconductor Logic)	P –MOSFET and N-MOSFET

# Logic families are classified according to the principle type of electronic components used in their circuitry



DL, RTL and DTL are not very useful due to some inherent disadvantages while TTL, ECL and CMOS are widely used in many digital circuit design applications

Figure 1 Classification of logic families

- TTL has an extensive list of digital functions and is currently the most popular logic family. ECL is used in systems requiring high-speed operations. MOS is used in circuits requiring a high component density, whereas CMOS is used in systems requiring low power consumption.

# Logic Family/Level of Integration

Scheme	# gates / chip
<b>Small Scale Integration (SSI)</b>	<b>&lt;12</b>
<b>Medium Scale Integration (MSI)</b>	<b>12 - 99</b>
<b>Large Scale Integration (LSI)</b>	<b>1000</b>
<b>Very large Scale Integration (VLSI)</b>	<b>10k</b>
<b>Ultra large Scale Integration (ULSI)</b>	<b>100k</b>
<b>Giga Scale Integration (GSI)</b>	<b>1Meg</b>

Note: Ratio gate count/transistor count is roughly 1/10  
IC logic gates fall under SSI, combinational logic circuits fall under MSI, and Microprocessor system come under LSI and VLSI.

# Nomenclature of Logic family

- The prefix of the part number represents the manufacturer code and the suffix at the middle denotes the subfamily of the ICs and suffix at the end denotes the packaging type.
- For example: If the part number is S74F08N. The 7408 is the basic number used by all manufacturer for quad AND gate. The S prefix is the manufacture's manufacture's code for Signetics, F stands for FAST TTL subfamily, and the N suffix at the end is used to specify the plastic dual in line packaging

- **Suffix used for packaging:**

N - Plastic dual in line package W - Ceramic flat pack

D - Surface mounted plastic package

- **Prefix used for manufacturers:**

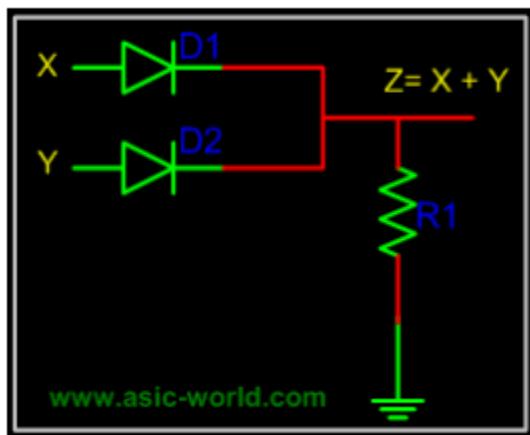
S - Signetics SN - Texas Instruments DM - National Semiconductor

- **Suffix used for subfamily:**

74H04 - High-speed 74L045- Low-Power 74S04 -  
Uses a Schottky Diode 74ALS04 - Advanced low  
power Schottky

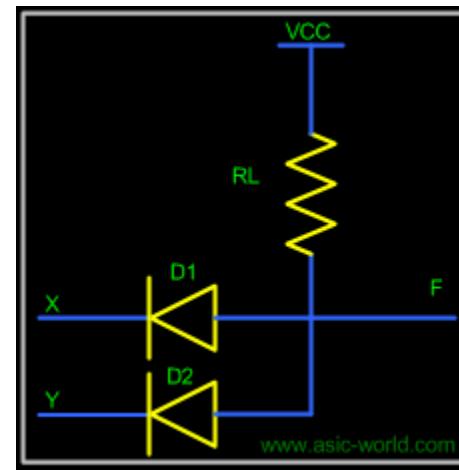
# Diode Logic Family

- In diode logic family, all the logic is implemented using diodes and resistors.



OR

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

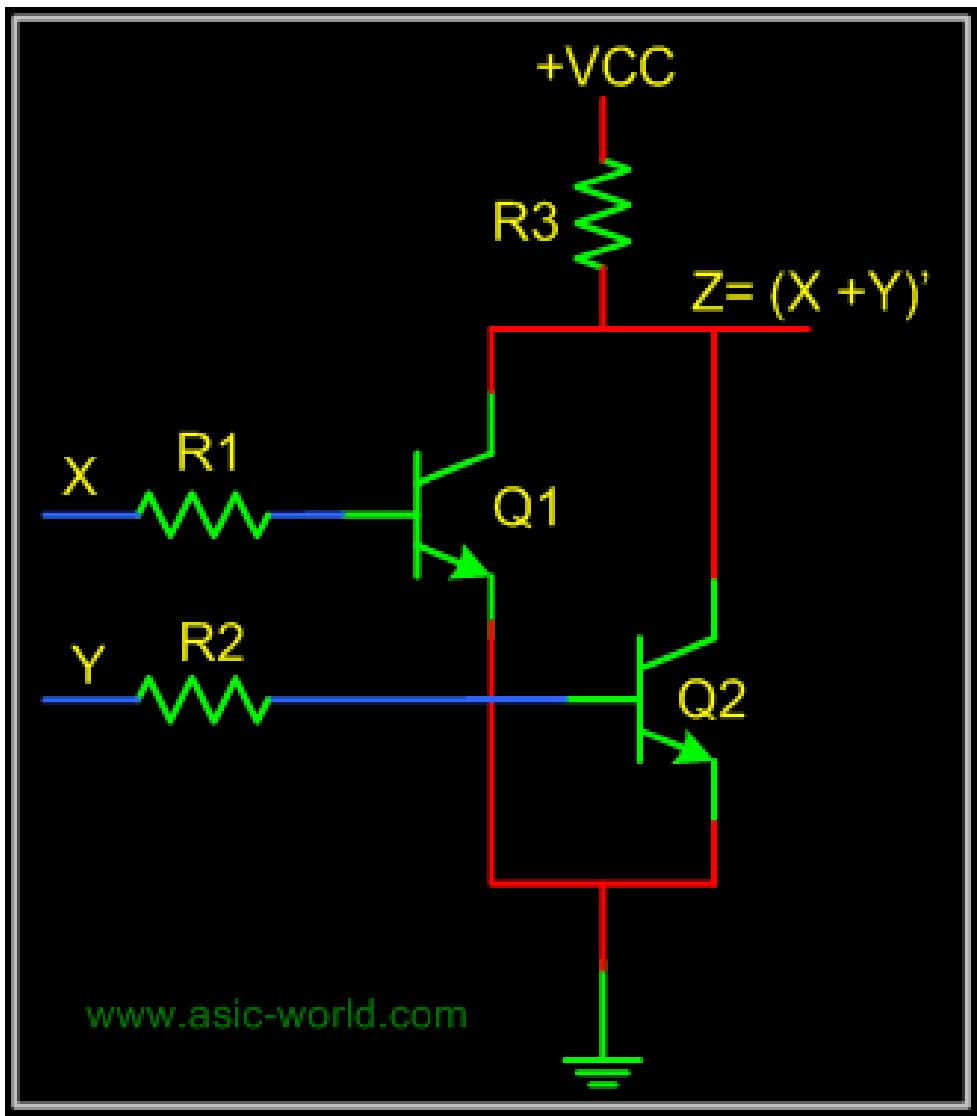


AND

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

- Diode Logic suffers from voltage degradation from one stage to the next.
- Diode Logic only permits OR and AND functions, cannot perform a NOT function.
- Diode Logic is used extensively but not in integrated circuits

# Resistor Transistor Logic (RTL) Family

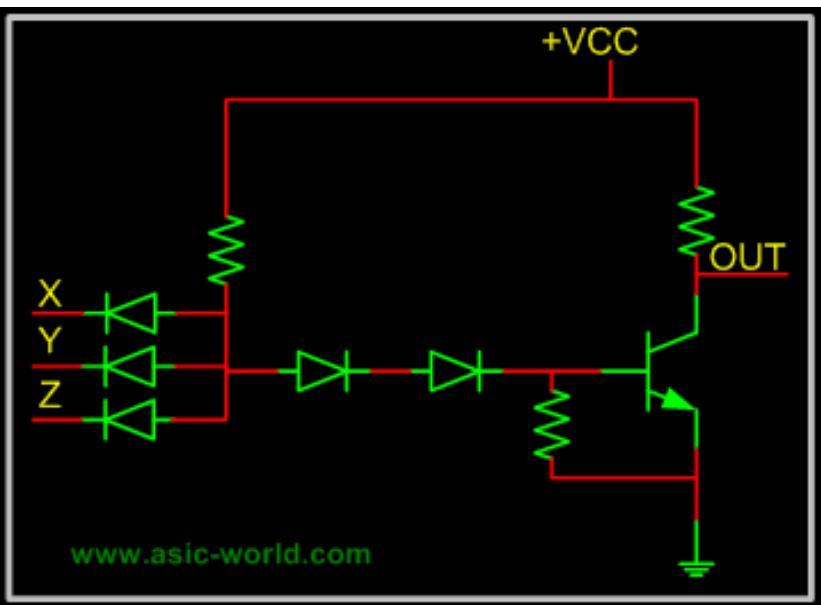


A basic circuit of an RTL NOR gate consists of two transistors Q1 and Q2, connected as shown in figure above. When either of input X or Y is driven HIGH, corresponding transistor goes to saturation and output Z is pulled to LOW.

X	Y	$Z = (X+Y)'$
0	0	1
0	1	0
1	0	0
1	1	0

- RTL draw a significant amount of current from the power supply for each gate. Another limitation is that RTL gates cannot switch at the high speeds used by today's computers, although they are still useful in slower applications

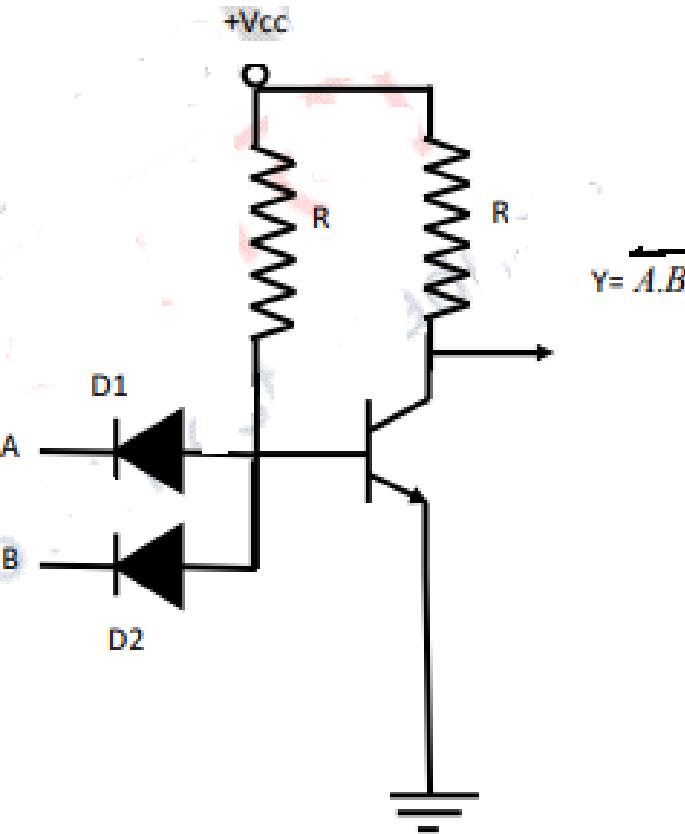
# Diode Transistor Logic



Each of the input is associated with one diode. The diodes and the 4.7K resistor form an AND gate. If input X, Y, Z is low, the corresponding diode conducts current, thorough the 4.7K resistor. Thus there is no current through the diodes connected in series to transistor base . Hence the transistor does not conduct, thus remains in cut-off, and output out is High.

If all the inputs X, Y , Z are driven high, the series diodes conduct and thus driving transistor into saturation. Thus output out is Low

# Diode Transistor Logic



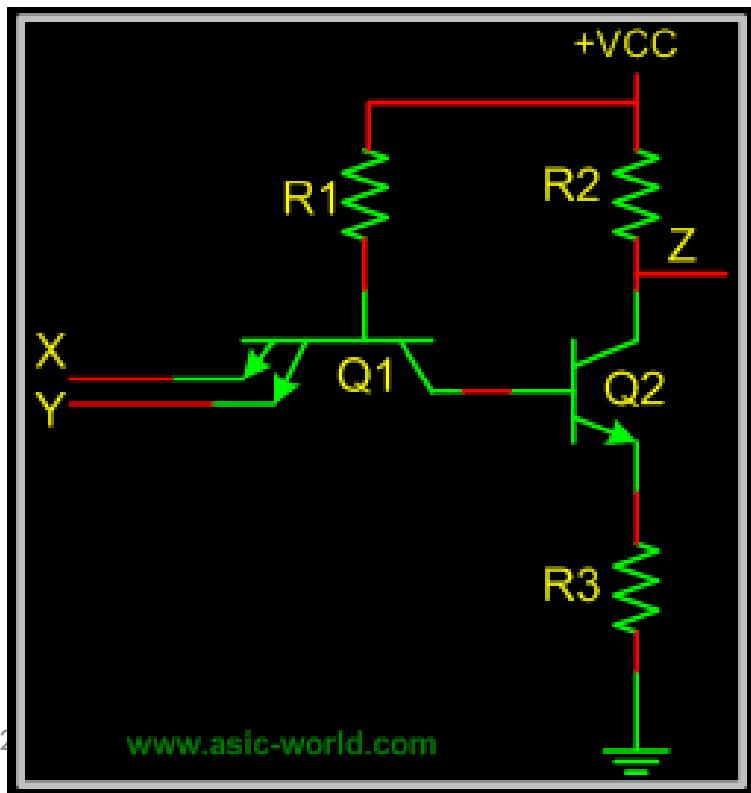
In this circuit, diodes and transistors are fabricated into a single IC. When both inputs A and B are logic 0, diodes D1 and D2 are forward biased and the transistor is OFF. This is because, the emitter base junction of transistor is reverse biased and output Y is at logic 1. Hence, if one of the inputs is a logic 0 output Y is at logic level 1. On the other hand, if both A and B are high, diodes are reverse biased and the transistor is ON and output Y is at logic 0. Therefore, this circuit behaves like simple NAND gate

A	B	$Z = (A \cdot B)'$
0	0	1
0	1	1
1	0	1
1	1	0

# Transistor Transistor Logic

- Many versions of TTL family
  - Standard TTL.
  - High Speed TTL
  - Low Power TTL.
  - Schhottky TTL
- TTL have three configuration at the output
  - Totem - Pole output.
  - Open Collector Output.
  - Tristate Output.

- The input stage, which is used almost with all the versions of TTL. This consists of input transistor and phase splitter transistor. Input stage consists of multi emitter transistor as shown in figure. When any of the input is driven low, i.e. emitter base junction is forward biased and input transistor conducts. This in turn drives the phase splitter transistor into cut-off.



**Multi-emitter input transistor is a striking feature of TTL logic family.**

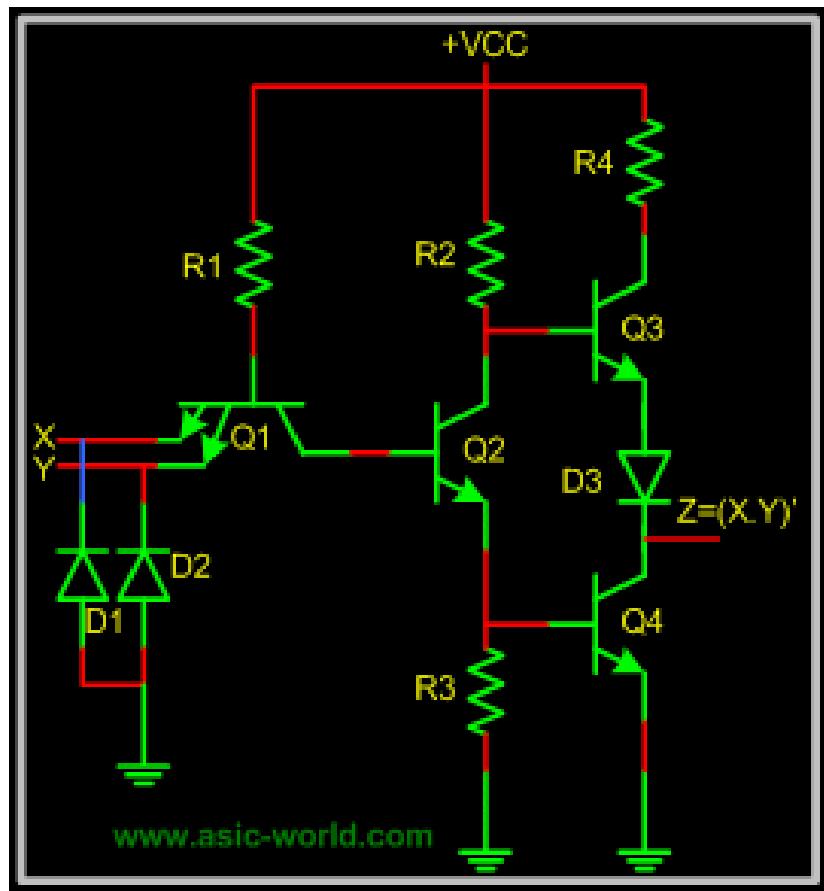
# Totem Pole output

- Below is the circuit of a totem-pole NAND gate, which has got three stages
  - Input Stage
  - Phase Splitter Stage
  - Output Stage

Output stage is called Totem-Pole because, the transistor Q3 sits upon Q4. Q3 and Q4 are stacked one above the other in such a way that while one of these conducts, the other is cut-off.

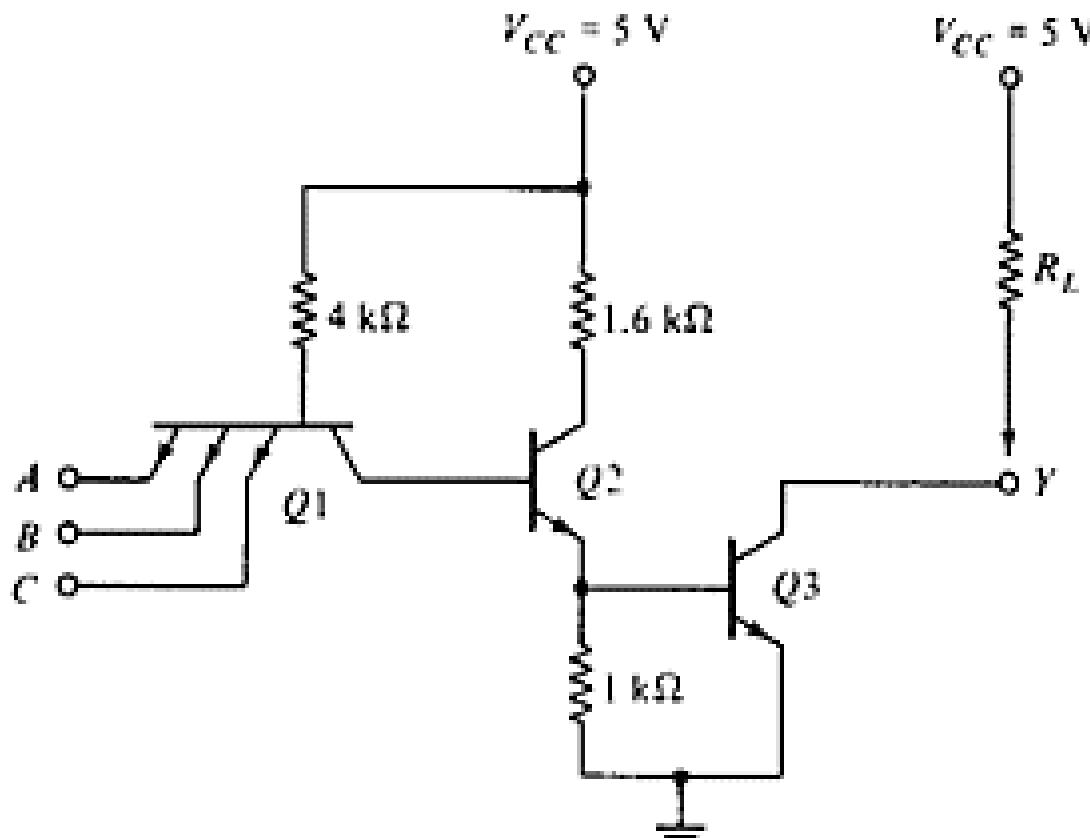
Q4 is called pull-down transistor, as it pulls the output voltage down, when it saturates and other is in cut-off (i.e. Q3 is in cut-off). Q3 is called pull-up transistor, as it pulls the output voltage up, when it saturates and other

- Diodes in input are protection diodes, which conduct when there is large negative voltage at input. Thus shorting the negative voltage to ground.



# Open Collector Output

- The main feature is that its output is 0 when low and floating when high. Usually, an external  $V_{cc}$  may be applied.

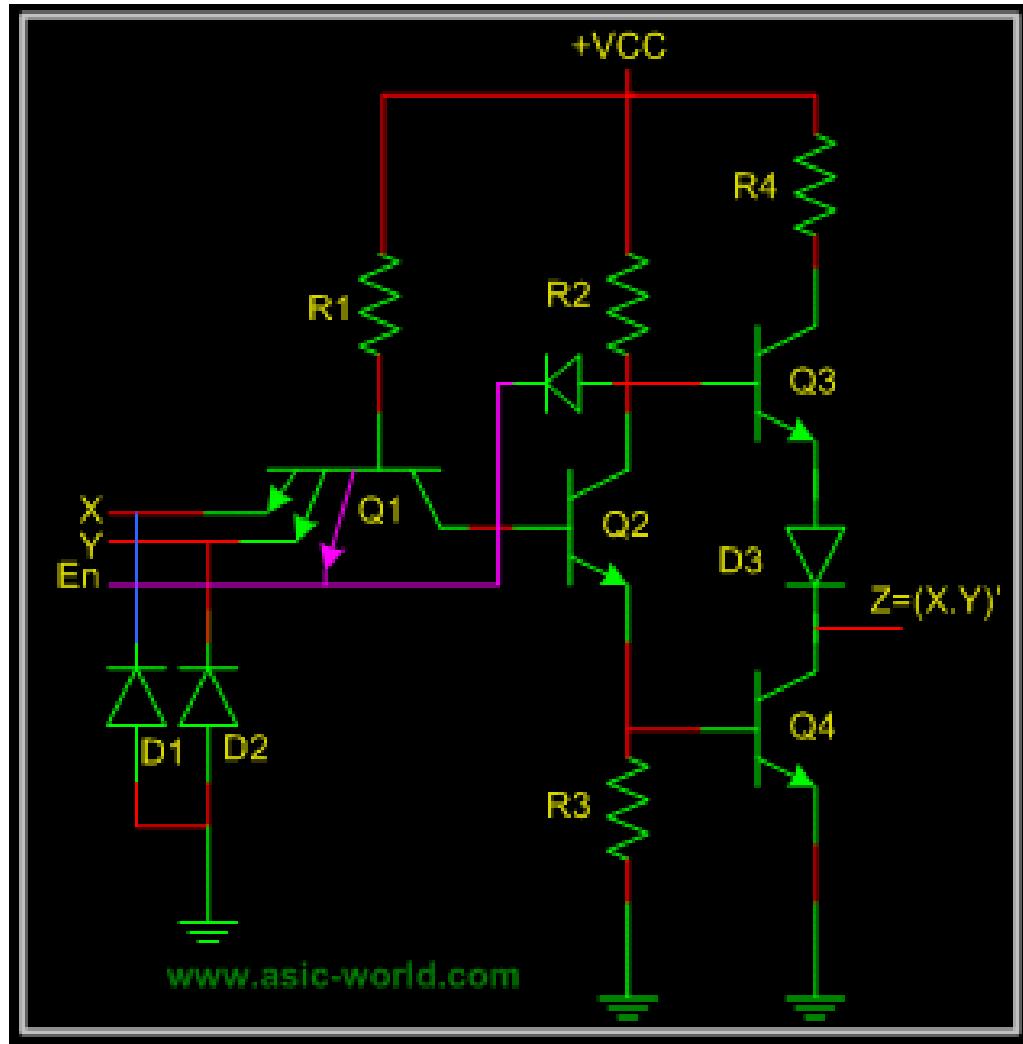


- Transistor Q1 behaves as a cluster of diodes placed back to back. With any of the input at logic low, the corresponding emitter-base junction is forward biased and the voltage drop across the base of Q1 is around 0.9V, not enough for the transistors Q2 and Q3 to conduct. Thus the output is either floating or  $V_{cc}$ , i.e. High level.
- Similarly, when all inputs are high, all base-emitter junctions of Q1 are reverse biased and transistor Q2 and Q3 get enough base current

# Tristate Output

- Below circuit is tri-state NAND gate, when Enable En is HIGH, below circuits works like any other NAND gate. But when Enable En is driven LOW. Q1 Conducts, and diode connecting emitter of Q1 and collector of Q2 conducts. Thus driving Q3 into cut-off. Since Q2 is not conducting, Q4 is also at cut-off. When both the pull-up and pull-down transistors are not conducting, out Z is in high-impedance state.

# Tristate Output



- Depending upon the components used for fabrication, the digital ICs are classified into different families as TTL, CMOS and ECL. One has to use the same logic family for designing the logic circuit in order to avoid complexity in the circuit design and address the issue of compatibility

- **Emitter-Coupled Digital Logic Gate**

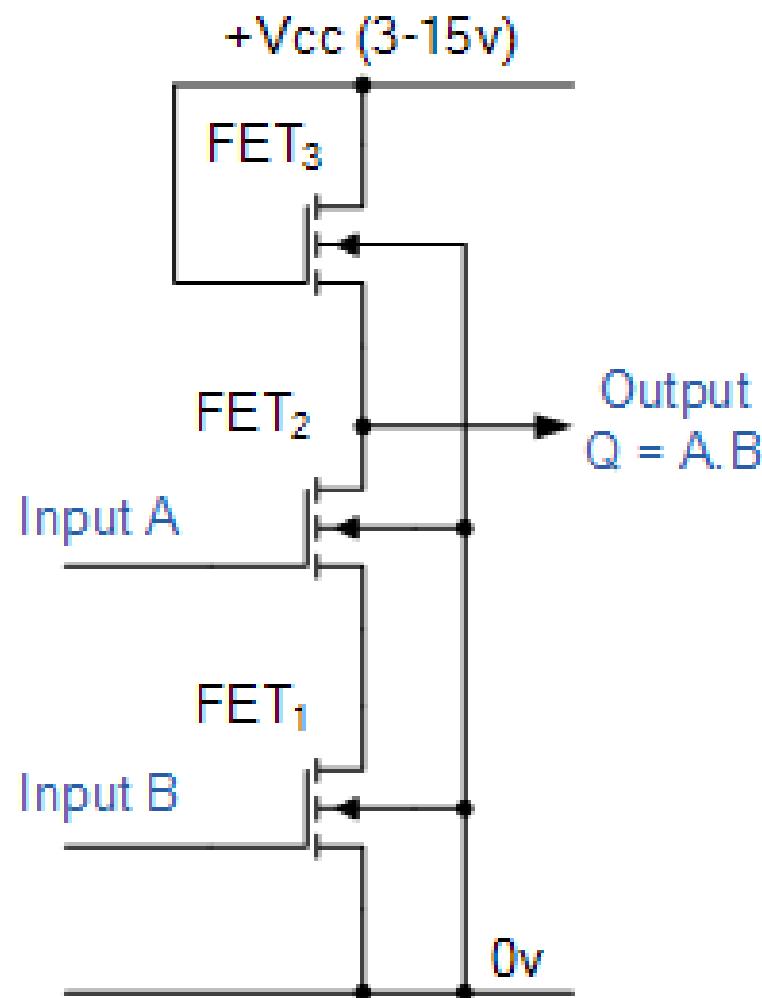
ECL uses bipolar transistor logic where the transistors are not operated in the saturation region, as they are with the standard TTL digital logic gate. Instead the input and output circuits are push-pull connected transistors with the supply voltage negative with respect to ground.

- This has the effect of increasing the speed of operation of the emitter coupled logic gates up to the Gigahertz range compared with the standard TTL types, but noise has a greater effect in ECL logic, because the unsaturated transistors operate within their active region and amplify as well as switch signals

# Basic CMOS Digital Logic Gate

- The main disadvantages with the TTL digital logic gate series is that the logic gates are based on bipolar transistor logic technology and as transistors are current operated devices, they **consume large amounts of power** from a fixed +5 volt power supply.
- Also, TTL bipolar transistor gates have **a limited operating speed** when switching from an “OFF” state to an “ON” state and vice-versa called the “gate” or “propagation delay”. To overcome these limitations complementary MOS called “CMOS” (**Complementary Metal Oxide Semiconductor**) logic gates which use “Field Effect Transistors” or

- As these gates use both P-channel and N-channel MOSFET's as their input device, at quiescent conditions with no switching, the **power consumption of CMOS gates is almost zero**, (1 to  $2\mu A$ ) making them **ideal for use in low-power battery circuits and with switching speeds upwards of 100MHz for use in high frequency timing and computer circuits.**
- This basic CMOS gate example contains three N-channel normally-off **enhancement** MOSFET's, one for each input consisting of FET<sub>1</sub> and FET<sub>2</sub>, and an additional switching MOSFET, FET<sub>3</sub> which is biased permanently “ON” through its gate.



## 2-input NAND Gate

12/20/2022

When one or both inputs "A" and "B" are grounded to logic level "0", the corresponding input MOSFET, FET<sub>1</sub> or FET<sub>2</sub> are switched "OFF" producing a logic "1" (HIGH) output condition from the source terminal of FET<sub>3</sub>.

Only when both inputs "A" and "B" are held HIGH at logic level "1", does current flow through the corresponding MOSFET switching it "ON" producing an output state at Q equivalent to a logic level "0" as both MOSFETs, FET<sub>1</sub> and FET<sub>2</sub> are conducting. Therefore producing the switching action.

- Like TTL logic, complementary MOS (CMOS) circuits take advantage of the fact that both N-channel and P-channel devices can be fabricated together on the same substrate material to form various logic functions.
- One of the **main disadvantage** with the CMOS range of IC's compared to their equivalent TTL types is that they **are easily damaged by static electricity**. Also unlike TTL logic gates that operate on **single +5V** voltages for both their input and output levels, CMOS digital logic gates operate on a single supply voltage of between **+3 and +18 volts**.

- Note that CMOS logic gates and devices are static sensitive, so always take the appropriate precautions of working on antistatic mats or grounded workbenches, wearing an antistatic wristband and not removing a part from its antistatic packaging until required.

# Digital IC Family Parameters

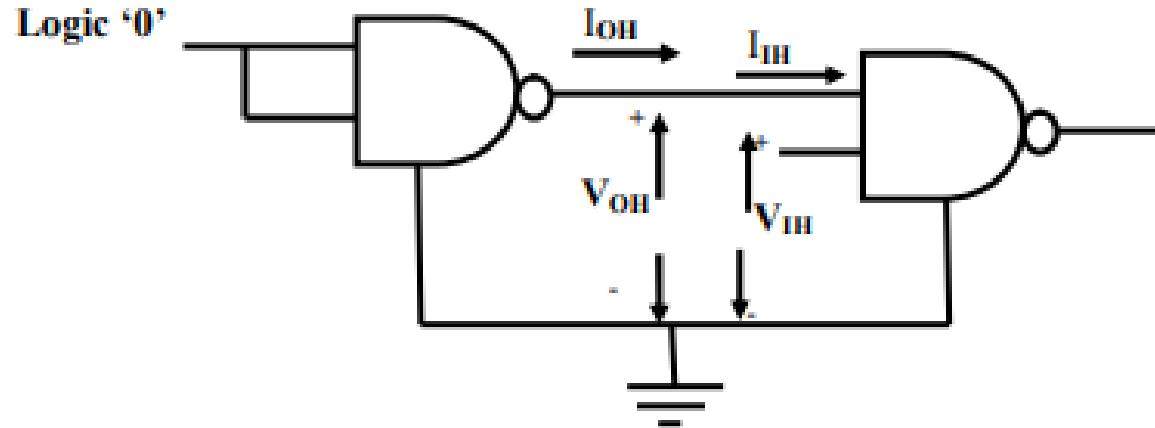
## Performance Parameters of logic families

- Voltage Parameters:

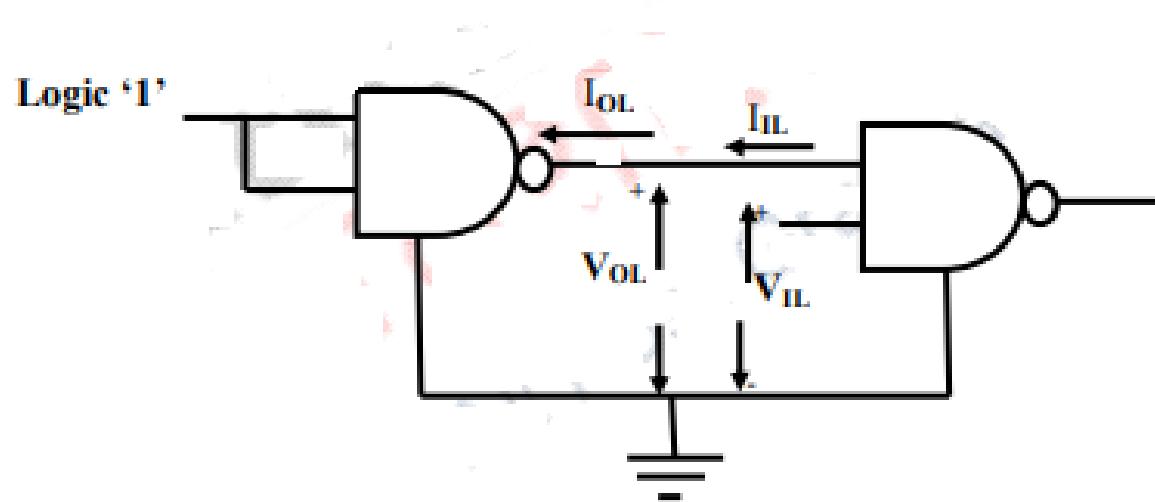
- $V_{IH}(\text{min})$ : high-level input voltage, the minimum voltage level required for a logic 1 at an *input*.
- $V_{IL}(\text{max})$ : low-level input voltage
- $V_{OH}(\text{min})$ : high-level output voltage
- $V_{OL}(\text{max})$ : low-level output voltage

### Current Parameters

- $I_{IH}(\text{min})$ : high-level input current, the current that flows into an input when a specified high-level voltage is applied to that input.
- $I_{IL}(\text{max})$ : low-level input current
- $I_{OH}(\text{min})$ : high-level output current
- $I_{OL}(\text{max})$ : low-level output current

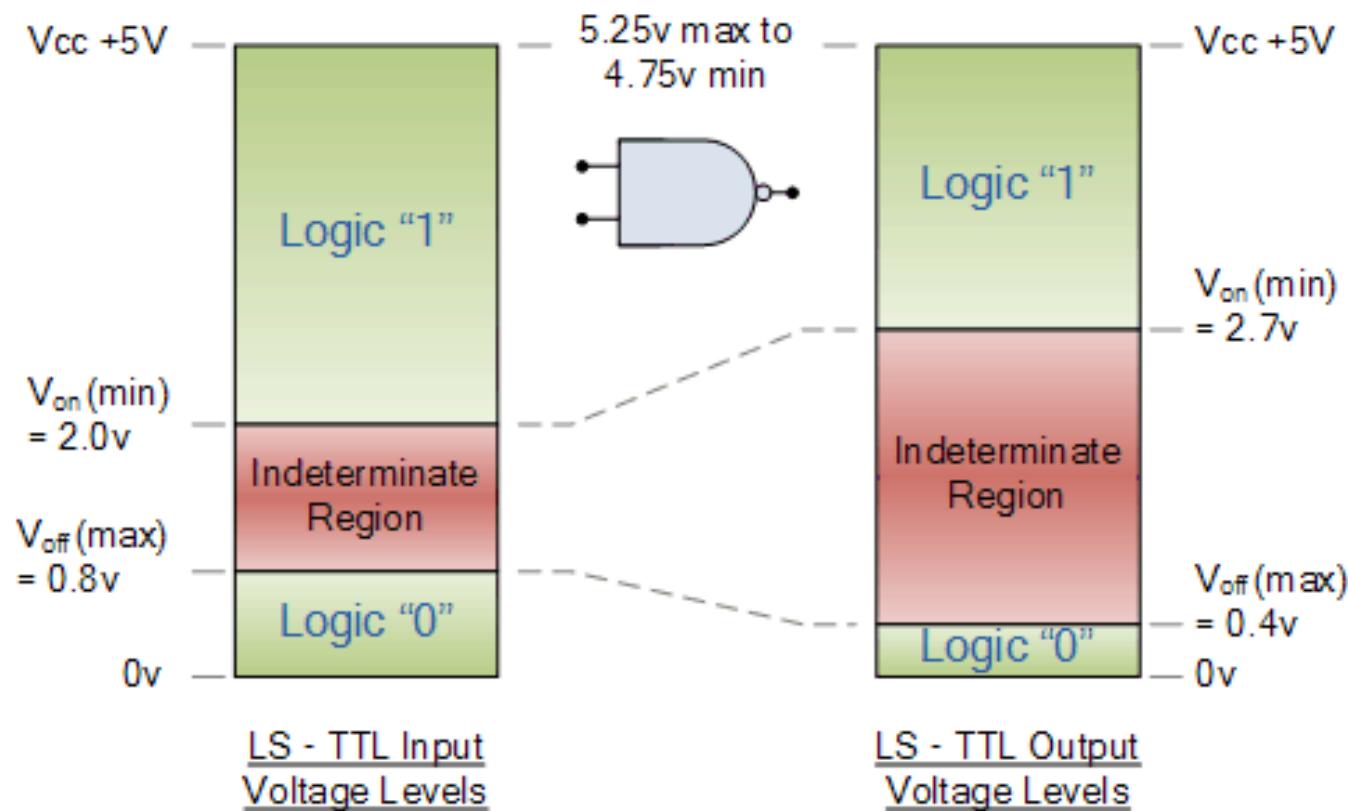


**High level Input and output current and voltage requirements**



**Low level Input and output current and voltage requirements**

# TTL Input & Output Voltage Levels



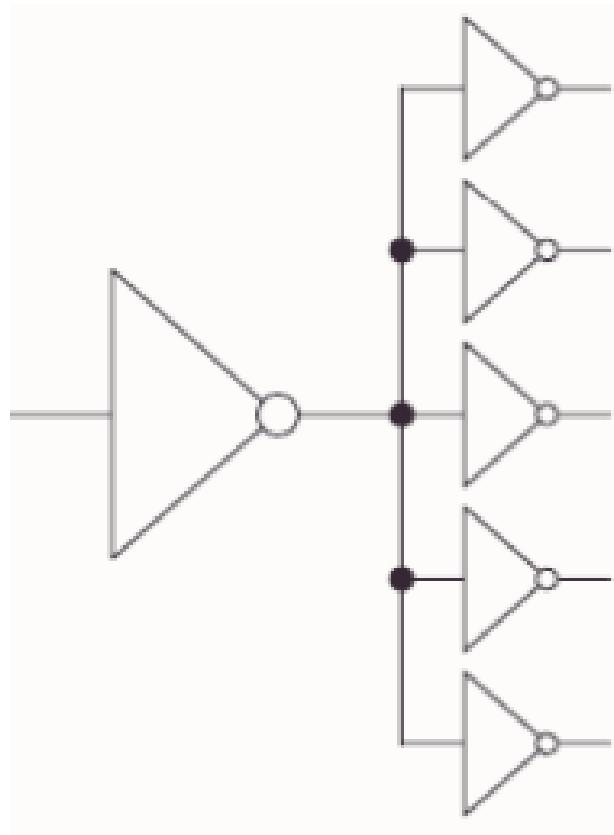
## TTL and CMOS Logic Levels

Device Type	Logic 0	Logic 1
TTL	0 to 0.8v	2.0 to 5v (V <sub>CC</sub> )
CMOS	0 to 1.5v	3.0 to 18v (V <sub>DD</sub> )

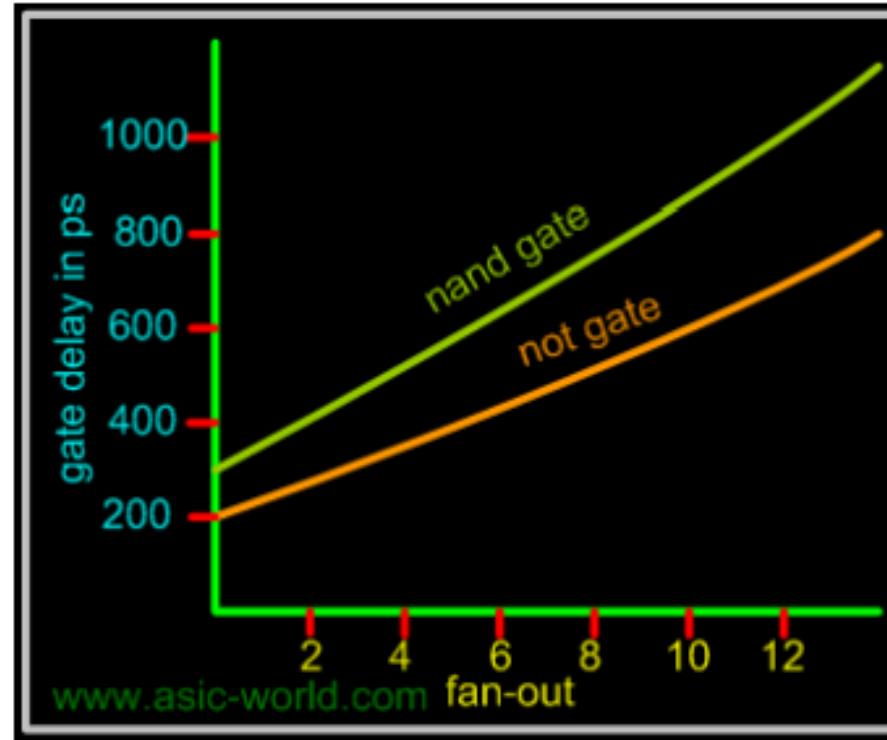
# Performance Parameters of logic families

- Fan-out
- Input and Output Voltage level
- Noise Margin
- Rise and Fall time, and Propagation delay
- Power Dissipation.

- The **fan-out** of a subfamily is defined as the number of gate inputs of the same subfamily that can be connected to a single output without exceeding the current ratings of the gate. A typical fan-out for most TTL subfamilies is 10

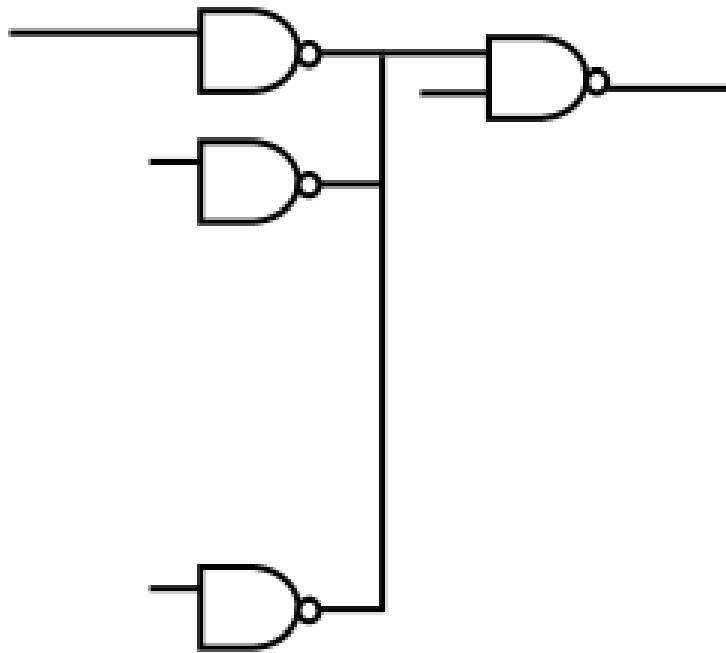


- The fan-out really depends on the amount of electric current a gate can source or sink while driving other gates. The effects of loading a logic gate output with more than its rated fan-out will degrade the performance of the circuit. The gate delay increases with increase in fan-out



- The output current capability for the HIGH condition is abbreviated  $I_{OH}$  and is called source current.  $I_{OH}$  for the 7400 is -400uA maximum. (- sign shows current is leaving the gate) The input current required under HIGH condition is abbreviated  $I_{IH}$  and for 74xx subfamily is equal to 40uA maximum. **Fan -out =  $400/40 = 10$**
- For the LOW condition, the maximum output current for the 74xx subfamily is 16mA, and the input requirement is -1.6mA maximum. The fan-out is usually same for both the HIGH and LOW conditions for 74xx subfamily; if not, we use the lower of the two. Because a LOW output level is close to 0V, the current actually flows into the output terminal and sinks down to ground. This is called sink current.

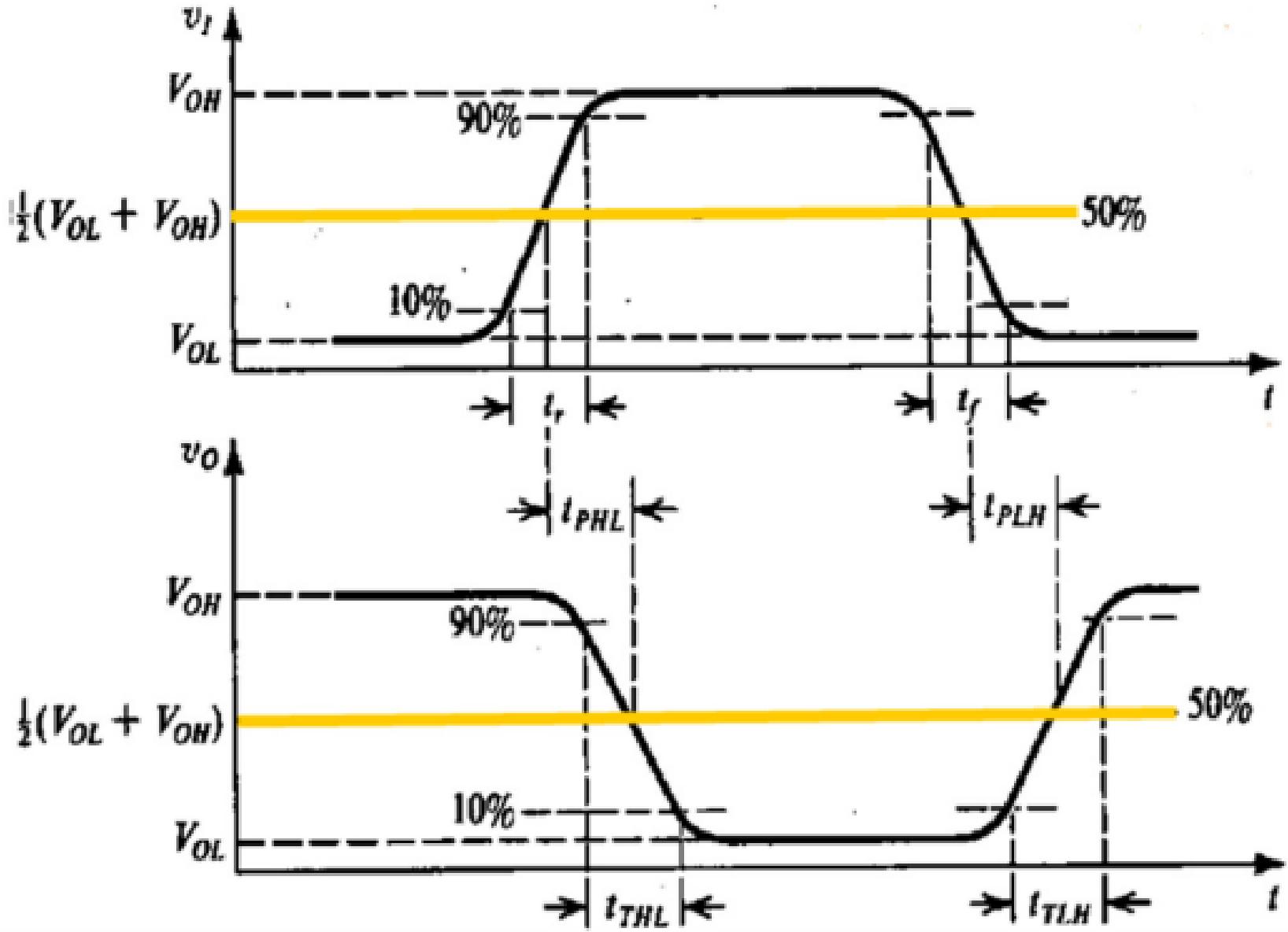
- **Fan in:** This is the number of inputs of a logic gate. It is decided by the input current sinking capability of a logic gate as shown in Figure



- . **Power Dissipation**: This is the power supplied required to operate the gate. It is expressed in milliwatt (mW) and represents actual power dissipated in the gate. It is the number that represents power delivered to gate from the power supply. The total power dissipated in the digital system is sum of power dissipated in each digital IC.
- The power dissipation parameter for a logic family is specified in terms of power consumption per gate and is the product of supply voltage VCC and supply current ICC. The supply current is taken as the average of the HIGH-level supply current ICCH and the LOW-level supply current ICCL

- **Rise time,  $t_r$** : This is the time that elapses between 10% and 90 % of the final signal level when the signal makes a transition from logic LOW to logic HIGH.
- **Fall time,  $t_f$** : This is the time that elapses between 90 and 10 % of the signal level when the signal makes a transition from logic LOW to logic HIGH

- **Propagation delay  $t_p$** : The propagation delay is the time delay between the occurrence of change in the logical level at the input and before it is reflected at the output. It is the time delay between the specified voltage points on the input and output waveforms. Propagation delays are separately defined for LOW-to-HIGH and HIGH-to-LOW transitions at the output. In addition, we also define enable and disable time delays that occur during transition between the high-impedance state and defined logic LOW or HIGH states.



- The propagation delay time is defined as the average of low-to-high (t<sub>PLH</sub>) propagation delay time and the high-to-low (t<sub>PHL</sub>) propagation delay time. Propagation delay time  $t_P = (t_{PLH} + t_{PHL}) / 2$ . The propagation delay time is directly proportional to the switching time and increases as the Fan-out increases.

- It is the average transition delay time for a signal to propagate from input to output when the binary signals change in value. The signal through gate takes a certain amount of time to propagate from the inputs to the output. The interval of time is defined as the propagation delay of the gate. Propagation delay is expressed in nanoseconds(ns). The signals travelling from input to output of the system pass through a number of gates. **The propagation delay of the system is the sum of the propagation delays of all these gates.**

**Speed-power product.** The speed of a logic circuit can be increased, that is, the propagation delay can be reduced, at the expense of power dissipation.

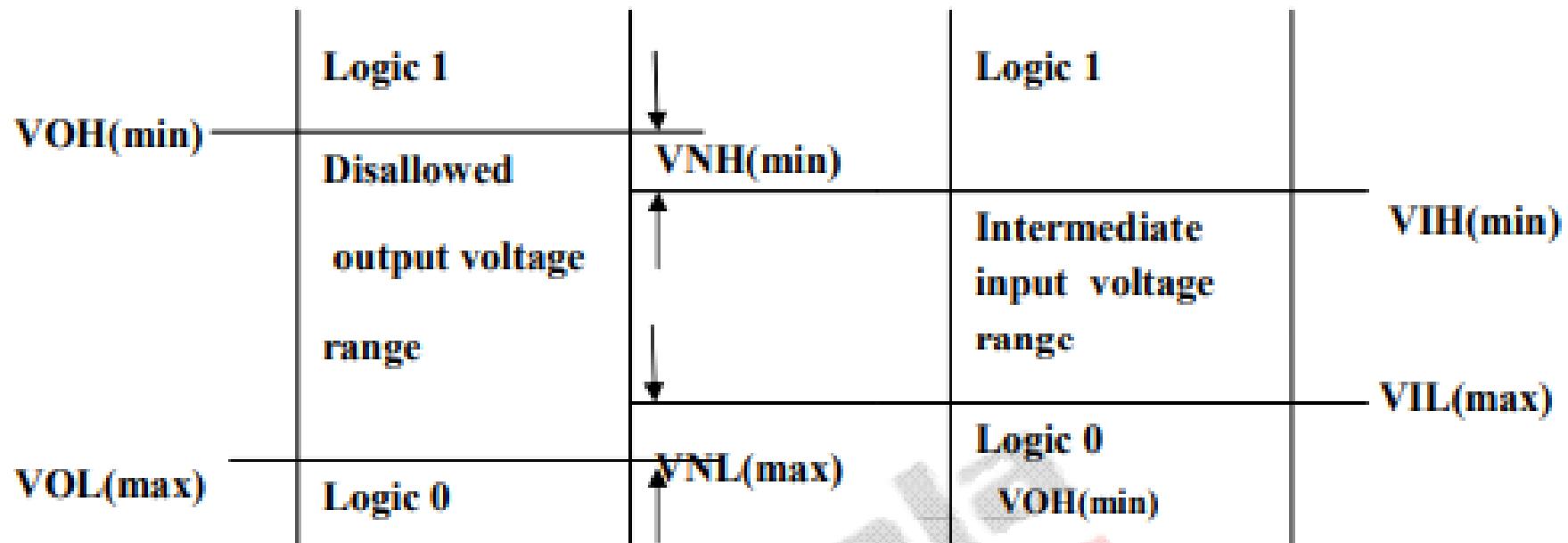
- When a bipolar transistor switches between cut-off and saturation, it dissipates the least power, but has a large associated switching time delay.
- On the other hand, when the transistor is operated in the active region, power dissipation goes up, while the switching time decreases drastically.

# Speed-power product

- It is always desirable to have low values for both propagation delay, and power dissipation parameters.
- A useful figure-of-merit used to evaluate different logic families is the speed-power product, expressed in picojoules, which is the product of the propagation delay (measured in nanoseconds) and the power dissipation per gate (measured in milliwatts).

# Noise Margin

- This is the maximum noise voltage added to the input signal of digital circuit that does not cause an undesirable change in the circuit output. There are two types of noise to be considered here
  - DC noise :This is caused by a drift in the voltage levels of a signal
  - AC noise: This is caused by random pulse that may be created by other switching signals.



## Noise Margin

Figure shows the generalized case of legal HIGH and LOW voltage levels for output.

The LOW output state can tolerate a positive voltage spike equal to  $(VIL(\text{max.}) - VOL(\text{max}))$ ; and still be a legal LOW input.

The HIGH output state can tolerate a negative voltage spike equal to  $(VOH(\text{min.}) - VIH(\text{min.}))$  and still be a legal HIGH input.

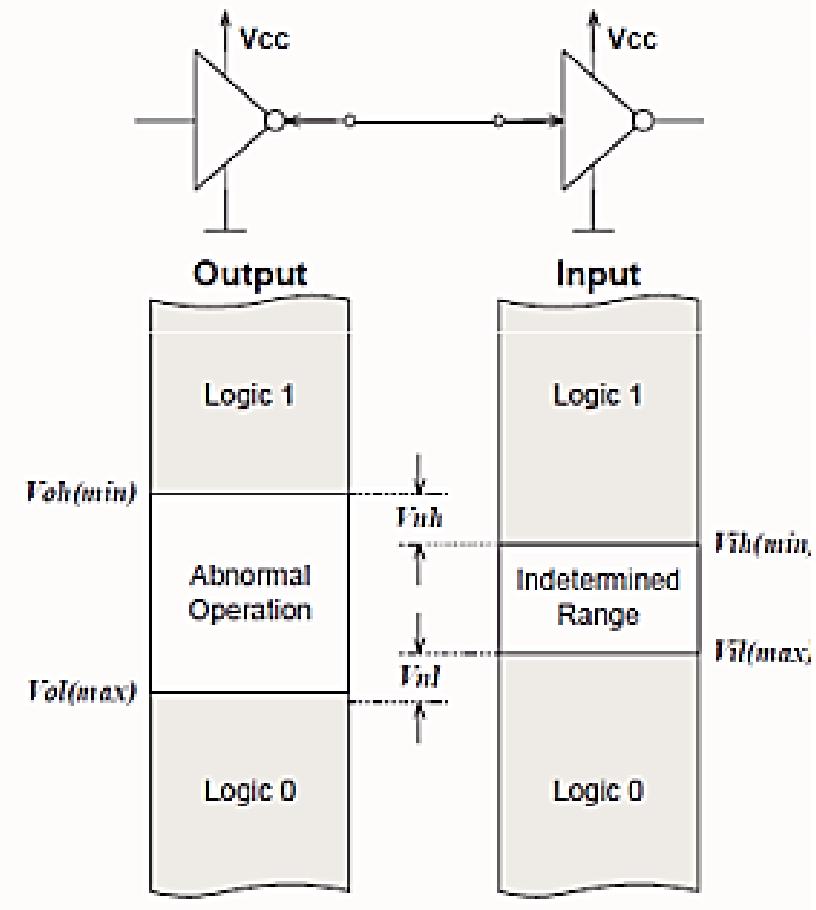
**$(VIL(\text{max.}) - VOL(\text{max.}))$  and  $(VOH(\text{min.}) - VIH(\text{min.}))$  are respectively known as the LOW-level and HIGH-level noise margin.**

- Noise-Margin measures how much external electrical noise a gate can withstand before producing an incorrect output. TTL will take anything below about 0.8 volt as a 0, and anything above about 2 volts as a high.
- LNM (Low noise margin): The largest noise amplitude that is guaranteed not to change the output voltage level when superimposed on the input voltage of the logic gate (when this voltage is in the LOW).  $\text{LNM} = \text{VILmax} - \text{VOLmax} = 0.8\text{V} - 0.4\text{V} = 0.4\text{V}$

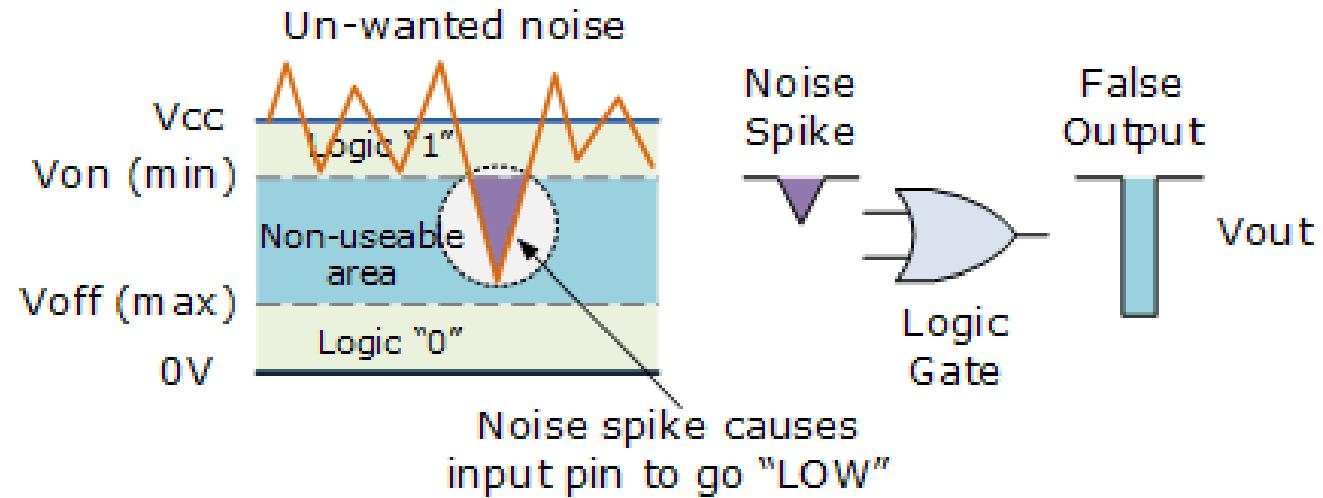
- HNM (High noise margin):
 

The largest noise amplitude that is guaranteed not to change the output voltage level if superimposed on the input voltage of the logic gate (when this voltage is in the HIGH).

$$\text{HNM} = V_{OH\min} - V_{IH\min} = 2.4 - 2.0 = 0.4V$$



# Digital Logic Gate Noise Immunity



# Evolution of TTL Logic Family

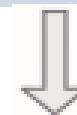
## TTL 74 Series

Standard TTL logic – saturated BJT, Obsolete now, Don't use in new designs



## TTL 74H Series

High speed TTL logic – decrease the resistance to lower the internal time constant but increase in  $P_{dis}$ . Typical  $P_{dis} = 22\text{mW}$  and  $t = 6\text{ns}$



## TTL 74S Series

Schottky TTL logic – Deep saturation prevented by BC Schottky Diode. Reduced storage time delay. Practically obsolete. Typical  $P_{dis} = 20\text{mW}$  and  $t = 3\text{ns}$



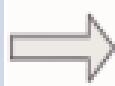
## TTL 74L Series

Low Power TTL logic – Increase the resistance to lower the  $P_{dis}$  but increase in internal time constant . Typical  $P_{dis} = 1\text{mW}$  and  $t = 35\text{ns}$



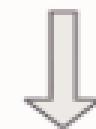
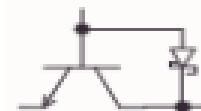
## TTL 74LS Series

Low power Schottky TTL. Typical  $P_{dis} = 2\text{mW}$  and  $t = 10\text{ns}$



## TTL 74ALS Series

Advanced Low power Schottky Low power, high speed Schottky TTL logic-Innovations in IC design and fabrication. Improvement in speed and power dissipation. Popular.



74F-Fast  
TTL

# Comparision of TTL logic families

# Comparsion of TTL and CMOS

Parameter	TTL	CMOS
Basic gate	NAND	INVERTER
Circuit	Transistor-Transistor	Complementary MOS
Speed of operation	More	Less
Propagation delay per gate	4 - 12 ns	50 ns
Nominal supply voltage	5 V	3 to 15 V
Wired collector capability	With passive pull up	With tristate output
Fan-out	10	50
Noise immunity	Good	Very good to excellent
Compatibility with other families	With DTL	No, but compatible with TTL for 5 V supply
Available functions	Very high	High

Parameter	TTL	CMOS
Power Consumption	A single gate on a TTL chip can consume around 10mW of power.	An equivalent single gate in a CMOS chip can consume around 10nW.

# Logic Gates using CMOS

- Refer the write-up

# Interfacing of logic families

## TTL to CMOS

- Figure-1 depicts TTL to CMOS **interfacing** and CMOS to TTL interfacing circuits. When 5V supply is given to TTL and CMOS ICs, logic levels of TTL and CMOS are different. One TTL IC can drive any number of CMOS ICs. However, **TTL output in 'high state' yields 2.4 Volt which is lower than the minimum voltage required by CMOS IC (which is 3.5V)**. For TTL to CMOS interfacing, standard pull up resistor is connected which solves the interfacing problem as mentioned. This is shown in figure-1(a).

# TTL to CMOS Interfacing

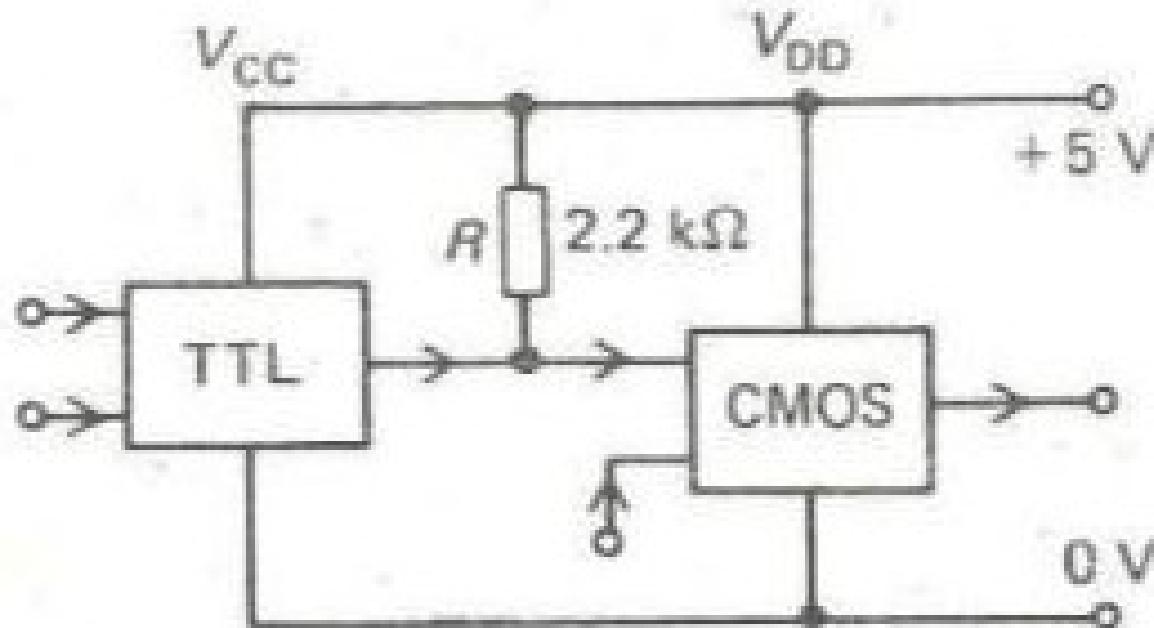


Fig-1(a) TTL to CMOS interfacing

# Interfacing of logic families

## CMOS to TTL

- A CMOS IC can easily drive any low power schottky TTL IC directly. But to interface standard TTL IC, buffer is provided in between CMOS and TTL ICs. This is shown in figure-1(b).
- The CMOS output can supply enough voltage and current to satisfy the TTL input requirements in the HIGH state, but TTL input current requirements at LOW state can not be met directly

- Therefore, an interface circuit with a low input current requirement and a sufficiently high output current rating is required. A COS buffer serves this purpose.

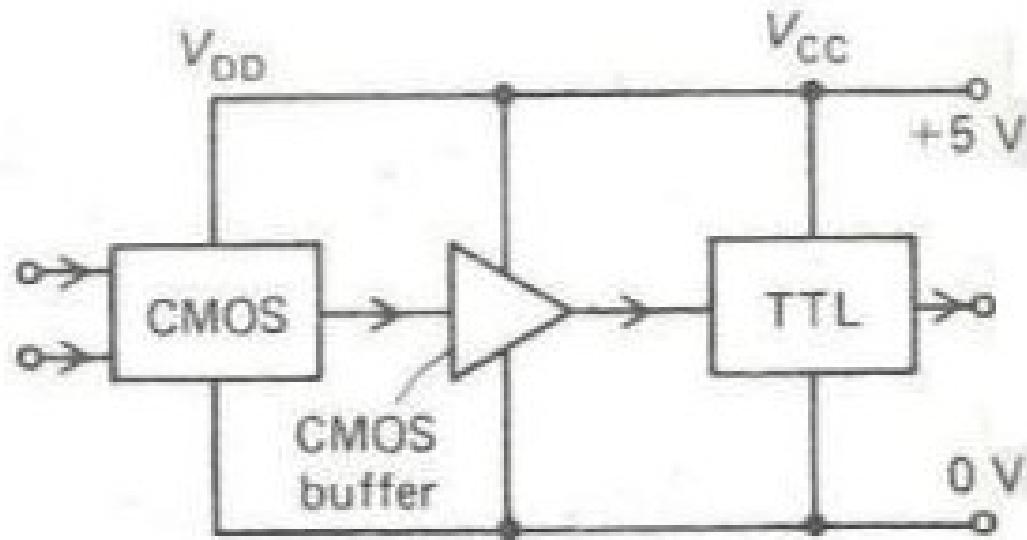


Fig-1(b) CMOS to TTL interfacing

# Unit 4:Finite State Machines

- Mealy and
- Moore machines representation
- Basic design steps
- Finite state machine design, Sequence
- detector moore and mealy, Serial
- binary adder

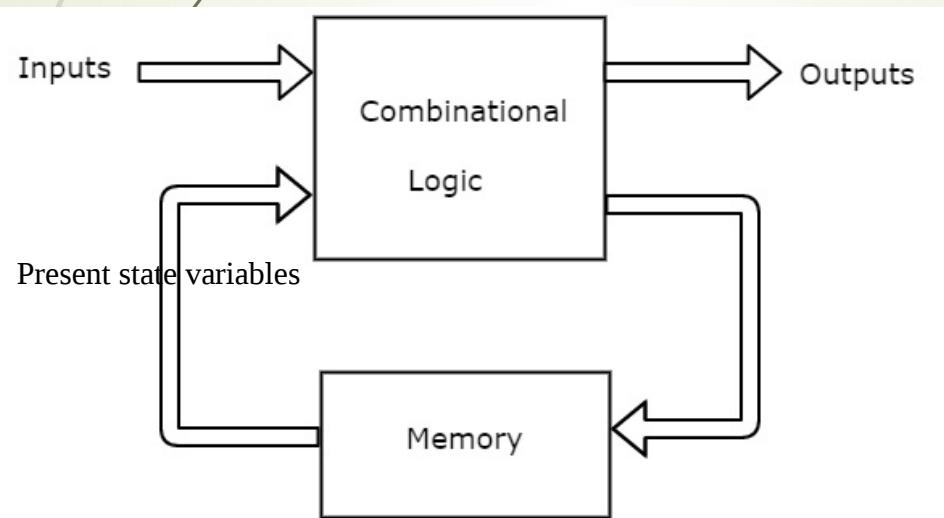
# Finite State Machine

2

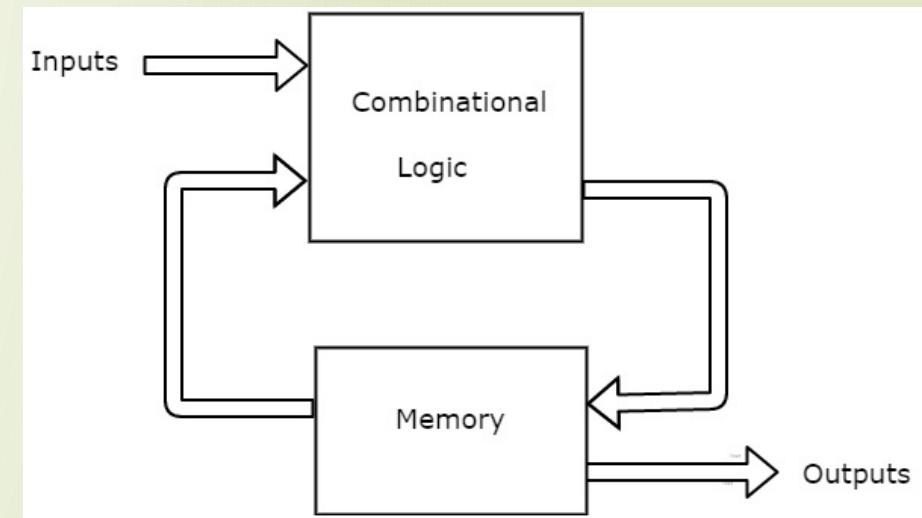
A synchronous sequential circuit is also called as **Finite State Machine FSM**, if it has finite number of states. There are two types of FSMs.

- Mealy State Machine
- Moore State Machine

• **Mealy State Machine:** **Mealy state machine, if outputs depend on both present inputs & present states.**



**Moore State Machine:** **Moore state machine, if outputs depend only on present states**



12/20/2022

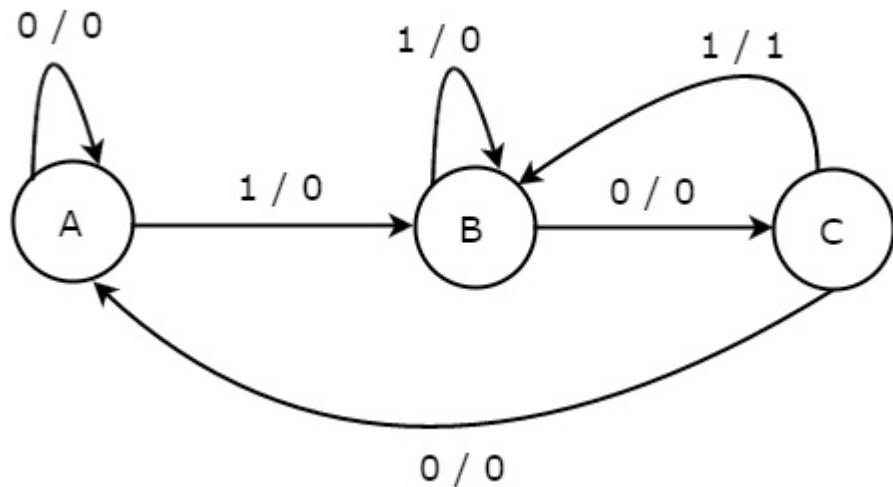
# State Diagram

- A state diagram or a state transition diagram is a graphical representation among present state, the input, the next state and the output of the finite state sequential machine.
- The states are labelled inside the circles & each circle corresponds to one state. Transitions between these states are represented with directed lines. Here, 0 / 0, 1 / 0 & 1 / 1 denotes **Input / output - state diagram** of Mealy state machine

## State Diagrams

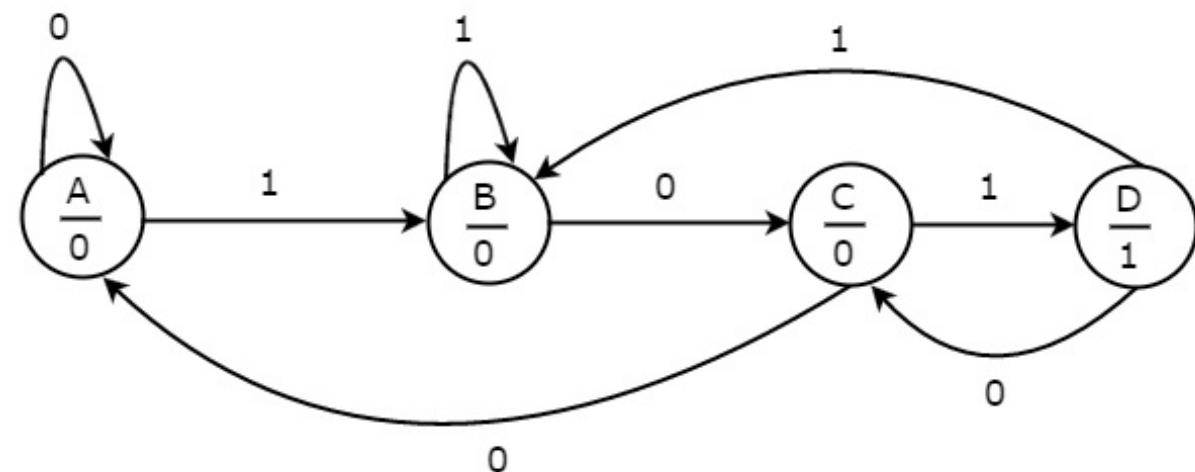
4

- The **state diagram** of Mealy state machine is shown in the following figure.



**A, B & C States.** These states are labelled inside the circles. Transitions between these states are represented with directed lines. Here, 0 / 0, 1 / 0 & 1 / 1 denotes input / output. there are two transitions from each state based on the value of input, x.

- The **state diagram** of Moore state machine is shown in the following figure.



**A, B, C & D. States and the respective outputs are labelled inside the circles. Input value is labeled on each transition. there are two transitions from each state based on the value of input, x.**

# State Table

- The state table is a tabular representation of the relationship between the present state, the input, the next state, and the output.
- State diagram and state table consists of the same information.

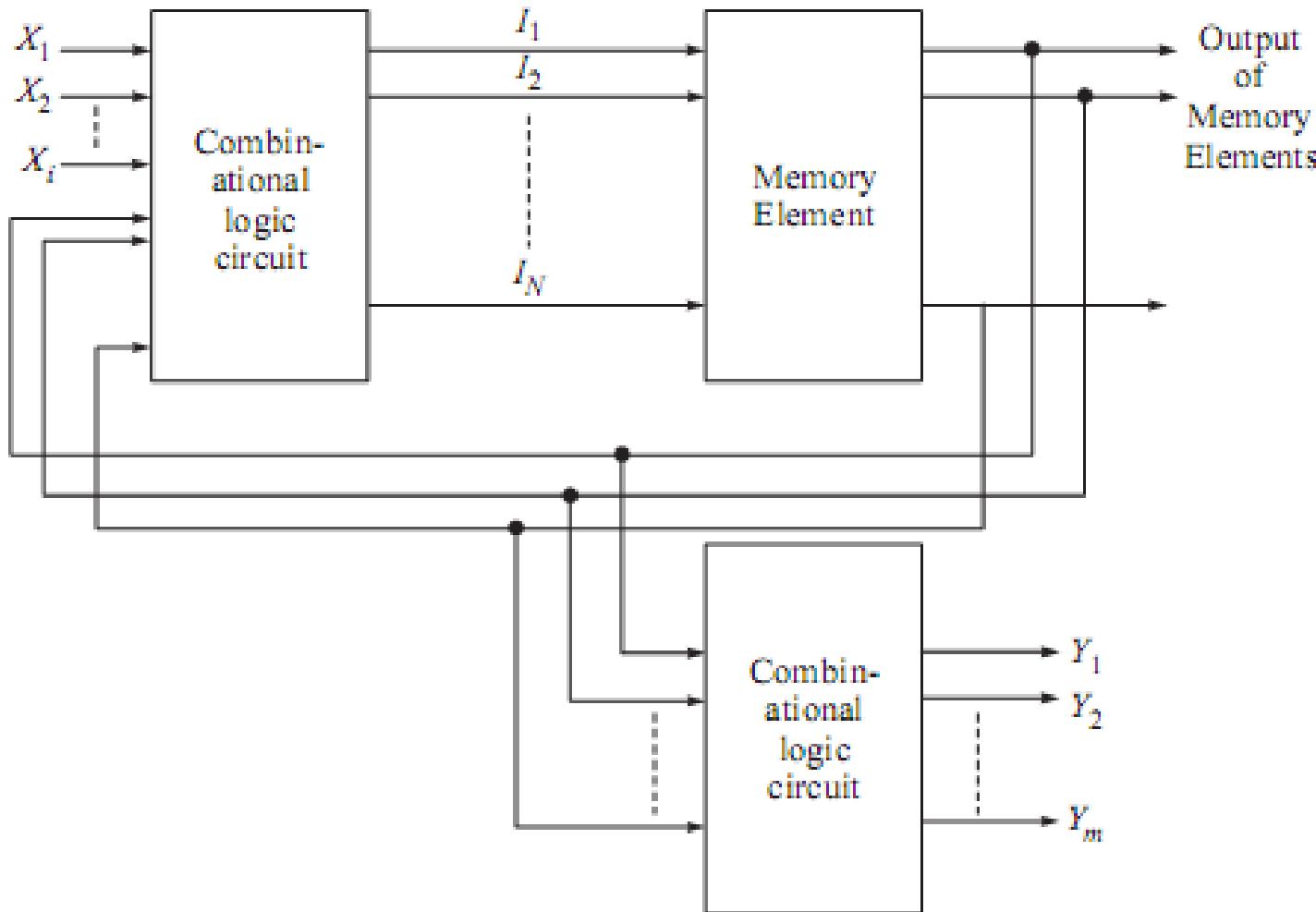
# Transition and Output table

- Obtained from state table
- Excitationtable:

# Synchronous Sequential Circuit

Synchronous sequential circuits are also known as clocked sequential circuits

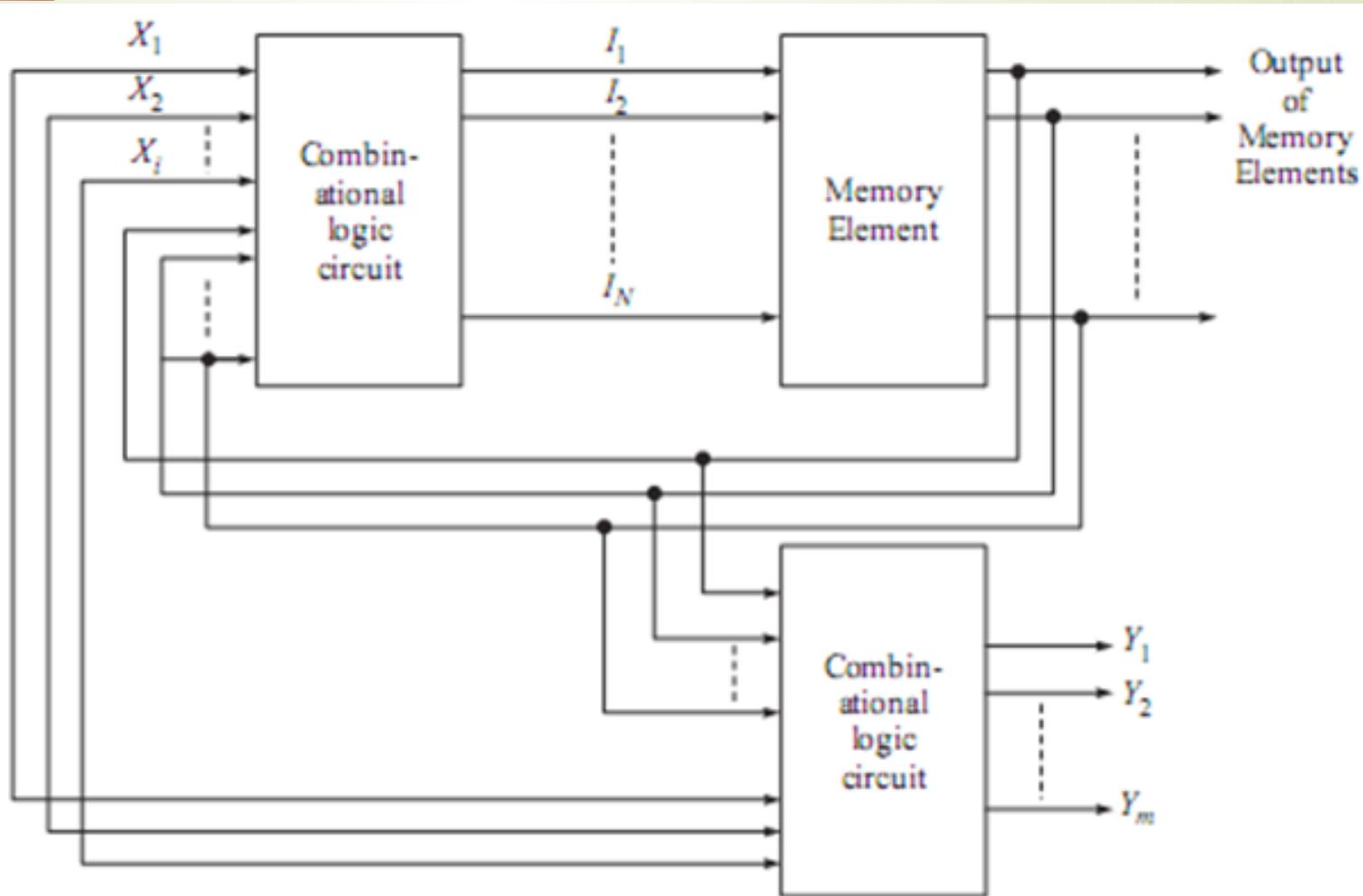
Moore Machine



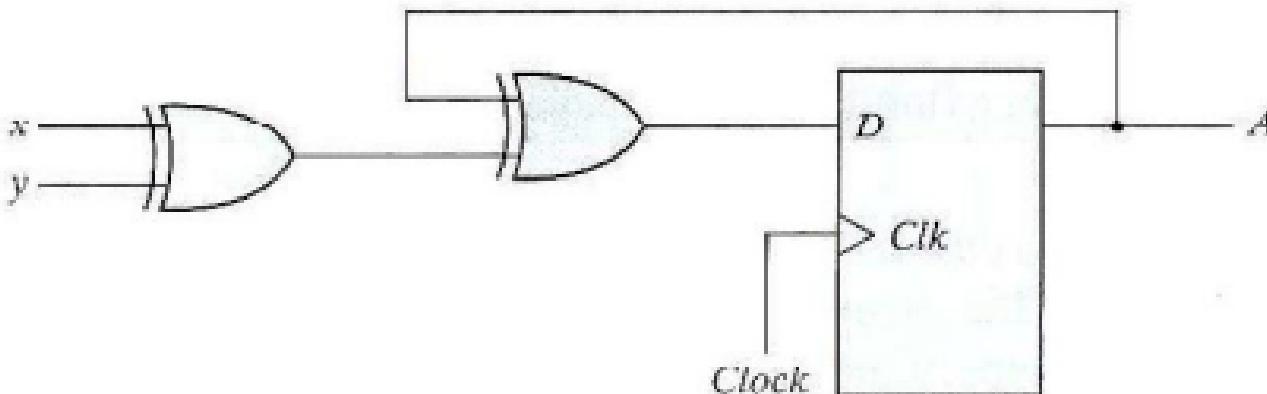
# Synchronous Sequential Circuit

8

Mealy Machine



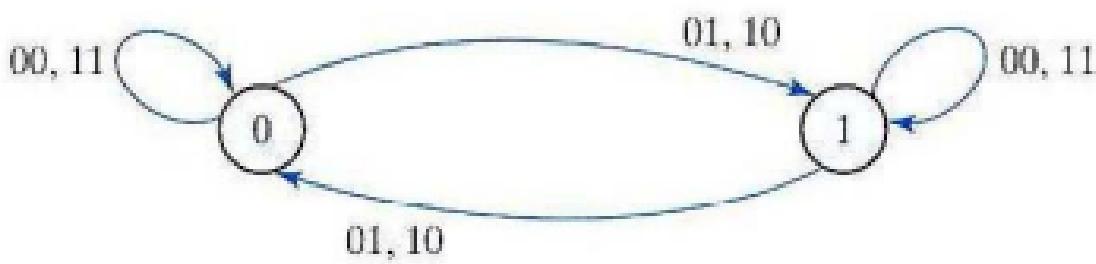
# Circuit, State Diagram, State Table



(a) Circuit diagram

Present state	Inputs		Next state
$A$	$x$	$y$	$A$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

# Circuit, State Diagram, State Table

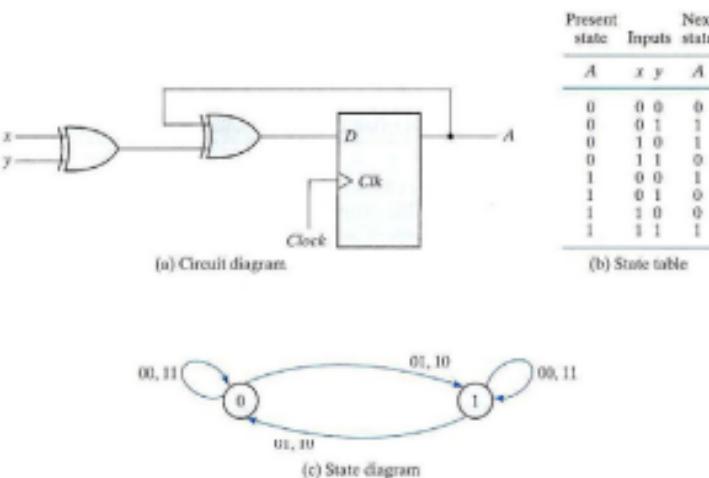


FIGURE 5.17  
Sequential circuit with *D* flip-flop

Sequential circuit components:

- Flip-flop(s)
- Clock
- Logic gates
- Input
- Output

Terms:

**State:** flip-flop output combination

**Present state:** before clock

**Next state:** after clock

State transition  $\leq$  clock

1 flip-flop  $\Rightarrow$  2 states

2 flip-flops  $\Rightarrow$  4 states

3 flip-flops  $\Rightarrow$  8 states

4 flip-flops  $\Rightarrow$  16 states

...

$N$  flip-flops  $\Rightarrow$   $2^N$  states

State diagram:

Circle  $\Rightarrow$  state

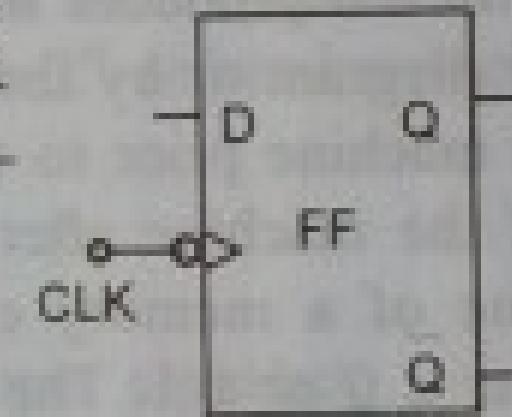
Arrow  $\Rightarrow$  transition  
input/output

Circuit change Required		
From	To	input
$Q(t)$	$Q(t+1)$	$D(t)$
0	0	0
0	1	1
1	0	0
1	1	1

(a) Excitation requirements

Present state (PS)	Input to FF		Next state (NS)
	$Q(t)$	$D(t)$	
0	0	0	0
0	1	1	1
1	0	0	0
1	1	1	1

(b) Excitation table



(c) Logic symbol



(d) State diagram

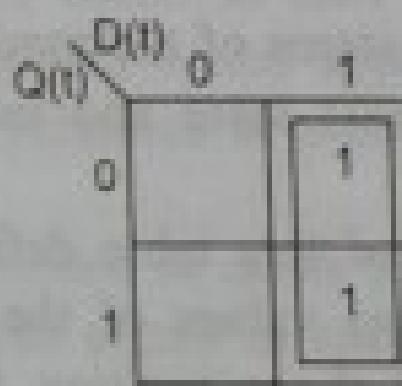
PS	N/S, Q/P	
	$D = 0$	$D = 1$
0	0, 0	1, 1
1	0, 0	1, 1

(e) State table

**State Diagram is known as Mealy Model  
D Flip Flop**



(f) General state diagram



(g) K-map for  $Q(t+1)$



(h) Moore model

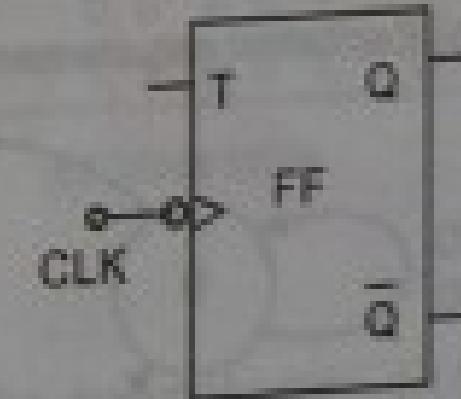
**$Q(t+1) = D(t)$**   
**D Flip Flop**

Circuit change Required		input T(t)
From	To	
Q(t)	Q(t+1)	
0	0	0
0	1	1
1	0	1
1	1	0

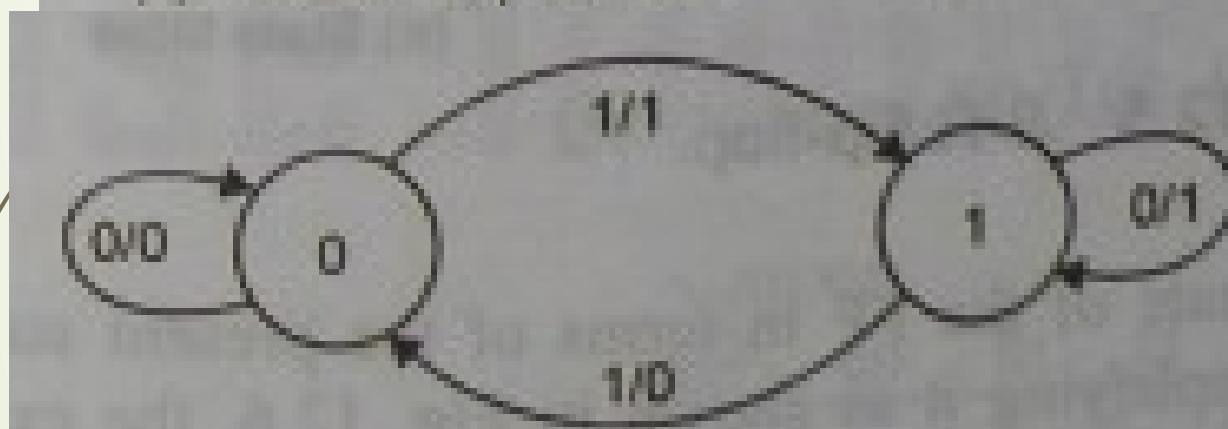
(a) Excitation requirements

Present state (PS)	Input to FF		Next state (NS)
	Q(t)	T(t)	
Q(t)			
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

(b) Excitation table



(c) Logic symbol

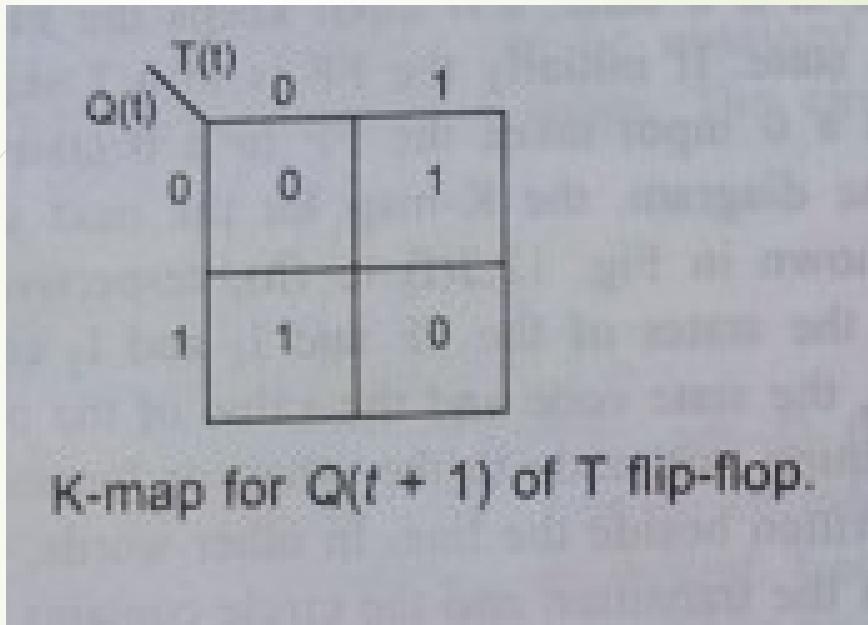


(d) State diagram

PS	NS. O/P	
	T = 0	T = 1
0	0, 0	1, 1
1	1, 1	0, 0

(e) State table

## T Flip Flop



$$Q(t + 1) = \bar{Q}(t)T(t) + Q(t)\bar{T}(t) = Q(t) \oplus T(t)$$

Circuit change From	To	Required inputs		Present state (PS)	Inputs to FF		Next state (NS)
		Q(t)	Q(t+1)		S(t)	R(t)	
0	0	0	X	0	0	1	0
0	1	1	0	1	0	0	1
1	0	0	1	1	0	1	0
1	1	X	0	1	1	0	1

(a) Excitation requirements

(b) Excitation table

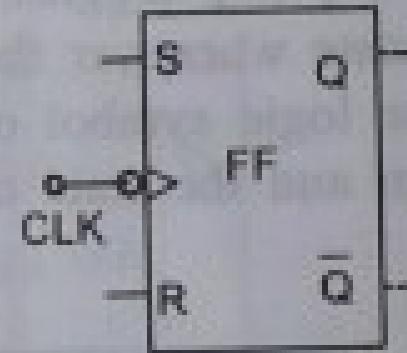
(c) Logic symbol



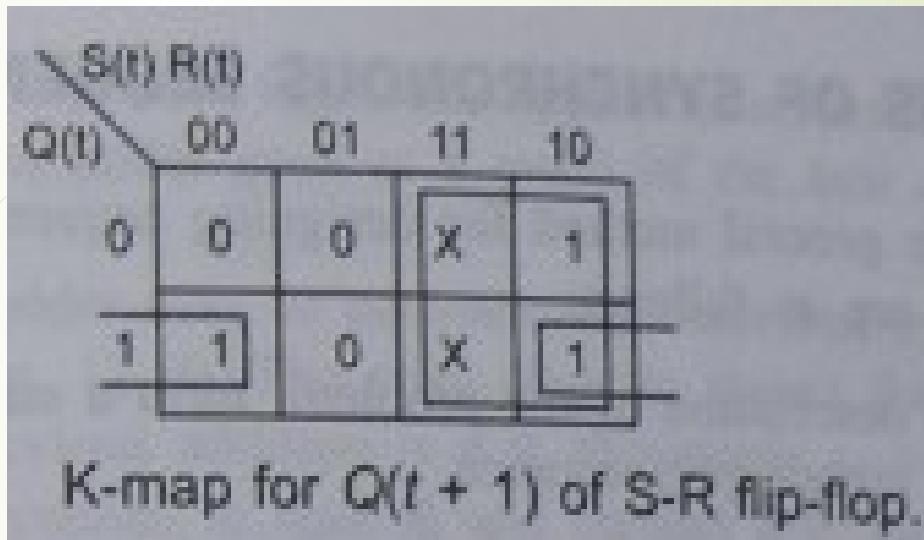
(d) State diagram

PS	NS, O/P		
	SR	SR	SR
0	0 0	0 1	1 0
1	1 1	0 0	1 1

(e) State table



## S-R Flip Flop



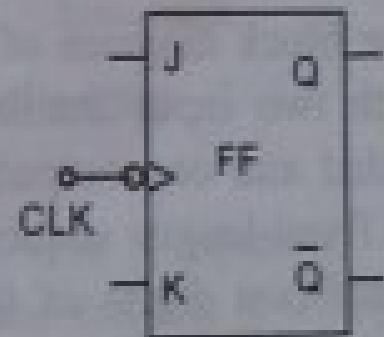
$$Q(t + 1) = Q(t)\overline{R}(t) + S(t)$$

Circuit change From      To		Required inputs	
$Q(t)$	$Q(t+1)$	$J(t)$	$K(t)$
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

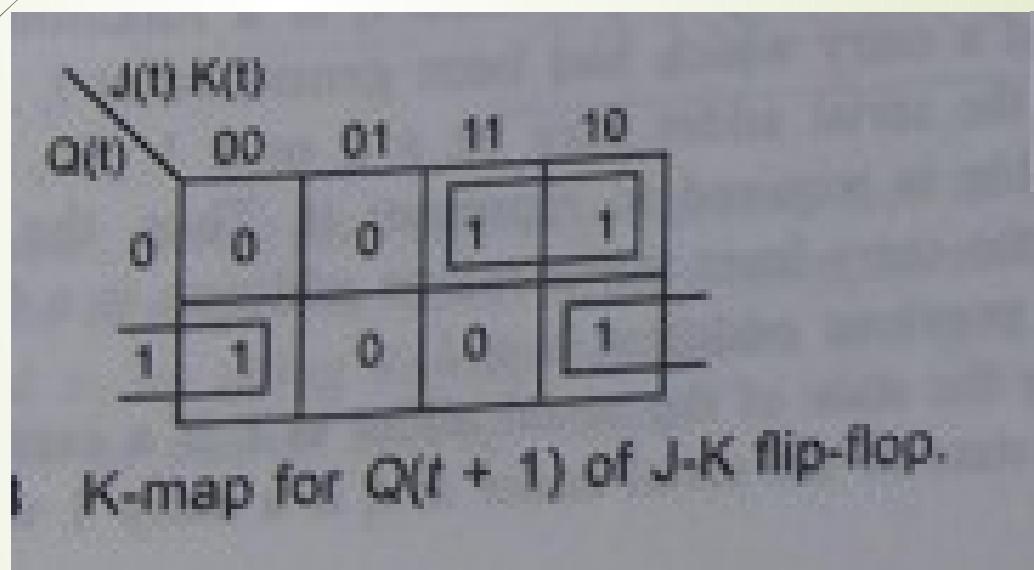
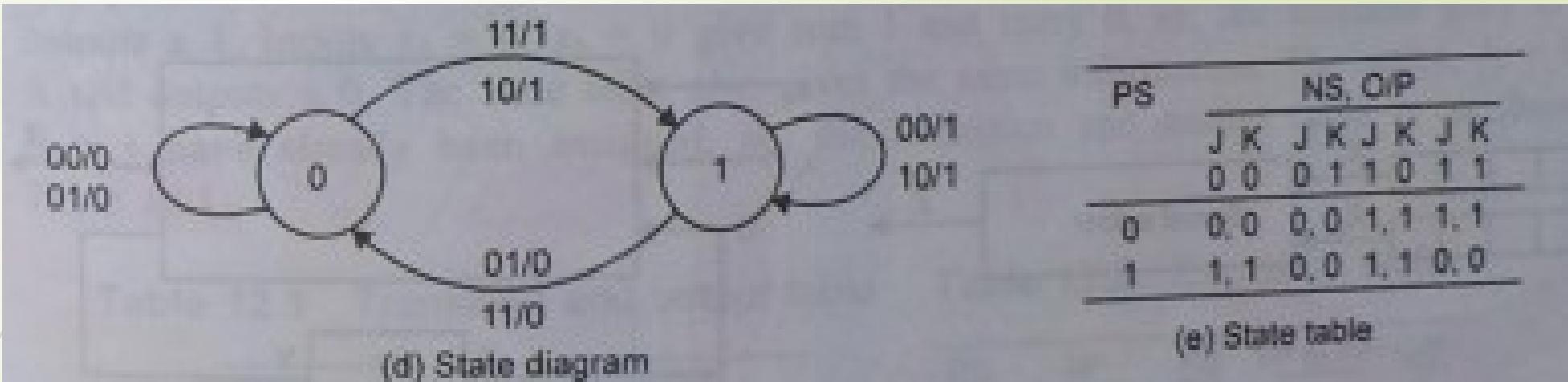
(a) Excitation requirements

Present state (PS)	Inputs to FF		Next state (NS)	
	$Q(t)$	$J(t)$	$K(t)$	$Q(t+1)$
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0

(b) Excitation table



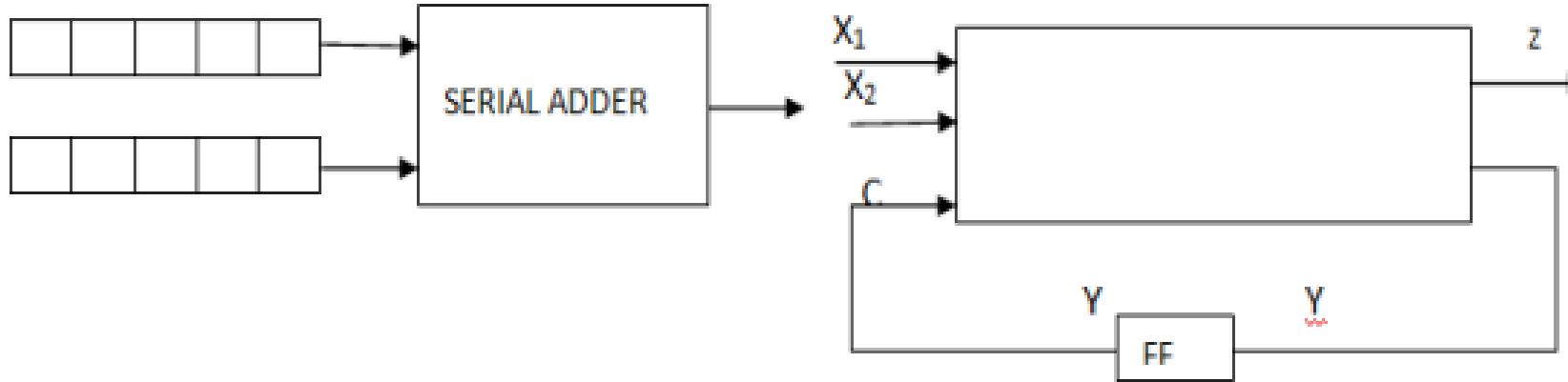
(c) Logic symbol



$$Q(t + 1) = J(t)\bar{Q}(t) + Q(t)\bar{K}(t)$$

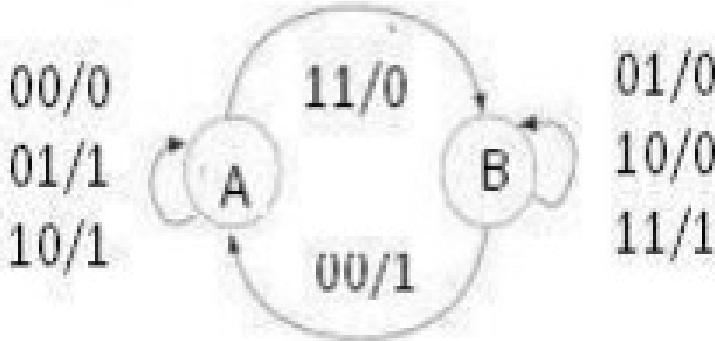
# Serial Binary Adder

- Step1: word statement of the problem: the block diagram of a serial binary adder is shown in fig.
- it is a synchronous circuit with two input terminals designated  $X_1$  and  $X_2$  which carry the two binary numbers to be added and one output terminal  $Z$  which represents the sum.
- The inputs and outputs consist of fixed-length sequences 0s and 1s. the output of the serial  $Z_i$  at time  $t_i$  is a function of the inputs  $X_1(t_i)$  and  $X_2(t_i)$  at that time  $t_{i-1}$  and of carry which had been generated at  $t_{i-1}$ .
- The carry which represent the past history of the serial adder may be a 0 or 1.
- The circuit has two states. If one state indicates that carry from the previous addition is a 0, the other state indicates that the carry from the previous addition is a 1



**Figure: block diagram of serial binary adder**

Step2 and 3: state diagram and state table: let  $a$  designate the state of the serial adder at  $t_i$  if a carry 0 was generated at  $t_{i-1}$ , and let  $b$  designate the state of the serial adder at  $t_i$  if carry 1 was generated at  $t_{i-1}$ . the state of the adder at that time when the present inputs are applied is referred to as the present state(PS) and the state to which the adder goes as a result of the new carry value is referred to as next state(NS). The behavior of serial adder may be described by the state diagram and state table.



PS	NS, QNP			
	$X_1 X_2$			
	00	01	10	11
A	A,0	A,1	A,1	B,0
B	A,1	B,0	B,0	B,1

Figures: serial adder state diagram and state table

If the machine is in state A, i.e., carry from the previous addition is a 0, inputs  $X_1=0$  and  $X_2=0$  gives sum, 0 and carry 0. So the machine remains in state A and outputs a 0. Inputs  $X_1=1$  and  $X_2=0$  gives sum, 1 and carry 0, So the machine remains in state A and outputs a 1.

Inputs  $X_1=0$  and  $X_2=1$  gives sum1 and carry 0. So the machine goes to state A and outputs a 1.

Inputs  $X_1=1$  and  $X_2=1$  gives sum, 0 and carry 1. So the machine goes to state B and outputs a 0. The state table also gives the same information.

If the machine is in state B, i.e., carry from the previous addition is a 1, inputs  $X_1=0$  and  $X_2=1$  gives sum, 0 and carry 1. So the machine remains in state B and outputs a 0. Inputs  $X_1=1$  and  $X_2=0$  gives sum, 0 and carry 1. So the machine remains in state B and outputs a 0. Inputs  $X_1=1$  and  $X_2=1$  gives sum, 1 and carry 0. So the machine remains in state B and outputs a 1. Inputs  $X_1=0$  and  $X_2=0$  gives sum, 1 and carry 0. So the machine goes to state A and outputs a 1. The state table also gives the same information.

Step4: state assignment and transition and output table: The states,  $A=0$  and  $B=1$  have already been assigned. So, the transition and output table is as shown.

**Table 12.1 Transition and output table**

PS	NS				Q/P			
	$x_1, x_2$		$x_1, x_2$		$x_1, x_2$		$x_1, x_2$	
	00	01	10	11	00	01	10	11
0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

**Table 12.2 Excitation table**

PS	I/P		NS	I/P to FF	Q/P
	$x_1$	$x_2$		$y$	D
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	1	1

- Step 5-To write the excitation table, select the memory element . Obtain the minimal expressions for D and Z in terms of  $y,x_1$  and  $x_2$  by using k map as shown in fig

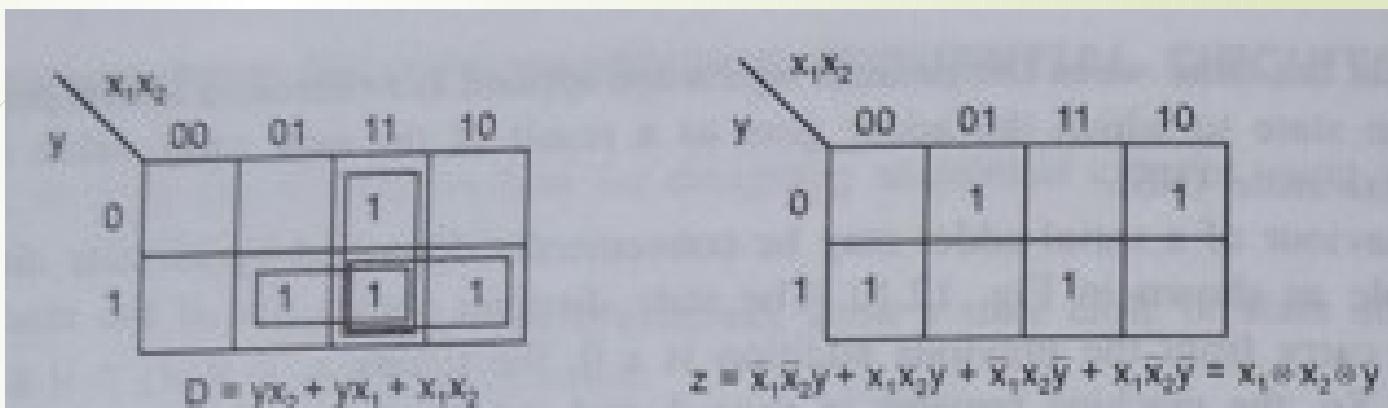


Fig. 12.11 K-maps for the serial adder.

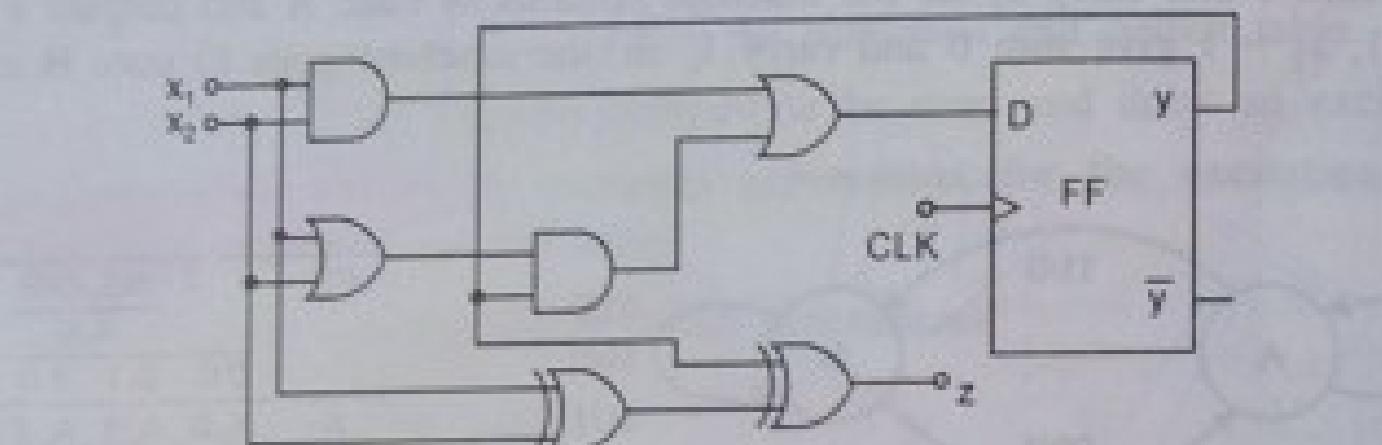


Fig. 12.12 Logic diagram of the serial binary adder.

## State table for Mealy state machine model

24

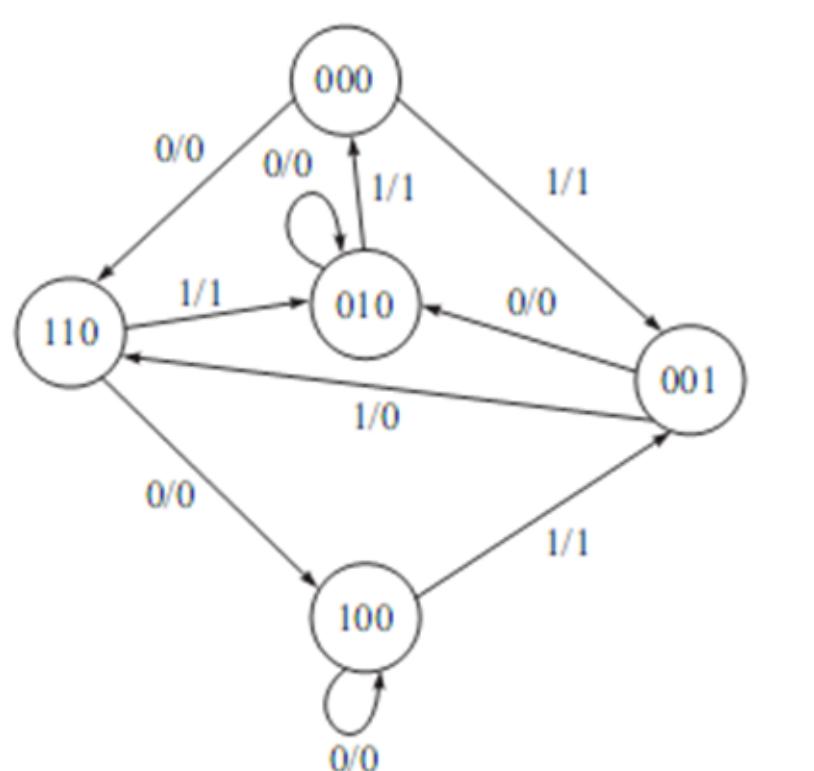
Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	a	b	1	0
b	c	b	0	1
c	c	d	0	0
d	d	a	1	0

## State table for Moore state machine model

Present state	Next state		Output
	X = 0	X = 1	
a	a	b	0
b	c	b	1
c	c	d	0
d	d	a	0

Since, in Moore state machine model, the output depends only on the present state, the last column has only output. Criterion criteria

# Design the sequential circuit for the state diagram shown in Fig. given using J-K flip-flops



## Step 1: State table for state diagram

Present state	Next state			Output					
	X=0	X=1		X=0	X=1				
Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	Y	Y		
0	0	0	1	1	0	0	1	0	1
0	0	1	0	1	0	1	0	0	1
0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1
1	1	0	1	0	0	0	1	0	1

## Step 2: State reduction:

From the state table; it is observed that all the states are different; there is no possibility to reduce the state table.

### Step 3: Excitation table for the given state diagram using J-K flip-flop

26

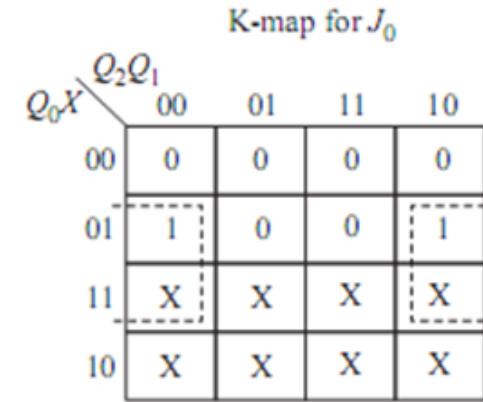
Present state			Inp ut	Next state			Outp ut	Input of the flip-flops						
$Q_2$	$Q_1$	$Q_0$	X	$Q_2$	$Q_1$	$Q_0$	Y	$J_0$	$K_0$	$J_1$	$K_1$	$J_2$	$K_2$	
0	0	0	0	1	1	0	0	0	X	1	X	1	X	
0	0	1	0	0	1	0	0	X	1	1	X	0	X	
0	1	0	0	0	1	0	0	0	X	X	0	0	X	
1	0	0	0	1	0	0	0	0	X	0	X	X	0	
1	1	0	0	1	0	0	0	0	X	X	1	X	0	
0	0	0	1	0	0	1	1	1	X	0	X	0	X	
0	0	1	1	1	0	0	1	X	1	0	X	1	X	
0	1	0	1	0	0	0	1	0	X	X	1	0	X	
1	0	0	1	0	0	1	1	1	X	0	X	X	1	
1	1	0	1	0	1	0	1	0	X	X	0	X	1	

Q Output		Inputs	
Present State	Next State	$J_n$	$K_n$
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

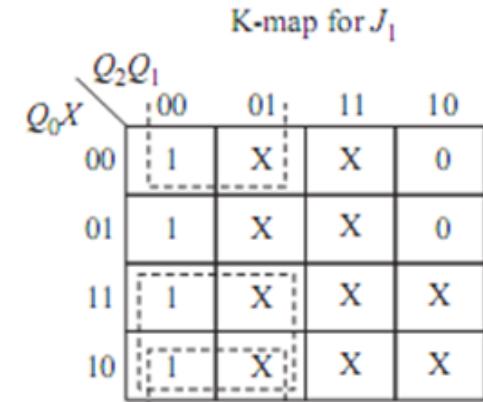
# Step 4: K Maps for Flipflops inputs

27

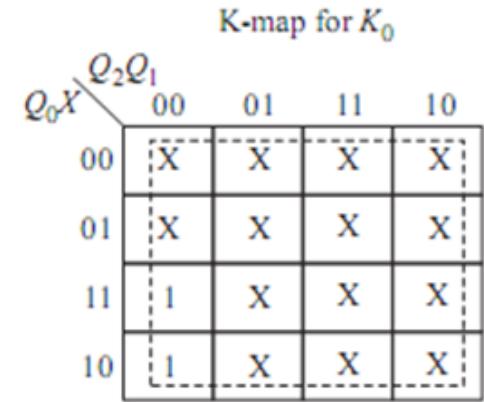
Present state			Input	Next state			Output	Input of the flip-flops						
$Q_2$	$Q_1$	$Q_0$	$X$	$Q_2$	$Q_1$	$Q_0$	$Y$	$J_0$	$K_0$	$J_1$	$K_1$	$J_2$	$K_2$	
0	0	0	0	1	1	0	0	0	X	1	X	1	X	X
0	0	1	0	0	1	0	0	X	1	1	X	0	X	X
0	1	0	0	0	1	0	0	0	X	X	0	0	0	X
1	0	0	0	1	0	0	0	0	X	0	X	X	X	0
1	1	0	0	1	0	0	0	0	X	X	1	X	0	X
0	0	0	1	0	0	1	1	1	X	0	X	0	0	X
0	0	1	1	1	0	0	1	X	1	0	X	1	X	X
0	1	0	1	0	0	0	1	0	X	X	1	0	X	X
1	0	0	1	0	0	1	1	1	X	0	X	X	X	1
1	1	0	1	0	1	0	1	0	X	X	0	X	1	1



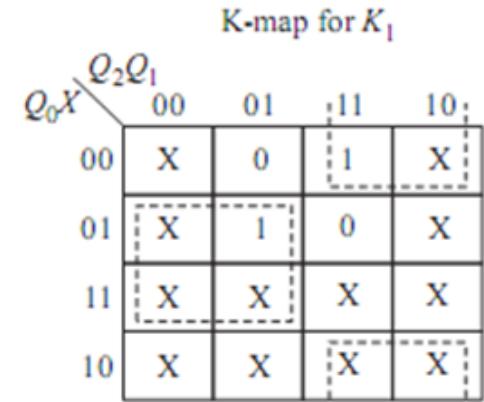
$$J_0 = \overline{Q}_1 X$$



$$J_1 = \overline{Q}_2 X + \overline{Q}_2 Q_0$$



$$K_0 = 1$$



$$K_1 = \overline{Q}_2 X + Q_2 \overline{X} \\ = Q_2 \oplus X$$

## Step 4: K Maps for Flipflops inputs

K-map for $J_2$					
$Q_0X$	$Q_2Q_1$	00	01	11	10
00	1	0	X	X	
01	0	0	X	X	
11	1	X	X	X	
10	0	X	X	X	

$$J_2 = Q_0X + \overline{Q}_1\overline{Q}_0\overline{X}$$

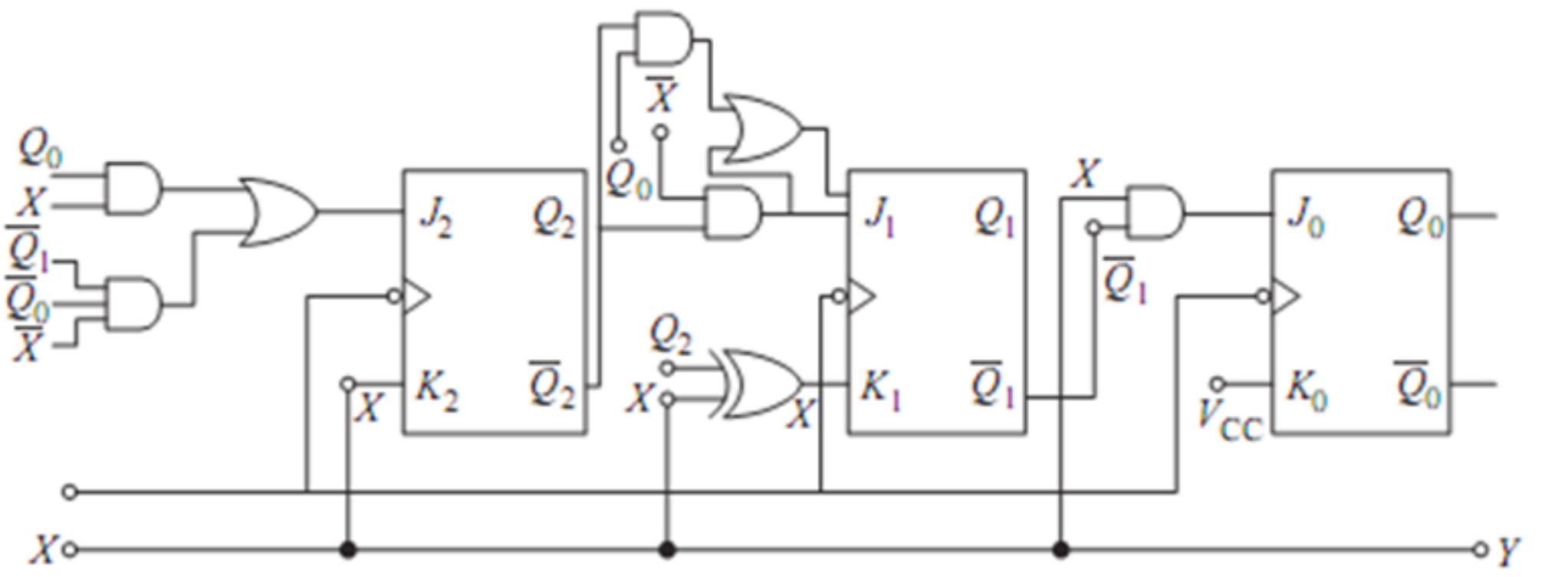
K-map for $K_2$					
$Q_0X$	$Q_2Q_1$	00	01	11	10
00	X	X	0	0	
01	X	X	1	1	
11	X	X	X	X	
10	X	X	X	X	

$$K_2 = X$$

K-map for $Y$					
$Q_0X$	$Q_2Q_1$	00	01	11	10
00	0	0	0	0	
01	1	1	1	1	
11	1	X	X	X	
10	0	X	X	X	

$$Y = X$$

## Step 5: logic diagram



$$\overline{J_0} = \overline{Q}_1 X$$

$$K_0 = 1$$

$$J_1 = \overline{Q}_2 \dot{X} + \overline{Q}_2 Q_0$$

$$\begin{aligned} K_1 &= \overline{Q}_2 X + Q_2 \overline{X} \\ &= Q_2 \oplus X \end{aligned}$$

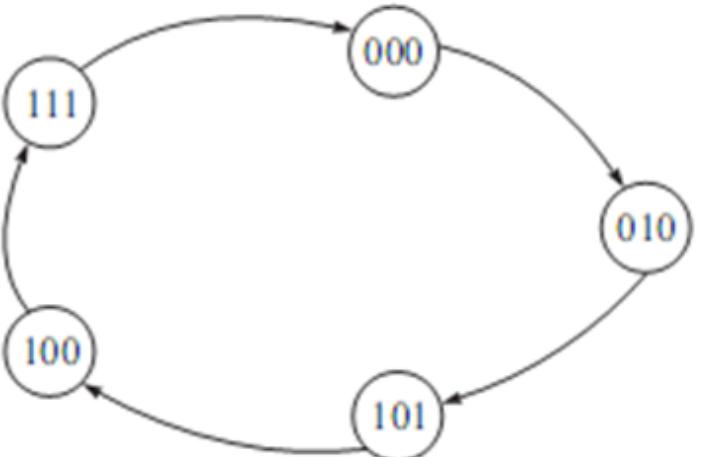
$$\overline{J_2} = Q_0 X + \overline{Q}_1 \overline{Q}_0 \overline{X}$$

$$K_2 = X$$

$$Y = X$$

**Step 1: State diagram**

30

**Step 2: State table for the State diagram**

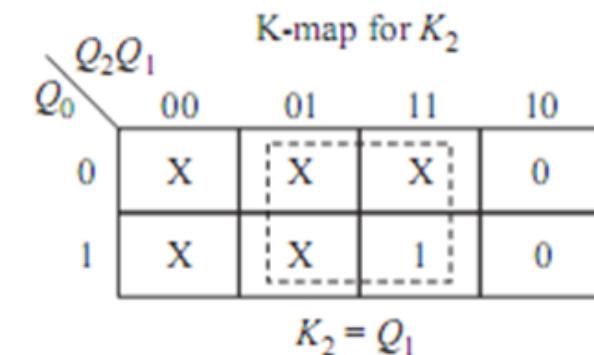
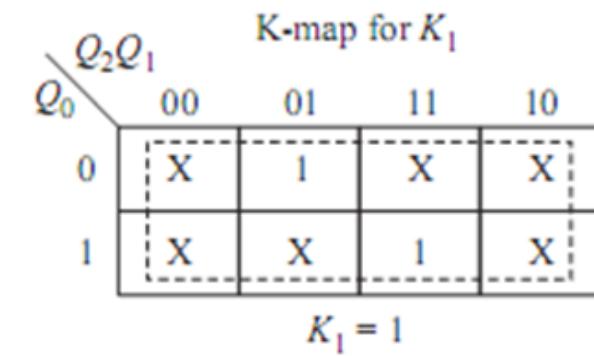
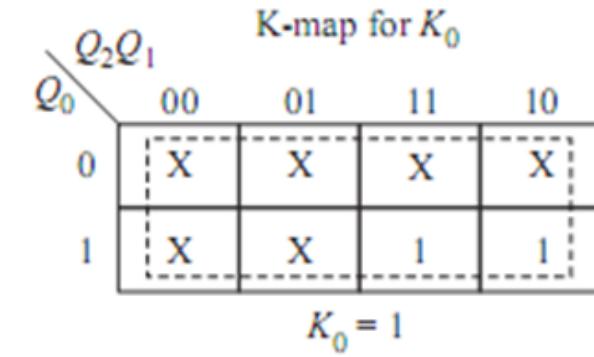
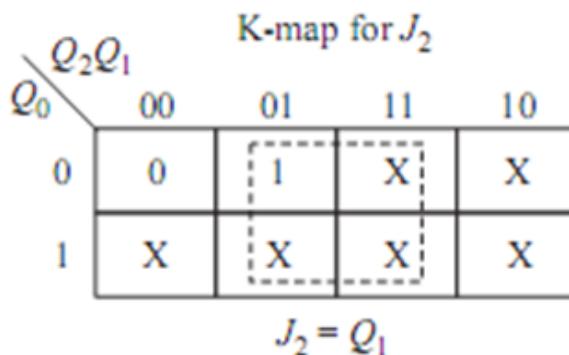
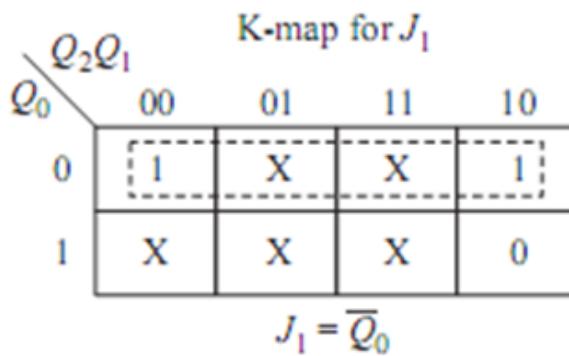
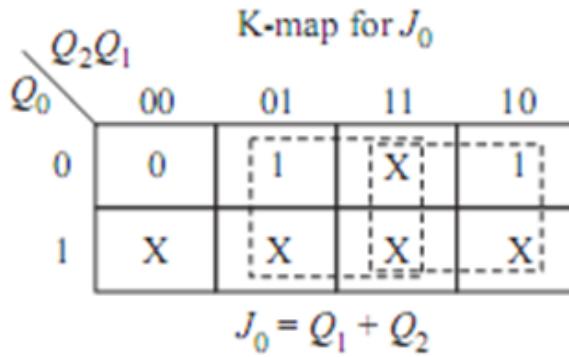
Present state			Next state		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	1	0
0	1	0	1	0	1
1	0	1	1	0	0
1	0	0	1	1	1
1	1	1	0	0	0

**Step 3: State reduction:**

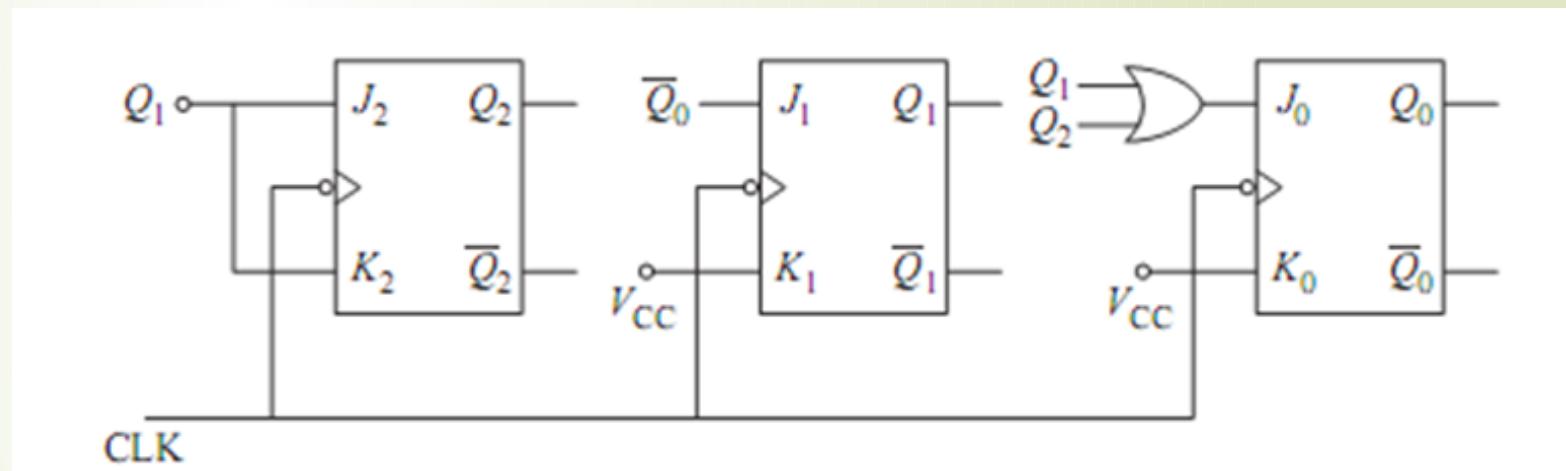
From the state table it is observed that all the states are different, there is no possibility to reduce the state table.

**Step 4: Excitation table for the state table using J-K flip-flop / Transition Table**

Present state			Next state			Input of the flip-flops					
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$J_0$	$K_0$	$J_1$	$K_1$	$J_2$	$K_2$
0	0	0	0	1	0	0	X	1	X	0	X
0	1	0	1	0	1	1	X	X	1	1	X
1	0	1	1	0	0	X	1	0	X	X	0
1	0	0	1	1	1	1	X	1	X	X	0
1	1	1	0	0	0	X	1	X	1	X	1

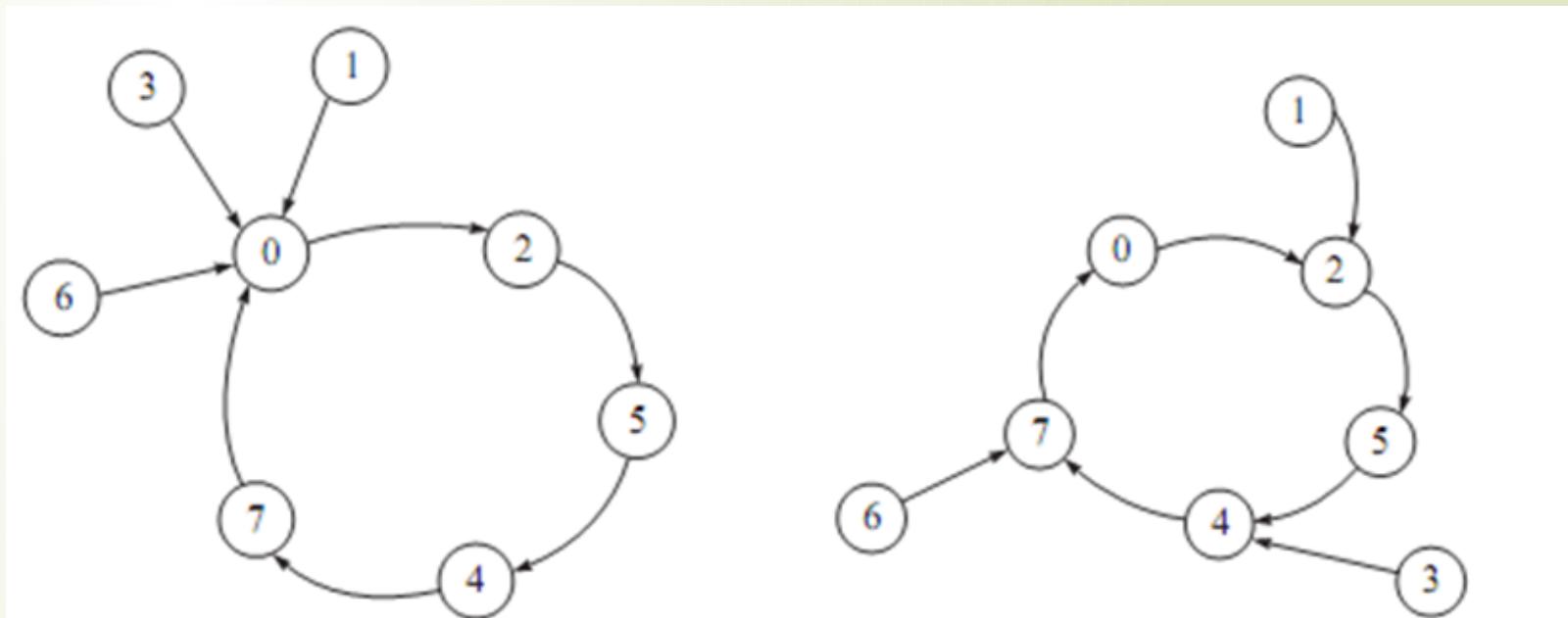


## Step 5: Logic diagram



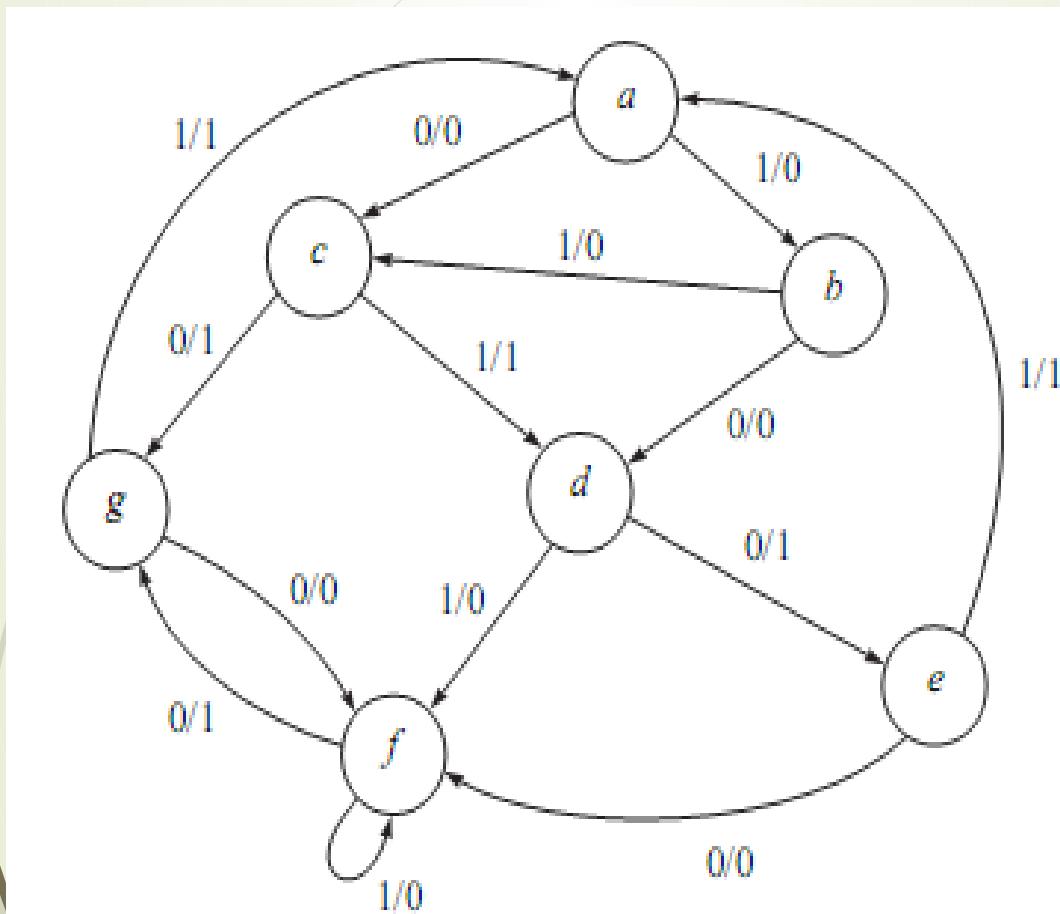
## Lockout condition:

- designed to generate the sequence 0-2-5-4-7-0, the states 1, 3 and 6 are the unused states. If by chance the sequence generator finds itself in any one of the unused states, the next state is unknown. It may be possible that the sequence generator goes from one unused state to another unused state, it never arrives at the used state. The circuit is said to be locked. To avoid the condition of lockout, there is need to design the circuit such that, when the circuit finds itself in an unused state the next state should be known and it must be a used state. The state diagrams of sequence generator to generate the sequence 0-2-5-4-7-0 with lockout condition as shown



# Analysis Of Clocked Sequential Circuit

34



**Step 1: State table for state diagram**

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	c	b	0	0
b	d	c	0	0
c	g	d	1	1
d	e	f	1	0
→e	f	a	0	1
f	g	f	1	0
→g	f	a	0	1

The states 'e' and 'g' are equivalent because the next state and outputs are same for the input X is equal to 0 as well as X is equal to 1; and hence 'g' is replaced by 'e' and the state 'g' is removed from the table.

## Step 2: State Reduction

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	c	b	0	0
b	d	c	0	0
c	(g)e	d	1	1
→d	e	f	1	0
e	f	a	0	1

The states (g)e and 'f' are equivalent because the next state and output are same for the input X is equal to 0 and X is equal to 1; and hence 'f' is replaced by 'd' and the state 'f' is removed from the table

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	(f)d	1	0
e	The state 'c' and 'd' are not equivalent because next state is same for input X is equal to 0 and X is equal to 1, but outputs are not same.	a	0	1

The state 'c' and 'd' are not equivalent because next state is same for input X is equal to 0 and X is equal to 1, but outputs are not same.

### Step 3: State Assignment

#### Variable Assign value

a 000

b 001

c 010

d 011

e 100

### Step 4: Transition/ Excitation Table

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
$Q_1Q_2Q_3$	$Q_1Q_2Q_3$	$Q_1Q_2Q_3$		
000	010	001	0	0
001	011	010	0	0
010	100	011	1	1
011	100	011	1	0
100	Nex	011	Inp	0
			Output	1

	Input	Present state	Next state	to F/F	Output
	x	$Q_1Q_2Q_3$	$Q_1Q_2Q_3$	$D_1D_2D_3$	
0	0	000	010	010	0
1	0	001	011	011	0
2	0	010	100	100	1
3	0	011	100	100	1
4	0	100	011	011	0
8	1	000	001	001	0
9	1	001	010	010	0
10	1	010	011	011	1
11	1	011	011	011	0
12	1	100	000	000	1

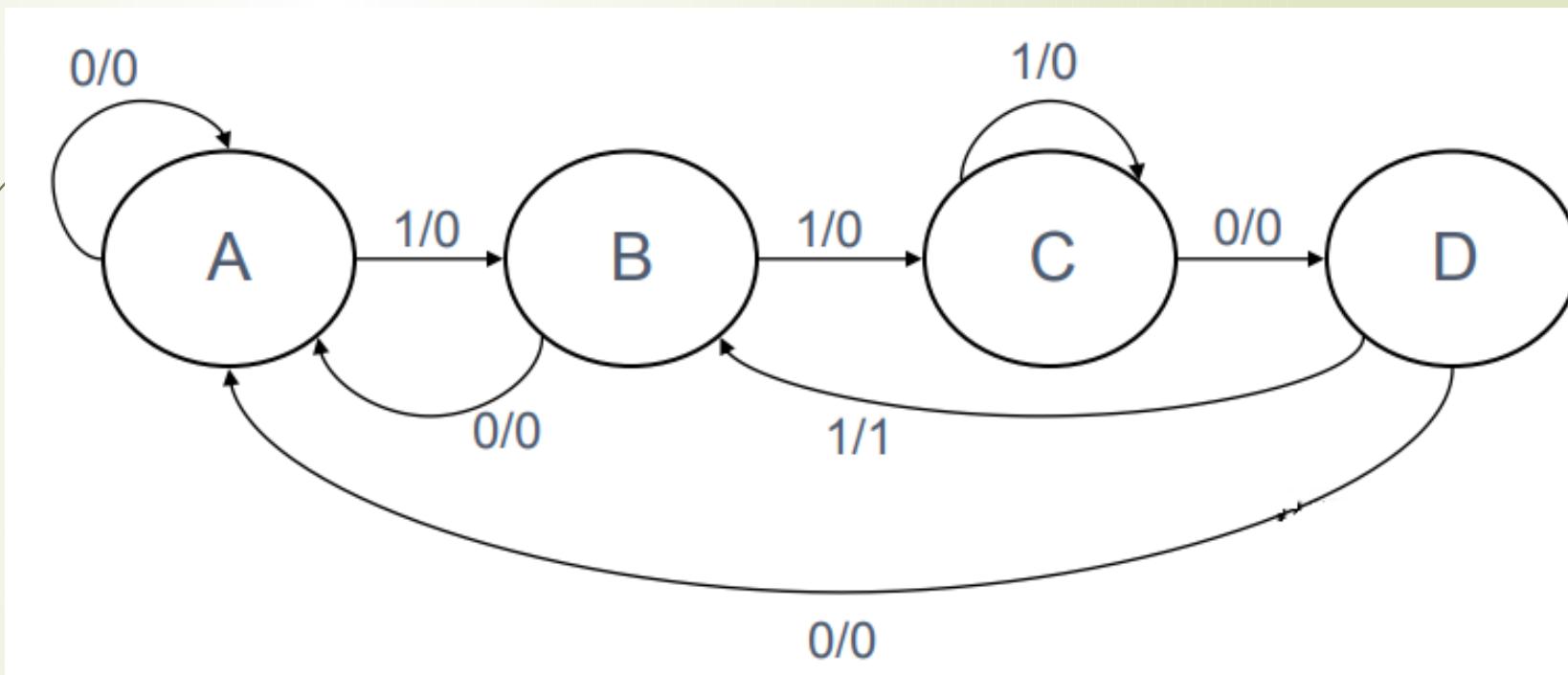
## Step 5: K Maps

37

# Example

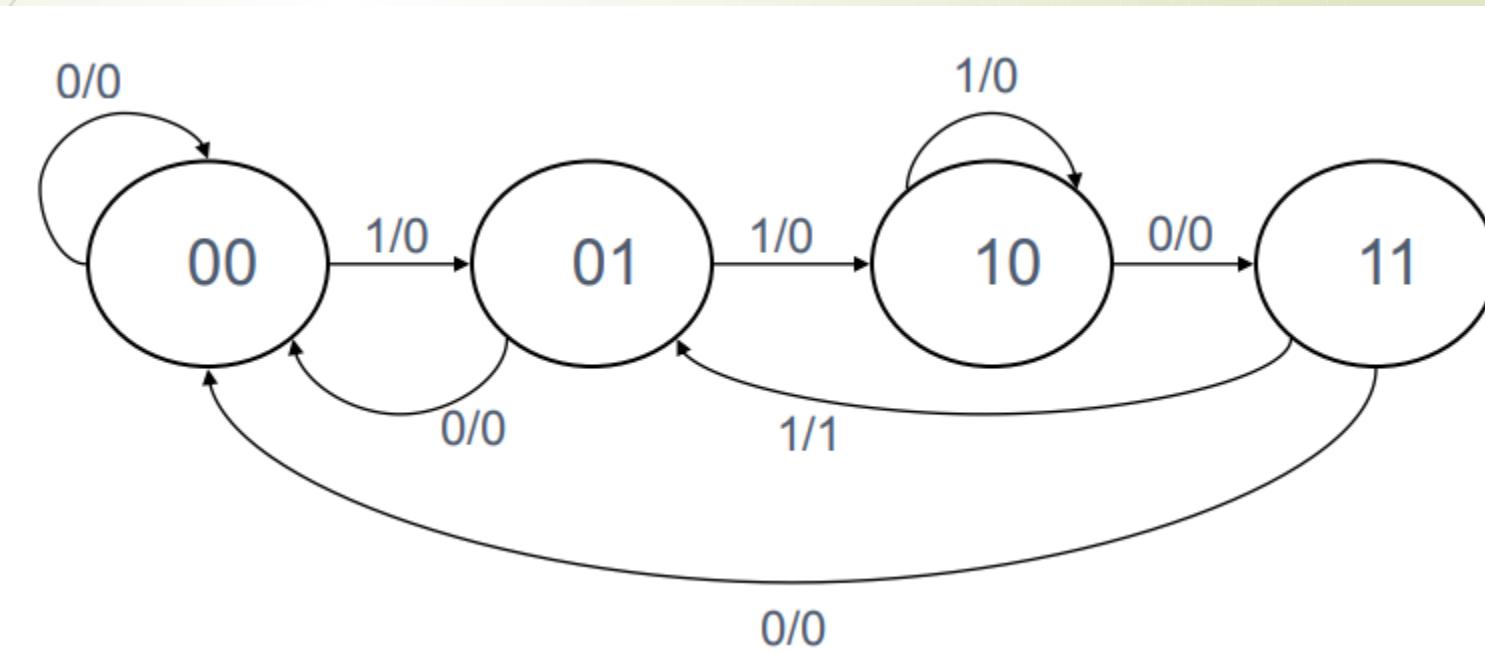
38

- Design a sequential circuit to recognize the input sequence 1101.
- That is, output 1 if the sequence 1101 has been read, output 0 otherwise.



# Assign States

- 4 states, so we need 2 bits



# State Table

Present State		Input X	Next State		Output Y
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	1

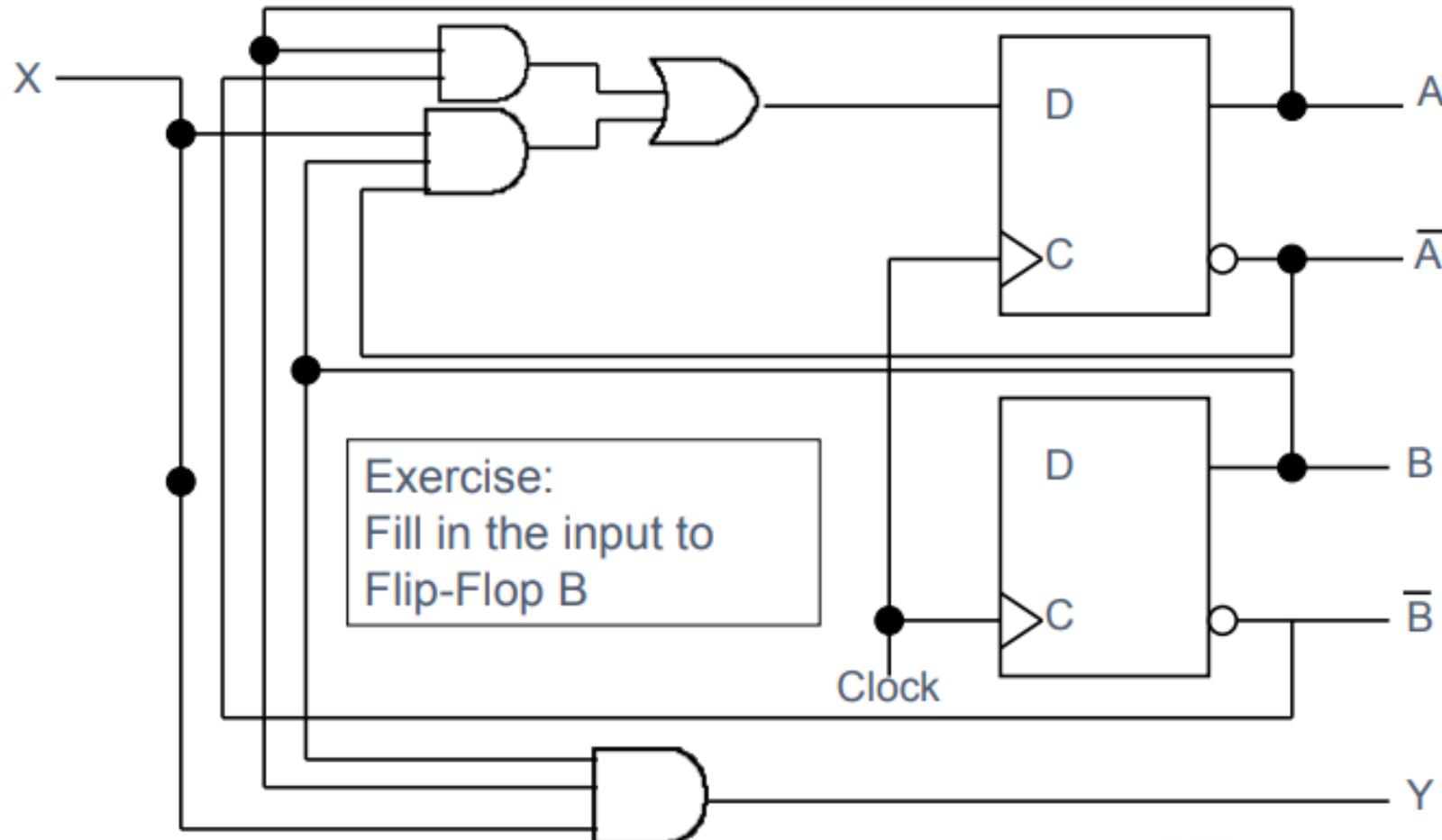
# Input Equations

$$A_{\text{next}} = A'BX + AB'$$

$$B_{\text{next}} = A'B'X + AB'X' + ABX$$

$$Y = ABX$$

# Circuit Diagram



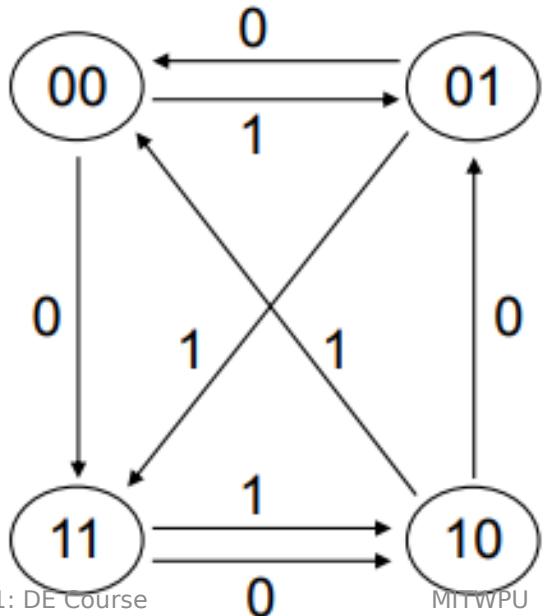
# A1 batch(PBL Activity)

43

## More Example: Word Problem

Design a 2-bit complex counter with one input  $x$  that can be

- a down counter when  $x=0$  ( $\dots \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00 \rightarrow 11 \rightarrow \dots$ )
- a Johnson counter when  $x=1$  ( $\dots \rightarrow 00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \dots$ )



Lecture 1: DE Course

MITWPU

present state	next state	
	$x=0$	$x=1$
AB	AB	AB
00	11	01
01	00	11
10	01	00
11	10	10

12/20/2022

present state	next state	
	x=0	x=1
AB	AB	AB
00	11 01	
01	00 11	
10	01 00	
11	10 10	

D<sub>A</sub>

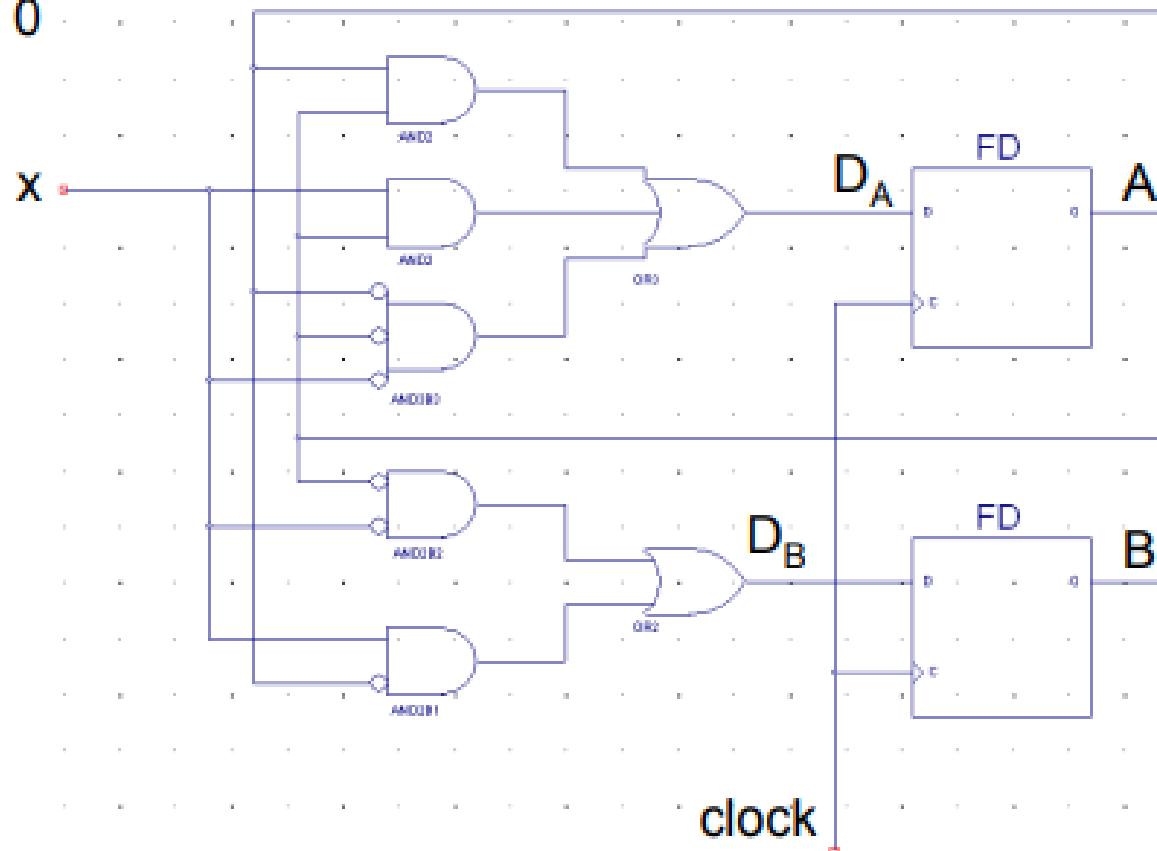
x\AB	00	01	11	10
0	1	0	1	0
1	0	1	1	0

$$D_A = AB + Bx + A'B'x'$$

D<sub>B</sub>

x\AB	00	01	11	10
0	1	0	0	1
1	1	1	0	0

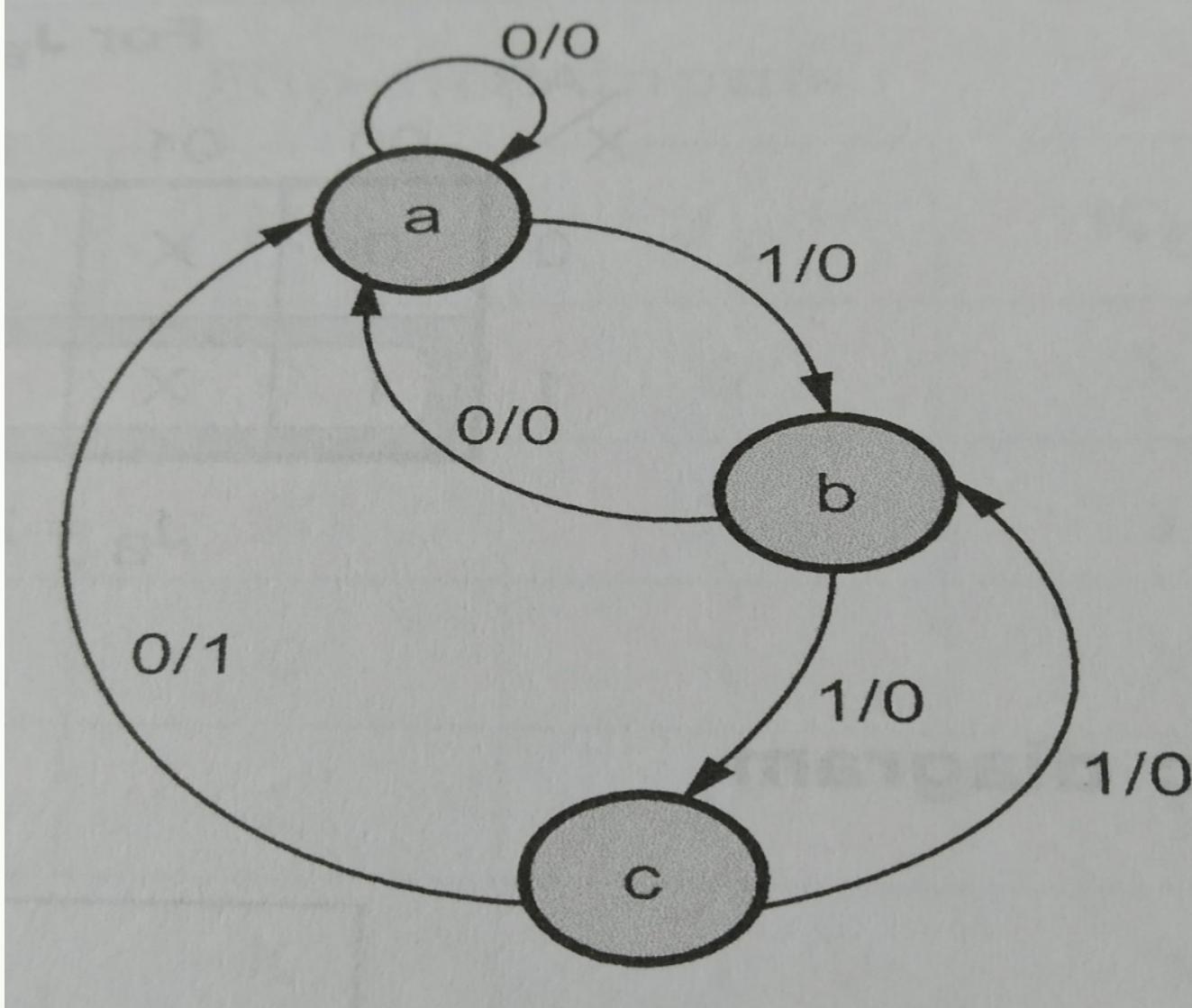
$$D_B = B'x' + A'x$$





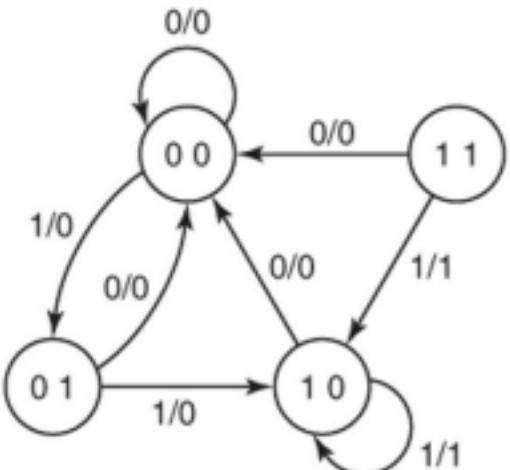
## A2 batch: PBL2:

□ **Design a 3-bit gray code Counter**



**Example:** state diagram = state table  
state table/state diagram

→ circuit



$q$	$q^*$		$z$	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1
1 1	0 0	1 0	0	1

D-FF characteristic eq:  $D = Q^*$

D <sub>A</sub>	x	AB			
		00	01	11	10
0		0	0	0	0
1		0	1	1	1

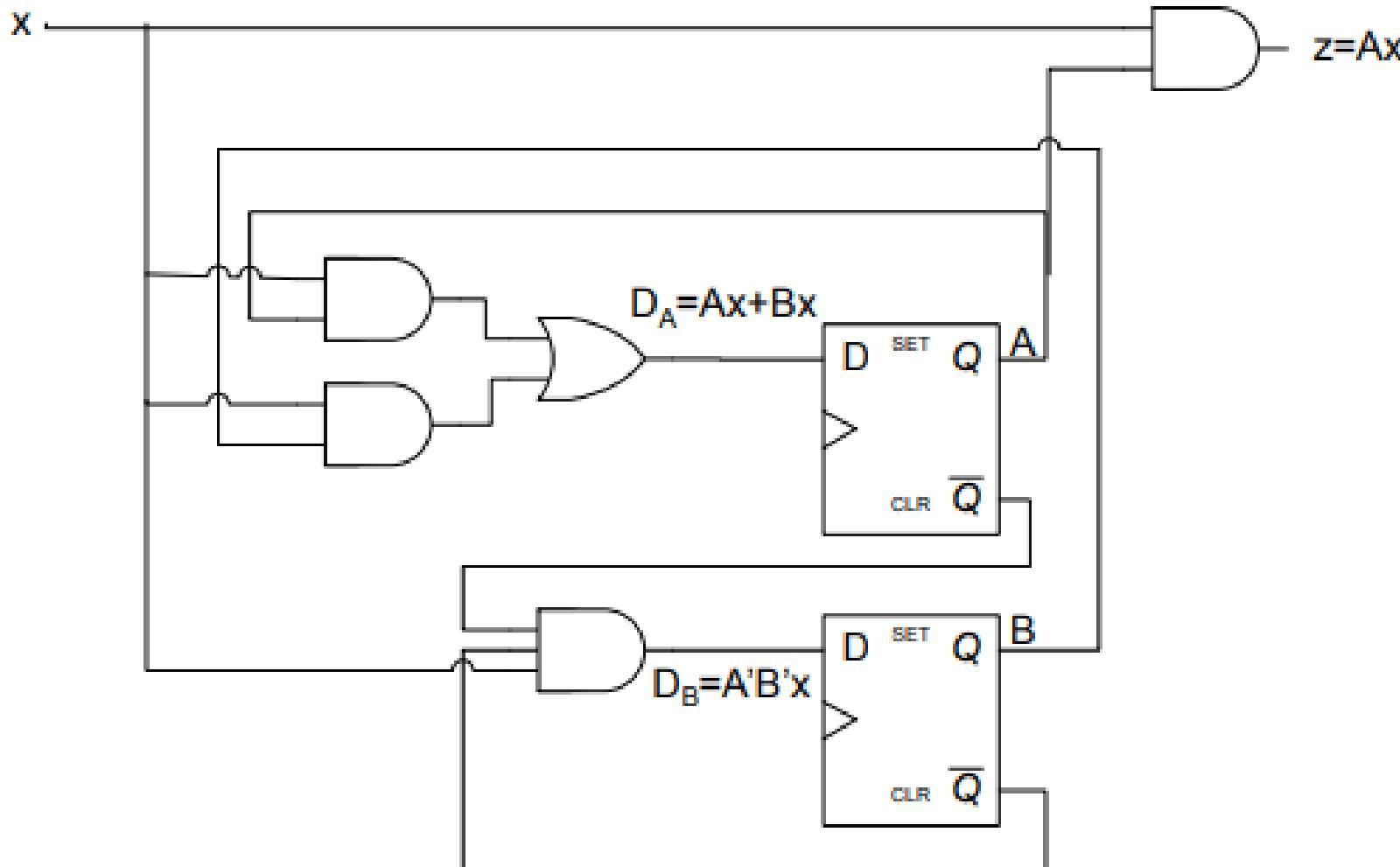
$D_A = Ax + Bx$

D <sub>B</sub>	x	AB			
		00	01	11	10
0		0	0	0	0
1		1	0	0	0

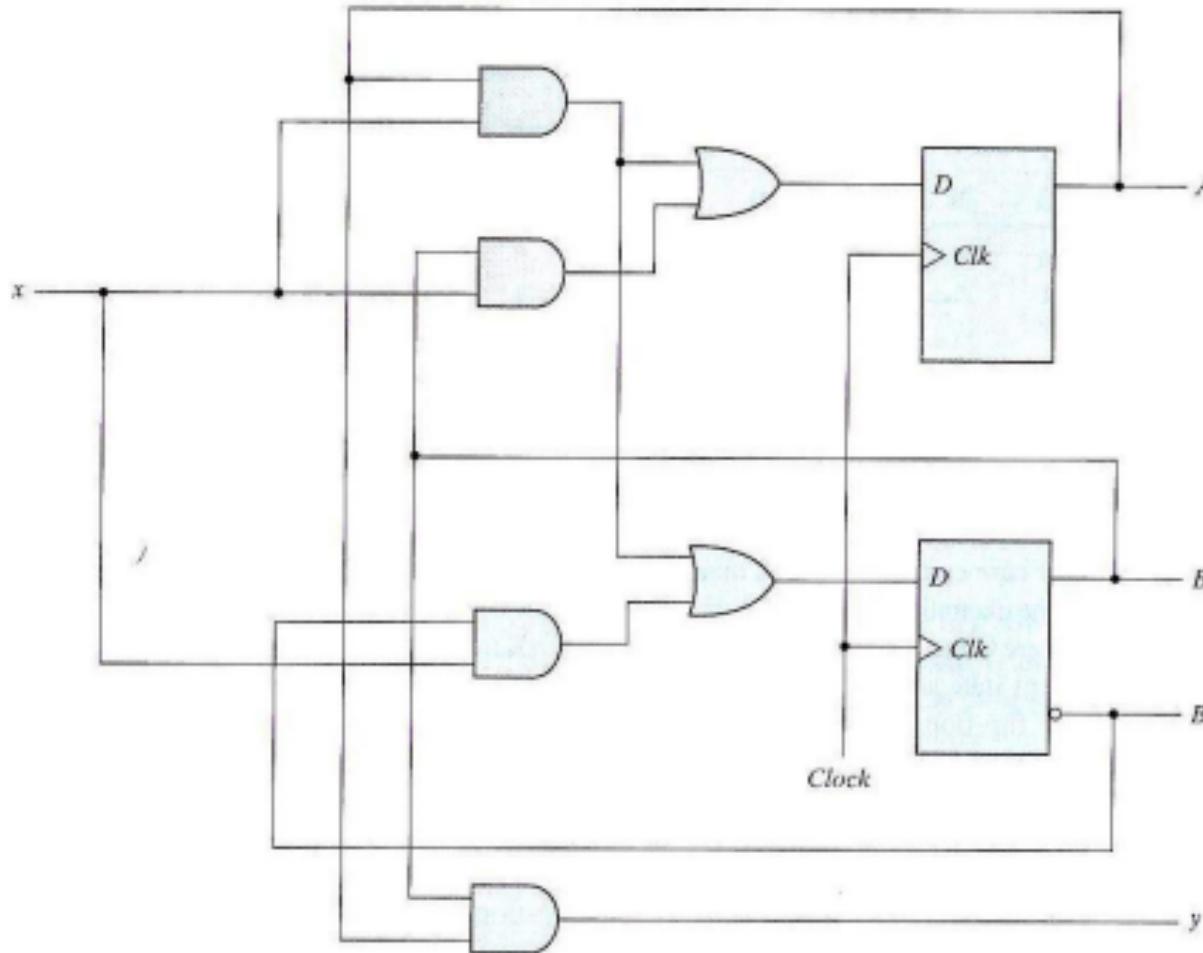
$D_B = A'B'x$

z	x	AB			
		00	01	11	10
0		0	0	0	0
1		0	0	1	1

$z = Ax$



**Example:** Show the state diagram of following circuit



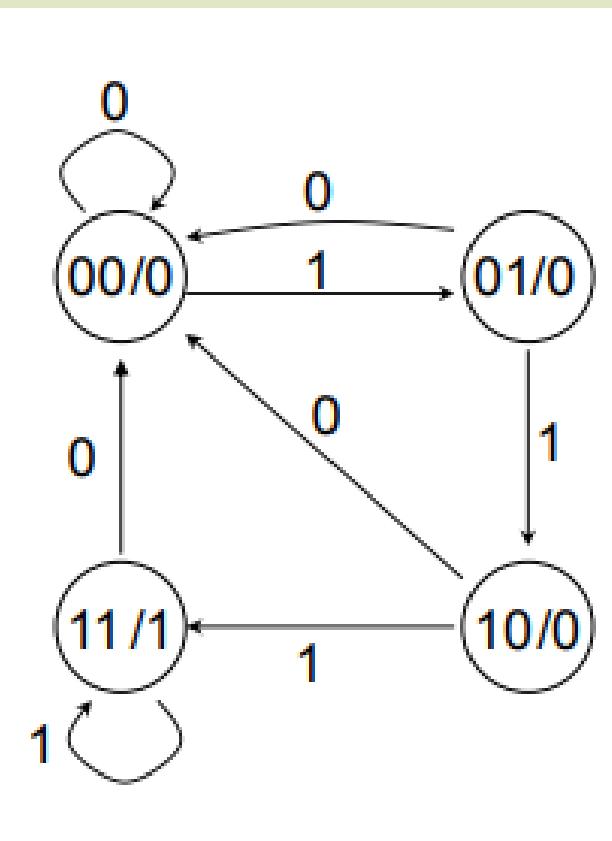
**FIGURE 5.29**  
Logic diagram of sequence detector

$$\begin{aligned}y &= AB \\D_A &= Ax+Bx \\D_B &= Ax+B'x\end{aligned}$$

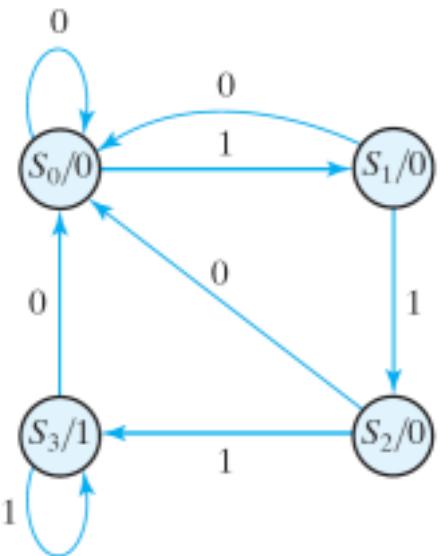
$$\left. \begin{array}{l} y = AB \\ D_A = Ax + Bx \\ D_B = Ax + B'x \end{array} \right\}$$

x: input, y: output  
 A, B: present state  
 D<sub>A</sub>, D<sub>B</sub>: next state (D-FF)

Present State	Next State				Output
	x = 0		x = 1		
A	B	A	B	y	
0	0	0	1		0
0	0	1	0		0
0	0	1	1		0
0	0	1	1		1



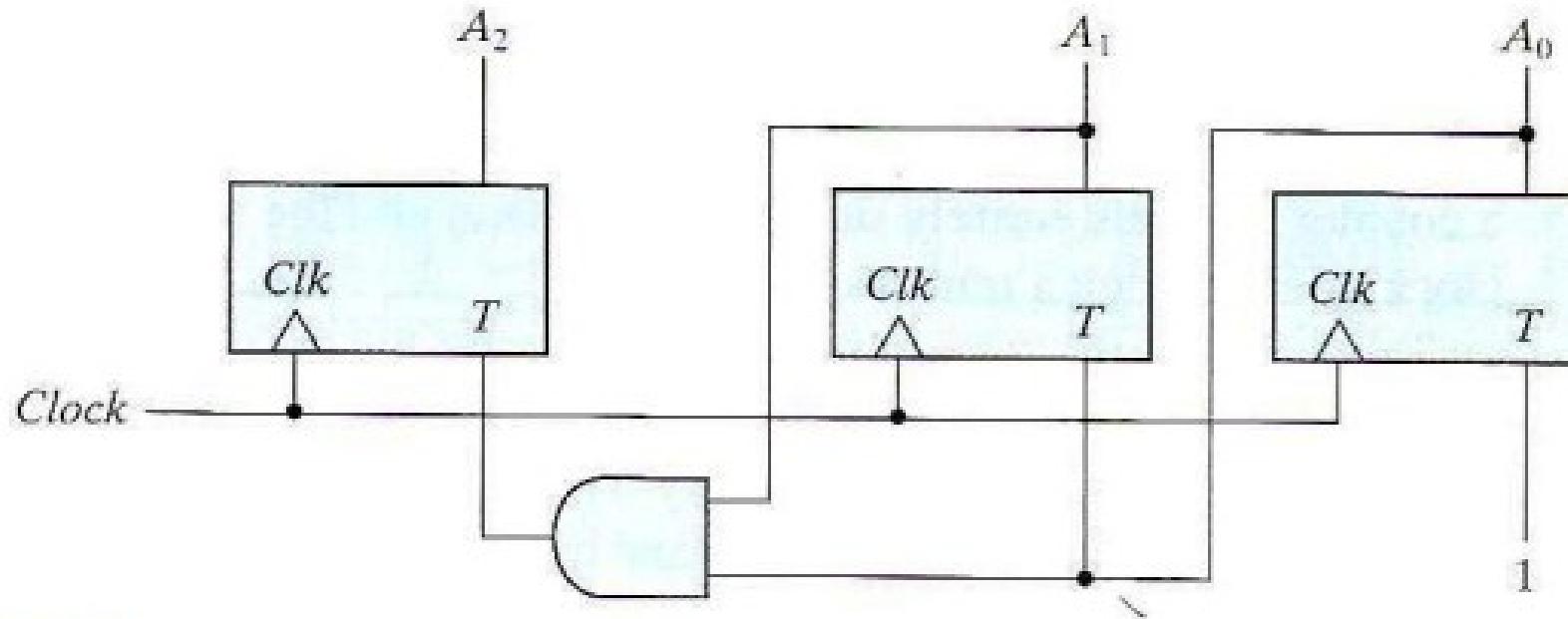
From state diagram



<b>Present State</b>	<b>Next State</b>				<b>Output</b>
	$x = 0$		$x = 1$		
$A$	$B$	$A$	$B$		$y$
0	0	0	1		0
0	0	1	0		0
0	0	1	1		0
0	0	1	1		1

## Circuit, State Diagram, State Table

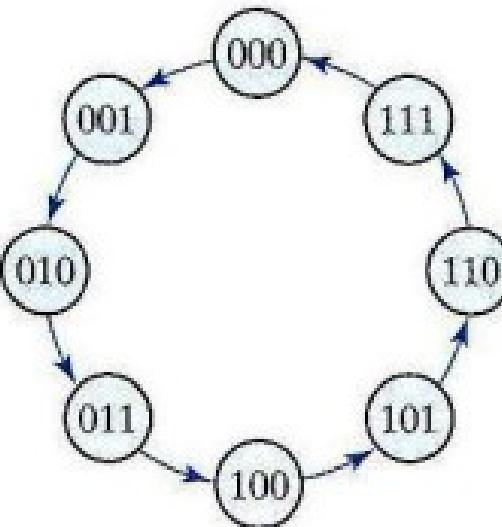
More Example: Binary Counter – show state diagram and table



**FIGURE 5.34**  
Logic diagram of three-bit binary counter

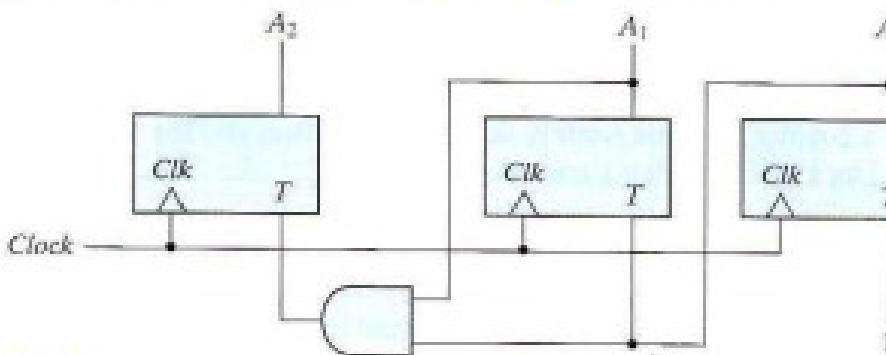
# Circuit, State Diagram, State Table

**More Example:** Binary Counter – show state diagram and table



**FIGURE 5.32**  
State diagram of three-bit binary counter

present state	next state
$A_2 A_1 A_0$	$A_2 A_1 A_0$
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0



**FIGURE 5.34**  
Logic diagram of three-bit binary counter

## Design Example 2: Sequential circuit using JK Flip-flop

Present State		Input $x$	Next State		Flip-Flop Inputs			
$A$	$B$		$A$	$B$	$J_A$	$K_A$	$J_B$	$K_B$
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

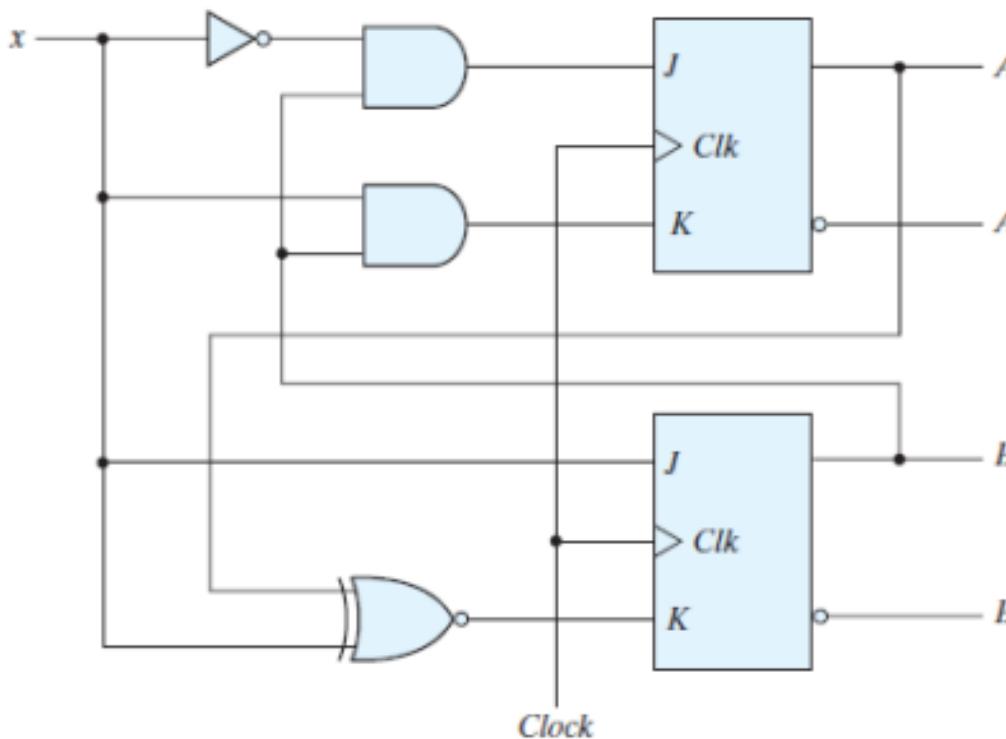
$A$	$Bx$	00	01	11	10
0		$m_0$	$m_1$	$m_3$	$m_2$
1		$m_4$	$m_5$	$m_7$	$m_6$
		$m_0$	$m_1$	$m_3$	$m_2$
		$m_4$	$m_5$	$m_7$	$m_6$

$A$	$Bx$	00	01	11	10
0		$m_0$	$m_1$	$m_3$	$m_2$
1		$m_4$	$m_5$	$m_7$	$m_6$
		$m_0$	$m_1$	$m_3$	$m_2$
		$m_4$	$m_5$	$m_7$	$m_6$

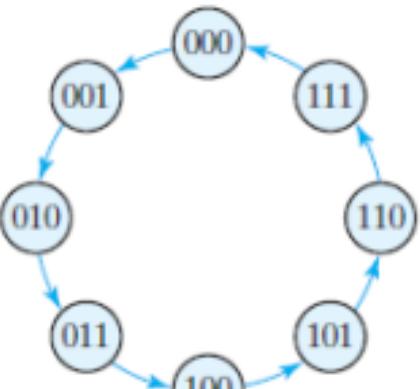
$A$	$Bx$	00	01	11	10
0		$m_0$	$m_1$	$m_3$	$m_2$
1		$m_4$	$m_5$	$m_7$	$m_6$
		$m_0$	$m_1$	$m_3$	$m_2$
		$m_4$	$m_5$	$m_7$	$m_6$

$A$	$Bx$	00	01	11	10
0		$m_0$	$m_1$	$m_3$	$m_2$
1		$m_4$	$m_5$	$m_7$	$m_6$
		$m_0$	$m_1$	$m_3$	$m_2$
		$m_4$	$m_5$	$m_7$	$m_6$

## Design Example 2: Sequential circuit using JK Flip-flop



# Design Example 3: Counter using T Flip-flop



Present State			Next State			Flip-Flop Inputs		
$A_2$	$A_1$	$A_0$	$A_2$	$A_1$	$A_0$	$T_{A2}$	$T_{A1}$	$T_{A0}$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

$A_2$	$A_1 A_0$	00	01	$\overbrace{11}^{A_1}$	10
$A_2$	0	$m_0$	$m_1$	$m_2$	$m_3$
$A_2$	1	$m_4$	$m_5$	$m_6$	$m_7$
$A_2$	$A_1 A_0$	00	01	$\overbrace{11}^{A_1}$	10

$$T_{A2} = A_1 A_0$$

$A_2$	$A_1 A_0$	00	01	$\overbrace{11}^{A_1}$	10
$A_2$	0	$m_0$	$m_1$	$m_2$	$m_3$
$A_2$	1	$m_4$	$m_5$	$m_6$	$m_7$
$A_2$	$A_1 A_0$	00	01	$\overbrace{11}^{A_1}$	10

$$T_{A1} = A_0$$

$A_2$	$A_1 A_0$	00	01	$\overbrace{11}^{A_1}$	10
$A_2$	0	$m_0$	$m_1$	$m_2$	$m_3$
$A_2$	1	$m_4$	$m_5$	$m_6$	$m_7$
$A_2$	$A_1 A_0$	00	01	$\overbrace{11}^{A_1}$	10

$$T_{A0} = 1$$

## Design Example 3: Counter using T Flip-flop

