

Department of Electronics & Communication Engineering

**Basic Electronics Notes (ECE111)**  
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# Chapter 1

## Diodes and their Applications

### 1.1 Background

Materials can be classified into three types as mentioned below. The Figure 1.21 shows the energy band gap of different materials.

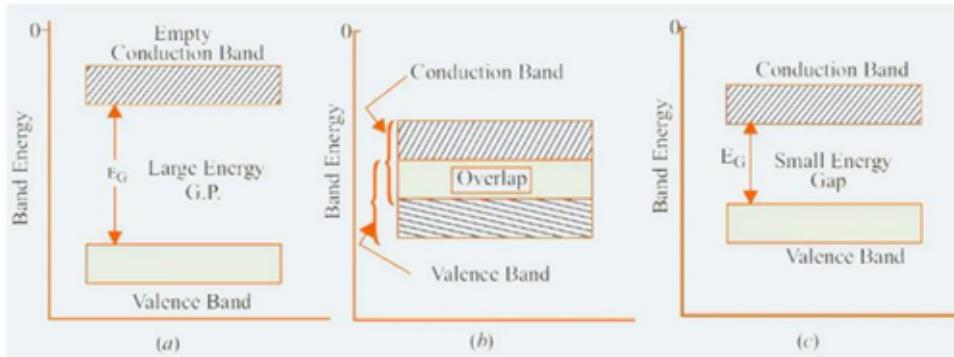


Figure 1.1: Energy Band Gap of different Materials: (a) Insulators, (b) Conductors, (c) Semiconductors

- ★ **Conductors:** Are very good carriers of electricity. They have a large number of free electrons since there is no energy gap between conduction band and valence band. E.g., Copper, Aluminium.
- ★ **Insulators:** Do not conduct electricity. There is a large energy gap between conduction band and valence band. Eg: Wood, glass.
- ★ **Semi-Conductors:** Are neither insulators, nor conductors. The band Gap between conduction band and valence band is very narrow. Eg: Germanium (Ge), Silicon (Si) conductivity lies between conductors and insulators. There are 2 types of semiconductors.
  - **Intrinsic semiconductors:** Semiconductor in its purest form is intrinsic semiconductor. It behaves as an insulator at zero temperature. At room temperature, electron hole pairs are created, due to the drift of electrons to the conduction bond. This creates a vacancy called as a ‘hole’. Holes are positively charged while electrons are negatively charged.

Thus, the movement of electrons in conduction band yields electron and the movement of holes in valence band gives rises to a hole current.

- **Extrinsic semiconductors:** Are created by adding impurities (or other materials) to intrinsic semiconductors to improve conductivity or conduction nature of the materials used in diodes, transistors etc. Depending upon the type of impurities added, we have 2 types: P-type semiconductors and N-type semiconductors.
  - \* **P-type semiconductors:** Are produced by doping intrinsic semiconductors with trivalent impurities also known as acceptor impurities (ions). In this hole are majority charge carriers and electrons are the minority charge carriers. Eg: trivalent impurities are Boron, Aluminium.
  - \* **N-type semiconductors:** are generated by doping intrinsic semiconductors with pentavalent impurities. Eg: Arsenic, phosphorous. These impurities are known as donor ions. In n-type semiconductors, electrons are the majority charge carriers and holes are minority charge carriers.

#### NOTE:

- Active components: Transforms one form of signals to another form. Eg: Transistors, MOSFETS, OP-Amp, Gates.
- Passive Components: Diodes, Resistor (R), Inductor (L) and Capacitor (C) utilizes Power (P) or Voltage (V) from other sources.

## 1.2 PN DIODE

- N- type and P-type semiconductor materials are chemically combined with a special fabrication technique to form P-N junction. Such P-N junction forms a popular electronic device called P-N Junction diode.

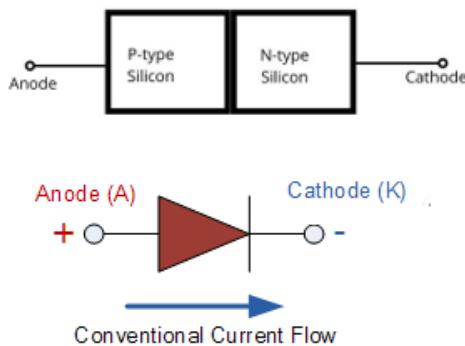


Figure 1.2: Diode Symbol

- A diode is a basic element for the number of electronic circuits.
- Diode is connected in two modes. That is Forward Bias and Reverse Bias
- P-N junction diode allows current flow when forward biased and blocks the current flow when reverse biased.

- It is a Uni-directional (one-way) device offering low-resistance when forward biased and behaving almost as open switch when reverse biased.
- Arrow head indicates the conventional direction of current flow when the diode is forward biased.
- Manufacturers provide datasets that specify the maximum forward current and reverse voltages for various types of diodes.
- Some diodes are low current diodes that are used in switching circuits. High current diodes are often used as rectifiers for ac to dc conversion.
- P-N junction diode can be get damaged if
  - A high forward current overheats the device
  - A large reverse voltage causes the junction breakdown.

### 1.2.1 Unbiased PN Junction Diode

- Unbiased P-N junction is the one where no external source is connected across the terminals of the device. Consider a zero bias P-N junction as shown in figure 1.3.

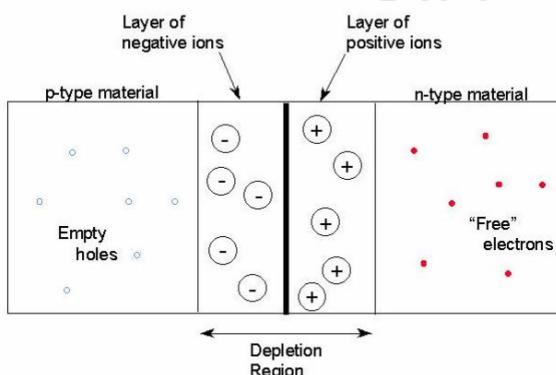


Figure 1.3: Unbiased Diode

- At N-type semiconductor, large number of free electrons are present while at P-type, small number of free electrons are present.
- Due to this high concentration of electrons at N-side, they get repelled from each other and hence try to move towards lower concentration region. Hence, the free electrons from N-side are attracted towards the holes at P-side. Thus, the free electrons move from N-side (high concentration region) to P-side (low concentration region) (called Diffusion)
- At P-type semiconductor, large number of holes are present while at N-type, semiconductor, small number of holes are present.
- Due to this high concentration of holes at P-side they get repelled and move towards lower concentration N-side. Hence, the holes from P-side are attracted towards the free electrons at N-side. Thus, the holes move from P-side (high concentration) to N-side (low concentration)

- As holes enter the N region, they recombine with the donor atoms. As donor atoms accept additional holes, they become positively charged immobile ions. Hence number of positively charged immobile ions get formed near the junction on N-side.
- Similarly the electrons diffusing from N side to P side recombine with the acceptor atoms on P side. As acceptor atoms accept additional electrons, they become negatively charged immobile ions. Such large number of negatively charged immobile ions get formed near the junction on p-side. The formation of immobile ions near the junction is shown in the Figure 1.3.
- In the region near the junction, there exists a wall of negative immobile charges on P side and a wall of positive immobile charges on N side. In this region, there are no mobile charge carriers. Such a region is depleted of the free mobile charge carriers and hence called depletion region or depletion layer.
- In equilibrium condition, the depletion region gets widened upto a point where no further electrons or holes can cross the junction. Thus depletion region acts as the barrier.
- Thus, a barrier is built up near the junction which prevents the further movement of electrons and holes. The total charge formed at the P-N junction is called barrier voltage, barrier potential or junction potential.
- The size of the barrier voltage at the P-N junction depends on the amount of doping, junction temperature and type of material used. The barrier potential for Si diode is 0.7V and for Ge is 0.3V.

### 1.2.2 VI Characteristics and Biasing of the Diode

- Applying an external voltage across the terminals of the P-N junction diode is known as **biasing**.
- There are two types:
  - Forward biasing
  - Reverse biasing

#### Forward Biased P-N Junction

- A diode is said to be **forward biased** when its **anode** is connected to the **positive terminal** of the battery and **cathode** is connected to the **negative terminal**.

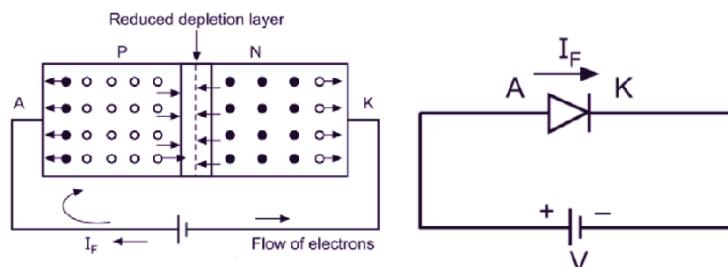


Figure 1.4: Forward Biasing of the Diode

- When the diode is forward biased, as long as the applied voltage  $V$  is less than the barrier potential, there is no conduction.
- When the applied voltage  $V$  exceeds the barrier potential, the diode becomes forward biased.
  - Holes on the P-side are repelled by the positive terminal of the battery and are driven towards the junction.
  - Electrons on the N-side are repelled by the negative terminal of the battery and move towards the junction.
- As a result, the width of the **depletion region** decreases.
- As the forward bias voltage  $V$  increases further:
  - The depletion layer reduces further.
  - Eventually, it disappears almost completely.
  - A large number of charge carriers flow across the junction.
  - This causes an **exponential rise in current**.

## Reverse Biased P-N Junction

- A diode is said to be **reverse biased** when the **anode (P-region)** is connected to the **negative terminal** of the battery and the **cathode (N-region)** is connected to the **positive terminal**.

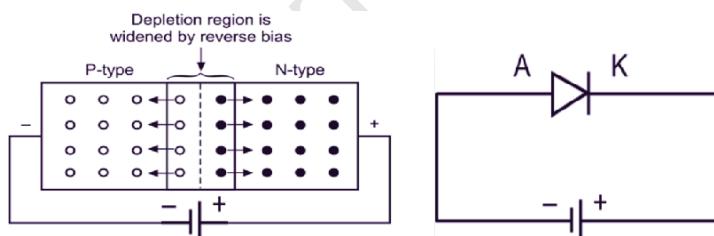


Figure 1.5: Reverse Biasing of the Diode

- Electrons from the N-region are attracted towards the positive terminal of the battery, and holes from the P-region are attracted towards the negative terminal.
- No charge carrier is able to cross the junction. As electrons and holes both move away from the junction, the depletion region widens. This creates more positive ions and hence more negative ions in the N region.
- This causes the **depletion region to widen** and the **barrier potential to increase**, reducing the flow of majority charge carriers across the junction to nearly zero.
- Due to increased barrier potential, the electrons from P-region towards the positive of battery. Similarly negative side of barrier potential drags the holes from N-region towards the negative of battery. The electrons on P-side and holes on N-side are minority charge carriers, which constitute the current in reverse biased condition. This is called the **reverse saturation current ( $I_S$ )**.

- As a result, a reverse biased diode allows only a **very small reverse current**, and hence can be considered to have a **high reverse resistance**.
  - Typically in the nanoampere (nA) range for silicon diodes and microampere ( $\mu\text{A}$ ) or milliampere (mA) for germanium diodes.
- If reverse voltage is increased, at a particular value, velocity of minority carriers increases. Due to the kinetic energy associated with the minority carriers, more minority carriers are generated when there is collision of minority carriers with the atoms. The collision make the electrons to break the co-valent bonds. These electrons are available as minority carriers and get accelerated due to high reverse voltage. They again collide with another atoms to generate more minority carriers.
- Finally large number of minority carriers move across the junction, breaking the PN junction. These large number of minority carriers give rise to a very high reverse current. This effect is called **avalanche effect** and the mechanism of destroying the junction is called **reverse breakdown** of a p-n junction.
- So, when the reverse voltage  $V_R$  is sufficiently increased, the diode enters **breakdown**.
- Caution:** Reverse breakdown can permanently damage the diode unless the reverse current is limited by a suitable series resistor.

### 1.3 Forward and Reverse characteristics of the Si and Ge diode:

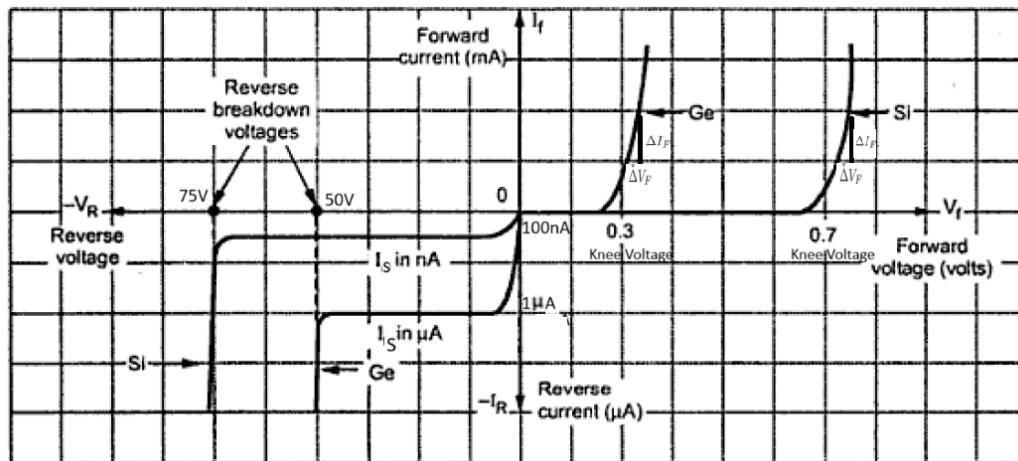


Figure 1.6: Reverse Biasing of the Diode

- V-I characteristics of PN junction is the graph of voltage applied across the PN junction and the current flowing through the PN junction. The Fig. 1.4 shows the forward biased diode.

- The applied voltage is  $V$  while the voltage across the diode is  $V_F$ . The current flowing in the circuit is the forward current  $I_F$ . The graph of forward current  $I_F$  against the forward voltage  $V_F$  across the diode is called forward characteristics of a diode.
- As long as  $V_F$  is less than knee voltage, the current flowing is very small. Practically this current is assumed to be zero.
- As  $V_F$  increases towards knee voltage, the width of depletion region goes on reducing. When  $V_F$  exceeds knee voltage, the depletion region becomes very thin and current increases suddenly. This increase in the current is exponential as shown in the Fig. 1.6
- At one point, the forward current starts increasing exponentially is called knee of the curve.
- The Fig. 1.5 shows the reverse biased diode. The reverse voltage across the diode is  $V_R$  while the current flowing is reverse current  $I_R$  flowing due to minority charge carriers. The graph of  $I_R$  against  $V_R$  is called reverse characteristics of a diode.
- As reverse voltage is increased, reverse current increases initially but after a certain voltage, the current remains constant equal to reverse saturation current  $I_s$  though reverse voltage is increased. At one point, where breakdown occurs and reverse current increases rapidly is called knee of the reverse characteristics. This is shown in the reverse **VI characteristics** of the diode in Figure 1.6

## Diode Parameters

- **Forward Voltage Drop ( $V_F$  or  $V_K$ ):**

The voltage drop across the diode in forward bias condition is known as **forward voltage drop**. It is represented as  $V_F$  and is generally equal to the **knee voltage**  $V_K$ .

Typical values:

- Silicon (Si): 0.7 V
- Germanium (Ge): 0.3 V

- **Maximum Forward Current ( $I_{F\max}$ ):**

It is the maximum current a diode can conduct under forward bias without causing permanent damage to the P-N junction due to overheating.

- **Reverse Breakdown Voltage ( $V_{BR}$ ):**

It is the reverse bias voltage at which the P-N junction breaks down and a large current flows, potentially damaging the diode.

- For silicon diodes, breakdown occurs around 75 V.
- For germanium diodes, breakdown occurs around 50 V.

- **Reverse Saturation Current ( $I_s$ ):**

It is the very small current that flows through the diode in reverse bias due to minority carriers.

Typical values:

- Germanium (Ge): in  $\mu A$
- Silicon (Si): in  $nA$

- **Dynamic Resistance ( $r_d$ ):**

It is the resistance offered by the diode to changing voltages in forward bias. Also called **incremental or AC resistance**.

It is given by:

$$r_d = \frac{\Delta V_F}{\Delta I_F}$$

From the  $V$ - $I$  graph of the diode:

$$\text{Slope} = \frac{\Delta I_F}{\Delta V_F} \Rightarrow r_d = \frac{1}{\text{Slope}}$$

- **Forward Resistance ( $R_F$ ):**

It is the ratio of forward voltage to forward current. Also known as **static forward resistance**:

$$R_F = \frac{V_F}{I_F}$$

- **Reverse Resistance ( $R_R$ ):**

It is the ratio of reverse voltage to reverse current. Also called **static reverse resistance**:

$$R_R = \frac{V_R}{I_R}$$

## 1.4 Diode Models

An equivalent circuit for a device is a circuit that models or simulates its electrical behavior. It is made up of basic components such as resistors and voltage sources.

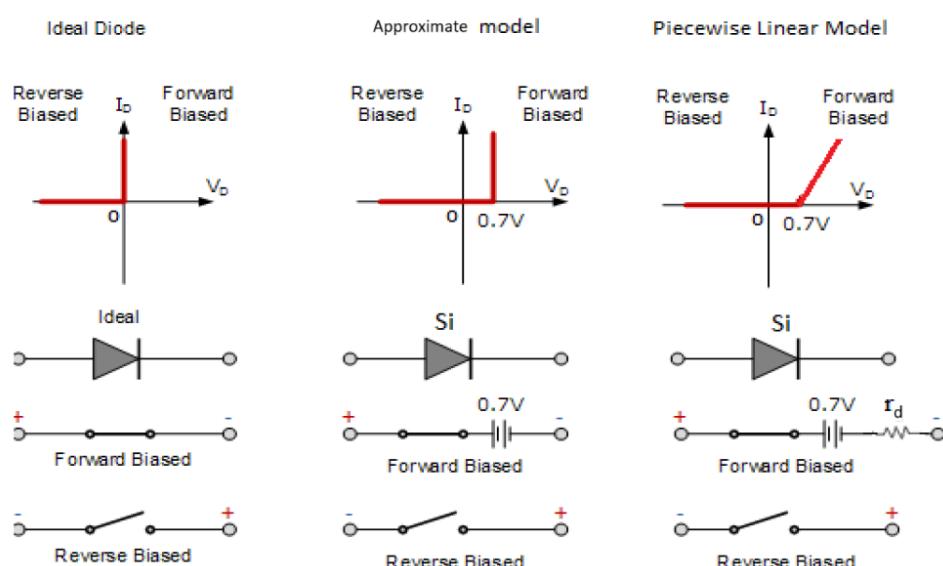


Figure 1.7: Diode Models

## 1. Ideal Diode Model

- In an ideal diode:
  - **Forward Voltage Drop ( $V_F$ ) = 0**
  - **Forward Resistance ( $R_F$ ) = 0**
  - **Reverse Resistance ( $R_R$ ) =  $\infty$**
  - **Reverse Current ( $I_R$ ) = 0**
- This implies perfect conduction in forward bias and perfect insulation in reverse bias.

## 2. Approximate Diode Model

- The approximate model includes:
  - An ideal diode switch
  - A **voltage source  $V_F = 0.7$**  in series to represent the threshold voltage (barrier potential)
- It neglects the dynamic resistance ( $r_d$ ) and models only the threshold behavior.

## 3. Piecewise Linear Model

- This model consists of:
  - An ideal diode
  - A voltage cell (threshold voltage  $V_F = 0.7$ )
  - A **dynamic resistance  $r_d$**  in series
- This model provides a more accurate approximation of a real diode's forward characteristic.
- **Note:** When the actual forward characteristics of a diode are not available, this model provides a **straight-line approximation** and is called the *piecewise linear model*.

## 1.5 Numerical on Diodes

1. Find the value of current  $I$  in the following circuit.

**Answer:** A Si diode is reverse biased. So it does not conduct.

2. For the circuit shown, calculate  $I_D$ .

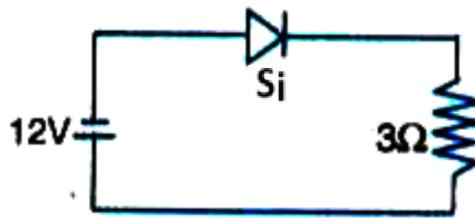


Figure 1.8: Problem 1

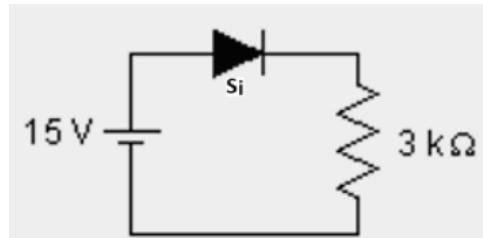


Figure 1.9: Problem 2

**Solution:** Applying KVL, we get:

$$15 \text{ V} - 0.7 \text{ V} - I_D \times 3 \text{ k}\Omega = 0$$

$$I_D = \frac{15 - 0.7}{3\text{k}\Omega} = \frac{14.3}{3\text{k}\Omega} = 4.76 \text{ mA}$$

3. For the circuit shown, calculate  $I_D$  and  $V_o$ .

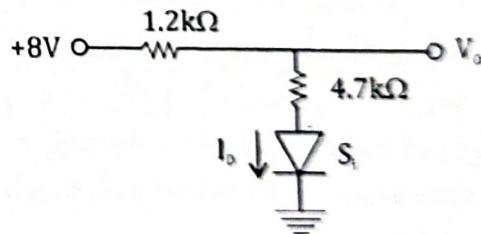


Figure 1.10: Problem 3

**Solution:**

Applying KVL, we get:

$$8 \text{ V} - I_D \times 1.2 \text{ k}\Omega - I_D \times 4.7 \text{ k}\Omega - 0.7 \text{ V} = 0$$

$$I_D = \frac{8 - 0.7}{(4.7 + 1.2) \text{ k}\Omega} = \frac{7.3}{5.9 \text{ k}\Omega} = 1.237 \text{ mA}$$

$$V_o = I_D \times 4.7 \times 10^3 + 0.7$$

$$= 1.237 \times 10^{-3} \times 4.7 \times 10^3 + 0.7 = 5.8119 + 0.7 = \underline{\underline{6.51 \text{ V}}}$$

4. For the circuit shown, calculate  $I_D$  and  $V_o$ .

**Solution**

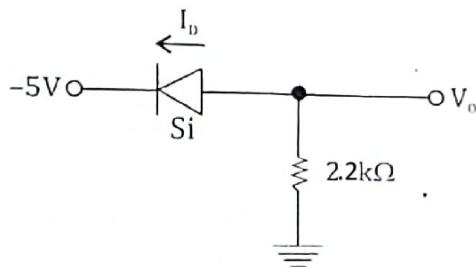


Figure 1.11: Problem 4

Applying KVL, we have:

$$-5 \text{ V} + 2.2 \text{ k}\Omega \times I_D + 0.7 \text{ V} = 0$$

$$\therefore I_D = \frac{5 - 0.7}{2.2 \text{ k}\Omega} = 1.95 \text{ mA}$$

$$V_o = 1.95 \text{ mA} \times 2.2 \text{ k}\Omega = 4.3 \text{ V}$$

5. For the circuit shown, calculate the current in the circuit.

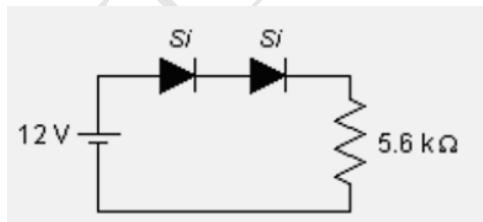


Figure 1.12: Problem 5

**Solution:** Applying KVL, we get:

$$12 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} - I_D \times 5.6 \text{ k}\Omega = 0$$

$$I_D = \frac{12 - 1.4}{5.6 \text{ k}\Omega} = \frac{10.6}{5.6 \text{ k}\Omega} = 1.893 \text{ mA}$$

## 1.6 Rectifiers

- One of the most important applications of a junction diode is **rectification**.
- **Rectification** is the process of converting **alternating current (AC)** into **direct current (DC)**.

- Rectification can be performed using:
  - **Half-wave rectifier** (uses one diode)
  - **Full-wave rectifier** (uses two or four diodes)
- Depending on the type of AC supply and the configuration of the rectifier circuit, the output voltage may contain both DC and AC components. This output is called **pulsating DC** and includes **AC ripples**.
- Many applications, such as power supplies for radios, televisions, and computers, require a **steady and constant DC voltage**.
- In such applications, the output of the rectifier is passed through a **filter circuit** to reduce the ripple content and provide a smooth DC voltage.
- Filter circuits typically consist of:
  - Capacitors
  - Inductors (chokes)
  - Resistors (optional)
  - Or a combination (e.g., RC filters, LC filters)
- The filtering process generally involves the use of a **large capacitor**, which charges to the peak of the input voltage and discharges slowly, thus providing a relatively constant **DC output voltage**.
- Filter types:
  - **RC Filter**: Uses resistor and capacitor
  - **LC Filter**: Uses inductor and capacitor

### 1.6.1 Half Wave Rectifier (HWR)

- A Half Wave Rectifier requires only **one diode** for its construction.

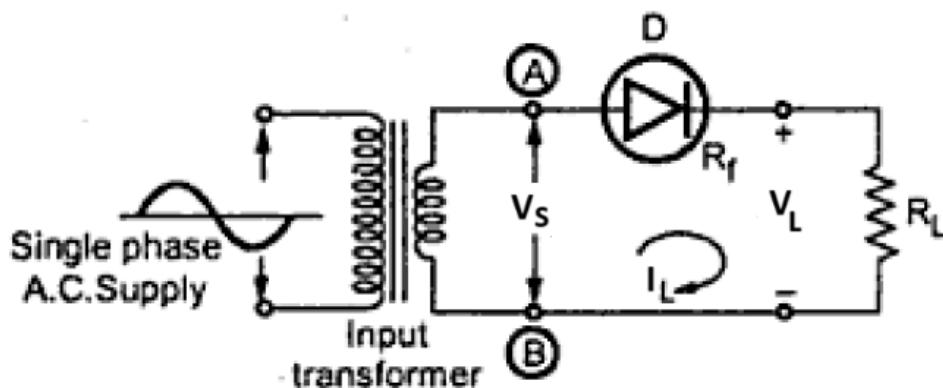


Figure 1.13: Half Wave Rectifier

- In HWR, the diode conducts only during the **positive half cycle** of the input AC signal.
- The **negative half cycle** is blocked, resulting in a unidirectional (pulsating DC) output.
- The input is a sinusoidal AC voltage. The instantaneous secondary voltage is:

$$V_s = V_m \sin \omega t \quad \text{for } 0 \leq \omega t \leq 2\pi$$

where,  $\omega = 2\pi f$ , and  $V_m$  is the peak value of voltage.

## Working

- During the **positive half cycle** of the input AC signal, i.e.,  $0 \leq \omega t \leq \pi$ :
  - The secondary winding of the transformer has node A more positive than node B.
  - The diode  $D$  becomes **forward biased** and acts as a **closed switch**.
  - Current flows through the load resistor  $R_L$ , producing a voltage across it.
  - Since the load is resistive, the current waveform follows the voltage waveform.
- The **load current** is given by:

$$I_L = I_m \sin \omega t \quad \text{for } 0 \leq \omega t \leq \pi$$

- Where:

$$I_m = \frac{V_m}{R_s + R_f + R_L}$$

is the **peak value of the current**.

- The output voltage is a **pulsating DC**, and is discontinuous.
- The **average or DC value** of the output voltage or current is obtained by integrating over one full cycle.
- During the **negative half cycle**, i.e.,  $\pi \leq \omega t \leq 2\pi$ :
  - Node A becomes negative and node B becomes positive.
  - The diode  $D$  is **reverse biased** and acts as an **open switch**.
  - No current flows through the load resistor  $R_L$ .
  - Therefore,

$$I_L = 0 \quad \text{for } \pi \leq \omega t \leq 2\pi$$

- The load voltage is:

$$V_L = V_m \sin \omega t \quad \text{for } 0 \leq \omega t \leq \pi$$

$$V_L = 0 \quad \text{for } \pi \leq \omega t \leq 2\pi$$

## Waveform

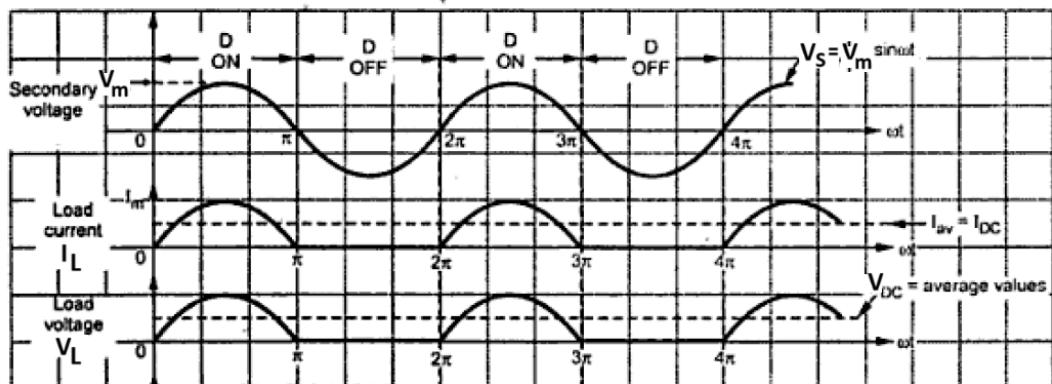


Figure 1.14: HWR Waveforms

## Parameters

1. **Average DC Load Current ( $I_{DC}$ ):** The average value of an alternating current is calculated as the area under the one cycle of load current  $I_L$  from 0 to  $2\pi$ , divided by the period of  $I_L$ , i.e.,  $2\pi$ :

$$I_{DC} = \sqrt{\frac{\text{Area under the one cycle of load current } I_L}{\text{period of } I_L}}$$

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} I_L d(\omega t)$$

Given,  $I_L = I_m \sin(\omega t)$ , we have:

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} I_m \sin(\omega t) d(\omega t)$$

Since the current is zero from  $\pi \leq \omega t \leq 2\pi$ , the integral becomes:

$$I_{DC} = \frac{I_m}{2\pi} \int_0^{\pi} \sin(\omega t) d(\omega t)$$

$$I_{DC} = \frac{I_m}{2\pi} [-\cos(\omega t)]_0^{\pi}$$

$$I_{DC} = -\frac{I_m}{2\pi} [\cos(\pi) - \cos(0)]$$

$$\cos(\pi) = -1, \quad \cos(0) = 1$$

$$I_{DC} = -\frac{I_m}{2\pi} (-2)$$

$$I_{DC} = \frac{I_m}{\pi}$$

## 2. Average DC Load Voltage ( $V_{DC}$ ):

The average value of the output voltage is given by:

$$V_{DC} = \frac{1}{2\pi} \int_0^{2\pi} V_L d(\omega t)$$

Given that  $V_L = V_m \sin(\omega t)$ , we substitute:

$$V_{DC} = \frac{1}{2\pi} \int_0^{2\pi} V_m \sin(\omega t) d(\omega t)$$

Since the voltage is zero from  $\pi \leq \omega t \leq 2\pi$ , we split and simplify the integral:

$$V_{DC} = \frac{V_m}{2\pi} \int_0^{\pi} \sin(\omega t) d(\omega t)$$

$$V_{DC} = \frac{V_m}{2\pi} [-\cos(\omega t)]_0^{\pi}$$

$$V_{DC} = -\frac{V_m}{2\pi} [\cos(\pi) - \cos(0)]$$

$$\cos(\pi) = -1, \quad \cos(0) = 1$$

$$V_{DC} = -\frac{V_m}{2\pi} (-2) = \frac{V_m}{\pi}$$

$$V_{DC} = \frac{V_m}{\pi}$$

## Alternate Derivation:

The average DC voltage can also be expressed as the product of DC load current  $I_{DC}$  and the load resistance  $R_L$ :

$$V_{DC} = I_{DC} \times R_L = \frac{I_m}{\pi} R_L$$

Also, since:

$$I_{DC} = \frac{V_m}{\pi(R_L + R_S + R_f)}$$

Then:

$$V_{DC} = I_{DC} \cdot R_L = \frac{V_m}{\pi(R_L + R_S + R_f)} \cdot R_L$$

$$V_{DC} = \frac{V_m}{\pi \left(1 + \frac{R_S + R_f}{R_L}\right)}$$

Since  $R_S + R_f \ll R_L$ , we approximate:

$$\frac{R_S + R_f}{R_L} \ll 1$$

Therefore:

$$V_{DC} = \frac{V_m}{\pi}$$

### 3. RMS Value of Load Current ( $I_{RMS}$ ):

The RMS value of the load current is defined as:

$$I_{RMS} = \sqrt{\frac{(\text{Area under the one cycle of load current } I_L)^2}{\text{period of } I_L}}$$

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_L^2 d(\omega t)}$$

Since the current is zero for  $\pi \leq \omega t \leq 2\pi$ :

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^\pi I_L^2 d(\omega t)}$$

Given  $I_L = I_m \sin(\omega t)$ :

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^\pi I_m^2 \sin^2(\omega t) d(\omega t)}$$

Using identity  $\sin^2(\omega t) = \frac{1-\cos(2\omega t)}{2}$ :

$$I_{RMS} = \sqrt{\frac{I_m^2}{2\pi} \int_0^\pi \frac{1 - \cos(2\omega t)}{2} d(\omega t)}$$

$$I_{RMS} = \sqrt{\frac{I_m^2}{4\pi} \left[ \omega t - \frac{\sin(2\omega t)}{2} \right]_0^\pi}$$

$$\sin(2\pi) = 0, \quad \sin(0) = 0 \Rightarrow I_{RMS} = \sqrt{\frac{I_m^2}{4\pi} \cdot \pi} = \frac{I_m}{2}$$

$$I_{RMS} = \frac{I_m}{2}$$

#### 4. RMS Value of Load Voltage ( $V_{RMS}$ )

Similarly,

$$\begin{aligned} V_{RMS} &= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} V_L^2 d(\omega t)} = \sqrt{\frac{1}{2\pi} \int_0^\pi V_m^2 \sin^2(\omega t) d(\omega t)} \\ &= \sqrt{\frac{V_m^2}{4\pi} \left[ \omega t - \frac{\sin(2\omega t)}{2} \right]_0^\pi} = \sqrt{\frac{V_m^2}{4\pi} \cdot \pi} = \frac{V_m}{2} \\ V_{RMS} &= \frac{V_m}{2} \end{aligned}$$

**Alternate Derivation:**

$$V_{RMS} = I_{RMS} \cdot R_L = \frac{I_m}{2} R_L \quad \text{and} \quad I_m = \frac{V_m}{R_S + R_L + R_f}$$

So,

$$\begin{aligned} V_{RMS} &= \frac{V_m}{2(R_L + R_S + R_f)} \cdot R_L \\ V_{RMS} &= \frac{V_m}{2 \left( 1 + \frac{R_S + R_f}{R_L} \right)} \end{aligned}$$

Since  $R_S + R_f \ll R_L$ , we approximate:

$$\frac{R_S + R_f}{R_L} \ll 1$$

Therefore:

$$V_{RMS} = \frac{V_m}{2}$$

#### 5. Ripple Factor ( $\gamma$ ):

Ripple factor is defined as the ratio of RMS value of AC component to DC component of the output. Ripple factor is defined as the ratio of the RMS value of the AC component to the DC component of the output:

$$\gamma = \frac{I_{AC}}{I_{DC}} = \frac{\text{RMS value of AC component of output}}{\text{DC component of output}}$$

Here,  $I_{RMS}$  is the total RMS current of the rectifier output. It includes both AC and DC components:

$$I_{RMS}^2 = I_{AC}^2 + I_{DC}^2$$

Solving for  $I_{AC}^2$ :

$$I_{AC}^2 = I_{RMS}^2 - I_{DC}^2$$

Therefore, the ripple factor becomes:

$$\gamma = \frac{I_{AC}}{I_{DC}} = \sqrt{\frac{I_{RMS}^2}{I_{DC}^2} - 1}$$

Given:

$$I_{DC} = \frac{I_m}{\pi}, \quad I_{RMS} = \frac{I_m}{2} \Rightarrow \gamma = \sqrt{\frac{(I_m/2)^2}{(I_m/\pi)^2} - 1} = \sqrt{\frac{1/4}{1/\pi^2} - 1} = \sqrt{\frac{\pi^2}{4} - 1} \approx 1.21$$

Hence, ripple content in output = 121% of DC component, indicating poor rectification.

#### 6. Efficiency ( $\eta$ ):

Efficiency is the ratio of output DC power to input AC power:

$$\begin{aligned} \eta &= \frac{P_{DC}}{P_{AC}} = \frac{\text{output DC power}}{\text{input AC power}} = \frac{I_{DC}^2 R_L}{I_{RMS}^2 (R_f + R_L)} \\ \eta &= \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{2}\right)^2 (R_f + R_L)} = \frac{I_m^2 / \pi^2}{I_m^2 / 4} \cdot \frac{R_L}{R_f + R_L} \\ &= \frac{4}{\pi^2} \cdot \frac{R_L}{R_f + R_L} \end{aligned}$$

If  $R_f \ll R_L$ , then:

$$\eta \approx \frac{4}{\pi^2} = 0.406 \Rightarrow \eta \approx 40.6\%$$

In Half Wave Rectifiers, the ripple content is high and efficiency is low. Therefore, output is not very close to pure DC.

#### 1.6.2 Full Wave Bridge Rectifier (FWBR)

- It is a Full Wave Rectifier (FWR) circuit with four diodes.
- An AC voltage is applied to one diagonal of the bridge through a transformer, and the rectified DC output voltage is taken from the other diagonal of the bridge.

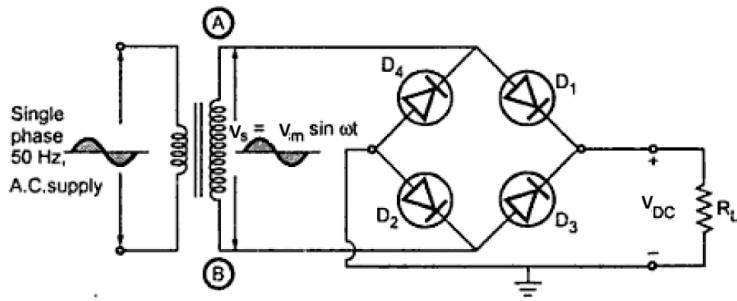


Figure 1.15: Full Wave Rectifier

## Working

- During the positive half cycle of the AC input signal, node A at the secondary of the transformer is positive while node B is negative. Hence, diodes  $D_1$  and  $D_2$  are forward biased and conduct current, while diodes  $D_3$  and  $D_4$  are reverse biased and do not conduct.
- The diodes  $D_1$  and  $D_2$  are connected in series with the load resistance  $R_L$ , allowing current to flow through the load.
- During the negative half cycle of the AC input signal, node A becomes negative while node B becomes positive. In this case, diodes  $D_3$  and  $D_4$  are forward biased and conduct current, whereas diodes  $D_1$  and  $D_2$  are reverse biased and remain off.
- Now, diodes  $D_3$  and  $D_4$  conduct current through the load resistance  $R_L$ .

In a Full Wave Rectifier (FWR), load current flows during both the half cycles of the AC input signal, and in the same direction through the load resistance. As a result, the negative half cycle of the input signal is also rectified and appears above the axis in the output waveform.

The **load current** is given by:

$$I_L = I_m \sin \omega t \quad \text{for } 0 \leq \omega t \leq \pi$$

Where:

$$I_m = \frac{V_m}{R_s + 2R_f + R_L}$$

is the **peak value of the current**. The load voltage is:

$$V_L = V_m \sin \omega t \quad \text{for } 0 \leq \omega t \leq \pi$$

where,  $V_m$  is the peak value of voltage.

## Waveform

The input and output waveform of the Bridge rectifiers is shown in the Figure 1.16.

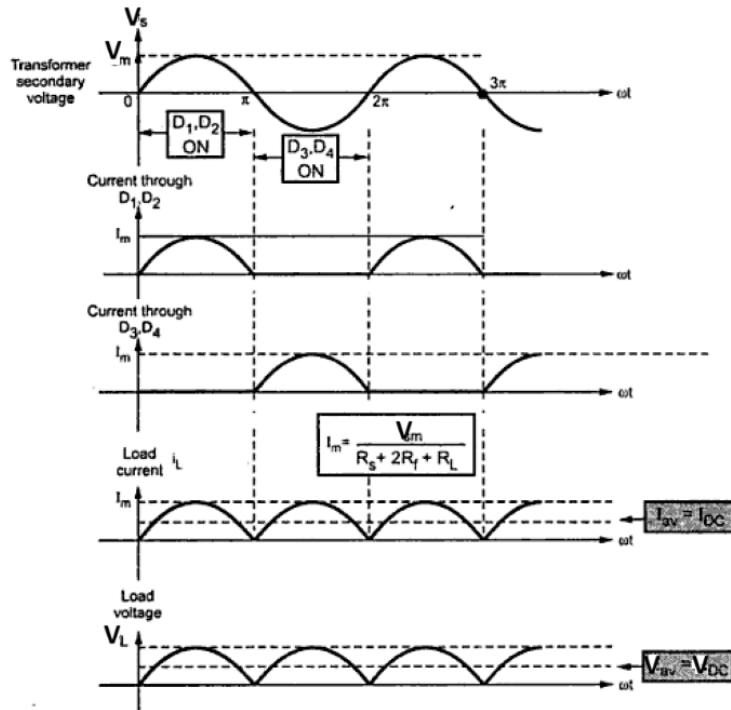


Figure 1.16: FWR Waveforms

## Parameters

### 1. Average Value of Load Current (\$I\_{DC}\$):

The average value of current is given by the area under the curve of load current \$I\_L\$ over one full cycle:

$$I_{DC} = \frac{1}{\pi} \int_0^\pi I_L d(\omega t)$$

Given: \$I\_L = I\_m \sin \omega t\$

$$\begin{aligned} \Rightarrow I_{DC} &= \frac{1}{\pi} \int_0^\pi I_m \sin \omega t d(\omega t) \\ &= \frac{1}{\pi} \int_0^\pi I_m \sin \omega t d(\omega t) \\ &= \frac{I_m}{\pi} \int_0^\pi \sin \omega t d(\omega t) \\ &= \frac{I_m}{\pi} [-\cos \omega t]_0^\pi \\ &= \frac{I_m}{\pi} [-\cos \pi + \cos 0] \end{aligned}$$

Since \$\cos \pi = -1\$ and \$\cos 0 = 1\$,

$$\begin{aligned} I_{DC} &= \frac{I_m}{\pi} [ -(-1) + 1 ] = \frac{I_m}{\pi} \cdot 2 \\ \Rightarrow I_{DC} &= \frac{2I_m}{\pi} \end{aligned}$$

## 2. Average DC Load Voltage ( $V_{DC}$ ):

$$\begin{aligned}
 V_{DC} &= \frac{1}{\pi} \int_0^{\pi} V_L d(\omega t) \\
 V_L &= V_m \sin \omega t \\
 V_{DC} &= \frac{1}{\pi} \int_0^{\pi} V_m \sin \omega t d(\omega t) \\
 &= \frac{1}{\pi} \int_0^{\pi} V_m \sin \omega t d(\omega t) \\
 &= \frac{V_m}{\pi} \int_0^{\pi} \sin \omega t d(\omega t) \\
 &= \frac{V_m}{\pi} [-\cos \omega t]_0^{\pi} \\
 &= \frac{V_m}{\pi} [-\cos \pi + \cos 0]
 \end{aligned}$$

Since  $\cos \pi = -1$  and  $\cos 0 = 1$ ,

$$V_{DC} = \frac{V_m}{\pi} \cdot 2 = \frac{2V_m}{\pi}$$

### Alternate Derivation:

$$V_{DC} = I_{DC} \times R_L = \frac{I_m}{\pi} R_L$$

Also, since:

$$I_{DC} = \frac{V_m}{\pi(R_L + R_S + R_f)}$$

Then:

$$V_{DC} = I_{DC} \cdot R_L = \frac{V_m}{\pi(R_L + R_S + R_f)} \cdot R_L$$

$$V_{DC} = \frac{V_m}{\pi \left( 1 + \frac{R_S + R_f}{R_L} \right)}$$

Since  $R_S + R_f \ll R_L$ , we approximate:

$$\frac{R_S + R_f}{R_L} \ll 1$$

Therefore:

$$V_{DC} = \frac{V_m}{\pi}$$

## 3. RMS Value of Load Current ( $I_{RMS}$ ):

$$\begin{aligned}
 I_{RMS} &= \sqrt{\frac{1}{\pi} \int_0^\pi I_L^2 d(\omega t)} \\
 I_L &= I_m \sin \omega t \\
 \Rightarrow I_{RMS} &= \sqrt{\frac{1}{\pi} \int_0^\pi I_m^2 \sin^2 \omega t d(\omega t)} \\
 &= \sqrt{\frac{I_m^2}{\pi} \int_0^\pi \frac{1 - \cos 2\omega t}{2} d(\omega t)} \\
 &= \sqrt{\frac{I_m^2}{2\pi} \left[ \omega t - \frac{\sin 2\omega t}{2} \right]_0^\pi}
 \end{aligned}$$

Since  $\sin 0 = \sin 2\pi = 0$ ,

$$\begin{aligned}
 I_{RMS} &= \sqrt{\frac{I_m^2}{2\pi} (\pi - 0)} = \sqrt{\frac{I_m^2 \pi}{2\pi}} \\
 &= \frac{I_m}{\sqrt{2}}
 \end{aligned}$$

#### 4. RMS Value of Load Voltage ( $V_{RMS}$ ):

$$\begin{aligned}
 V_{RMS} &= \sqrt{\frac{1}{\pi} \int_0^\pi V_L^2 d(\omega t)} \\
 V_L &= V_m \sin \omega t \\
 \Rightarrow V_{RMS} &= \sqrt{\frac{1}{\pi} \int_0^\pi V_m^2 \sin^2 \omega t d(\omega t)} \\
 &= \sqrt{\frac{V_m^2}{\pi} \int_0^\pi \frac{1 - \cos 2\omega t}{2} d(\omega t)} \\
 &= \sqrt{\frac{V_m^2}{2\pi} \left[ \omega t - \frac{\sin 2\omega t}{2} \right]_0^\pi}
 \end{aligned}$$

Since  $\sin 0 = \sin 2\pi = 0$ ,

$$\begin{aligned}
 V_{RMS} &= \sqrt{\frac{V_m^2}{2\pi} (\pi - 0)} = \sqrt{\frac{V_m^2 \pi}{2\pi}} \\
 &= \frac{V_m}{\sqrt{2}}
 \end{aligned}$$

#### 5. Ripple Factor ( $\gamma$ ):

The ripple factor is defined as the ratio of the RMS value of the AC component to the DC component of the output:

$$\gamma = \frac{I_{AC}}{I_{DC}} = \sqrt{\frac{I_{AC}^2}{I_{DC}^2}}$$

Since  $I_{AC}^2 = I_{RMS}^2 - I_{DC}^2$ ,

$$\Rightarrow \gamma = \sqrt{\frac{I_{RMS}^2 - I_{DC}^2}{I_{DC}^2}} = \sqrt{\frac{I_{RMS}^2}{I_{DC}^2} - 1}$$

Substituting:  $I_{RMS} = \frac{I_m}{\sqrt{2}}$ ,  $I_{DC} = \frac{2I_m}{\pi}$

$$\begin{aligned}\Rightarrow \gamma &= \sqrt{\frac{\left(\frac{I_m^2}{2}\right)}{\left(\frac{4I_m^2}{\pi^2}\right)} - 1} \\ &= \sqrt{\frac{\pi^2}{8} - 1} \\ &= \sqrt{1.2337 - 1} = \sqrt{0.2337} \approx 0.483 \\ \Rightarrow \% \gamma &= 48.3\%\end{aligned}$$

**Conclusion:** The ripple content in the output is 48.3% of the DC component, i.e.,  $I_{AC} < I_{DC}$ , hence it offers good rectification.

## 6. Efficiency ( $\eta$ ):

Efficiency is defined as the ratio of DC output power to AC input power:

$$\begin{aligned}\eta &= \frac{\text{Output DC Power}}{\text{Input AC Power}} = \frac{P_{DC}}{P_{AC}} \\ &= \frac{I_{DC}^2 R_L}{I_{RMS}^2 (R_S + 2R_f + R_L)}\end{aligned}$$

Substitute:  $I_{DC} = \frac{2I_m}{\pi}$ ,  $I_{RMS} = \frac{I_m}{\sqrt{2}}$

$$\begin{aligned}\Rightarrow \eta &= \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_S + 2R_f + R_L)} \\ &= \frac{\left(\frac{4I_m^2}{\pi^2}\right) R_L}{\left(\frac{I_m^2}{2}\right) (R_S + 2R_f + R_L)} \\ &= \frac{8}{\pi^2} \cdot \frac{R_L}{R_S + 2R_f + R_L}\end{aligned}$$

If  $\frac{R_S + 2R_f}{R_L} \ll 1$ ,  $\Rightarrow \frac{R_L}{R_S + 2R_f + R_L} \approx 1$

$$\begin{aligned}\Rightarrow \eta &\approx \frac{8}{\pi^2} \approx 0.812 \\ \Rightarrow \% \eta &\approx 81.2\%\end{aligned}$$

**Conclusion:** In a Full Wave Rectifier, ripple contents are lower, and hence, the efficiency is higher.

## Advantages of Full Wave Rectifier (FWR)

- DC load voltage and current are more than Half Wave Rectifier (HWR)
- Efficiency is high
- Provides large DC power output
- Ripple factor is less
- Widely used in regulated power supplies

## 1.7 Filter Circuits

The output from a half-wave or full-wave rectifier circuit isn't a pure direct current (DC); it contains unwanted fluctuations known as ripple. To reduce these ripples, filter circuits are introduced. These filters are placed between the rectifier and the load to help smooth the output is shown in Figure 1.17. Filter circuits are used at the output of rectifiers

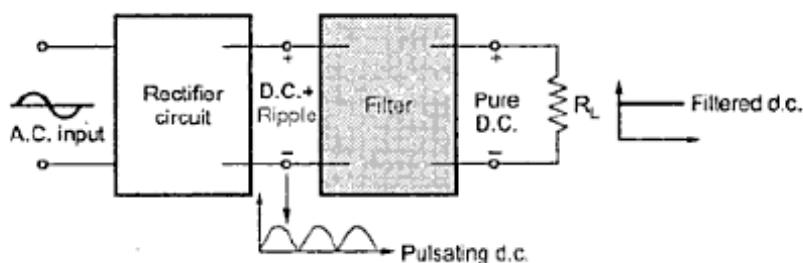


Figure 1.17: Filter Circuit

to obtain ripple-free DC voltage. They minimize the ripples in the output as much as possible. Two components used by the filter circuits are

- **Inductor Filter:** Blocks AC and allows DC to pass through. Hence, it is connected in series with the load.
- **Capacitor Filter:** Blocks DC and allows AC components to pass through. Hence, it is connected in parallel with the load.

The inductor filter is not in use now a days as inductors are bulky, costly, and consume more power, so they're not commonly used anymore.

## Bridge Rectifier with Capacitor Filter

- The capacitor charges to the peak value  $V_m$  during the diode conduction period and delivers this energy during the non-conduction period to the load  $R_L$ .
- Charging time of the capacitor must be small so that it quickly reaches the peak value. The discharging time must be large so that it slowly discharges until the next peak.

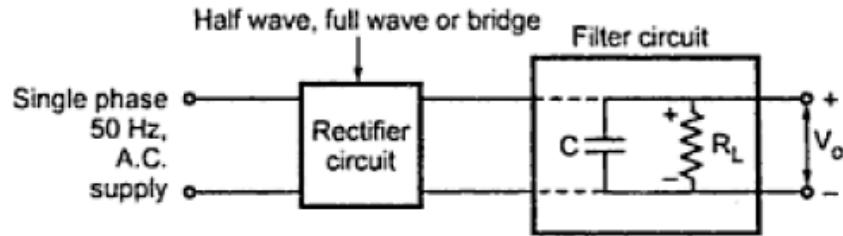


Figure 1.18: Capacitor Filter

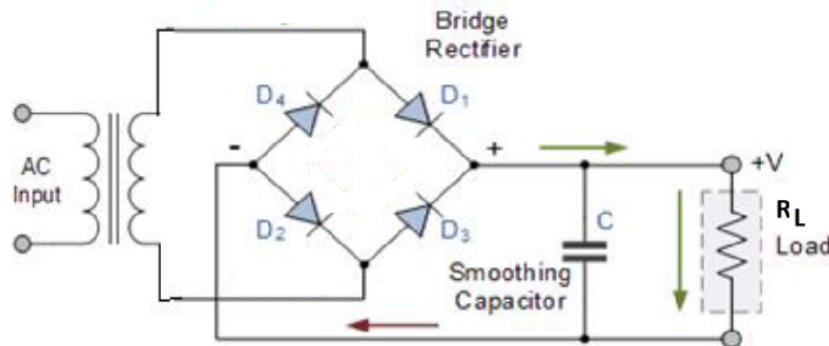


Figure 1.19: Capacitor Filter in Bridge Rectifier

- During the positive half cycle of the AC supply, diodes  $D_1$  and  $D_2$  conduct and charge the capacitor to the peak value  $V_m$ . They stop conducting when the transformer secondary voltage drops below  $V_m$ . This is because the capacitor voltage, which is the cathode voltage of diode becomes more positive than anode.
- So the capacitor then starts discharging through  $R_L$ , and the voltage across the capacitor falls gradually.
- The discharging of capacitor is decided by  $R_L C$  time constant which is very large and hence capacitor discharges very little from  $V_m$
- In the next positive half cycle, when the transformer secondary voltage, becomes more than the capacitor voltage, the diodes  $D_3$  and  $D_4$  becomes forward biased and charges the capacitor  $C$  back to  $V_m$
- Due to short charging time and long discharging time, the ripples in the output voltage are considerably reduced.

### Time Constants

$$\text{Charging time: } T_1 = 2R_f C$$

$$\text{Discharging time: } T_2 = R_L C$$

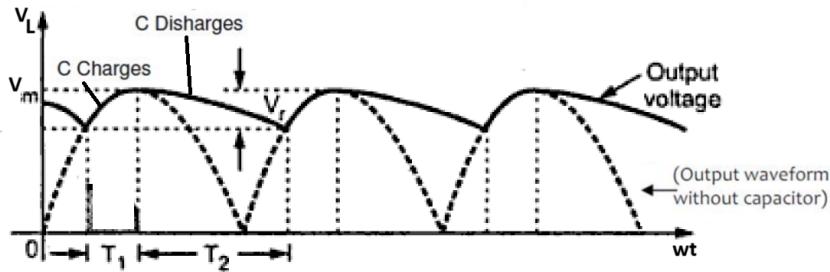


Figure 1.20: Bridge Rectifier with filter waveform

## Output Voltage Variation

- **Without filter:** 0 to  $V_m$
- **With filter:**  $(V_m - V_f)$  to  $V_m$

This indicates that the parallel combination of  $R_L$  and  $C$  significantly reduces the ripple content in the output voltage.

## Ripple Factor with Capacitor Filter

- For FWR:

$$\gamma = \frac{1}{4\sqrt{3}fCR_L}$$

By selecting a large value of  $C$ , the output can be made smoother, thereby reducing the ripple content.

## 1.8 Numerical on Rectifiers

1. A sinusoidal voltage of peak value 40V and frequency 50 Hz is applied to a HWR without filter. It has a load  $R_L = 800 \Omega$

Calculate:

- Peak, DC and RMS value of Load current
- DC output power
- AC input power
- Rectifier efficiency

**Solution:**

Given:  $V_m = 40 \text{ V}$ ,  $f = 50 \text{ Hz}$ ,  $R_L = 800 \Omega$ ,  $R_f = 8 \Omega$

- a) Peak value of the load current  $I_m$ :

$$I_m = \frac{V_m}{R_L + R_f} = \frac{40}{800 + 8} = 49.5 \text{ mA}$$

$$I_{DC} = \frac{I_m}{\pi} = \frac{49.5}{\pi} = 15.757 \text{ mA}$$

$$I_{rms} = \frac{I_m}{2} = \frac{49.5}{2} = 24.75 \text{ mA}$$

b) DC power to load,  $P_{DC}$ :

$$P_{DC} = I_{DC}^2 \cdot R_L = (15.75 \times 10^{-3})^2 \times 800 = 198.45 \text{ mW}$$

c) AC input power  $P_{AC}$ :

$$P_{AC} = I_{rms}^2 \cdot (R_L + R_f) = (24.75 \times 10^{-3})^2 \cdot 808 = 494.95 \text{ mW}$$

d) Efficiency  $\eta$ :

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{198.45}{494.95} = 0.4009$$

$$\% \eta = 40.09\%$$

2. An input to a HWR is  $v = 23 \sin 314t$ . If  $R_f = 50 \Omega$  and  $R_L = 500 \Omega$ , determine:

- DC load voltage
- RMS load voltage
- DC power delivered to the load
- Rectification efficiency

**Solution:**

Given:

$$v = V_m \sin \omega t = 23 \sin 314t, \quad R_f = 50 \Omega, \quad R_L = 500 \Omega$$

**DC Load Voltage:**

$$I_{DC} = \frac{I_m}{\pi}, \quad I_m = \frac{V_m}{R_L + R_f} = \frac{23}{50 + 500} = 41.81 \text{ mA}$$

$$I_{DC} = \frac{41.81 \text{ mA}}{\pi} = 13.31 \text{ mA}$$

$$V_{DC} = I_{DC} \times R_L = 13.31 \text{ mA} \times 500 = 6.65 \text{ V}$$

**RMS Load Voltage:**

$$I_{rms} = \frac{I_m}{2} = \frac{41.81 \text{ mA}}{2} = 20.90 \text{ mA}$$

$$V_{rms} = I_{rms} \times R_L = 20.90 \text{ mA} \times 500 = 10.45 \text{ V}$$

**DC Power Delivered to Load:**

$$P_{DC} = I_{DC}^2 \times R_L = (13.31 \times 10^{-3})^2 \times 500 = 88.57 \text{ mW}$$

**Rectification Efficiency:**

$$\eta = \frac{P_{DC}}{P_{AC}} = 0.3691$$

$$\% \eta = 36.91\%$$

3. In a full wave bridge rectifier, the transformer secondary voltage is

$$V_S = 100 \sin \omega t$$

The forward resistance of each diode is  $R_f = 25 \Omega$  and load resistance is  $R_L = 950 \Omega$ . Calculate:

- DC Output Voltage
- Ripple Factor
- Efficiency

**Solution:**

Given:

$$V_S = V_m \sin \omega t, \quad V_m = 100 \text{ V}, \quad R_f = 25 \Omega, \quad R_L = 950 \Omega$$

**1. DC Output Voltage:**

$$I_m = \frac{V_m}{2R_f + R_L} = \frac{100}{2 \times 25 + 950} = \frac{100}{1000} = 100 \text{ mA}$$

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2 \times 100 \text{ mA}}{\pi} = 63.66 \text{ mA}$$

$$V_{DC} = I_{DC} \times R_L = 63.66 \text{ mA} \times 950 = 60.478 \text{ V}$$

**2. Ripple Factor:**

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{100 \text{ mA}}{\sqrt{2}} = 70.71 \text{ mA}$$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{70.71}{63.66}\right)^2 - 1} = \sqrt{1.233 - 1} = \sqrt{0.2337} = 0.4834$$

$$\% \gamma = 48.34\%$$

### 3. Efficiency:

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 \times R_L}{I_{rms}^2 \times (2R_f + R_L)}$$

$$\eta = \frac{(63.66 \times 10^{-3})^2 \times 950}{(70.71 \times 10^{-3})^2 \times 1000} = \frac{3.85}{5} = 0.77$$

$$\eta = 77\%$$

4. A bridge rectifier uses 4 diodes with an RMS input voltage of 110 V. The forward resistance of each diode is  $25\Omega$ , and the load resistance is  $R_L = 1\text{k}\Omega$ . Find:

- Maximum value of current
- DC value of current through the load
- DC load voltage

#### Solution:

Given:

$$V_{rms} = 110\text{ V}, \quad R_f = 25\Omega, \quad R_L = 1000\Omega$$

#### 1. Find $V_m$ :

$$V_{rms} = \frac{V_m}{\sqrt{2}} \Rightarrow V_m = V_{rms} \times \sqrt{2} = 110 \times \sqrt{2} = 155.56\text{ V}$$

#### 2. Maximum value of current $I_m$ :

$$I_m = \frac{V_m}{2R_f + R_L} = \frac{155.56}{2 \times 25 + 1000} = \frac{155.56}{1050} = 148.15\text{ mA}$$

#### 3. DC value of current:

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2 \times 148.15\text{ mA}}{\pi} = 94.36\text{ mA}$$

#### 4. DC load voltage:

$$V_{DC} = I_{DC} \times R_L = 94.36\text{ mA} \times 1000 = 94.36\text{ V}$$

5. Determine the ripple factor of a bridge rectifier using a capacitor filter. The load used is  $2\text{k}\Omega$  and DC output voltage is 12 V. Assume supply frequency of 50 Hz and ideal diodes. A capacitor of  $100\mu\text{F}$  is used in the filter circuit.

#### Solution:

Given:

$$R_L = 2\text{k}\Omega, \quad V_{DC} = 12\text{ V}, \quad f = 50\text{ Hz}, \quad C = 100\mu\text{F}$$

Ripple factor for bridge rectifier with capacitor filter:

$$\gamma = \frac{1}{4\sqrt{3}fCR_L}$$

Substituting the values:

$$\gamma = \frac{1}{4\sqrt{3} \times 50 \times 2 \times 10^3 \times 100 \times 10^{-6}} = \frac{1}{69.28}$$

$$\gamma = 0.0144 \Rightarrow \% \gamma = 1.44\%$$

6. Calculate the value of capacitor  $C$  that has to be used for the filter of a bridge rectifier to get a ripple factor of 0.01. The rectifier supplies current to a load of  $2\text{k}\Omega$  and the supply frequency is 50 Hz.

**Solution:**

Given:

$$\gamma = 0.01, R_L = 2\text{k}\Omega, f = 50\text{Hz}$$

$$\gamma = \frac{1}{4\sqrt{3}fCR_L} \Rightarrow C = \frac{1}{4\sqrt{3}fR_L\gamma}$$

Substituting the values:

$$C = \frac{1}{4\sqrt{3} \times 50 \times 2 \times 10^3 \times 0.01} = \frac{1}{6928.203} = 1.443 \times 10^{-4} \text{F}$$

$$C = 144.3 \mu\text{F}$$

## 1.9 Zener Diode

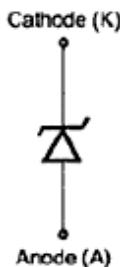


Figure 1.21: Zener Diode Symbol

- Zener diode is a special purpose diode; it is heavily doped compared to a junction diode.
- Zener diodes are designed for operation in the reverse breakdown region.
- The zener diodes have breakdown voltage range from 3 V to 200 V.

### 1.9.1 VI Characteristics of Zener Diode

The forward and reverse biasing of the zener diode is shown in the Figure 1.22. The VI characteristics of the Zener diode is shown in Figure 1.23

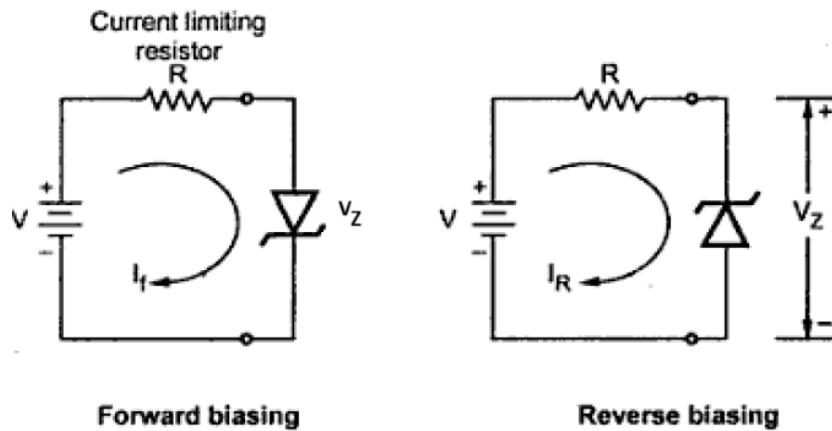


Figure 1.22: Forward and Reverse biasing of the Zener diode

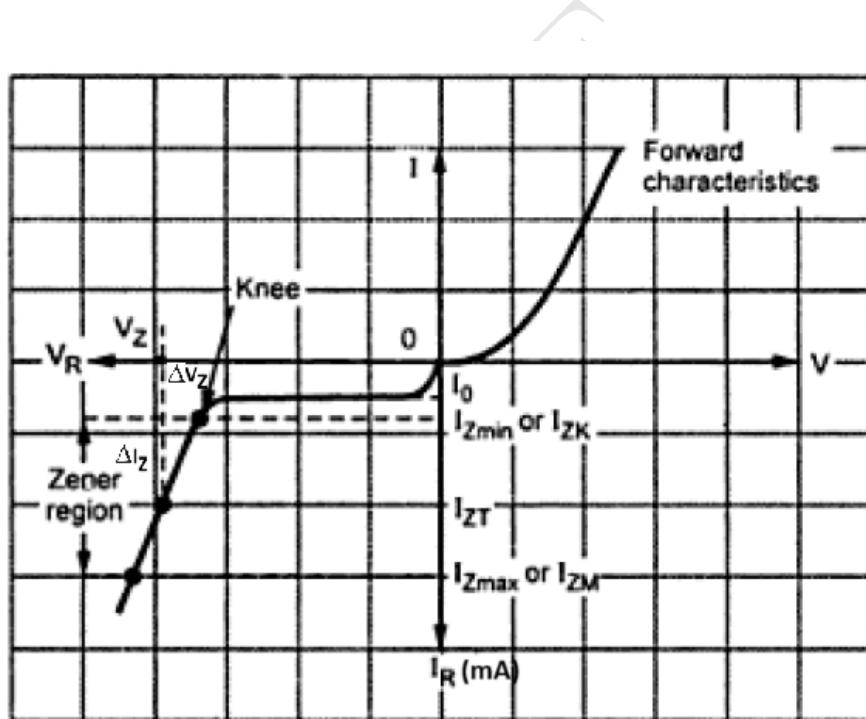


Figure 1.23: VI Characteristics of the Zener diode

- In the forward biased condition, As long as forward voltage is less than barrier voltage, the current flowing is very small. As it increases beyond this voltage the depletion region becomes very thin and current increases suddenly. This increase in the current is exponential as shown in the Fig. 1.23.
- When a narrow junction with a narrow depletion region is applied with a high reverse voltage, due to the high electric field, electrons break away from the atoms.

Hence, electron hole pairs are generated in large numbers and a sudden increase of current is observed. This ionization by electric field is known as **Zener breakdown**.

- When a junction diode is reverse biased, there is normally a small amount of reverse saturation current due to the minority charge carriers till the reverse voltage applied is less than the reverse breakdown voltage.
- When the reverse voltage is sufficiently increased, the junction breaks down and a large reverse current flows but the voltage across it remains almost constant.
- Under this condition, the diode may be continuously operated in reverse breakdown.
- Every zener diode has a capacity to carry current. As current increases, the power dissipation  $P_Z$  increases. If this dissipation increases beyond a certain value, the diode may get damaged.
- If the reverse current is limited by means of a suitably connected series resistor, the power dissipation in the diode can be kept to a level that will not destroy the device.
- This property of breakdown may be useful in applications such as a voltage reference source or voltage regulator.

## Zener Parameters

- **Zener Breakdown Voltage ( $V_Z$ ):**

It is the voltage beyond which there is a sharp increase in current for a small change in reverse voltage. It is the voltage across the Zener diode in the breakdown region.

- **Reverse Knee Current ( $I_{ZK}$ ):**

It is the Zener current corresponding to the knee region of the V-I characteristics.

- **Maximum Zener Current ( $I_{ZM}$ ):**

It is the maximum Zener current that can pass through the diode without damaging the device.

- **Zener Test Current ( $I_{ZT}$ ):**

It is the standard test current used for checking the working condition of a Zener diode.

- **Dynamic Resistance ( $r_Z$ ):**

It is the ratio of the change in reverse voltage to the corresponding change in reverse current beyond the knee region.

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

- **Maximum Power Dissipation ( $P_D$ ):**

It is given by the product of the Zener breakdown voltage and the maximum Zener current:

$$P_D = V_Z \times I_{Z\_max}$$

**Note:** Many low power Zener diodes have a test current specified as  $I_{ZT} = 20 \text{ mA}$ .

### 1.9.2 Zener diode as a Voltage Regulator

- Voltage regulators are devices used to maintain constant voltage across a load irrespective of fluctuations in the input voltage and load currents.
- After rectification, the voltage is pulsating DC with ripples those are unwanted fluctuations.
- A filter circuit helps smoothen this, reducing ripple. But it doesn't completely eliminate it, so the result is unregulated DC.
- To achieve smooth and stable output, a regulator circuit is added after the filter. It:
  - Minimizes remaining ripple,
  - Keeps the output voltage constant even if input voltage or load conditions change.
- The output of the regulator is called DC supply.
- Zener diodes are widely used as voltage regulators to regulate the voltage across small loads.
- Zener diodes have a sharp reverse breakdown voltage, which remains nearly constant over a wide range of currents.
- They can produce a stabilized output voltage with low ripple under varying load current conditions.

#### Working:

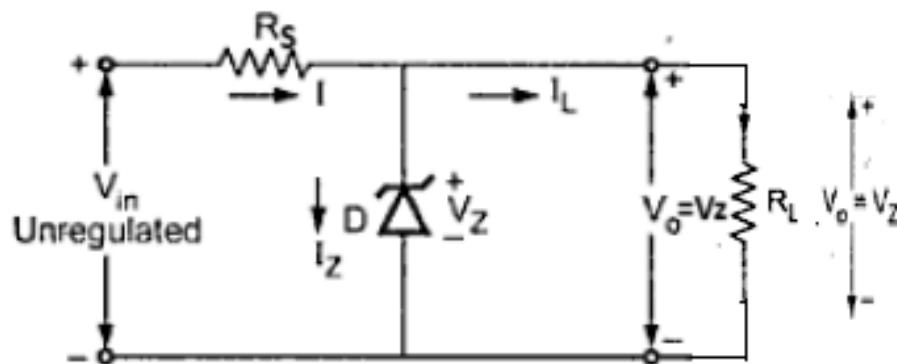


Figure 1.24: Zener Voltage Regulator

- The Zener diode is connected with its cathode terminal to the positive terminal of the DC supply, hence it is reverse biased and operates in breakdown region. The large current flows through the zener diode. Under this condition the voltage across the zener is constant and is equal to  $V_z$ .

- A resistor  $R_s$  is connected in series with the Zener diode to limit the maximum current in the circuit.
- As the voltage across the zener diode remains constant, equal to  $V_Z$ , it is connected across the load, and hence the load voltage  $V_o$  is equal to the zener voltage  $V_Z$ .
- Zener current must remain above  $I_{Z(min)}$  for voltage stabilization.
- $I_{Z(max)}$  depends on the Zener's power rating.

### Case 1: No Load Condition ( $I_L = 0$ )

- The load current is zero, so the entire current flows through the Zener diode ( $I = I_Z$ )

$$I = \frac{V_{in} - V_Z}{R_S} = I_z$$

- The diode dissipates maximum power.
- $R_s$  must be chosen to keep power dissipation within safe limits.

### Case 2: With Load Condition ( $I_L \neq 0$ )

#### 1. Regulation with Varying line voltage:

- Load  $R_L$  is connected in parallel with the Zener diode.
- The voltage across  $R_L$  is equal to Zener voltage.

$$V_o = V_Z \text{ is constant.}$$

$$\therefore I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \text{constant}$$

And

$$I = \frac{V_{in} - V_Z}{R_S} = I_Z + I_L$$

- Now if  $V_{in}$  increases, then the total current  $I$  increases. But  $I_L$  is constant as  $V_Z$  is constant. Hence, the current  $I_Z$  increases to keep  $I_L$  constant.
- But as long as  $I_Z$  is between  $I_{Z\min}$  and  $I_{Z\max}$ , the  $V_Z$ , i.e., output voltage  $V_o$ , is constant. Thus, the changes in input voltage get compensated and the output is maintained constant.
- Similarly, if  $V_{in}$  decreases, then current  $I$  decreases. But to keep  $I_L$  constant,  $I_Z$  decreases. As long as  $I_Z$  is between  $I_{Z\max}$  and  $I_{Z\min}$ , the output voltage remains constant.

Key Note:

#### 2. Regulation with Varying Load:

$V_{in}$ increases	$\rightarrow I = I_L + I_Z \rightarrow I_L$ is constant ( $V_Z/R_L$ )	$\rightarrow$ So $I_Z$ increases ( $I_Z = I - I_L$ )	$\rightarrow$ As long $I_Z < I_{Z_{max}}$ , $V_Z$ is constant i.e. output voltage is constant
$V_{in}$ decreases	$\rightarrow I = I_L + I_Z \rightarrow I_L$ is constant ( $V_Z/R_L$ )	$\rightarrow$ So $I_Z$ decreases ( $I_Z = I - I_L$ )	$\rightarrow$ As long $I_Z > I_{Z_{min}}$ , $V_Z$ is constant i.e. output voltage is constant

- The input voltage  $V_{in}$  is constant, and the output voltage  $V_o$  across the load is also constant due to the Zener diode maintaining a fixed voltage  $V_Z$ . Assuming the series resistance  $R_s$  is constant, the total current  $I$  through  $R_s$  remains constant.

$$I = \frac{V_{in} - V_Z}{R_S} \quad (\text{constant}) = I_L + I_Z$$

Where:

- $I$  is the total current through the resistor  $R_s$
- $I_L$  is the load current through  $R_L$
- $I_Z$  is the current through the Zener diode

- As the **load resistance  $R_L$  decreases**, the load current  $I_L$  increases. The voltage  $V_Z$  is constant. Hence, the current  $I_Z$  decreases to keep  $I$  constant.
- But as long as  $I_Z$  is between  $I_{Z_{min}}$  and  $I_{Z_{max}}$ , the  $V_Z$ , i.e., output voltage  $V_o$ , is constant. Thus, the changes in input voltage get compensated and the output is maintained constant.
- Similarly, if the **load resistance  $R_L$  increases**, the load current  $I_L$  decreases. The voltage  $V_Z$  is constant. Hence, the current  $I_Z$  increases to keep  $I$  constant. As long as  $I_Z$  is between  $I_{Z_{max}}$  and  $I_{Z_{min}}$ , the output voltage remains constant.

Key Note:

$R_L$ increases $I_L$ decreases	$\rightarrow I = \frac{V_{in} - V_Z}{R}$ constant	$\rightarrow I_Z = I - I_L$ increases	$\rightarrow$ As long $I_Z < I_{Z_{max}}$ , $V_Z$ is constant i.e. output voltage is constant.
$R_L$ decreases $I_L$ increases	$\rightarrow I = \frac{V_{in} - V_Z}{R}$ constant	$\rightarrow I_Z = I - I_L$ decreases	$\rightarrow$ As long $I_Z > I_{Z_{min}}$ , $V_Z$ is constant i.e. output voltage is constant.

## 1.10 Numerical on Zener Diode

- A 24 V, 600 mW zener diode is used for providing a 24 V stabilized supply to a variable load from a 32 V supply. Calculate:
  - Value of series resistance required
  - Zener current when the load is 1200  $\Omega$

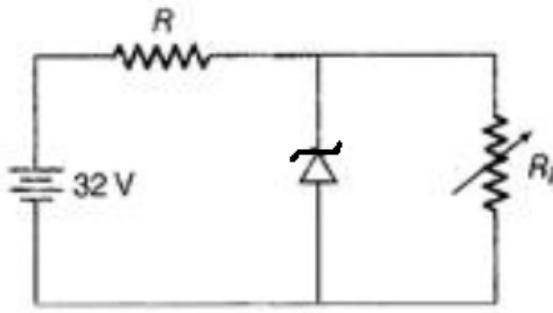


Figure 1.25: Problem 1

**Given:**

$$V_Z = 24 \text{ V}$$

$$P_Z = 600 \text{ mW} = 0.6 \text{ W}$$

$$V_S = 32 \text{ V}$$

**(i) Value of Series Resistance  $R_S$** 

When the load is disconnected ( $R_L = \infty$ ), i.e.,  $I_L = 0$ , then:

$$I_s = I_Z + I_L = I_Z + 0 = I_{Z\max}$$

$$I_{Z\max} = \frac{P_Z}{V_Z} = \frac{600 \times 10^{-3}}{24} = 25 \text{ mA}$$

Applying KVL:

$$V_S - I_S R_S - V_Z = 0$$

Substituting values:

$$32 - (25 \times 10^{-3})R_S - 24 = 0 \Rightarrow R_S = \frac{32 - 24}{25 \times 10^{-3}} = \frac{8}{0.025} = 320 \Omega$$

**Therefore, the value of series resistance is  $R_S = 320 \Omega$ .**

**(ii) Zener Current when Load is  $R_L = 1200 \Omega$** 

We know:

$$V_Z = V_O = V_L = I_L \cdot R_L \Rightarrow I_L = \frac{V_Z}{R_L} = \frac{24}{1200} = 0.02 \text{ A} = 20 \text{ mA}$$

**Load current is  $I_L = 20 \text{ mA}$ .**

Now,

$$I_Z = I_S - I_L = 25 \text{ mA} - 20 \text{ mA} = 5 \text{ mA}$$

**Therefore, the zener current when the load is  $1200 \Omega$  is  $I_Z = 5 \text{ mA}$ .**

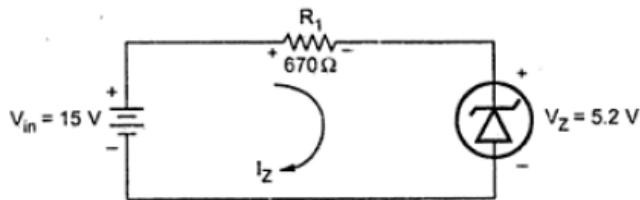


Figure 1.26: Problem 2

2. For the circuit shown, calculate the zener diode current and the power dissipation.

**Given:**

$$V_{in} = 15 \text{ V}$$

$$V_Z = 5.2 \text{ V}$$

$$R_1 = 670 \Omega$$

**Solution:** Applying KVL,

$$-I_Z R_1 - V_Z + V_{in} = 0$$

$$\Rightarrow I_Z = \frac{V_{in} - V_Z}{R_1} = \frac{15 - 5.2}{670} = 14.6268 \text{ mA}$$

**Power Dissipation:**

$$P_D = V_Z \cdot I_Z = 5.2 \times 14.6268 \times 10^{-3} = 76.059 \text{ mW}$$

**Answer:**

Zener current  $I_Z = 14.6268 \text{ mA}$

Power dissipation  $P_D = 76.059 \text{ mW}$

3. A circuit has a zener diode connected across the load with the following details. Find the source current  $I$ , the load current  $I_L$ , and the zener power dissipation  $P_Z$ .

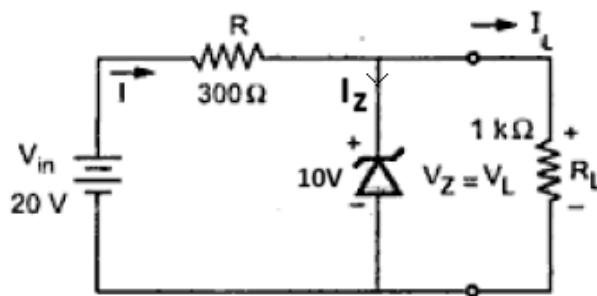


Figure 1.27: Problem 3

**Given:**

- Source voltage,  $V_{in} = 20 \text{ V}$
- Series resistance,  $R = 200 \Omega$
- Zener voltage,  $V_Z = 10 \text{ V}$
- Load resistance,  $R_L = 1 \text{ k}\Omega = 1000 \Omega$

**To find:**  $I$ ,  $I_L$ , and zener power dissipation  $P_Z$

## Solution

Applying KVL to the input loop:

$$V_{in} - IR_S - V_Z = 0$$

$$20 - I \cdot 200 - 10 = 0 \Rightarrow I = \frac{20 - 10}{200} = \frac{10}{200} = 0.05 \text{ A} = 50 \text{ mA}$$

**Load current:**

$$V_L = V_O = I_L R_L = V_Z \Rightarrow I_L = \frac{V_Z}{R_L} = \frac{10}{1000} = 0.01 \text{ A} = 10 \text{ mA}$$

**Power dissipation across Zener:**

$$P_Z = V_Z \cdot I_{Zmax} = 10 \cdot 40 \times 10^{-3} = 400 \text{ mW}$$

4. In the circuit shown in Figure 1.28 determine,
- the load current
  - the zener current
  - power dissipated in zener diode

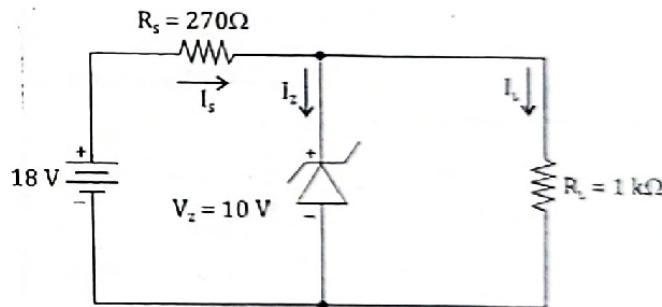


Figure 1.28: Problem 4

## Solution

**Given:**  $V_i = 18 \text{ V}$ ,  $R_S = 270 \Omega$   
 $V_z = 10 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

**Source Current:**

$$I_S = \frac{V_i - V_z}{R_S} = \frac{18 - 10}{270} = 29.62 \text{ mA}$$

(a) **Load current**

$$I_L = \frac{V_z}{R_L} = \frac{10}{1 \times 10^3} = 10 \text{ mA}$$

(b) **Zener current**

$$I_S = I_Z + I_L \Rightarrow I_Z = I_S - I_L$$

$$I_Z = 29.62 \times 10^{-3} - 10 \times 10^{-3} = 19.62 \text{ mA}$$

(c) **Power dissipated in zener diode**

$$P_Z = V_Z \cdot I_Z = 10 \times 19.62 \times 10^{-3} = 196.2 \text{ mW}$$

# Chapter 2

## Transistors and their Applications

### 2.1 Introduction of Bipolar junction transistors (BJT)

- BJT is a three-terminal device constructed using doped semiconductor materials.
- It is mainly used in amplifying and switching applications.
- It is called **bipolar** because both holes and electrons take part in the conduction of current.
- The three terminals of a BJT are:
  - E: Emitter
  - B: Base
  - C: Collector
- Two junctions present in a BJT are:
  - B-E junction (Base-Emitter)
  - C-B junction (Collector-Base)

### Types of Transistors

1. **NPN transistor:** A P-type semiconductor material is sandwiched between two N-type materials.
2. **PNP transistor:** An N-type semiconductor material is sandwiched between two P-type materials.

Junction representations of NPN and PNP transistors with terminals can be illustrated in Figure 2.1 using circuit diagrams or symbolic representations.

- **Emitter:** It is highly doped and is the supplier of electrons (in NPN transistor).
- **Base:** It is thin and lightly doped.
- **Collector:** It is moderately doped and large in size. It collects the electrons emitted by the emitter (in NPN transistor).

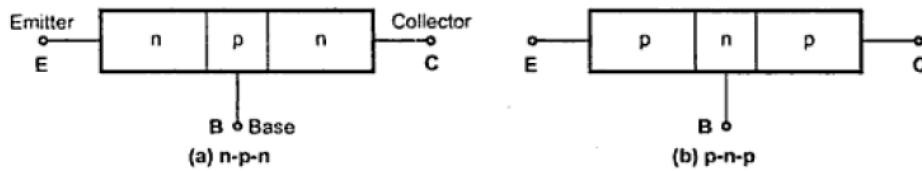


Figure 2.1: Types of Transistor

**Transistor symbols:**

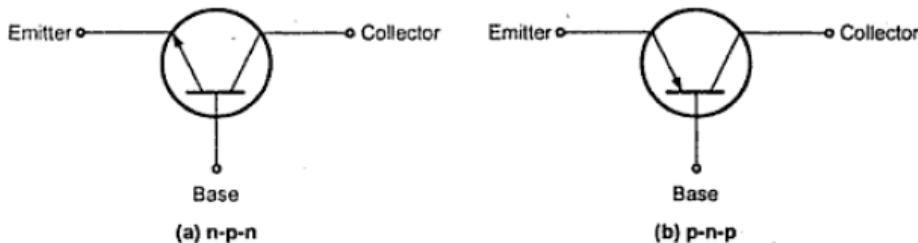


Figure 2.2: Transistor Symbols

- The arrow indicates the emitter terminal of the transistor. It also indicates the connectional direction for the current flow (P to N).
- In NPN transistor the arrowhead points outwards from base to emitter.
- In PNP transistor the arrowhead points inwards for emitter towards the base.

### 2.1.1 NPN Transistor Operation

#### Unbiased Transistor

An unbiased transistor means a transistor with no external voltage (biasing) is applied. There will be no current flowing from any of the transistor leads. Since a transistor is like two pn junction diodes connected back to back, there are depletion regions at both the junctions, emitter junction and collector junction, as shown in the Figure 2.3.

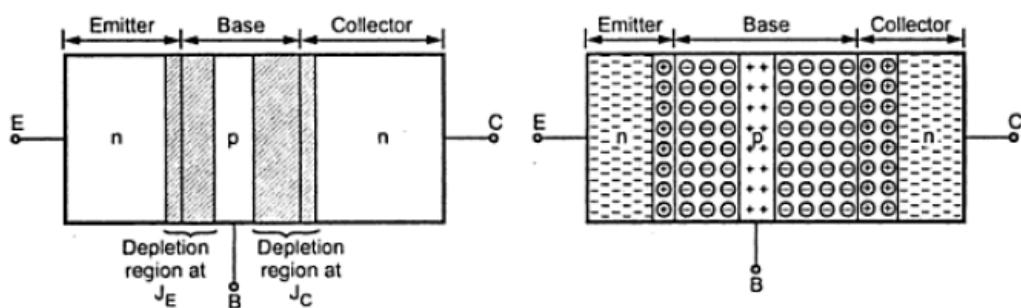


Figure 2.3: Unbiased Transistor

During diffusion process, depletion region penetrates more deeply into the lightly doped side in order to include an equal number of impurity atoms in each side of the

junction. As shown in the Figure 2.3, depletion region at emitter junction penetrates less in the heavily doped emitter and extends more in the base region. Similarly, depletion region at collector junction penetrates less in the heavily doped collector and extends more in the base region. As collector is slightly less doped than the emitter, the depletion layer width at the collector junction is more than the depletion layer width at the emitter junction.

## Operation of NPN Transistor with Biasing

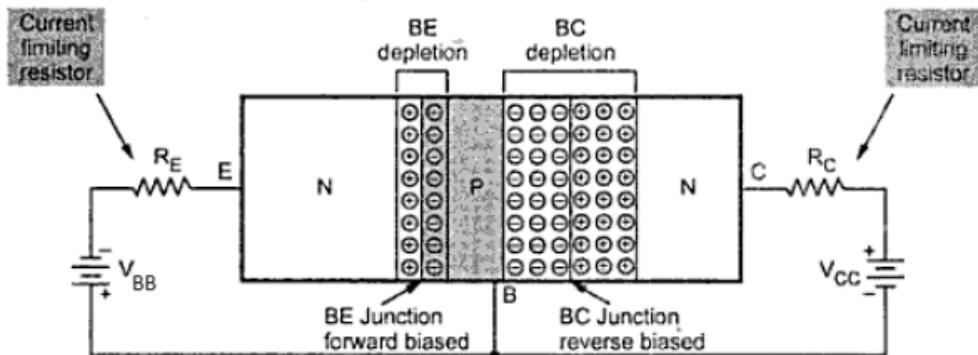


Figure 2.4: Biased Transistor

- Emitter and collector are heavily doped, whereas the base is lightly doped.
- The figure shows an NPN transistor with external bias voltages applied.
- The emitter-base (E-B) junction is forward biased by an external DC source. This reduces the barrier voltage and causes electrons in the N-type emitter to flow toward the P-type base. As a result, the depletion region at the E-B junction becomes narrow.  
(Electrons are emitted into the base region, hence the name **emitter**, and the resulting current is called **emitter current  $I_E$** .)
- The collector-base (C-B) junction is reverse biased by the external DC source. This increases the barrier voltage and widens the C-B depletion region.
- Electrons flow from the emitter through the P-type base and combine with holes in the base. Since the base region is thin and lightly doped, only a few electrons recombine with holes to form the **base current  $I_B$** .
- The remaining electrons reach the C-B depletion region and are drawn across the junction by the external DC bias supply. These electrons are collected in the collector region, giving rise to the **collector current  $I_C$** .
- Thus, electron current is dominant in an NPN transistor.
- Since approximately 98% of the electrons from the emitter flow into the collector circuit and only a few recombine in the base, the base current is small and the collector current is large.

## 2.1.2 BJT Voltages and Currents (NPN)

### Terminal Voltages

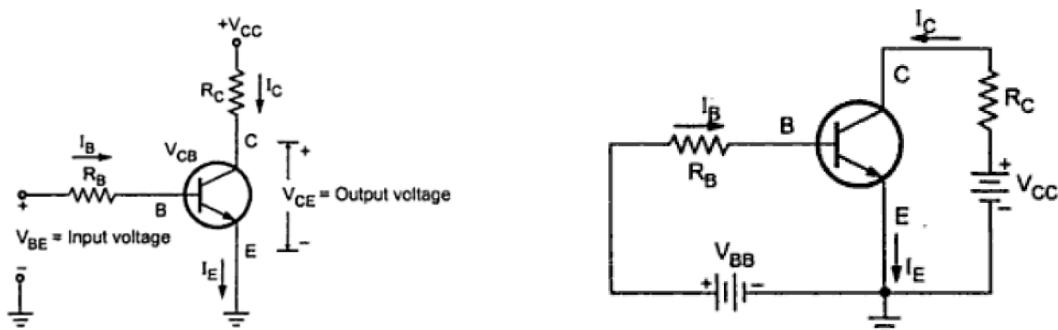


Figure 2.5: Transistor Currents and Voltages

- The direction of the arrowhead indicates the conventional current direction.
- For an NPN transistor, the base is biased with a positive voltage with respect to the emitter.
- The collector is biased with a higher positive voltage than the base.
- In the figure,  $V_{BB}$  is the base bias voltage connected through  $R_B$ , and the collector supply  $V_{CC}$  is connected through  $R_C$ .
- The negative terminals of both sources are connected to the emitter terminal.
- To ensure the collector-base junction is reverse biased,  $V_{CC} > V_{BB}$  (i.e., positive on collector and negative on base).

#### Note:

- Typical base-emitter voltages: 0.3 V for germanium, 0.7 V for silicon.
- Typical collector voltages: 3 V to 20 V.

## Transistor Currents (NPN)

- For an NPN transistor,  $I_B$  and  $I_C$  flow into the device (conventional current), and  $I_E$  flows out.
  - The current relationship is:
- $$I_E = I_B + I_C$$
- Electrons are the majority carriers and move opposite to the conventional current direction.
  - Low-power transistors:  $I_C = 1 \text{ mA}$  to  $20 \text{ mA}$ .

- High-power transistors:  $I_C = 100 \text{ mA}$  to several amperes.

Nearly 96% to 99% of  $I_E$  flows across the collector-base junction to become collector current  $I_C$ .

- **Common-base current gain:**

$$I_C = \alpha I_E$$

Where,  $\alpha$  is the **emitter to collector current gain**. It is also referred to as **common base current gain**. It is the ratio of collector current to emitter current,

$$\alpha = \frac{I_C}{I_E}, \quad \text{typically } \alpha \in [0.96 \text{ to } 0.99]$$

Hence, the collector current is almost equal to emitter current. In many circuits, it is assumed that  $I_C \approx I_E$ .

**Leakage current:** Since CB junction is reverse biased, very small **reverse saturation current**  $I_{CBO}$  flows across the junction. It is known as collector to base leakage current.

- **Common-emitter current gain:**

$$I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_B}, \quad \text{typically } \beta \in [25 \text{ to } 300]$$

Where,  $\beta$  is the base to collector current gain. It is also referred to as **common emitter current gain**. It is the ratio of collector to base current.

### 2.1.3 Relation between $\alpha$ and $\beta$ :

$$I_E = I_C + I_B \quad (1)$$

and

$$\alpha = \frac{I_C}{I_E}, \quad \beta = \frac{I_C}{I_B}$$

$$I_C = \alpha I_E \quad (2)$$

Substituting 1 in 2,

$$I_C = \alpha(I_C + I_B)$$

$$I_C - \alpha I_C = \alpha I_B$$

$$I_C(1 - \alpha) = \alpha I_B$$

$$\frac{I_C}{I_B} = \frac{\alpha}{1 - \alpha}$$

$$\therefore \beta = \frac{\alpha}{1 - \alpha}$$

Also,

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\text{or } \beta(1 - \alpha) = \alpha$$

$$\beta - \beta\alpha = \alpha$$

$$\beta = \alpha + \beta\alpha$$

$$= (1 + \beta)\alpha$$

$$\therefore \alpha = \frac{\beta}{1 + \beta}$$

## 2.2 Numerical on Transistor Currents and Current Gain

- Calculate  $I_C$  and  $I_E$  for a transistor that has  $\alpha = 0.98$  and  $I_B = 100 \mu\text{A}$ . Determine the value of  $\beta$  for the transistor.

**Solution:**

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = \frac{0.98}{0.02} = 49$$

$$I_C = \beta \cdot I_B = 49 \times 100 \times 10^{-6} = 4.9 \text{ mA}$$

$$I_E = I_C + I_B = 4.9 \text{ mA} + 0.1 \text{ mA} = 5 \text{ mA}$$

- Calculate  $\alpha$  and  $\beta$  for  $I_C = 1 \text{ mA}$  and  $I_B = 25 \mu\text{A}$ . Determine new  $I_B$  for  $I_C = 5 \text{ mA}$ .

**Solution:**

$$\beta = \frac{I_C}{I_B} = \frac{1 \text{ mA}}{25 \mu\text{A}} = 40$$

$$I_E = I_C + I_B = 1.025 \text{ mA}$$

$$\alpha = \frac{I_C}{I_E} = \frac{1}{1.025} \approx 0.976$$

$$I_{B_{\text{new}}} = \frac{I_C}{\beta} = \frac{5 \text{ mA}}{40} = 125 \mu\text{A}$$

- Determine  $\beta$  and  $I_E$  for  $I_B = 50 \mu\text{A}$  and  $I_C = 3.65 \text{ mA}$ .

**Solution:**

$$I_E = I_C + I_B = 3.65 \text{ mA} + 0.05 \text{ mA} = 3.70 \text{ mA}$$

$$\beta = \frac{I_C}{I_B} = \frac{3.65}{0.05} = 73$$

- Given  $I_C = 3 \text{ mA}$  and  $I_E = 3.03 \text{ mA}$ , find  $\beta$ . Determine new  $I_C$  if  $\beta = 70$ .

**Solution:**

$$I_B = I_E - I_C = 3.03 \text{ mA} - 3 \text{ mA} = 0.03 \text{ mA} = 30 \mu\text{A}$$

$$\beta = \frac{I_C}{I_B} = \frac{3}{0.03} = 100$$

$$I_{C_{\text{new}}} = \beta \cdot I_B = 70 \times 30 \times 10^{-6} = 2.1 \text{ mA}$$

5. Find  $I_C$  and  $I_E$  for  $\alpha = 0.99$  and  $I_B = 20 \mu\text{A}$ .

**Solution:**

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.99}{0.01} = 99$$

$$I_C = \beta \cdot I_B = 99 \times 20 \times 10^{-6} = 1.98 \text{ mA}$$

$$I_E = I_C + I_B = 1.98 \text{ mA} + 0.02 \text{ mA} = 2 \text{ mA}$$

## 2.3 Transistor Characteristics

The graphs showing the relationship between different currents and voltages of a transistor are known as the **characteristics** of the transistor.

### Types of Characteristics

- Input Characteristics
- Output Characteristics

Any transistor circuit can be designed using three types of configurations, based on the connection of transistor terminals:

- Common Emitter Configuration (CE)
- Common Base Configuration (CB)
- Common Collector Configuration (CC)

Each configuration has its own characteristic curves.

#### 2.3.1 Common Emitter Configuration (NPN)

In this configuration, the emitter terminal is common to both input and output terminals as shown in Figure 2.6.

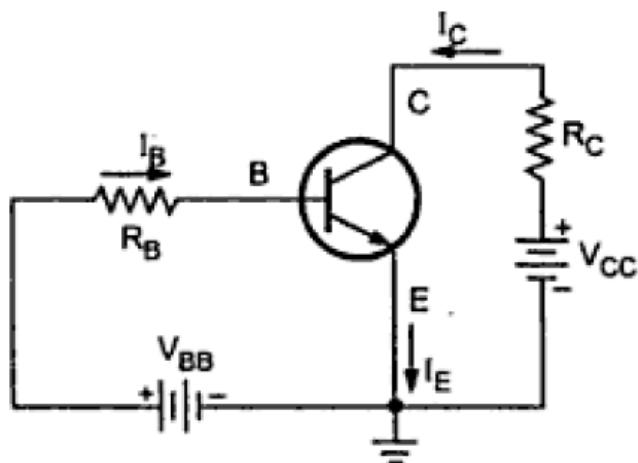


Figure 2.6: CE Configuration of NPN transistors

- Input is applied between the base-emitter (B-E) terminals, and output is taken between collector-emitter (C-E) terminals.
- This configuration is widely used as an inverting amplifier.
- It introduces a phase shift of  $180^\circ$  at the output.
- The B-E junction is forward biased and the C-B junction is reverse biased using supplies  $V_{BB}$  and  $V_{CC}$ .
- The negative terminal of  $V_{BB}$  repels electrons in the emitter, causing current to flow from emitter to base and then to collector.
- Input current:  $I_B$ , Output current:  $I_C$ , and  $I_E = I_B + I_C$

## Input Characteristics

Input characteristics are obtained by plotting input current  $I_B$  versus input voltage  $V_{BE}$  at constant output voltage  $V_{CE}$ .

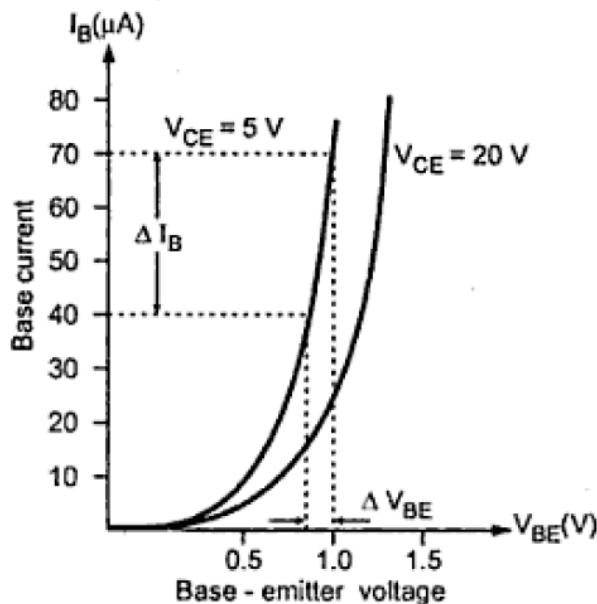


Figure 2.7: Input Characteristics of CE Configuration

- When  $V_{CE}$  is constant, after the cut-in voltage, the base current ( $I_B$ ) increases rapidly with a small increase in the  $V_{BE}$ . This means that dynamic input resistance is small in the CE configuration.
- Dynamic input resistance is defined as the ratio of change in base-emitter voltage to change in base current at constant  $V_{CE}$ :

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad (\text{with } V_{CE} \text{ constant})$$

- For a fixed value  $V_{BE}$ ,  $I_B$  decreases as  $V_{CE}$  is increased. A larger value of  $V_{CE}$  results in a large reverse bias at collector-base PN junction. This increases the

depletion region and reduces the effective width of the base. Hence, there are fewer recombinations in the base region, reducing the base current  $I_B$ .

- This shifts the input characteristic curves to the right.

## Output Characteristics

Output characteristics are obtained by plotting output current  $I_C$  versus output voltage  $V_{CE}$  at constant input current  $I_B$ .

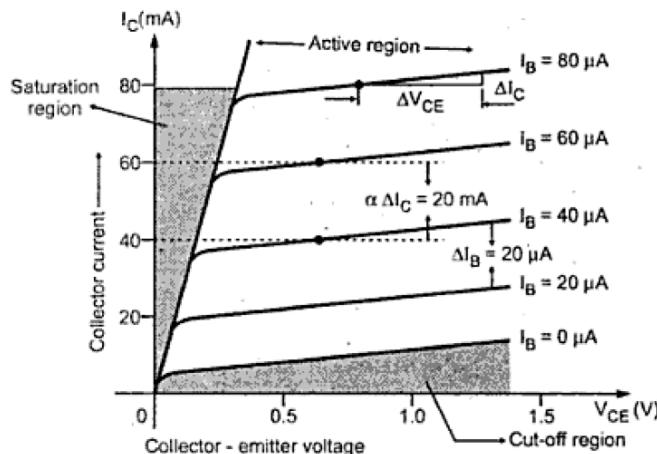


Figure 2.8: Output Characteristics of CE Configuration

- Even with constant  $I_B$ ,  $I_C$  increases slightly with  $V_{CE}$ , making the slope.
- If  $V_{CE}$  exceeds a certain limit, the C-B junction breaks down, causing  $I_C$  to rise rapidly—this is the **breakdown region**.
- For the fixed value of  $V_{CE}$ , the ratio of small change in  $I_c$ ,  $\Delta I_C$  to small change in  $I_B$ ,  $\Delta I_B$ , then  $\beta$  is:

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

- From the output characteristics, the change in collector emitter voltage(  $\Delta V_{CE}$ ) causes little change in the collector current( $\Delta I_C$ ) for constant base current  $I_B$ . Thus, the output dynamic resistance is high in CE configuration,

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \quad (\text{with } I_B \text{ constant})$$

- The output characteristics of common emitter configuration consists of three regions:
  - **Active Region:** As  $V_{CE}$  is increased, reverse bias increases. This causes the depletion region to spread more in the base region than in the collector, reducing the chances of recombination in the base. This causes collector current  $I_C$  to rise more sharply with increasing  $V_{CE}$ . B-E junction is forward biased, C-B junction is reverse biased. A transistor acts as an amplifier.

- **Saturation Region:** If the  $V_{CE}$  is reduced, the CB junction becomes forward biased, since the EB junction is already forward biased,  $I_C$  also decreases rapidly. Here both the junctions are forward biased. A transistor acts as a closed switch.
- **Cut-off Region:** When the input base current is made equal to zero, the  $I_C$  is the small leakage current. Here, both junctions are reverse-biased biased and hence no current flows through the transistor. A transistor acts as an open switch.
- In the active region, the CB junction is reverse biased. If the  $V_{CE}$  is exceeds the maximum limit, width of the depletion region at the CB junction increases such that it penetrates into the base until it makes contact with EB depletion region. This condition is called **punch through effect**. When this situation occurs, breakdown of transistor occurs. That is large  $I_C$  flows and which destroys the transistor.

## 2.4 CE-RC Coupled Amplifier (Single Stage)

Single-stage Common Emitter (CE) RC coupled amplifiers are designed to improve the strength of weak signals for further amplification.

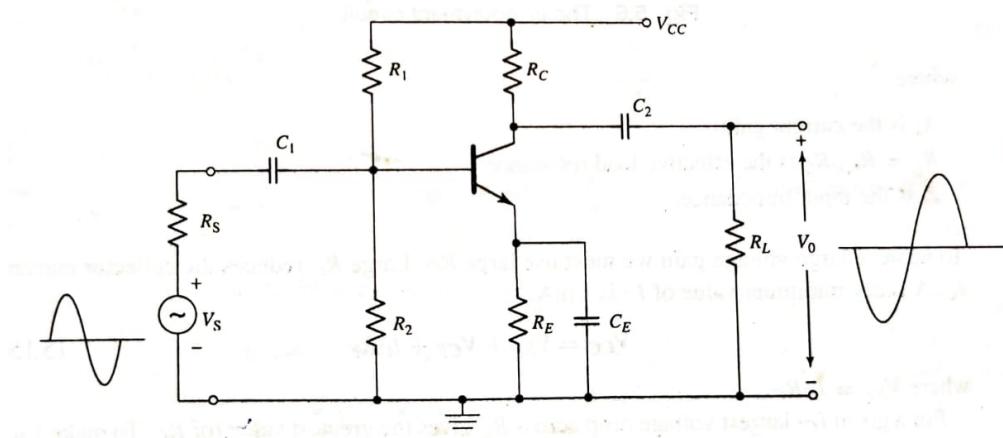


Figure 2.9: Single Stage Common Emitter RC Coupled Amplifier

### Significance of the each Components

- **Input Coupling Capacitor  $C_1$ :**  $C_1$  Couples the small signal AC,  $V_s$  to the base of the transistor. Blocks DC and allows only AC to pass, preventing external DC from affecting the transistor's biasing. If the  $C_1$  is not connected, then the  $R_s$  is in parallel with  $R_2$ . This will reduce the bias voltage at the transistor base and alter the collector current. To avoid this and maintain the stability of bias condition coupling capacitors are connected.
- **Biasing Circuit ( $R_1$ ,  $R_2$  and  $R_E$ ):** The  $R_1$  and  $R_2$  provides necessary base bias using a voltage divider network to operate the transistor in the active region. It sets the proper operating point for the CE amplifier. The  $R_E$  provides bias stabilization.

- **Emitter Bypass Capacitor  $C_E$ :** Connected in parallel to  $R_E$ , it offers a low-resistance path to the amplified AC signal, thereby increasing the gain.

*Note:* Without  $C_E$ , the amplified signal passes through  $R_E$ , causing a large voltage drop and reducing output voltage and gain.

- **Output Coupling Capacitor  $C_2$ :** Connected at the collector to block DC and pass AC to the load or next stage. If the  $R_L$  is connected directly to the output without connecting the  $C_2$ , the DC levels of  $V_{CE}$  and  $V_c$  will change. To avoid this Coupling capacitors are used at the output.

## Phase Reversal Concept

- During the **positive half cycle** of the input signal  $V_s$ , the AC and DC voltages add together, increasing the forward bias across the base-emitter (B-E) junction. This leads to an increase in base current  $I_B$ . Consequently, the collector current increases as:

$$I_C = \beta I_B$$

The increase in  $I_C$  causes an increase in the voltage drop across  $R_C$ .

- Since the collector voltage is given by:

$$V_C = V_{CC} - I_C R_C$$

An increase in  $I_C$  increases  $I_C R_C$ , causing  $V_C$  to decrease (i.e., move in the negative direction).

- During the **negative half cycle** of the AC input signal  $V_s$ , the AC and DC voltages oppose each other, reducing the forward bias across the B-E junction. As a result, the base current  $I_B$  decreases, which also reduces the collector current  $I_C$ .
- The reduction in  $I_C$  decreases the voltage drop  $I_C R_C$  across  $R_C$ . Since:

$$V_C = V_{CC} - I_C R_C$$

For a fixed  $V_{CC}$ , when  $I_C R_C$  reduces, the collector voltage  $V_C$  increases (moves in the positive direction).

Thus, as  $V_s$  increases in the positive direction, the collector voltage  $V_C$  moves in the negative direction. Hence, we obtain a **negative half cycle** of the output voltage for a **positive half cycle** at the input.

Similarly, a **positive half cycle** is observed at the output for a **negative half cycle** at the input. Therefore, we conclude that there exists a  $180^\circ$  **phase shift** between the input and output voltages in a CE amplifier, making it an **inverting amplifier**.

## 2.5 Transistor as a Switch

A transistor can be made to operate as an ON/OFF switch.

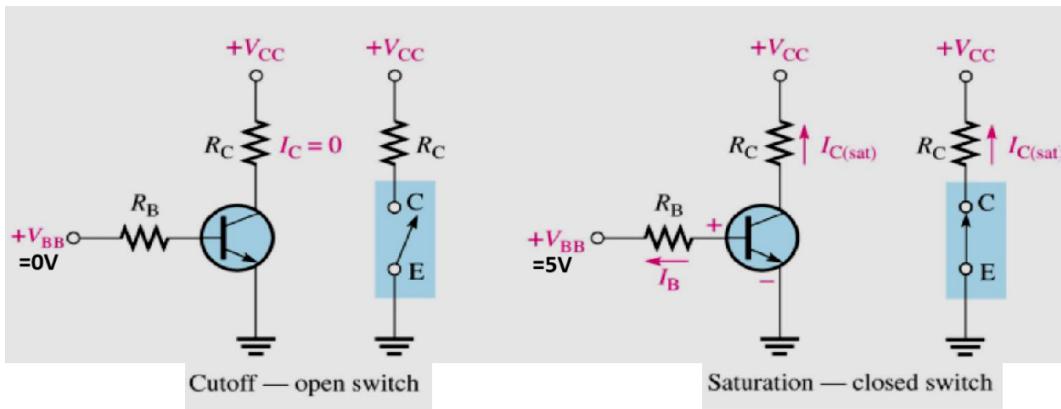


Figure 2.10: Transistor as Switch

### Case 1: Cut-off State (Open Switch)

When base voltage  $V_{BB} = 0V$ , both the EB and CB junctions are reverse biased. No base current  $I_B$  flows. Hence,  $I_C = 0$ . Therefore, the collector (C) and emitter (E) terminals are open-circuited.

**Output collector voltage:**  $V_O = V_{CC}$

Therefore, the transistor is in the cut-off state.

### Case 2: Saturation State (Closed Switch)

When a higher level of base voltage  $V_{BB}$  is applied, both EB and CB junctions are forward biased. A large base current  $I_B$  flows due to  $+V_{BB}$  which makes the collector current reach saturation level. Hence, collector (C) and emitter (E) terminals are short-circuited.

**Output collector voltage:**  $V_O = 0V$

**Saturation current:**

$$I_{C(sat)} = \frac{V_{CC} - V_{CE}}{R_C}$$

Therefore, the transistor is in the saturation state.

## 2.6 Field Effect Transistor

- Field Effect Transistor known as FET is a 3-terminal semiconductor device in which current flow is only due to one of the two kinds of charge carriers namely electrons or holes. Hence, it is a unipolar device.
- BJT is a current controlled device ( $I_B$  controls  $I_C$  in CE configuration) while FET is a voltage controlled device (input voltage controls output current).
- FET construction is simple compared to BJT and uses less area in an integrated circuit (IC). It is less noisier than BJT.
- Low power consumption and are used in MOS circuits.

- Input resistance is high compared to BJT.

**Two Types of FETs are:**

1. Junction Field Effect Transistor (JFET)
2. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

### 1. JFET

- n-channel JFET
- p-channel JFET

### 2. MOSFET

- Depletion type
  - n-channel
  - p-channel
- Enhancement type
  - n-channel
  - p-channel

#### 2.6.1 N channel Enhancement Type Metal Oxide Semiconductor (N-EMOSFET)

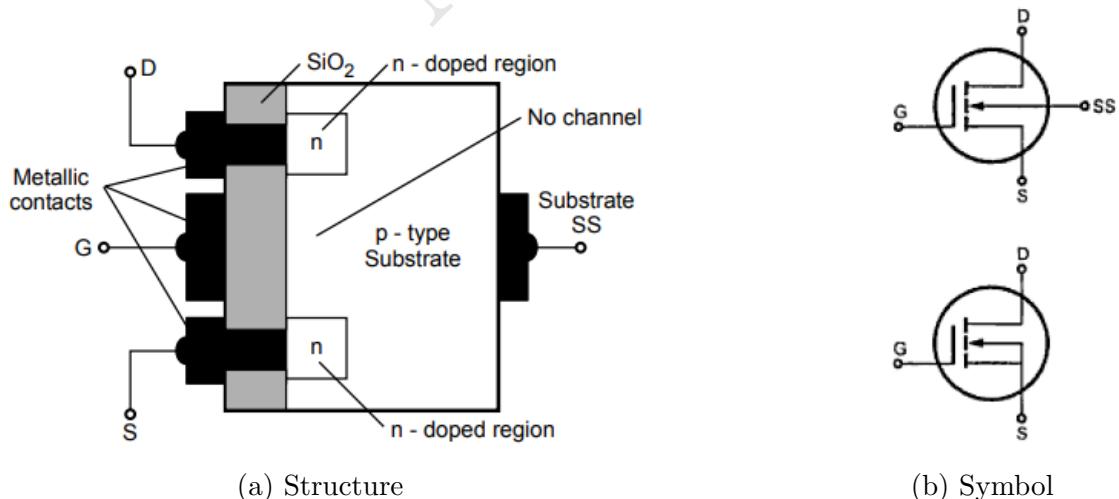


Figure 2.11: N-EMOSFET

### Basic Construction

- A slab of *p-type* material is formed from a silicon base and is referred to as substrate. The substrate is internally connected to the source terminal.

- The source and drain terminals are connected through metallic contacts to the *n-doped* regions. There is an absence of channel between the two *n-doped* regions.
- SiO<sub>2</sub> layer is present to isolate the gate metallic platform from drain and source terminals.

## Drain and Transfer Characteristics of n-channel MOSFET

- If  $V_{GS}$  is set to 0V and a positive voltage is applied between drain and source terminals, the absence of an n-channel will result in a current of zero mA.
- Both  $V_{GS}$  and  $V_{DS}$  are set at some positive voltage greater than zero volts. This establishes a positive potential between the drain and gate with respect to the source.
- The positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO<sub>2</sub> layer to leave the area and enter deeper regions of the p-substrate, as in Figure 2.12.

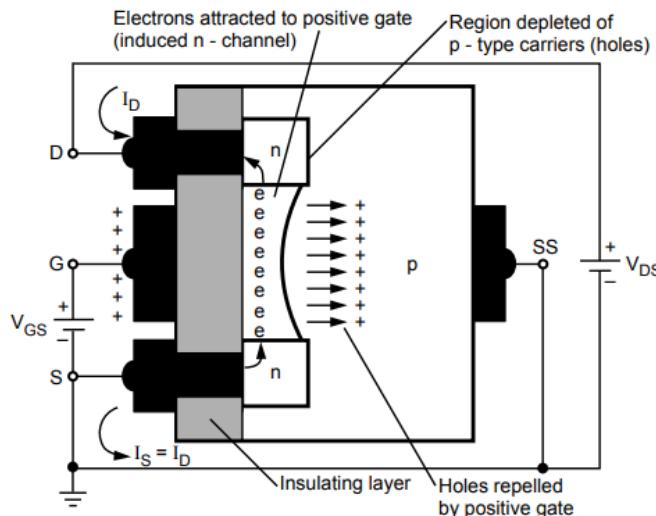


Figure 2.12: Channel formation in the NEMOSFET

- The electrons (minority carriers) in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO<sub>2</sub> layer.
- The SiO<sub>2</sub> layer and its insulating qualities will prevent the electrons from being absorbed by the gate.
- As  $V_{GS}$  increases in magnitude, the concentration of electrons near the SiO<sub>2</sub> surface increases until it can control the flow of current between drain and source.
- The level of  $V_{GS}$  that results in significant increase in drain current is called as **threshold voltage  $V_T$** .

- Since the channel is non-existent with  $V_{GS} = 0V$  and is enhanced by the application of positive gate-to-source voltage, this type of MOSFET is called an **enhancement type MOSFET**.
- The Figure 2.13 shows the drain characteristics of an N channel enhancement type MOSFET. Here, as  $V_{GS}$  is increased beyond the threshold level  $V_T$ ,  $V_{GS} > V_T$ , the density of free carriers in the induced channel will increase, resulting in increased drain current  $I_D$ .

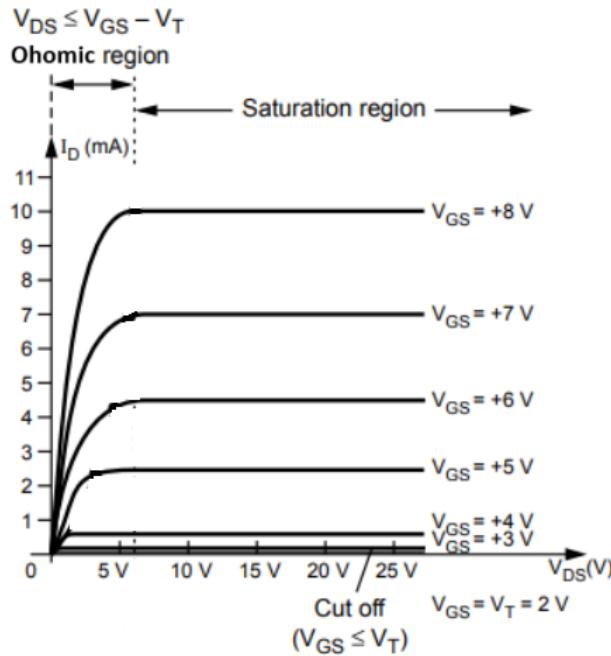


Figure 2.13: Drain Characteristics of the N-EMOSFET

- If  $V_{GS}$  is held constant, and  $V_{DS}$  is increased, the drain current  $I_D$  increases in the initial portion of the curve, and this region is called **Ohmic region**. As the  $V_{DS}$  is further increased  $I_D$  reaches a **Saturation level**. At this condition, pinching off occurs.
- When saturation occurs, the channel becomes narrow toward the drain, as shown in Figure 2.14.
- With  $V_{GS}$  held constant and  $V_{DS}$  increased, the gate-to-drain voltage  $V_{GD}$  will drop. So, the gate will be less and less positive with respect to the drain.
- This reduction in gate-to-drain voltage causes a reduction in channel width. Hence, the channel will be reduced to a point of pinch-off and a saturation condition will be established.

#### Saturation Condition:

$$V_{DS(\text{sat})} = V_{GS} - V_T$$

- When  $V_{DS}$  is less than  $V_T$ , the drain current drops to zero and hence the device shifts to **Cut off region**.

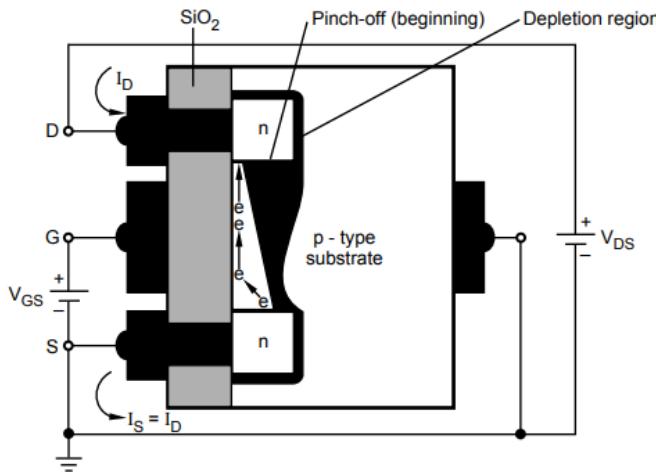


Figure 2.14: Change in channel and depletion in MOSFET

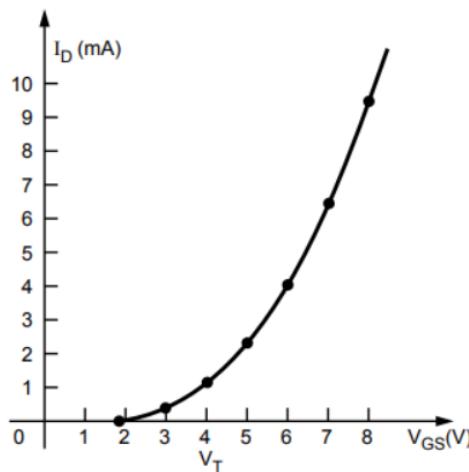


Figure 2.15: Transfer Characteristics of the NEMOSFET

The Figure 2.15 shows the Transfer characteristics of the MOSFET.

- For  $V_{GS} < V_T$ ,  $I_D = 0 \text{ mA}$
- For  $V_{GS} > V_T$ ,  $I_D$  depends on  $V_{GS}$  and is applied by a nonlinear relation:

$$I_D = K(V_{GS} - V_T)^2$$

Where,

$$K \text{ is a constant} = 0.278 \times 10^{-3} \text{ A/V}^2$$

$$K = \frac{I_{D(\text{ON})}}{(V_{GS} - V_T)^2}$$

## 2.7 CMOS Inverter

- **CMOS** → Complementary MOS. It uses two E-MOSFETs for its construction.

- A P-channel and N-channel E-MOSFET when placed on the same substrate is known as **Complementary MOS**.
- It has low input impedance, fast switching speeds and low power consumption.
- It is used in computer logic design.
- One N-type MOS (NMOS) and one P-type MOS (PMOS) are connected in pairs to form CMOS.
- Gates of the two devices are connected to form the input terminal, and the two drain terminals are connected together to form the output terminal, as shown in Figure 2.16.

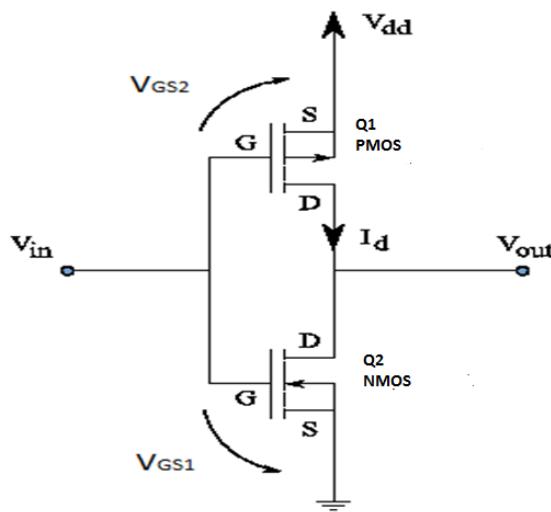


Figure 2.16: CMOS Inverter

**Case 1:** When  $V_{in} = 5V$  (State 1)

$$V_{GS2} = V_{in} - V_{DD} = 5 - 5 = 0V$$

Hence, PMOS is non-conducting or **OFF** (open circuited). It offers high resistance.

$$V_{GS1} = V_{in} - V_G = 5 - 0 = 5V$$

Therefore, for  $V_{GS1} = 5V$ , NMOS is conducting or **ON** (short circuited to ground). It offers low resistance.

NMOS is ON with low resistance. Hence,

$$V_{out} = 0V \quad (\text{State 0})$$

**Case 2:** When  $V_{in} = 0V$  (State 0)

$$V_{GS2} = 0 - 5 = -5V$$

For negative gate voltage, PMOS is ON and acts as a closed switch. It conducts and offers low resistance.

$$V_{GS1} = 0 - 0 = 0V$$

NMOS is non-conducting for  $V_{GS1} = 0V$ .

Hence, it is **OFF** and open circuited. It offers high resistance.

$\therefore$  PMOS is ON with  $V_{out} = 5V$  (State 1)

# Chapter 3

## Op-Amp & Linear IC Applications

### 3.1 Introduction

- Operational amplifiers, also known as op-amps, are voltage amplifying device designed to be used with components like capacitors and resistors between input and output terminals.
- They are high gain amplifiers consisting of one or more differential amplifiers.
- They are often used in signal conditioning, filtering and operations (mathematical) such as addition, subtraction, multiplication, integration and differentiation.
- OP-Amps are the most useful device in analog electronic circuitry. With only a few external components it can be made to perform a variety of analog signal processing tasks. It can amplify both AC and DC input signals.

### 3.2 History

- In 1963, the first monolithic integrated circuit (IC) or Op-Amp IC was introduced. It was  $\mu$ A702 from Fairchild semiconductors – designed by an engineer Bob Widlar.
- In 1968, some of the instability issues in  $\mu$ A709 were resolved and the IC was re-introduced by the name as  $\mu$ A741. It is a widely used IC for many applications. Here  $\mu$ A  $\rightarrow$  (micro amperes).
- Op-Amp is a very high gain negative feedback amplifier that can amplify signals having wide range of frequencies.
- With the addition of suitable external feedback components, Op-Amps can also be used for variety of applications such as signal amplification, filter, oscillators, regulators, comparators etc.

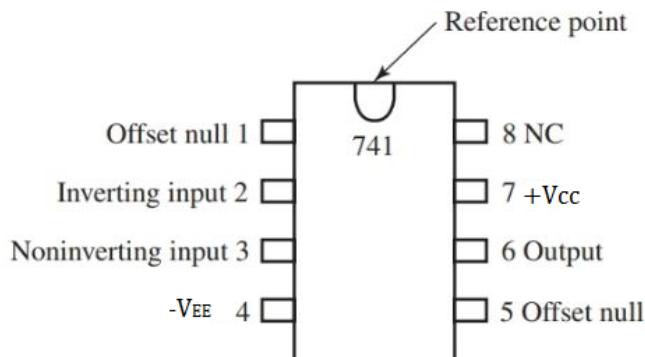
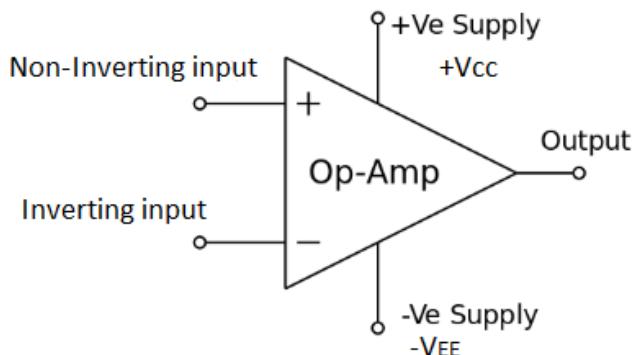
**IC Diagram:**Figure 3.1: 8 pin IC package of  $\mu$ A741 Op-Amp**Schematic symbol of Op-Amp:**

Figure 3.2: Schematic symbol

- Figure 3.2 shows the schematic symbol of Op-Amp. It has two inputs and one output terminal. The input with positive sign is called as **non-inverting terminal** and that with negative sign is called as **inverting terminal**.
- $+V_{CC}$  and  $-V_{EE}$  are DC power supply terminals.
- The output voltage  $V_o$  is in phase with input if the signal is connected to the non inverting terminal as shown in Figure 3.3. The output voltage  $V_o$  is out of phase with the input if the signal is connected to the inverting terminal as shown in Figure 3.4.

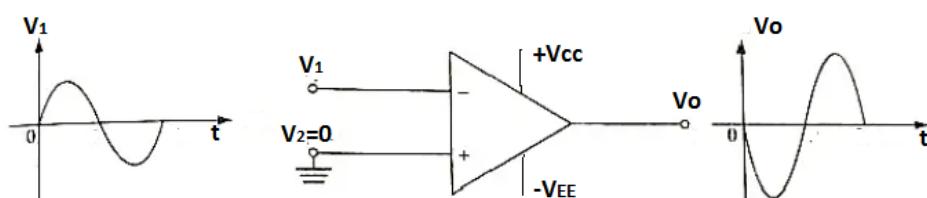


Figure 3.3: Inverting amplifier

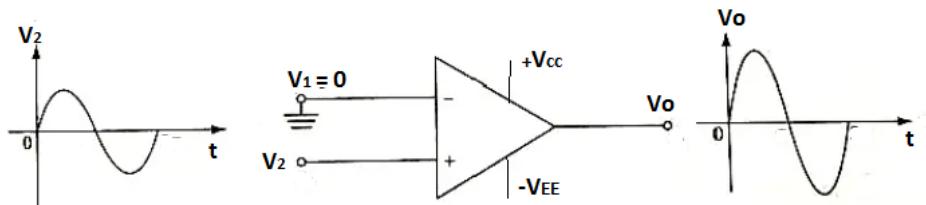


Figure 3.4: Non-Inverting amplifier

### Equivalent circuit of an Op-Amp:

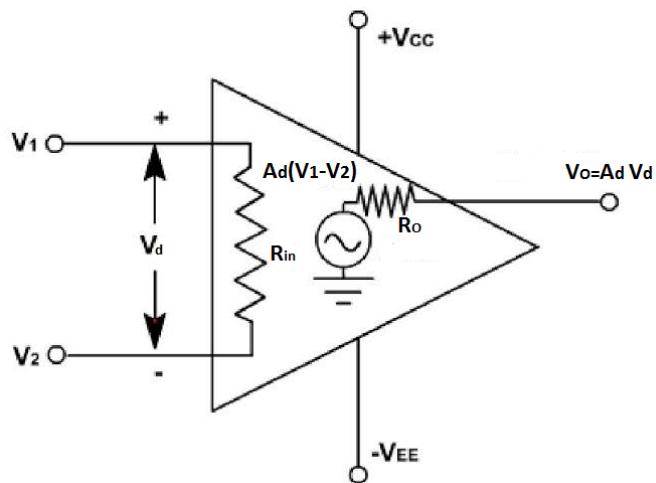


Figure 3.5: Equivalent Circuit of Op Amp

In the above equivalent circuit, the output voltage  $V_o$  is given by

$$V_o = A_d(V_1 - V_2) \quad (1)$$

$$V_o = A_d V_d$$

- where,  $V_d$  is the differential input voltage,  $V_1$  is the voltage at the non-inverting terminal w.r.t ground and  $V_2$  is the voltage at the inverting terminal w.r.t ground.  $A_d$  is the differential gain of an Op-Amp. It is given by

$$A_d = \frac{V_o}{V_d}$$

- In equation 1, output voltage  $V_o$  is directly proportional to the difference between the two input voltages. i.e., Op-Amp amplifies the difference between the two input voltages. The polarity of  $V_o$  depends on the polarity of the difference voltage  $V_d$  (open loop gain).
- A graph of  $V_o$  versus  $V_d$  is plotted as shown in Figure 3.6 by keeping  $A_d$  as constant.
- It can be seen that the output voltage  $V_o$  cannot exceed the positive and negative saturation voltages  $+V_{CC}$  and  $-V_{EE}$ .
- Hence, the output voltage  $V_o$  is directly proportional to the difference input voltage  $V_d$  until it reaches the saturation voltages and later it remains constant as shown in the transfer characteristics of Op-Amp in Figure 3.6.

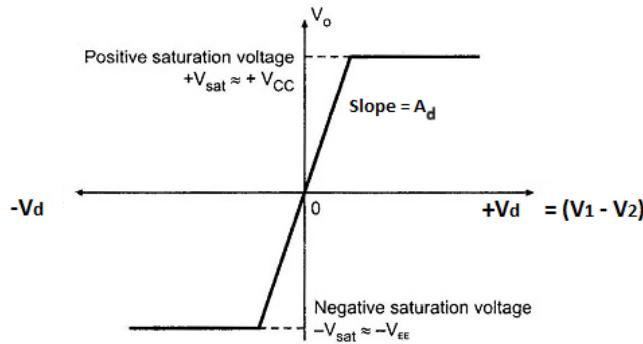


Figure 3.6: Transfer characteristics

Since open loop gain  $A_d$  is very large, a small difference input voltage  $V_d$  will produce a large swing as the output voltage that may reach  $\pm V_{sat} (+V_{CC}, -V_{EE})$ .

### 3.3 Op-Amp Parameters:

1. **Common Mode Rejection Ratio (CMRR):** CMRR is defined as the ratio of the differential gain  $A_d$  to the common mode gain  $A_c$ .

$$\text{CMRR, } \rho = \frac{A_d}{A_c}$$

When the same input voltages are applied to both input terminals of a differential amplifier, it is said to be operating in common mode configuration. Many disturbance signals, noise signals appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier. The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called **Common Mode Rejection Ratio**.

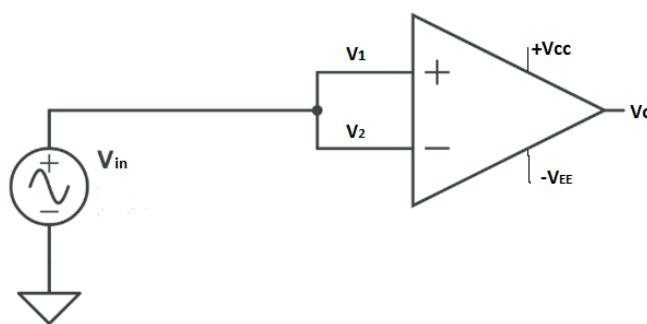


Figure 3.7: CMRR

**[Note: Common mode gain ( $A_c$ ):** When two input signals applied as inputs to an Op-Amp are equal, then the output voltage  $V_o = (V_1 - V_2)$  must be zero for an ideal Op-Amp. But the output voltage of a practical differential amplifier not only depends on difference voltage, but also depends on average common level of two input voltages. Such an average level of two input voltages is called as common

mode voltage  $V_C$ .

$$V_C = \frac{V_1 + V_2}{2}$$

The output voltage due to common mode voltage is  $V_O = A_C V_C$ . The common mode gain is given by

$$A_C = \frac{V_O}{V_C}$$

Hence, there exists some finite output for  $V_1 = V_2$  due to common mode gain  $A_C$  in case of practical differential amplifiers.]

Ideally, the common mode voltage gain is zero, hence the ideal value of CMRR is infinite. For a practical differential amplifier,  $A_d$  is large and  $A_c$  is small, hence the value of CMRR is also very large. Since CMRR is very large, it can be expressed in dB as

$$\text{CMRR in dB} = 20 \log_{10} \left| \frac{A_d}{A_c} \right| \text{dB}$$

2. **Input bias current ( $I_B$ ):** It is the average value of the current that flows into the inverting and non-inverting input terminals of an Op-Amp as shown in Figure 3.8.

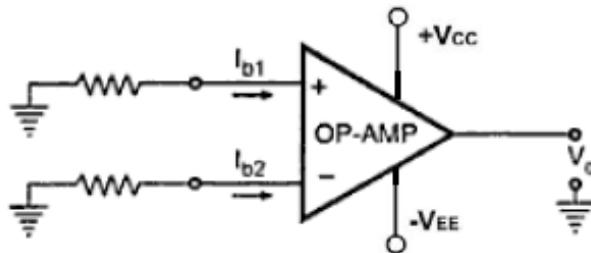


Figure 3.8: Input bias currents

Input bias current is given by,

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

3. **Input offset current ( $I_{io}$ ):** It is the algebraic difference between the currents flowing into inverting and non inverting terminals of an Op-Amp. It is given by

$$I_{io} = |I_{B1} - I_{B2}|$$

4. **Input offset voltage ( $V_{io}$ ) :** Whenever both the input terminals of the op-amp are grounded, ideally, the output voltage should be zero. However, in this condition, the practical op-amp shows a small non zero output voltage. To make this output voltage zero, a small voltage in millivolts is required to be applied to one of the input terminals. Such a voltage makes the output exactly zero. It is the voltage that must be applied between the two input terminals such that the output voltage becomes zero. This is shown in Figure 3.9

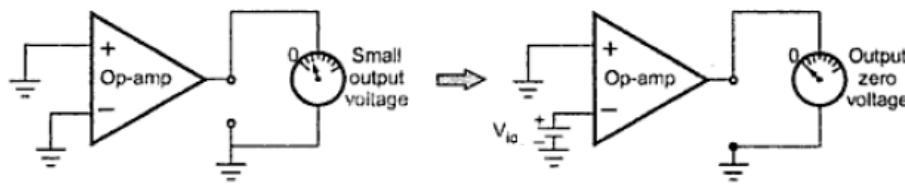


Figure 3.9: Input offset voltage

5. **Input impedance ( $R_i$ ):** It is the equivalent resistance that can be measured at either the inverting or non inverting terminal with the other terminal connected to ground.
6. **Output impedance ( $R_o$ ):** It is the equivalent resistance that can be measured between the output terminal of an op-amp and the ground.
7. **Slew rate ( $S$ ):** It is defined as maximum rate of change of output voltage per unit time. It is given by

$$\text{Slew rate} = \frac{dV_o}{dt} V/\mu\text{sec}$$

Slew rate indicates how fast the output of an OP-Amp can change in response to changes in the input signal frequency.

### 3.4 Ideal Op-Amp Characteristics

1. **Infinite voltage gain ( $A_{OL}$ ):** It is the differential open loop gain of an op-amp. We know that,

$$\begin{aligned} V_o &= A(V_1 - V_2) \\ \frac{V_o}{A} &= (V_1 - V_2), \\ \text{if, } V_1 &= V_2, \\ \text{then, } \frac{V_o}{A} &= 0, \\ \text{this implies, } \frac{V_o}{0} &= A = \infty = A_{OL}. \end{aligned}$$

2. **Infinite input impedance ( $R_i$ ):** An ideal op-amp does not draw any current at both input terminals.

$$\begin{aligned} \text{i.e., } I_1 &= I_2 = 0 \\ R_i &= \frac{V_i}{I_i} = \frac{V_i}{0} = \infty \end{aligned}$$

Thus, the ideal op-amp open-loop voltage gain is **infinity**. Thus, its input impedance is **infinity**. This ensures that no current flows through the terminals of an ideal op-amp.

3. **Zero Output impedance ( $R_O$ ):** In an ideal op-amp, the output voltage remains constant regardless of the current drawn by the load. This is represented by a **zero** output impedance.
4. **Zero Input offset voltage ( $V_{io}$ ):** The input offset voltage is the differential voltage required between the input terminals to make the output voltage zero. For an ideal op-amp,  $V_{io}$  is **zero**.
5. **Zero Input offset current ( $I_{io}$ ):** The input offset current is the difference between the currents flowing into the inverting and non-inverting input terminals when the output voltage is zero. For an ideal op-amp, this difference is **zero**.

$$\text{If } I_{B1} = I_{B2} = 0, \\ \text{then, } I_{io} = |I_{B1} - I_{B2}| = 0$$

6. **Zero Input bias current ( $I_B$ ):** It is the small DC current that flows into or out of the input terminals to bias the internal circuit. For an ideal op-amp it is **zero**.

$$\text{if } I_{B1} = I_{B2} = 0, \\ \text{then, } I_B = \frac{I_{B1} + I_{B2}}{2} = 0.$$

7. **Bandwidth (BW):** Bandwidth is the range of frequencies over which the output of op-amp is constant. For an ideal op-amp bandwidth (BW) is **infinity**.
8. **CMRR:** The ratio of differential gain  $A_d$  to common mode gain  $A_c$  is defined as CMRR.

$$\text{i.e., CMRR} = \frac{A_d}{A_c} \\ \text{if } A_c = 0, \\ \text{then, CMRR} = \frac{A_d}{0} = \infty$$

This implies that an ideal op-amp ensures **zero** common mode gain ( $A_c = 0$ )

9. **Slew rate** Higher the Slew rate, better is the performance of the OP-Amp. Ideally, slew rate is  $\infty$ .

### 3.5 Practical values:

- Voltage gain ( $A_{OL}$ ) =  $2 \times 10^5$
- Input impedance ( $R_i$ ) =  $2 \times 10^6 \Omega$
- Output impedance ( $R_O$ ) =  $75 \Omega$
- Input offset voltage ( $V_{io}$ ) =  $2mV$
- Input offset current ( $I_{io}$ ) =  $20nA$

- Input bias current ( $I_B$ ) =  $8\mu A$
- CMRR =  $90dB$
- Slew rate (S) =  $0.5V/\mu sec$

### 3.6 Numerical on Op-Amp Characteristics

1. Determine the input bias current and input offset current  $I_B$  and  $I_{io}$  for an op-amp if the current into non-inverting terminal is  $8.3 \mu A$  and inverting terminal is  $7.9 \mu A$ .

**Given:**

$$I_{B1}=8.3 \mu A, I_{B2}=7.9 \mu A$$

$$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{8.3 \mu A + 7.9 \mu A}{2} = 8.1 \mu A$$

$$I_{io} = |I_{B1} - I_{B2}| = |8.3 \mu A - 7.9 \mu A| = 0.4 \mu A$$

2. A certain Op-amp has a differential voltage gain of 1,00,000 and common mode gain of  $A_c = 0.25$ . Determine CMRR and express it in dB.

**Given:**

$$A_d = 1,00,000, \quad A_c = 0.25$$

Common Mode Rejection Ratio (CMRR):

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{1,00,000}{0.25} = 4,00,000$$

In decibels (dB):

$$\text{CMRR}_{\text{dB}} = 20 \log_{10}(4,00,000) = 112.04 \text{ dB}$$

3. An Op-amp has a differential voltage gain of 2500 and a CMRR of 30,000.

- i) Determine the common mode gain  $A_c$
- ii) Express CMRR in dB

**Given:**

$$A_d = 2500, \quad \text{CMRR} = 30,000$$

i)

$$\text{CMRR} = \frac{A_d}{A_c} \Rightarrow A_c = \frac{A_d}{\text{CMRR}} = \frac{2500}{30000} = 0.0833$$

ii)

$$\text{CMRR}_{\text{dB}} = 20 \log_{10}(30000) = 89.54 \text{ dB}$$

4. An Op-amp has a common mode input signal of 3.2 V to both the input terminals. This results in an output signal of 26 mV. Determine the common mode gain  $A_c$  and CMRR in dB. Given that the differential gain is 100.

**Given:**

$$V_c = 3.2 \text{ V}, \quad V_o = 26 \text{ mV}, \quad A_d = 100$$

Common Mode Gain:

$$A_c = \frac{V_o}{V_c} = \frac{26 \text{ mV}}{3.2 \text{ V}} = 0.0081$$

Common Mode Rejection Ratio:

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{100}{0.0081} = 12345.6$$

CMRR in decibels:

$$\text{CMRR}_{\text{dB}} = 20 \log_{10}(12345.6) = 81.83 \text{ dB}$$

### 3.7 Virtual Ground Concept

Virtual ground means, the differential input voltage  $V_d$  between the non-inverting and inverting terminal is zero.

Eg: If the output voltage is 10V and open loop gain  $A_{OL}$  is  $10^4$ , then

$$V_O = A_{OL}V_d$$

$$V_d = \frac{V_o}{A_{OL}} = \frac{10}{10^4} = 1 \text{ mV}$$

Hence,  $V_d$  is very small. It means that  $A_{OL}$  is  $\infty$  (large). The difference voltage  $V_d$  is small and in practice, it is assumed to be zero. Therefore,

$$V_d = \frac{V_o}{A_{OL}}$$

$$\Rightarrow (V_1 - V_2) = \frac{V_o}{\infty} = 0$$

$$\Rightarrow V_1 = V_2$$

i.e. There exists a virtual short circuit between the two input terminals, in the sense that their voltages are the same. So if one terminal is at ground, other terminal is at virtual ground. No current flows from the input terminals to the ground. The thick line in the Figure 3.10 indicates the virtual short circuit between the input terminals.

If one terminal is at a particular voltage level, the other terminal is at the same voltage level. This is the concept of Virtual Ground.

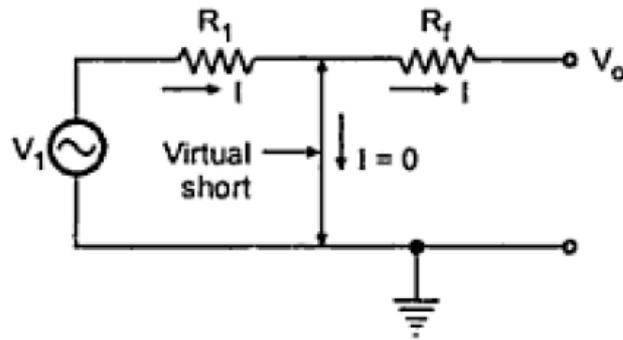


Figure 3.10: Virtual Ground Concept in Op-amp

### 3.8 Saturable Property of an Op-Amp:

The property by which the output voltage of an Op-Amp saturates at two saturation levels  $\pm V_{sat}$  decided by the supply voltages is called as saturable property of OP-Amp. Every OP-Amp has a property that its output can swing between two levels decided by supply voltage i.e.  $+V_{CC}$  and  $-V_{EE}$ . Thus if the output tries to rise more than  $+V_{CC}$  or less than  $-V_{EE}$ , then the output signal gets clipped off and shows that saturation limit has reached. Output signal cannot be produced exceeding the saturation voltage levels.

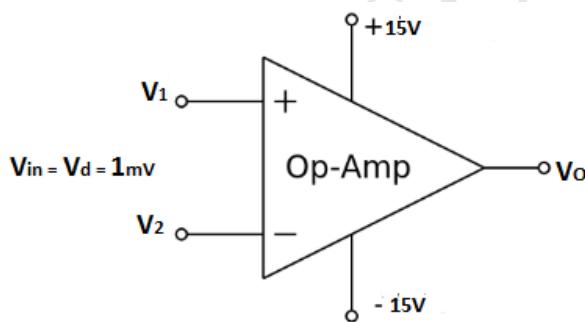


Figure 3.11: Saturable property

**For example:** Let a sine wave of 1 mV-pp be applied as the input to op-amp with gain  $A_{OL} = 10^5$ . Then the output voltage is obtained as a wave that is clipped at  $\pm V_{sat} = \pm 15V$

**Solution:**

Let the input be:  $V_{in} = V_d = 1\text{mV}$

Therefore,

$$V_o = A_{OL} \cdot V_d = 10^5 \times 1\text{mV} = 10^5 \times 1 \times 10^{-3} = 100\text{V}_{\text{p-p}}$$

This saturable property of Op-amp can be effectively used to obtain a device called as a comparator.

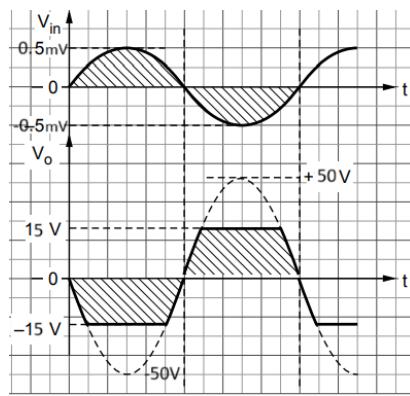
**Waveforms:**

Figure 3.12: Saturable property example

## 3.9 Op-Amp Applications

Main applications of the op-amp are:

- Inverting amplifier
- Non inverting amplifier
- Inverting Summer
- Integrator
- Differentiator
- Comparator
- IC voltage regulator

### 3.9.1 Inverting Amplifier

An inverting amplifier is a basic configuration of an operational amplifier (op-amp) that inverts and amplifies the input signal. Amplifier that has a phase shift of  $180^\circ$  at the output compared to that of input signal is known as inverting amplifier.

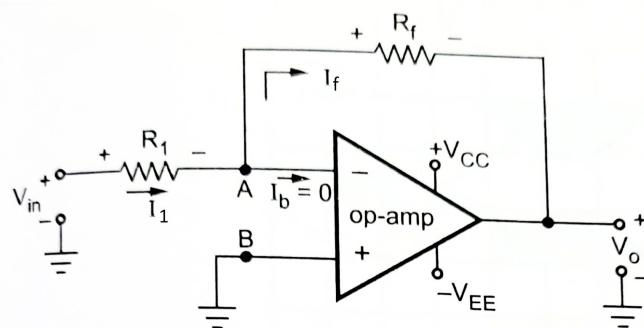


Figure 3.13: Inverting Amplifier

In the circuit shown in Figure 3.13, the input signal  $V_{in}$  is applied to the inverting input (-) of the op-amp through a resistor  $R_1$ . Hence it is called Inverting amplifier. The non-inverting input (+) is grounded. A feedback resistor  $R_f$  is connected from the output to the inverting input. Since the non-inverting terminal is grounded, potential at node B,  $V_B=0V$ .

According to virtual ground concept, node A is at virtual short with node B. Therefore, the potential at node A,  $V_A= 0V$ . That is  $V_A= V_B= 0V$

Since the current flowing through the input terminals of the opamp is zero, the entire current  $I_1$  through  $R_1$  also flows through  $R_f$  as  $I_f$ .

$$\therefore I_1 = I_f \quad (1)$$

From the input side, by applying KVL, we have:

$$\begin{aligned} V_{in} - I_1 R_1 - V_A &= 0V \\ I_1 &= \frac{V_{in} - V_A}{R_1} \\ I_1 &= \frac{V_{in}}{R_1} \quad \because V_A = 0 \end{aligned} \quad (2)$$

From the output side, by applying KVL,

$$\begin{aligned} V_A - I_f R_f - V_o &= 0V \\ I_f &= \frac{V_A - V_o}{R_f} \\ I_f &= -\frac{V_o}{R_f} \quad \because V_A = 0 \end{aligned} \quad (3)$$

Substituting the (2) and (3) in (1) we have,

$$\begin{aligned} \frac{V_{in}}{R_1} &= -\frac{V_o}{R_f} \\ \frac{V_o}{V_{in}} &= -\frac{R_f}{R_1} = A_{CL} \end{aligned}$$

$A_{CL}$  is the closed loop gain of an inverting amplifier and it depends on the value of  $R_f$  and  $R_1$ . The output voltage of the inverting amplifier is:

$$V_o = -\left(\frac{R_f}{R_1}\right) V_{in} \quad (4)$$

The negative sign indicates the presence of the phase shift of  $180^\circ$  between input and output signal  $V_{in}$  and  $V_o$ .

### Waveforms:

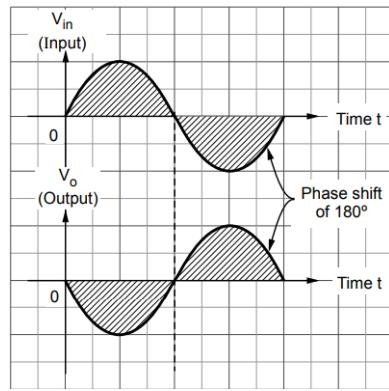


Figure 3.14: Inverting Amplifier Waveform

### 3.9.2 Noninverting Amplifier

An amplifier that amplifies the input signal  $V_{in}$  without generating any phase shift between input and output is called as non-inverting amplifier.

That is the output signal is in phase with input signal.

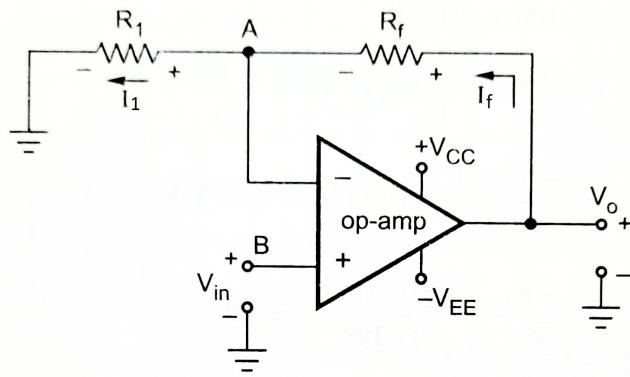


Figure 3.15: Noninverting Amplifier

$V_{in}$  is connected to the non-inverting terminal (+) of the op-amp. Feedback resistor  $R_f$  connects the output to the inverting terminal (-). Resistor  $R_1$  connects the inverting terminal (-) to ground. From the input side node B is connected to the non-inverting terminal and also to the input signal  $V_{in}$ . Hence at node B,  $V_B = V_{in}$ . According to the virtual ground, potential at node A( $V_A$ ) is same as potential at node B( $V_B$ ). That is,

$$V_A = V_B = V_{in}$$

Since the current flowing through the input terminals of the opamp is zero. Therefore entire current  $I_f$  through  $R_f$  also flows through  $R_1$  as  $I_1$ .

$$\therefore I_f = I_1 \quad (1)$$

From the output side, by applying KVL, we have,

$$\begin{aligned} V_o - I_f R_f - V_A &= 0V \\ I_f &= \frac{V_o - V_A}{R_f} \\ I_f &= \frac{V_o - V_{in}}{R_f} \quad \therefore V_A = V_{in} \end{aligned} \quad (2)$$

At the input side, we have,

$$\begin{aligned} V_A - I_1 R_1 &= 0 \\ I_1 &= \frac{V_A}{R_1} = \frac{V_{in}}{R_1} \quad \therefore V_A = V_{in} \end{aligned} \quad (3)$$

Substituting (2) and (3) in (1), we have,

$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_{in}}{R_1} + \frac{V_{in}}{R_f} = \frac{V_o}{R_f}$$

$$V_{in} \left( \frac{R_f + R_1}{R_1 R_f} \right) = \frac{V_o}{R_f}$$

Simplifying above equation, we get,

$$\frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1} = A_{CL}$$

$A_{CL}$  is the closed loop gain of the non-inverting amplifier. The output of the non-inverting amplifier is:

$$V_o = V_{in} \left( 1 + \frac{R_f}{R_1} \right) \quad (4)$$

Here there is no phase shift between input and output signal  $V_{in}$  and  $V_o$ .

### Waveforms:

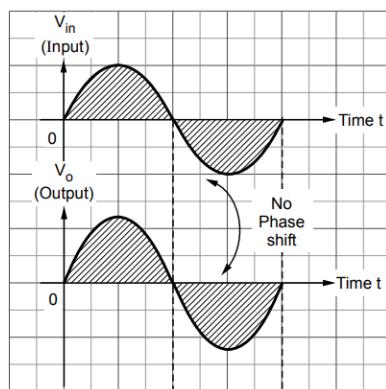


Figure 3.16: Noninverting Amplifier Waveform

### 3.9.3 Inverting Summer (Adder)

In this circuit, all the input signals to be added are applied to the inverting input terminal of the op-amp. The output signal  $V_o$  obtained is the sum of all the input signals, with the negative sign indicating the  $180^\circ$  phase shift between the input and output signals. Hence the name, inverting summer.

#### Circuit Diagram:

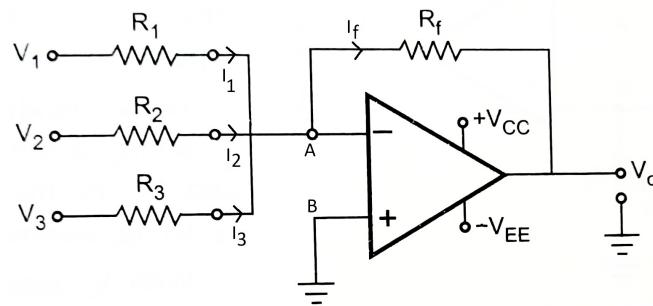


Figure 3.17: Inverting Summer

Input signals  $V_1$ ,  $V_2$ , and  $V_3$  are applied to the inverting terminal through  $R_1$ ,  $R_2$ , and  $R_3$ , and the non-inverting terminal is connected to ground.  $R_f$  is the feedback (negative feedback) resistor connected from the output terminal to the input terminal.

In the above circuit non-inverting terminal is grounded. Potential at node B,  $V_B = 0V$ . According to the virtual ground concept, the potential at node A( $V_A$ ) is same as potential at node B( $V_B$ ). That is,  $V_A = V_B = 0V$ .

In the circuit diagram, by applying KCL at inverting node,

$$I_1 + I_2 + I_3 = I_f$$

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = \frac{V_A - V_o}{R_f}$$

Since  $V_A = 0$  due to virtual ground concept. Therefore,

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_f}$$

$$\frac{V_o}{R_f} = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

If  $R_1 = R_2 = R_3 = R_f$  then,

$$V_o = -(V_1 + V_2 + V_3)$$

Hence, the output voltage is an algebraic sum of all the applied input voltages  $V_1 + V_2 + V_3 \dots V_N$  and hence it is called summer or adder circuit. Negative sign indicates the presence of a  $180^\circ$  phase shift between the input and the output.

### 3.9.4 Integrator

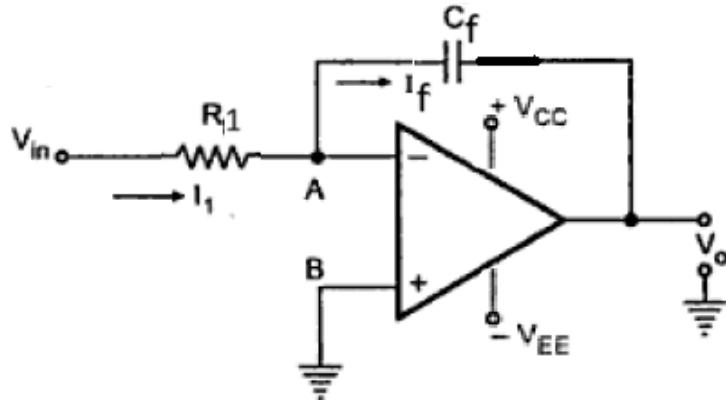


Figure 3.18: Integrator

The output of an op-amp integrator is the time integral of the applied input voltage  $V_{in}$ . In the given configuration, the non-inverting terminal is grounded. The inverting terminal is connected to the input signal  $V_{in}$  through a resistor  $R_1$ , and a capacitor  $C_f$  is connected from the output terminal back to the inverting terminal, forming a feedback loop.

Initially, when an input signal  $V_{in}$  is applied, the capacitor  $C_f$  is uncharged, and maximum current flows through resistor  $R_1$ . The capacitor begins charging based on the  $R_1C_f$  network during the positive half-cycle of  $V_{in}$ . During the negative half-cycle, the capacitor discharges. Since  $V_{in}$  is applied to the inverting terminal, the output  $V_0$  is inverted, introducing a  $180^\circ$  phase shift.

Let the potential at node A be  $V_A$ . Since node B is grounded, the potential at node B,  $V_B = 0V$ . By the virtual ground concept,

$$V_A = V_B = 0V$$

Due to the high input impedance of the op-amp, no current flows into its input terminals.

As input current  $I_1$  flows entirely through the feedback path:

$$\begin{aligned} I_1 &= I_f \\ \frac{V_{in} - V_A}{R_1} &= C_f \frac{d(V_A - V_0)}{dt} \end{aligned}$$

Since  $V_A=0V$  due to virtual ground concept,

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_0}{dt}$$

Integrating on both the sides:

$$\int_0^t \frac{V_{in}}{R_1} dt = -C_f V_0$$

$$V_0 = -\frac{1}{R_1 C_f} \int_0^t V_{in} dt$$

Hence, the output voltage  $V_0$  is the integration of the input voltage  $V_{in}$ . The negative sign indicates a  $180^\circ$  phase shift between input  $V_{in}$  and output  $V_0$ .

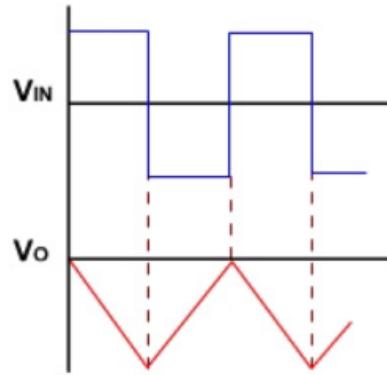


Figure 3.19: Integrator Output

### 3.9.5 Differentiator

The circuit that generates the differentiation of the input voltage  $V_{in}$  at the output is called as differentiator.

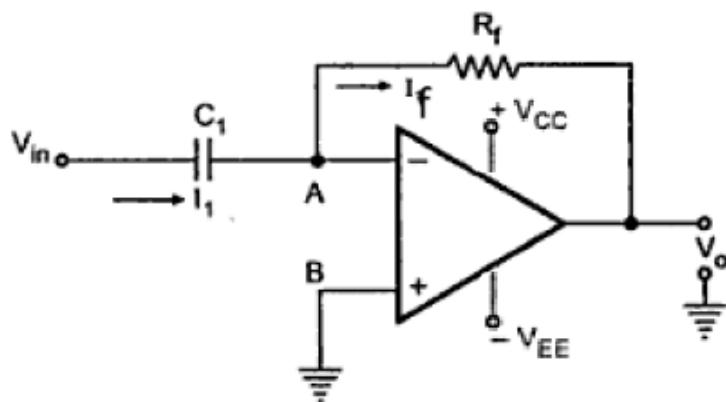


Figure 3.20: Differentiator

The input voltage  $V_{in}$  is applied to a capacitor. The capacitor blocks DC and allows only AC signals to pass. The capacitor begins charging based on the  $C_1R_f$  network during the positive half-cycle of  $V_{in}$ . It charges up to the peak value of the input voltage. During the negative half-cycle, the capacitor discharges.

Let the potential at node A be  $V_A$ . Since node B is grounded, the potential at node B,  $V_B = 0V$ . By the virtual ground concept,

$$V_A = V_B = 0V$$

The current into the input terminals of the op-amp is zero, so all current  $I_1$  flows through  $R_f$  as  $I_f$ .

$$I_1 = I_f$$

$$C_1 \frac{d(V_{in} - V_A)}{dt} = \frac{V_A - V_0}{R_f}$$

Since  $V_A=0V$  due to virtual ground concept,

$$C_1 \frac{dV_{in}}{dt} = -\frac{V_0}{R_f}$$

$$V_0 = -R_f C_1 \frac{dV_{in}}{dt}$$

Hence, the output voltage  $V_0$  is the differentiation of the input voltage  $V_{in}$ . The negative sign indicates a  $180^\circ$  phase shift between input  $V_{in}$  and output signal  $V_0$ .

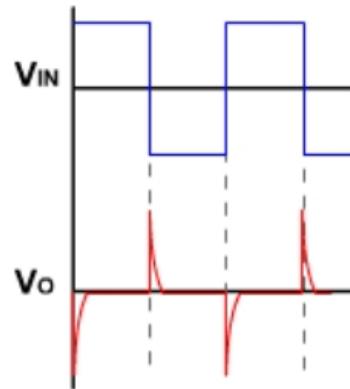


Figure 3.21: Differentiator Output

### 3.9.6 Comparators

- Comparator is a decision-making electronics circuit.
- Op-amp comparators compare the magnitude of two voltage levels at the input and determines as which is the largest of the two.

#### Types of comparators:

1. Inverting Comparator
  - (a) With +ve reference voltage
  - (b) With -ve reference voltage
2. Noninverting Comparator
  - (a) With +ve reference voltage
  - (b) With -ve reference voltage

#### 1. Inverting Comparator

Here, since  $V_{in}$  is applied to the inverting terminal of op-amp, it is called as Inverting Comparator.

(a) With +ve reference voltage ( $+V_{ref}$ ):

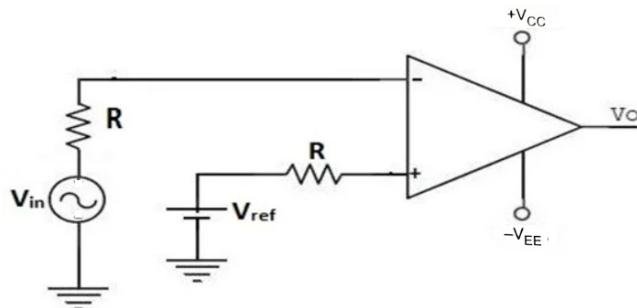


Figure 3.22: Inverting Comparator with  $+V_{ref}$

**Waveform:**

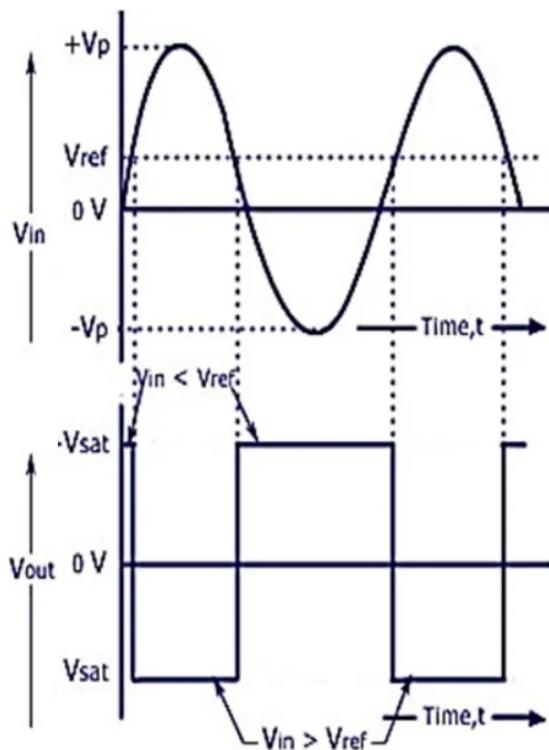


Figure 3.23: Output of Inverting Comparator with  $+V_{ref}$

**Working:** A fixed DC reference voltage  $+V_{ref}$  is connected to the non-inverting terminal.  $R$  are the current limiting resistors.

When  $V_{in} < +V_{ref}$ , output voltage  $V_0$  is at  $+V_{sat}$ . This is because  $+V_{ref}$  voltage at non inverting terminal is more compared to the  $V_{in}$  voltage at inverting terminal. Hence output voltage  $V_0$  is at  $+V_{sat}$ .

When  $V_{in} > +V_{ref}$ , output voltage  $V_0$  swings to  $-V_{sat}$  from  $+V_{sat}$ . This is because time varying signal  $V_{in}$  at inverting terminal is more compared to the

$+V_{ref}$  voltage at the non-inverting terminal. Hence output voltage  $V_0$  is at  $-V_{sat}$ . This process repeats for the next cycles as shown in the waveform.

**Note:** In short, when  $V_{in} < +V_{ref}$ ,  $V_0 = +V_{sat}$ , and when  $V_{in} > +V_{ref}$ ,  $V_0 = -V_{sat}$ .

(b) With -ve reference voltage ( $-V_{ref}$ ):

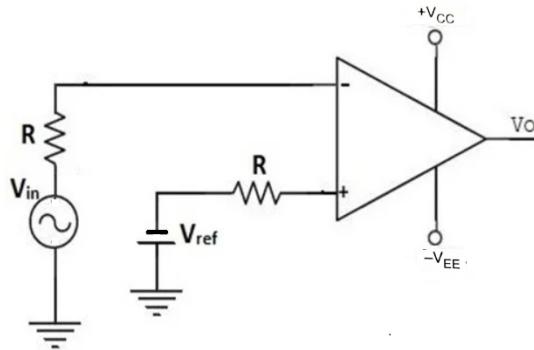


Figure 3.24: Inverting Comparator with  $-V_{ref}$

**Waveform:**

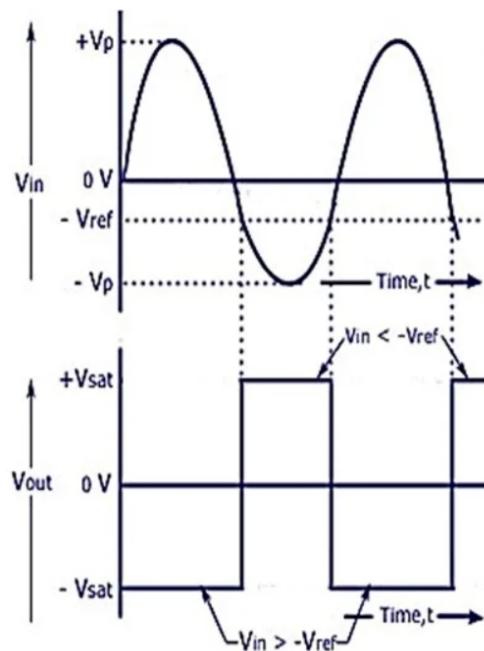


Figure 3.25: Output of Inverting Comparator with  $-V_{ref}$

**Working:** A fixed DC reference voltage  $-V_{ref}$  is connected to the non-inverting terminal.  $R$  are the current limiting resistors.

When  $V_{in} > -V_{ref}$ , output voltage  $V_0$  is at  $-V_{sat}$ . This is because time varying signal  $V_{in}$  at inverting terminal is more compared to the  $-V_{ref}$  voltage at the

non-inverting terminal. Hence output voltage  $V_0$  is at  $-V_{sat}$ .

When  $V_{in} < -V_{ref}$ , output voltage  $V_0$  swings to  $+V_{sat}$  from  $-V_{sat}$ . This is because  $-V_{ref}$  voltage at non inverting terminal is more compared to the  $V_{in}$  voltage at inverting terminal. Hence output voltage  $V_0$  is at  $+V_{sat}$ . This process repeats for the next cycles as shown in the waveform.

**Note:** In short, When  $V_{in} > -V_{ref}$ ,  $V_0 = -V_{sat}$  and when  $V_{in} < -V_{ref}$ ,  $V_0 = +V_{sat}$ .

## 2. Noninverting Comparator

Here, since  $V_{in}$  is applied to the noninverting terminal of op-amp, it is called as Noninverting Comparator.

(a) With +ve reference voltage ( $+V_{ref}$ ):

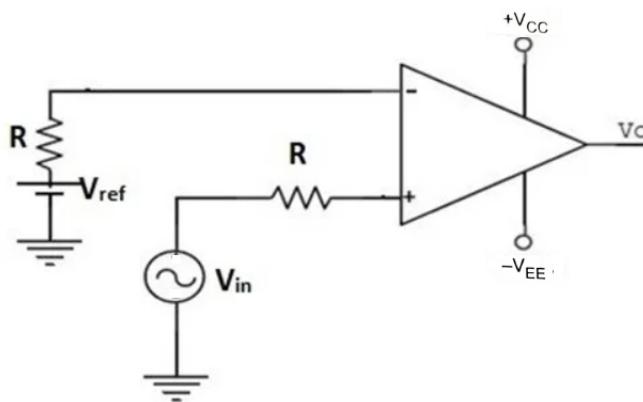


Figure 3.26: Noninverting Comparator with  $+V_{ref}$

**Waveform:**

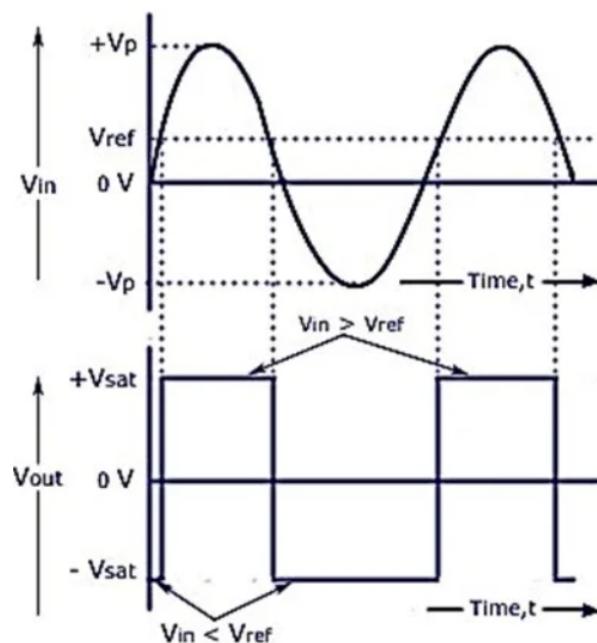


Figure 3.27: Output of NonInverting Comparator with  $+V_{ref}$

**Working:** A fixed DC reference voltage  $+V_{ref}$  is connected to the inverting terminal.  $R$  are the current limiting resistors.

When  $V_{in} < +V_{ref}$ , output voltage  $V_0$  is at  $-V_{sat}$ . This is because  $+V_{ref}$  voltage at inverting terminal is more compared to the  $V_{in}$  voltage at non-inverting terminal. Hence output voltage  $V_0$  is at  $-V_{sat}$ .

When  $V_{in} > +V_{ref}$ , output voltage  $V_0$  swings to  $+V_{sat}$  from  $-V_{sat}$ . This is because time varying signal  $V_{in}$  at non-inverting terminal is more compared to the  $+V_{ref}$  voltage at the inverting terminal. Hence output voltage  $V_0$  is at  $+V_{sat}$ . This process repeats for the next cycles as shown in the waveform.

**Note:** In short, when  $V_{in} < +V_{ref}$ ,  $V_o = -V_{sat}$ , and when  $V_{in} > +V_{ref}$ ,  $V_o = +V_{sat}$ .

(b) **With -ve reference voltage ( $-V_{ref}$ ):**

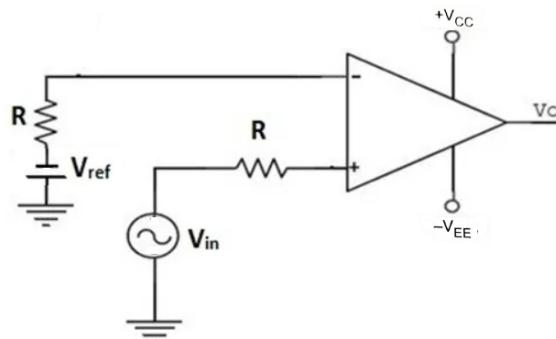


Figure 3.28: Non-inverting Comparator with  $-V_{ref}$

**Waveform:**

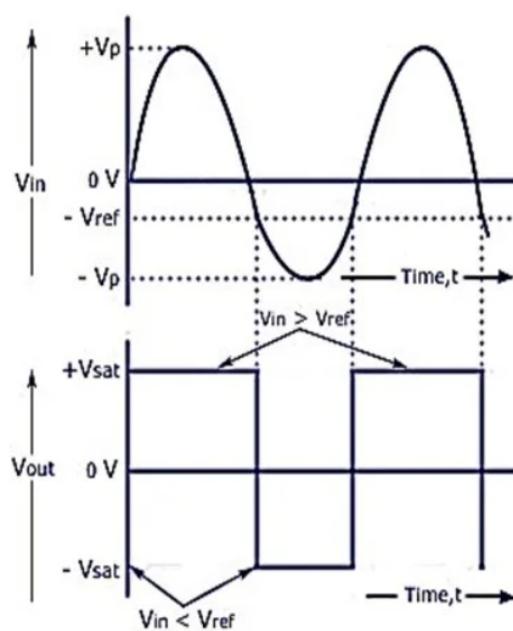


Figure 3.29: Output of non-inverting Comparator with  $-V_{ref}$

**Working:** A fixed DC reference voltage  $-V_{ref}$  is connected to the inverting terminal.  $R$  are the current limiting resistors.

When  $V_{in} > -V_{ref}$ , output voltage  $V_0$  is at  $+V_{sat}$ . This is because time varying signal  $V_{in}$  at non-inverting terminal is more compared to the  $-V_{ref}$  voltage at the inverting terminal. Hence output voltage  $V_0$  is at  $+V_{sat}$ .

When  $V_{in} < -V_{ref}$ , output voltage  $V_0$  swings to  $-V_{sat}$  from  $+V_{sat}$ . This is because  $-V_{ref}$  voltage at inverting terminal is more compared to the  $V_{in}$  voltage at non-inverting terminal. Hence output voltage  $V_0$  is at  $-V_{sat}$ . This process repeats for the next cycles as shown in the waveform.

**Note:** In short, When  $V_{in} > -V_{ref}$ ,  $V_0 = +V_{sat}$  and when  $V_{in} < -V_{ref}$ ,  $V_0 = -V_{sat}$ .

### 3.10 IC Voltage Regulator

One of the important sources of DC supply are batteries. But using batteries in sensitive electronic circuits is not a good idea, since batteries eventually drain out and lose their potential over time. Hence for obtaining constant and steady output, voltage regulators are implemented. The integrated circuits which are used for the regulation of voltage are termed Voltage regulator ICs.

78XX family of linear voltage regulators produce a regulated output voltage. XX in 78XX series represents the value of the fixed output voltage that the particular IC provides. E.g. : IC 7805 is a three terminal linear voltage regulator IC with a fixed output voltage of 5V.

The functional diagram of 78XX series based fixed IC voltage regulator is shown below. (Note that XX can be 05,06,08,10,12,15,18 or 24V)

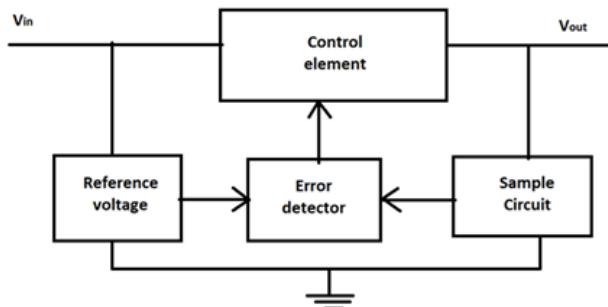


Figure 3.30: Block diagram of op-amp Series voltage regulator with feedback

IC voltage regulators can be used to regulate, the unregulated input voltage and provide a constant regulated output voltage.

**Advantages:** Inexpensive, versatile, provides current/voltage boosting, internal short circuit, current limiting and thermal shut down.

**Working:** An unregulated input voltage  $V_{in}$  is applied to the series voltage regulator. A regulated output voltage  $V_{out}$  is measured at the output terminal. A pass transistor  $Q_1$  is connected as a control element in series with load between the input and output.

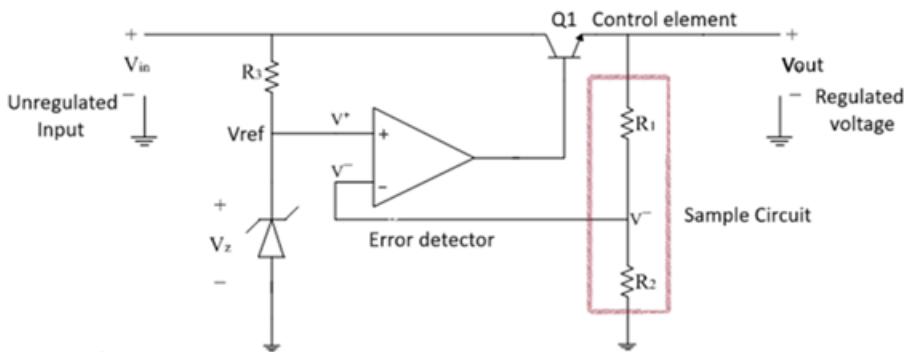


Figure 3.31: Circuit diagram of op-amp Series voltage regulator with feedback

A Zener diode reference voltage  $V_{ref}$  drives the non-inverting terminal of a high-gain amplifier. A voltage regulator network with the resistors  $R_1$  and  $R_2$  samples the output voltage and returns a feedback voltage to the inverting input terminal of a high-gain amplifier.

Where, the reference voltage  $V_{ref}$  is equivalent to the Zener voltage  $V_z$ .  $R_1$  and  $R_2$  are internal to the IC. They are already trimmed to get different output voltages (5V to 15V) in 78XX series. The pass transistor enhances the regulator output current. It can handle 1A of load current with the proper heat sinks. The output sample circuit senses a change in the output voltage. The error detector compares the sample voltage with a fixed reference voltage  $V_{ref}$ . The resulting difference voltage causes the transistor  $Q_1$  to control the conduction and to compensate the variation in the output voltage. The output voltage  $V_{out}$  will be maintained at a constant value as in below equation.

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_z$$

### 3.11 Numerical on Op-Amp Applications

1. A sine wave of 0.5 V peak voltage is applied to an **inverting amplifier** using  $R_1 = 10\text{ k}\Omega$  and  $R_f = 50\text{ k}\Omega$ . It uses supply voltages of  $\pm 12\text{ V}$ . Determine the output and sketch the waveform. If now the amplitude of the input sine wave is increased to 5 V, what will be the output? Is it practically possible? Sketch the waveform.

#### Solution:

For an inverting amplifier,

$$A_{CL} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1} = -\frac{50}{10} = -5$$

Now, for  $V_{in} = 0.5 \text{ V}$  (input),

$$V_o = (V_{in}) \times A_{CL} = 0.5 \times (-5) = -2.5 \text{ V} \text{ (peak)}$$

The input and output waveforms are inverted with respect to each other and are shown in Figure 3.32 (a).

Now, for  $V_{in} = 5 \text{ V}$  (input),

$$V_o = (V_{in}) \times A_{CL} = 5 \times (-5) = -25 \text{ V} \text{ (peak)}$$

But op-amp output saturates at  $\pm 12 \text{ V}$ , i.e., at the supply voltages used. So, the portion above  $+12 \text{ V}$  and below  $-12 \text{ V}$  will be clipped off from the output. Hence,  $25 \text{ V}$  peak output is not practically possible. The input and output waveform are shown in Figure 3.32(b).

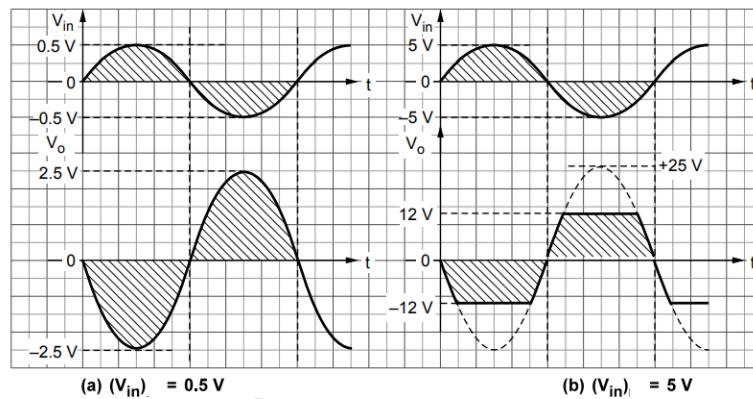


Figure 3.32: Problem 1

- For an inverting amplifier using an op-amp with  $R_1 = 10 \text{ k}\Omega$  and  $R_f = 1 \text{ M}\Omega$ , calculate the closed-loop voltage gain and the required input voltage to obtain an output voltage of  $3 \text{ V}$ .

### Solution:

The formula for the closed-loop voltage gain of an inverting amplifier is:

$$A_{CL} = -\frac{R_f}{R_1}$$

Substituting the given values:

$$A_{CL} = -\frac{1 \text{ M}\Omega}{10 \text{ k}\Omega} = -100$$

The formula for the input voltage  $V_{in}$  in an inverting amplifier is:

$$V_{in} = \frac{V_o}{A_{CL}}$$

$$V_{in} = \frac{3}{-100} = -0.03 \text{ V}$$

**Therefore, the required input voltage is  $-0.03 \text{ V}$ .**

3. For the given op-amp configuration in the figure 3.33, determine the value of  $R_f$  required to produce a closed-loop voltage gain of  $-100$ .

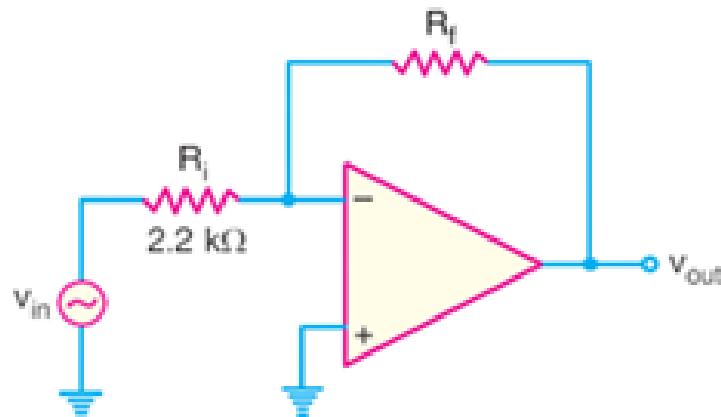


Figure 3.33: Problem 3

### Solution:

The formula for the closed-loop voltage gain of an inverting amplifier is:

$$A_{CL} = -\frac{R_f}{R_1}$$

Rearranging the formula to solve for  $R_f$ :

$$R_f = -A_{CL} \cdot R_1$$

Given  $A_{CL} = -100$ ,  $R_1 = 2.2 \text{ k}\Omega$ :

$$R_f = -(-100) \times 2.2 \text{ k}\Omega = 220 \text{ k}\Omega$$

**Therefore, the required value of  $R_f$  is  $220 \text{ k}\Omega$ .**

4. Determine the voltage gain of the op-amp circuit shown in Figure 3.34.

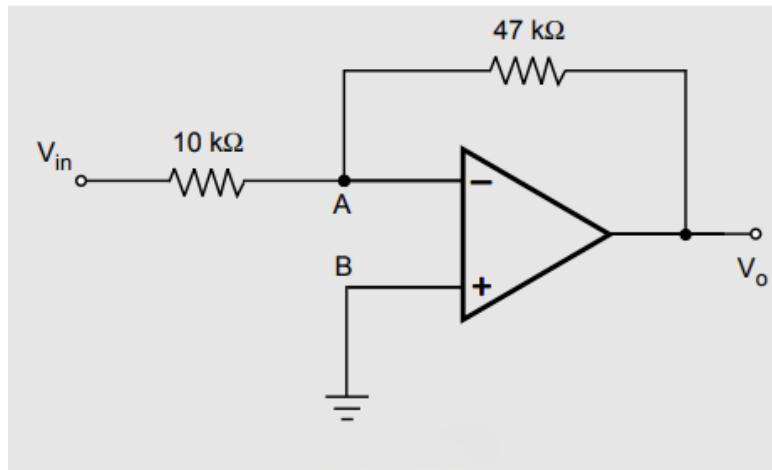


Figure 3.34: Problem 4

**Solution:**

From Figure, we have:

$$R_1 = 10 \text{ k}\Omega, \quad R_f = 47 \text{ k}\Omega$$

The circuit is an **inverting amplifier**.

The voltage gain  $A_{CL}$  of an inverting amplifier is given by:

$$A_{CL} = -\frac{R_f}{R_1}$$

Substituting the given values:

$$A_{CL} = -\frac{47 \text{ k}\Omega}{10 \text{ k}\Omega} = -4.7$$

Therefore, the gain is 4.7 and the negative sign indicates a 180° phase shift, i.e., the circuit operates in inverting mode.

5. The non-inverting amplifier circuit has a gain of 10 and a feedback resistor  $R_f = 90 \text{ k}\Omega$ . Calculate the value of the input resistance  $R_1$ .

**Solution:**

The gain  $A_{CL}$  of a non-inverting amplifier is given by:

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

Rearranging the formula to solve for  $R_1$ :

$$R_1 = \frac{R_f}{A_{CL} - 1}$$

Substituting the given values:

$$R_1 = \frac{90 \text{ k}\Omega}{10 - 1} = \frac{90 \text{ k}\Omega}{9} = 10 \text{ k}\Omega$$

**Therefore, the value of input resistance  $R_1$  is  $10 \text{ k}\Omega$ .**

6. For a non-inverting amplifier using an op-amp, assume  $R_1 = 470 \Omega$  and  $R_f = 4.7 \text{ k}\Omega$ . Calculate the closed-loop voltage gain of the amplifier.

**Solution:**

The voltage gain  $A_{CL}$  of a non-inverting amplifier is given by:

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

Substituting the given values:

$$A_{CL} = 1 + \frac{4.7 \times 10^3}{470} = 1 + 10 = 11$$

**Therefore, the closed-loop voltage gain of the amplifier is 11.**

7. For the non-inverting amplifier circuit shown in the figure 3.35, find the peak-to-peak output voltage when  $V_{in} = 2 \text{ V}_{pp}$ , and sketch the input and output waveforms.

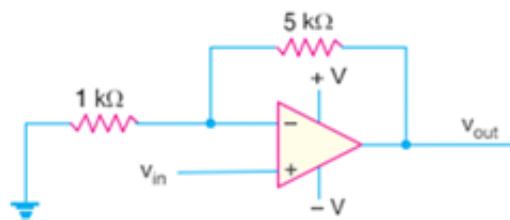


Figure 3.35: Problem 7

**Solution:**

The gain  $A_{CL}$  of a non-inverting amplifier is given by:

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

Substituting the given values:

$$A_{CL} = 1 + \frac{5 \text{ k}\Omega}{1 \text{ k}\Omega} = 1 + 5 = 6$$

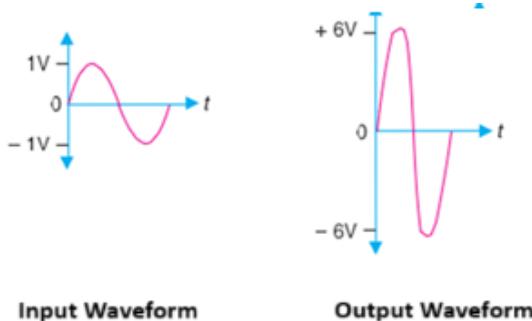
The peak-to-peak output voltage is calculated as:

$$V_{o(pp)} = A_{CL} \times V_{in(pp)}$$

$$V_{o(\text{pp})} = 6 \times 2 \text{ V}_{\text{pp}} = 12 \text{ V}_{\text{pp}}$$

Therefore, the peak-to-peak output voltage is 12 V<sub>pp</sub>.

**Waveforms:**



8. An inverting adder has the following parameters:  $R_1 = 2 \text{ k}\Omega$ ,  $R_2 = 4 \text{ k}\Omega$ ,  $R_f = 8 \text{ k}\Omega$ . If  $V_1 = 1.5 \text{ V}$  and  $V_2 = 0.5 \text{ V}$ , what is the output voltage?

**Solution:**

The output voltage  $V_o$  of an inverting adder is given by:

$$V_o = -R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} \right)$$

$$V_o = -8 \text{ k}\Omega \left( \frac{1.5}{2 \text{ k}\Omega} + \frac{0.5}{4 \text{ k}\Omega} \right) = -8 \text{ k}\Omega (0.75 + 0.125) = -8 \text{ k}\Omega \times 0.875 = -7 \text{ V}$$

Therefore, the output voltage is -7 V.

9. Design an inverting adder circuit using an op-amp to obtain the output voltage given by:

$$V_o = 2V_1 + 3V_2 + 4V_3$$

where  $V_1$ ,  $V_2$ , and  $V_3$  are input voltages. Given:  $R_f = 20 \text{ k}\Omega$ . Draw the circuit indicating all resistor values.

**Solution:**

The output voltage of an inverting adder is given by:

$$V_o = -R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) = - \left( \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right)$$

Given desired output:

$$V_o = 2V_1 + 3V_2 + 4V_3$$

Comparing coefficients:

$$\frac{R_f}{R_1} = 2 \Rightarrow R_1 = \frac{R_f}{2} = \frac{20 \text{ k}\Omega}{2} = 10 \text{ k}\Omega$$

$$\frac{R_f}{R_2} = 3 \Rightarrow R_2 = \frac{R_f}{3} = \frac{20 \text{ k}\Omega}{3} \approx 6.67 \text{ k}\Omega$$

$$\frac{R_f}{R_3} = 4 \Rightarrow R_3 = \frac{R_f}{4} = \frac{20 \text{ k}\Omega}{4} = 5 \text{ k}\Omega$$

Therefore, the resistor values are:

$$R_1 = 10 \text{ k}\Omega, \quad R_2 \approx 6.67 \text{ k}\Omega, \quad R_3 = 5 \text{ k}\Omega$$

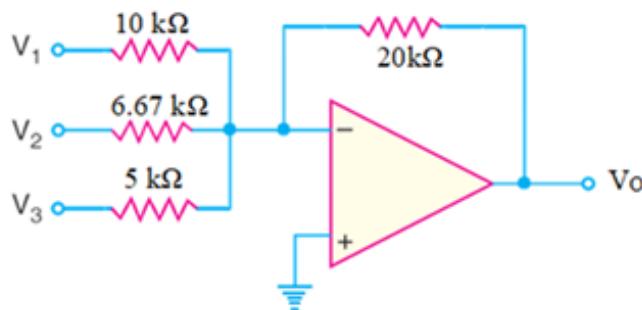


Figure 3.36: Problem 9

10. Design a summer circuit using an op-amp for the output voltage:

$$V_o = -2(0.1V_1 + 0.5V_2 + 2V_3)$$

Given: Feedback resistor  $R_f = 10 \text{ k}\Omega$ . Draw the circuit diagram for the same.

**Solution:**

The general expression for the output voltage of an inverting adder is:

$$V_o = -R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) = - \left( \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right)$$

Given:

$$V_o = -2(0.1V_1 + 0.5V_2 + 2V_3) = -(0.2V_1 + 1V_2 + 4V_3)$$

Comparing coefficients:

$$\frac{R_f}{R_1} = 0.2 \Rightarrow R_1 = \frac{R_f}{0.2} = \frac{10 \text{ k}\Omega}{0.2} = 50 \text{ k}\Omega$$

$$\frac{R_f}{R_2} = 1 \Rightarrow R_2 = \frac{R_f}{1} = 10 \text{ k}\Omega$$

$$\frac{R_f}{R_3} = 4 \Rightarrow R_3 = \frac{R_f}{4} = \frac{10 \text{ k}\Omega}{4} = 2.5 \text{ k}\Omega$$

Therefore, the required resistor values are:

$$R_1 = 50 \text{ k}\Omega, \quad R_2 = 10 \text{ k}\Omega, \quad R_3 = 2.5 \text{ k}\Omega, \quad R_f = 10 \text{ k}\Omega$$

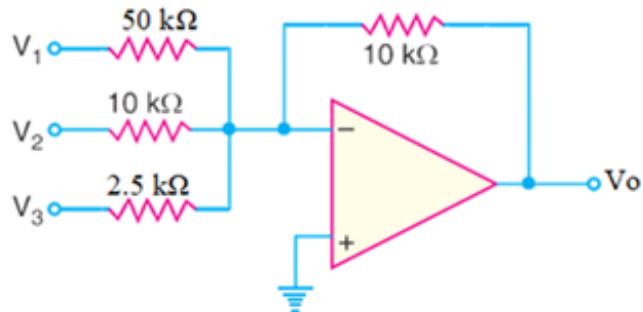


Figure 3.37: Problem 10

# Chapter 4

## Feedback and Oscillator Circuits

### 4.1 Introduction

- Feedback plays an important role in electronic circuits. It is used in amplifiers to improve its performance and make it more ideal.
- In feedback amplifiers, a part of the output is sampled and feedback to the input of the amplifier.
- At the input, there will be two signals, input signal and a part of the output. Both may be in phase or out of phase with each other.
- Depending on the polarity of the signal fed back into the circuit, it can be **negative** or **positive** feedback.
- When the input signal and the feedback signal are out of phase, it is **negative** feedback.
- When the input signal and the feedback signal are in phase, it is **positive** feedback.
- Negative feedback results in decreased voltage gain, for which a number of circuit factors are improved.
- Positive feedback drives the circuit into oscillations.

### 4.2 Negative Feedback Concepts

A typical feedback connection is shown in Figure 4.1. The input signal  $V_s$  is applied to the mixer network, where it is combined with a feedback signal  $V_f$ .  $V_i$  is the difference of these two signals. It is then applied as the input to the amplifier whose gain is  $A$ . A portion of the amplifier output  $V_o$  is connected to the feedback network ( $\beta$ ), which provides a reduced portion of the output as feedback signal to the input mixer network.

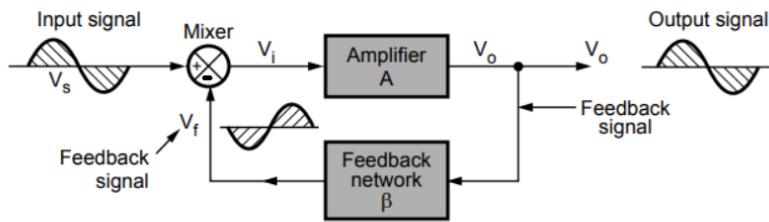


Figure 4.1: Negative Feedback Concept

**Advantages of negative feedback are:**

1. Reduced overall voltage gain
2. Higher input impedance
3. Improved frequency response
4. Lower output impedance
5. Reduced noise
6. More linear operation

### 4.3 Voltage series negative feedback amplifier

Here the voltage refers to connecting the output voltage of the amplifier as input to the feedback network. Series refers to connecting the feedback signal in series with the input signal. Series negative feedback connection tends to increase the input impedance, whereas voltage feedback tends to decrease the output impedance. Most of the cascade amplifiers require higher input impedance and lower output impedance. Both of those are provided using the voltage series feedback connection.

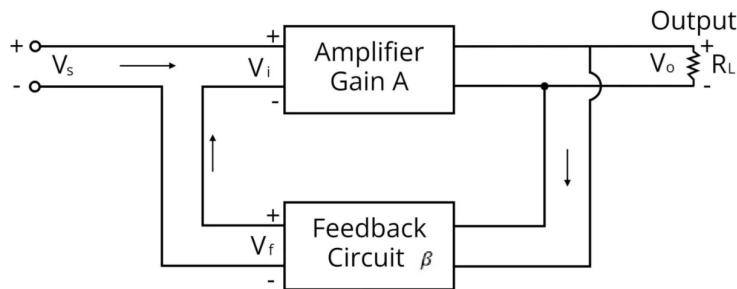


Figure 4.2: Voltage series negative feedback circuit

In the above figure,  $V_s$  is the overall input signal. The voltage  $V_i$  is the difference signal connected to the amplifier. Without feedback, amplifier gain is 'A'. The feedback

network has the feedback factor is  $\beta$ . The overall gain with feedback of the above system is  $A_f$ . In the voltage series feedback connection, the part of the output voltage  $V_o$ , is fed back in series with the input signal, that results in overall reduction in the gain. In a circuit, if there is no feedback (i.e.  $V_f=0$ ), the voltage gain of the amplifier stage is,

$$A = \frac{V_o}{V_i}$$

$$V_o = AV_i \quad (1)$$

From the circuit,

$$\beta = \frac{V_f}{V_o}$$

$$V_f = \beta V_o \quad (2)$$

If a feedback signal  $V_f$  is connected in series with the input, then,

$$V_i = V_s - V_f \quad (3)$$

Substitute (3) in (1),

$$V_o = AV_i = A(V_s - V_f) \quad (4)$$

Substitute (2) in (4),

$$V_o = AV_s - A\beta V_o$$

$$V_o + A\beta V_o = AV_s$$

$$V_o(1 + A\beta) = AV_s$$

So that, the overall gain with feedback is:

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

Here,  $|A_f| < |A|$ . The negative feedback reduces the gain of the amplifier by a factor of  $(1 + A\beta)$ .

## 4.4 Numerical on Voltage series feedback amplifier

1. Determine the voltage gain with feedback for a voltage series feedback system having:

$$A = -100, \quad \beta = -0.1 \text{ and } \beta = -0.5$$

**Solution:**

- For  $\beta = -0.1$ ,

$$A_f = \frac{-100}{1 + (-100)(-0.1)} = \frac{-100}{1 + 10} = \frac{-100}{11} \approx -9.09$$

- For  $\beta = -0.5$ ,

$$A_f = \frac{-100}{1 + (-100)(-0.5)} = \frac{-100}{1 + 50} = \frac{-100}{51} \approx -1.96$$

## 4.5 Oscillator operation

When the input signal and feedback signals are in-phase with each other it is known as positive feedback. Feedback amplifier circuit with positive feedback having closed loop or overall gain  $|A_f| > 1$  will result in operation as an oscillator circuit. If the output signal varies sinusoidally, it is referred to as sinusoidal oscillator.

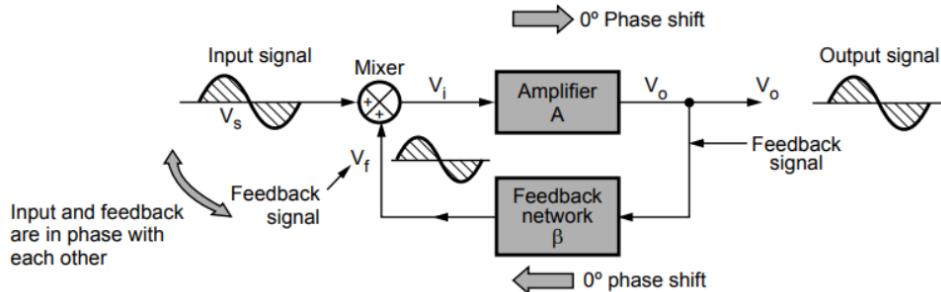


Figure 4.3: Positive feedback concept

If the output signal rises quickly to one voltage level and later drops to another level, it is referred to as a square wave oscillator. Here the overall gain with feedback is:

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 - A\beta}$$

Both  $V_s$  and the feedback signal  $V_f$  are in-phase with each other. The gain with feedback increases as the amount of positive feedback increases and becomes infinity. Consider various values of the  $\beta$  and corresponding values of  $A_f$  for constant amplifier gain,  $A=20$ .

A	$\beta$	$A_f$
20	0.005	22.22
20	0.04	100
20	0.045	200
20	0.05	$\infty$

Table 4.1: Feedback Gain for Different Values of  $\beta$

From the above table it is true that for a constant amplifier gain a small value of increase in  $\beta$  the overall gain reaches infinity. This indicates that circuit can produce output without external input ( $V_s = 0$ ), just by feeding the part of the output as its own input. Similarly, output cannot be infinite but gets driven into the oscillations. In other words, the circuit stops amplifying and starts oscillating.

Thus without an input, the output will continue to oscillate whose frequency depends upon the feedback network or the amplifier or both. Such a circuit is called as an **oscillator**.

#### 4.5.1 Barkhausen criterion

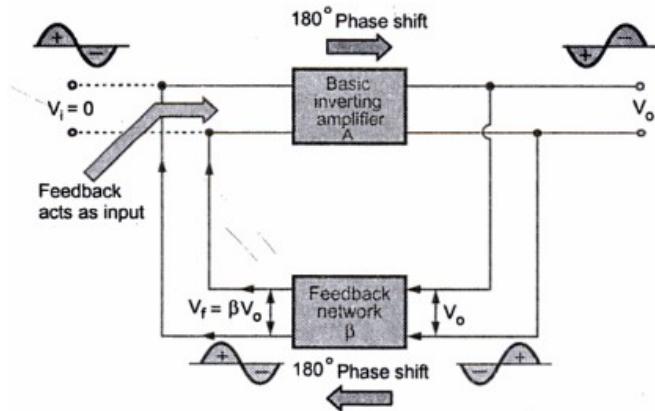


Figure 4.4: Oscillator Block diagram

Consider the block diagram shown in Figure 4.4 with **positive feedback**. Assume a fictitious voltage  $V_i$  at the amplifier input. This results in an output voltage:

$$V_o = AV_i$$

after the amplifier stage, and a feedback voltage:

$$V_f = \beta V_o$$

after the feedback network. Substituting for  $V_o$ :

$$V_f = \beta(AV_i) = A\beta V_i$$

Here, the product  $A\beta$  is referred to as the **loop gain**. For the circuit to work as an oscillator, the feedback voltage  $V_f$  must drive the amplifier. Hence,  $V_f$  must act as the input voltage  $V_i$ .

When the fictitious input voltage  $V_i$  is removed, the circuit continues to operate because the feedback voltage is sufficient to sustain the amplifier operation. The output waveform will continue to exist if the following condition is satisfied:

$$A\beta = 1$$

To achieve **sustained oscillations** using an electronic circuit, it must meet **Barkhausen's Criterion**, proposed by Heinrich Georg Barkhausen (a German Physicist). The criterion consists of two conditions:

- Phase Shift Condition:** The total phase shift around the loop, as the signal proceeds from input through the amplifier, feedback network, and back to the input again (amplifier-feedback network-amplifier circuit), should be:

$$0^\circ \text{ or } 360^\circ$$

- Magnitude Condition:** The magnitude of the product of the open-loop gain  $A$  and the feedback factor  $\beta$  must be unity:

$$|A\beta| = 1$$

By satisfying these two conditions, the circuit works as an oscillator, producing sustained oscillations.

However, in practice, if  $A\beta > 1$ , the system can start oscillating by amplifying ambient noise voltage. The oscillations are growing type. The amplitude of oscillations goes on increasing as shown in Figure 4.5. The resulting waveform may not be a perfect sinusoid. The closer the value of  $A\beta$  is to 1, the more sustained and sinusoidal the output waveform becomes shown in Figure 4.7. If  $A\beta < 1$  then the oscillations are decaying type is shown in Figure 4.6 . The oscillations' amplitude decreases exponentially, and the oscillations finally cease.

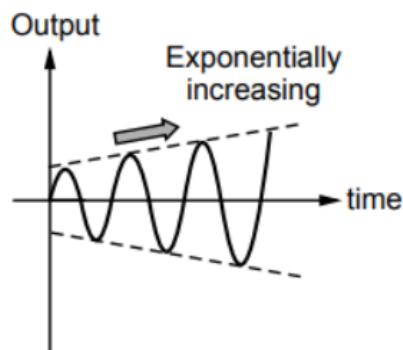


Figure 4.5: Growing  $A\beta > 1$

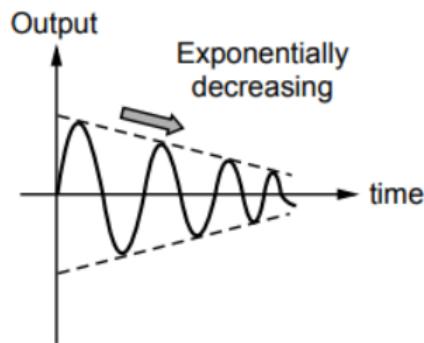


Figure 4.6: Decaying,  $A\beta < 1$

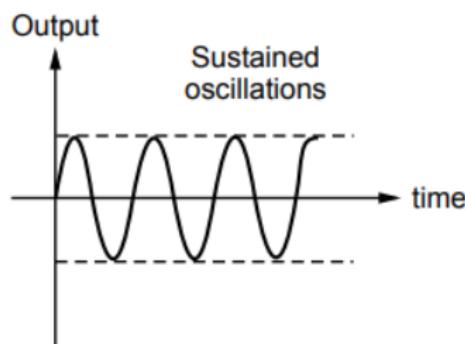


Figure 4.7: Sustainable,  $A\beta=1$

## 4.6 Types of Oscillators

1. RC Oscillator (Low frequency signal generator)
  - (a) RC Phase Shift Oscillator
2. LC Oscillator (High frequency signal generator)
  - (a) Hartley Oscillator
  - (b) Colpitts Oscillator

### 4.6.1 RC Phase Shift Oscillator

A **RC Phase Shift Oscillator** is an electronic circuit that generates a low frequency sine wave signal. It is designed for the generation of low-frequency sinusoidal oscillations with the audio frequencies typically ranging from 20 Hz to 20 kHz.

#### Circuit Operation

The circuit diagram of an RC phase shift oscillator is shown in Figure 4.8.

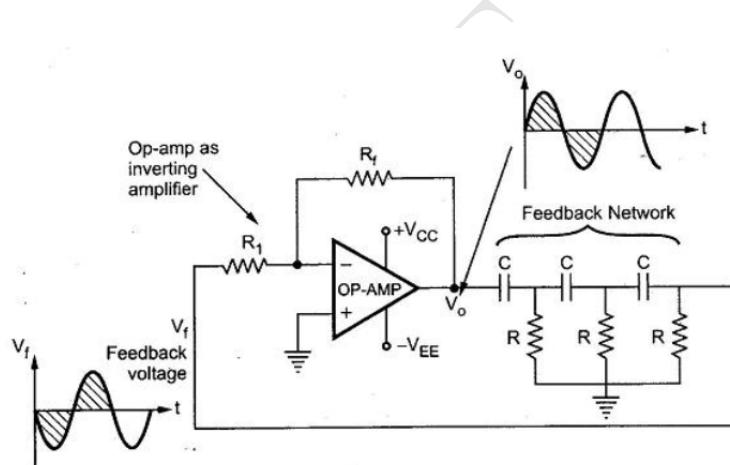


Figure 4.8: RC Phase Shift Oscillator

In this configuration:

- An **op-amp** is used as an **inverting amplifier**, generating a phase shift of  $180^\circ$ .
- The feedback network consists of **three RC sections** connected in a ladder configuration.
- Each RC section contributes a phase shift of approximately  $60^\circ$ , giving a total of  $180^\circ$ .

The impedance  $Z$  of the each RC circuit is given by:

$$\begin{aligned} Z &= R - jX_c \\ |Z| &= \sqrt{R^2 + X_c^2}, \\ \Phi &= \tan^{-1} \left( \frac{X_c}{R} \right) \end{aligned}$$

By choosing appropriate values of  $R$  and  $C$ , the phase angle  $\phi$  can be adjusted to equal  $60^\circ$ , as required by the RC phase shift oscillator.

No external input signal is required to start oscillations. The oscillations are self starting and begin as soon as DC power is applied. Under the room temperature, free electrons in the resistance generate a noise voltage, across the resistance. Such noise voltages or fluctuations are amplified in the circuit, initiating a weak oscillation. The output of the inverting amplifier is applied to the feedback network. This signal which is fed back to the amplifier drives it further.

Thus, the total phase shift around the loop is:

$$180^\circ \text{ (from amplifier)} + 180^\circ \text{ (from RC network)} = 360^\circ$$

This satisfies the condition for **positive feedback**, allowing the circuit to oscillate in accordance with Barkhausen criteria. The **frequency of oscillation** of the RC phase shift oscillator is given by:

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

#### 4.6.2 Hartley Oscillator

A **Hartley Oscillator** is an electronic circuit that generates a high frequency sine wave signal. It is designed for the generation of high-frequency sinusoidal oscillations with the radio frequencies typically ranging from 10 kHz to 100 MHz.

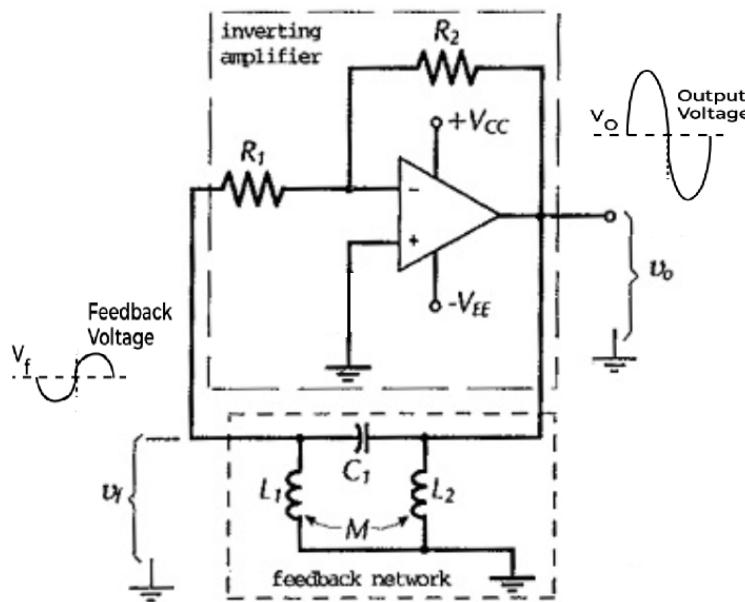


Figure 4.9: Hartley Oscillator

A Hartley oscillator uses an **operational amplifier (Op-Amp)** configured as an inverting amplifier, which introduces a phase shift of  $180^\circ$ . The feedback network of a **Hartley Oscillator** consists of two inductors  $L_1$  and  $L_2$ , and a single capacitor  $C$ . The LC tank circuit is formed by connecting two inductors  $L_1$  and  $L_2$  in series, and placing

them in parallel with the capacitor  $C$ .

Even though there is no input signal, the small noise voltages are amplified by the op-amp when the power supply is given to the circuit. At the same time, the capacitor  $C_1$  starts charging. When the capacitor is fully charged, it starts discharging through inductor  $L_2$ . The electrostatic energy stored in the capacitor gets transferred to the inductors as a magnetic flux when the capacitor is fully discharged. Once the energy is transferred, the inductors start discharging and capacitor get charged again. This transfer of energy between the capacitor and the inductors gives an oscillation across  $L_2$ . The oscillations from  $L_2$  are transferred to  $L_1$ . The voltage across  $L_1$  is fed back to the amplifier is in opposite phase to that of the voltage across  $L_2$ , since the ground is provided between  $L_1$  and  $L_2$ .

This results in a total phase shift of:

$$180^\circ \text{ (from amplifier)} + 180^\circ \text{ (from tank circuit)} = 360^\circ$$

This satisfies the condition for **positive feedback**, allowing the circuit to oscillate in accordance with Barkhausen criteria.

The **frequency of oscillation** is given by:

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

where

$$L_{eq} = L_1 + L_2$$

If mutual inductance  $M$  exists between  $L_1$  and  $L_2$ , then:

$$L_{eq} = L_1 + L_2 + 2M$$

The feedback factor is given by:

$$\beta = \frac{L_1}{L_2}$$

The condition for sustained oscillations is:

$$|A\beta| \geq 1$$

$$\Rightarrow |A| \geq \frac{1}{\beta}$$

$$\Rightarrow |A| \geq \frac{L_2}{L_1}$$

### 4.6.3 Colpitts Oscillator

A **Colpitts Oscillator** is an electronic circuit that generates a high frequency sine wave signal. It is designed for the generation of high-frequency sinusoidal oscillations with the radio frequencies typically ranging from 20 kHz to 300 MHz.

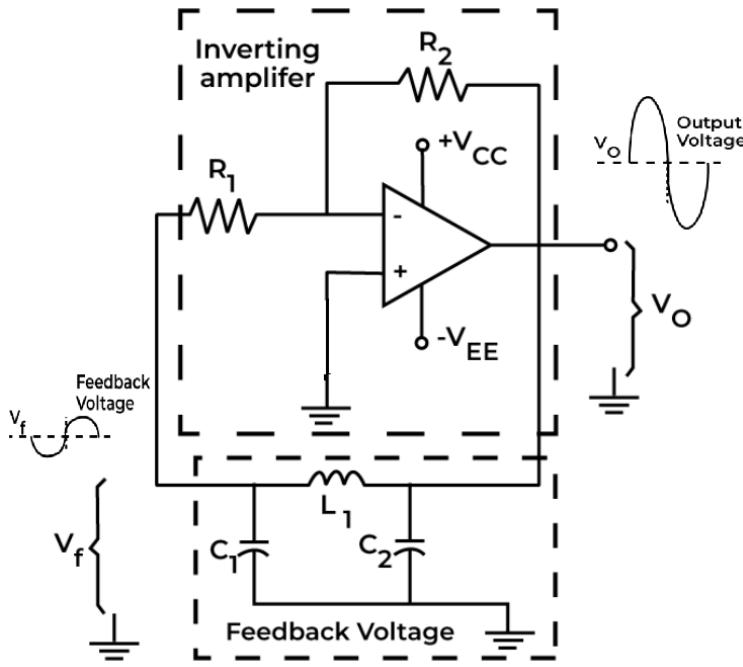


Figure 4.10: Colpitts Oscillator

A Colpitts oscillator uses an **operational amplifier (Op-Amp)** configured as an inverting amplifier, which introduces a phase shift of  $180^\circ$ . The feedback network of a **Colpitts Oscillator** consists of two capacitors  $C_1$  and  $C_2$ , and a single inductor  $L$ . The LC tank circuit is formed by connecting two capacitors  $C_1$  and  $C_2$  in series, and placing them in parallel with the inductor  $L_1$ .

Even though there is no input signal, the small noise voltages are amplified by the op-amp when the power supply is given to the circuit. At the same time, the capacitors  $C_1$  and  $C_2$  start charging. Once the capacitors are fully charged, they start discharging through the inductor  $L_1$ . The electrostatic energy stored in the capacitors gets transferred to the inductor as a magnetic flux when the capacitors are fully discharged. Once the energy is transferred, the inductors start discharging, and the capacitors get charged again. This transfer of energy between the capacitor and the inductor gives an oscillation. The voltage across  $C_1$  is fed back to the amplifier is in opposite phase to that of the voltage across  $C_2$ , since the ground is provided between  $C_1$  and  $C_2$ .

This results in a total phase shift of:

$$180^\circ \text{ (from amplifier)} + 180^\circ \text{ (from tank circuit)} = 360^\circ$$

This satisfies the condition for **positive feedback**, allowing the circuit to oscillate in accordance with Barkhausen criteria. **The frequency of oscillations** is given by,

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Where,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

The feedback factor is:

$$\beta = \frac{C_2}{C_1}$$

The condition for sustained oscillations is:

$$|A\beta| > 1$$

$$\Rightarrow |A| > \frac{1}{\beta}$$

$$\Rightarrow |A| > \frac{C_1}{C_2}$$

## 4.7 Numerical on Oscillator

- A RC phase shift oscillator uses three identical RC sections. Each resistor  $R = 10 k\Omega$  and each capacitor  $C = 0.01 \mu\text{F}$ . Calculate the frequency of oscillation.

**Solution:**

The frequency of oscillation for a RC phase shift oscillator is given by:

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

Substitute the values:

$$R = 10 k\Omega = 10 \times 10^3 \Omega, \quad C = 0.01 \mu\text{F} = 0.01 \times 10^{-6} \text{ F}$$

$$f = \frac{1}{2\pi \times 10 \times 10^3 \times 0.01 \times 10^{-6} \times \sqrt{6}}$$

$$f = \frac{1}{2\pi \times 10^{-4} \times \sqrt{6}} \approx \frac{1}{2\pi \times 10^{-4} \times 2.45}$$

$$f \approx \frac{1}{1.54 \times 10^{-3}} \approx 64.9 \text{ Hz}$$

**Answer:**  $f \approx 64.9 \text{ Hz}$

- In an RC phase shift oscillator,  $R = 500 \Omega$  and  $C = 0.1 \mu\text{F}$ . Calculate the frequency of oscillations.

**Given:**  $R = 500 \Omega, C = 0.1 \mu\text{F}$

**Frequency of oscillations is given by**

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$f = \frac{1}{2\pi \times 500 \times 0.1 \times 10^{-6} \times \sqrt{6}}$$

$$\therefore f = 1.299 \text{ kHz}$$

3. In an RC phase shift oscillator,  $R = 1000 \Omega$ . If the frequency of oscillations is 5 kHz, calculate the value of  $C$ .

**Given:**  $R = 1000 \Omega$ ,  $f = 5 \text{ kHz}$

**Frequency of oscillations is given by**

$$f = \frac{1}{2\pi RC\sqrt{6}} \quad \text{or} \quad C = \frac{1}{2\pi Rf\sqrt{6}}$$

$$\therefore C = \frac{1}{2\pi \times 1000 \times 5000 \times \sqrt{6}}$$

$$C = 0.0129 \mu\text{F}$$

4. Design an RC phase shift oscillator to generate a frequency of 1 kHz. Use equal resistor and capacitor values for simplicity.

**Solution:**

We are required to design an RC phase shift oscillator to generate a frequency of:

$$f = 1 \text{ kHz} = 1000 \text{ Hz}$$

The frequency of oscillation for a 3-stage RC phase shift oscillator is given by:

$$f = \frac{1}{2\pi RC\sqrt{6}} \Rightarrow RC = \frac{1}{2\pi f\sqrt{6}}$$

Substituting the known values:

$$RC = \frac{1}{2\pi \cdot 1000 \cdot \sqrt{6}} \approx 6.49 \times 10^{-5}$$

Let us choose:

$$C = 0.01 \mu\text{F} = 10^{-8} \text{ F}$$

Then, the required resistance is:

$$R = \frac{6.49 \times 10^{-5}}{10^{-8}} = 6.49 \times 10^3 = 6.49 \text{ k}\Omega$$

**Final Component Values:**

- $R = 6.49 \text{ k}\Omega$
- $C = 0.01 \mu\text{F}$
- Number of RC stages = 3

**Circuit:**

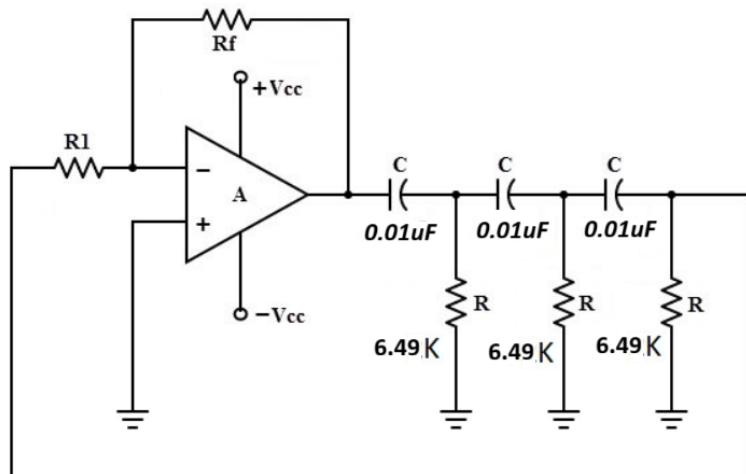


Figure 4.11: RC Phase Shift Oscillator

- In a Hartley oscillator, the value of the capacitor in the tuned circuit is  $500 \text{ pF}$ , and the two sections of the coil have inductances  $38 \mu\text{H}$  and  $12 \mu\text{H}$ . Find the frequency of oscillations and the feedback factor  $\beta$ .

**Solution:**

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

Where,

$$\begin{aligned} L &= L_1 + L_2 = 38 \times 10^{-6} + 12 \times 10^{-6} = 50 \times 10^{-6} \text{ H} \\ C &= 500 \text{ pF} \end{aligned}$$

$$\therefore f_o = \frac{1}{2\pi\sqrt{50 \times 10^{-6} \times 500 \times 10^{-12}}}$$

$$= 1 \text{ MHz}$$

**Feedback factor  $\beta$ :**

$$\beta = \frac{L_1}{L_2} = \frac{38 \times 10^{-6}}{12 \times 10^{-6}} = 3.166$$

- A Hartley oscillator uses two inductors  $L_1 = 10 \mu\text{H}$ ,  $L_2 = 40 \mu\text{H}$ , and a capacitor  $C = 100 \text{ pF}$ . Calculate the frequency of oscillation.

**Solution:** The frequency of oscillation is given by:

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

Substitute the values:

- $L_1 + L_2 = 50 \mu\text{H} = 50 \times 10^{-6} \text{ H}$

- $C = 100 \text{ pF} = 100 \times 10^{-12} \text{ F}$

$$f = \frac{1}{2\pi\sqrt{(50 \times 10^{-6}) \cdot (100 \times 10^{-12})}} = \frac{1}{2\pi\sqrt{5 \times 10^{-15}}}$$

$$f = \frac{1}{2\pi \cdot 7.07 \times 10^{-8}} \approx \frac{1}{4.44 \times 10^{-7}} \approx 2.25 \text{ MHz}$$

7. Design a Hartley oscillator to operate at  $f = 1 \text{ MHz}$  using a capacitor  $C = 100 \text{ pF}$ . Determine the total inductance  $L_1 + L_2$ .

The frequency of oscillation for a Hartley oscillator is given by:

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

Rearranging to solve for  $L_1 + L_2$ :

$$L_1 + L_2 = \frac{1}{(2\pi f)^2 C}$$

Substitute the known values:

- $f = 1 \text{ MHz} = 1 \times 10^6 \text{ Hz}$
- $C = 100 \text{ pF} = 100 \times 10^{-12} \text{ F}$

$$\begin{aligned} L_1 + L_2 &= \frac{1}{(2\pi \cdot 10^6)^2 \cdot 100 \times 10^{-12}} \\ &= \frac{1}{(4\pi^2 \cdot 10^{12}) \cdot 100 \times 10^{-12}} = \frac{1}{4\pi^2 \cdot 100} \\ &\approx \frac{1}{394.78} \approx 2.53 \times 10^{-4} \text{ H} = 2.53 \mu\text{H} \end{aligned}$$

Therefore, the total inductance should be:

$$L_1 + L_2 = 2.53 \mu\text{H}$$

8. A Colpitt's oscillator uses an inductor  $L = 1 \text{ mH}$ , and two capacitors:  $C_1 = 100 \text{ pF}$ ,  $C_2 = 200 \text{ pF}$ . Calculate the frequency of oscillation.

**Solution:** Given:

$$L = 1 \text{ mH} = 1 \times 10^{-3} \text{ H}, \quad C_1 = 100 \text{ pF} = 100 \times 10^{-12} \text{ F}, \quad C_2 = 200 \text{ pF} = 200 \times 10^{-12} \text{ F}$$

The equivalent capacitance of  $C_1$  and  $C_2$  in series is given by:

$$C_{\text{eq}} = \frac{C_1 \cdot C_2}{C_1 + C_2} = \frac{100 \times 10^{-12} \cdot 200 \times 10^{-12}}{100 \times 10^{-12} + 200 \times 10^{-12}} = \frac{2 \times 10^{-20}}{3 \times 10^{-10}} = 6.67 \times 10^{-11} \text{ F}$$

The frequency of oscillation is:

$$f = \frac{1}{2\pi\sqrt{L \cdot C_{\text{eq}}}} = \frac{1}{2\pi\sqrt{1 \times 10^{-3} \cdot 6.67 \times 10^{-11}}} = \frac{1}{2\pi \cdot \sqrt{6.67 \times 10^{-14}}}$$

$$f = \frac{1}{2\pi \cdot 8.17 \times 10^{-7}} \approx \frac{1}{5.13 \times 10^{-6}} \approx 195 \text{ kHz}$$

$$f \approx 195 \text{ kHz}$$

9. Design a Colpitt's oscillator to operate at a frequency of  $f = 1 \text{ MHz}$  using an inductor of  $L = 10 \mu\text{H}$ . Choose the capacitors such that  $C_1 = 2C_2$ . Find the values of  $C_1$  and  $C_2$ .

**Solution:** The frequency of oscillation for a Colpitt's oscillator is given by:

$$f = \frac{1}{2\pi\sqrt{L \cdot C_{\text{eq}}}}$$

where  $C_{\text{eq}}$  is the equivalent capacitance of  $C_1$  and  $C_2$  in series:

$$C_{\text{eq}} = \frac{C_1 \cdot C_2}{C_1 + C_2}$$

Given that  $C_1 = 2C_2$ , we substitute:

$$C_{\text{eq}} = \frac{2C_2 \cdot C_2}{2C_2 + C_2} = \frac{2C_2^2}{3C_2} = \frac{2}{3}C_2$$

Substitute into the frequency formula:

$$f = \frac{1}{2\pi\sqrt{L \cdot \frac{2}{3}C_2}} \Rightarrow C_2 = \frac{3}{2L} \left( \frac{1}{2\pi f} \right)^2$$

Now, substituting the known values  $L = 10 \times 10^{-6} \text{ H}$ , and  $f = 1 \times 10^6 \text{ Hz}$ :

$$C_2 = \frac{3}{2 \cdot 10 \times 10^{-6}} \cdot \left( \frac{1}{2\pi \cdot 10^6} \right)^2 = \frac{3}{20 \times 10^{-6}} \cdot \frac{1}{4\pi^2 \cdot 10^{12}}$$

$$C_2 \approx \frac{3}{7895.68 \times 10^6} \approx 0.38 \times 10^{-9} = 380 \text{ pF}$$

$$C_1 = 2C_2 = 2 \times 380 \text{ pF} = 760 \text{ pF}$$

$$C_1 = 760 \text{ pF}, \quad C_2 = 380 \text{ pF}$$

**Circuit:**

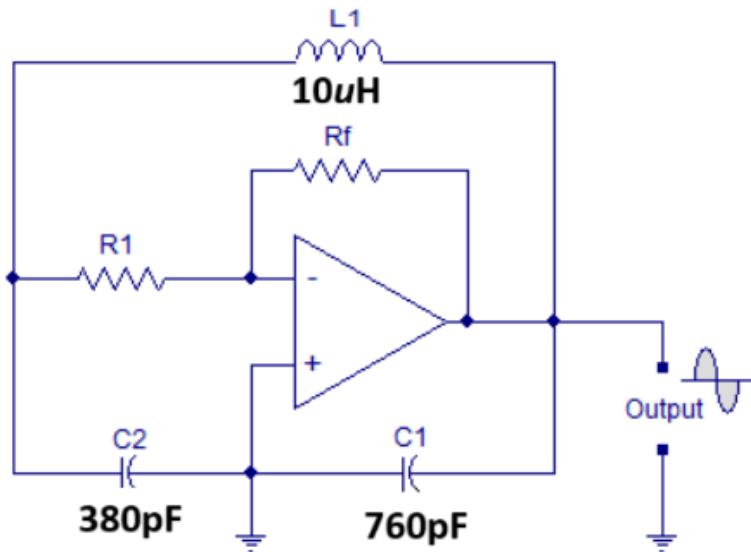


Figure 4.12: Colpitts Oscillator

10. In a Colpitts oscillator,  $C_1 = 100 \text{ pF}$ ,  $C_2 = 260 \text{ pF}$ . Find the value of  $L$  if the frequency of oscillations is  $40 \text{ kHz}$ .

**Given:**

$$C_1 = 100 \text{ pF}, \quad C_2 = 260 \text{ pF}, \quad f = 40 \text{ kHz}$$

**Frequency of oscillation:**

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

**Where**

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$C_{eq} = \frac{100 \times 10^{-12} \times 260 \times 10^{-12}}{100 \times 10^{-12} + 260 \times 10^{-12}} = 37.5 \text{ pF}$$

**To find  $L$ , square both sides:**

$$f^2 = \frac{1}{4\pi^2 L C_{eq}}$$

$$\Rightarrow L = \frac{1}{4\pi^2 f^2 C_{eq}}$$

$$L = \frac{1}{4\pi^2 (40 \times 10^3)^2 (37.5 \times 10^{-12})}$$

$$\therefore L = 0.422 \text{ H}$$

11. In a colpitt's oscillator,  $L = 5\text{mH}$ . Find the  $C_1$  and  $C_2$  if the frequency of oscillation is  $f = 50\text{ kHz}$ . Assume a feedback factor of  $\beta = 10\%$ .

$$L = 5\text{ mH} \quad f = 50\text{ kHz}, \quad \beta = 10\% = 0.1$$

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$C_{equ} = \frac{C_1 C_2}{C_1 + C_2}$$

Squaring  $f$  both sides,

$$f^2 = \frac{1}{4\pi^2 LC_{eq}}$$

$$C_{equ} = \frac{1}{4\pi^2 f^2 L} = \frac{1}{4\pi^2 \times (50 \times 10^3)^2 \times 5 \times 10^{-3}}$$

$$C_{equ} = 2 \cdot 02\text{nF}$$

$$C_{equ} = \frac{C_1 C_2}{C_1 + C_2}, \quad \beta = 0.1 = \frac{C_2}{C_1}$$

$$C_2 = 0.1C_1$$

$$C_{equ} = \frac{C_1 C_2}{C_1 + C_2} = \frac{C_1 \times 0.1C_1}{1.1C_1} = \frac{0.1C_1}{1.1}$$

$$2.02\text{nF} = \frac{0.1C_1}{1.1}$$

$$\therefore C_1 = 22 \cdot 22\text{nF}$$

$$\Rightarrow C_2 = 0.1 \times 22 \cdot 22\text{nF} = 2 \cdot 22\text{nF}$$

# Chapter 5

## Fundamentals of Communication and Embedded Systems

### 5.1 Introduction

Communication is the basic process of exchange of information or transmission of information from one point to another. Basically, the information is generated from the thought process in the human mind and it is sent to the receiver in the form of speech, sign or in any other understandable form.

Communication enters our daily life in many different ways – such as telephone, radio, TV, computers... etc. Communication provides directions for ships, aircrafts, rockets and satellites in space. A number of modern communication systems include mobile communication, point to point communication, radio telemetry and so on. Communication need not directly involve human beings always. For example communication between two or more computers, the human decision/intervention is required only while giving commands or to monitor the results.

### 5.2 Basic Blocks of Communication Systems

Irrespective of the applications, basic blocks of electronic communication system is as shown in figure 5.1. This involves transmitter, channel and receiver. The transmitter is located in one point and the receiver is located somewhere else and the channel is the medium that connects them.

The elements of communication system are as follows:

- Information
- Transmitter
- Communication channel or medium
- Noise
- Receiver

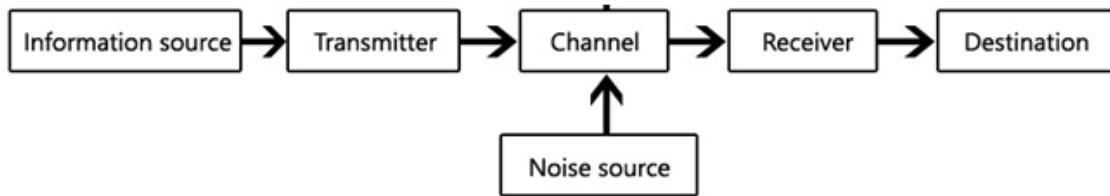


Figure 5.1: Block diagram of communication system

**Information:** Information or message to be communicated are generated from information sources. Examples for main sources of information are human brain or changes in the physical environment. Information may be the speech signal, image, data music, video etc. The amount of information is measured in bits.

**Transmitter:** The information generated from a source is not in a suitable form to be transmitted directly through the channel. The transmitter is an electronic circuit designed to convert the information into a signal suitable to be transmitted over a given communication channel. Signal in its original form will be non-electrical in nature, such signal cannot be transmitted through the channel. Using suitable transducers the messages are converted to the electrical form and then they are processed and coded before the transmission. The signal processing techniques are also applied at this stage to make the communication more effective. Transmitter includes – transducer, modulator, filters, encoder and also amplifiers to ensure faithful signal transmission and reception.

**Communication channel:** The communication channel is the medium through which the electronic signal is transmitted. The channel connects the transmitter and receiver either through wire or without wire.

In general the communication channel can be classified as:

- Wired channel or line communication
- Wireless channel or radio channel

**Wired channel:** The examples for a wired medium are: copper wire, coaxial cable, fibre optic cable. For applications like telephony two physical wires or conductors are connected between the transmitter and the receiver. Latest applications use optical fibre cables, which are well known for their high capacity and immunity to noise. In optical fibres the information will be transmitted in the form of light wave. Coaxial cables are preferred over pair of wires as they have higher bandwidth and lower losses. Optical fibres are logical extension of coaxial cables which can be operated at higher frequencies and greater bandwidths. Optical fibres are also cheaper and are more immune to interference and noise.

**Wireless channel:** most commonly known as radio channel or electromagnetic medium. This type of channel connects the transmitter and receiver wirelessly. No

physical wire is necessary to carry the information, signal is sent through air or free space. Radio communication requires two antennas for the transmission and reception. The signal received at the receiving antenna will be attenuated and hence its amplitude will be smaller. With proper amplification, the signal will be processed further to get back the original information. Radio communication allows the signal to be transmitted to any longer distance – thousands of kilometres, perhaps even more.

**Noise:** Noise is basically any unwanted signal that disturbs the communication. Noise enters the communication system normally in the medium or channel. Noise may also be generated at the transmitter or receiver. Means noise can be internally generated in a system or externally added to the signal.

Noises can also be classified as **natural noise and man-made noise**. **Natural noise** includes – lightening during rainy season, radiations from the sun and cosmic radiations. **Man-made noise** is the noise generated by the electric ignition systems, industrial noise, fluorescent lights etc. Noise imposes serious problem on electronic communication systems, if not controlled. Noise cannot be completely eliminated, but its effect can be reduced using different methods.

**Receiver:** The receiver is a collection of electronic circuits designed to convert the signal back to its original form. The process includes amplification, mixing, demodulation and decoding etc. The receiver performs the task of operating on the received signal to generate the estimation of the original signal. If the estimated signal is same as the original transmitted signal, then we say that the reception is proper.

### 5.3 Modulation

The transmission of an information-bearing signal over a communication channel requires a shift in the range of frequencies from the original to another frequency range suitable for transmission. This is accomplished through the process of modulation. Modulation is defined as the process by which some characteristic of a carrier signal is varied in accordance with a modulating signal. The message signal is referred to as modulating signal and the result of modulation is referred to as modulated signal. The carrier signal is usually a high frequency signal than the message signal. The message signal modifies the amplitude, frequency or phase of the carrier signal in the process of modulation. Hence, the types of modulation are:

1. Amplitude modulation – amplitude of the carrier is varied in accordance with the modulating signal, keeping the frequency and phase of the carrier constant
2. Frequency modulation – the frequency of the carrier signal is varied according to the modulating signal
3. Phase modulation – phase of the carrier is varied in accordance with the modulating signal.

### 5.3.1 Need for modulation

The message signal cannot be transmitted in its direct form, over the communication channel. It should be modulated suitably. The advantages of the modulation are:

1. Reduces the antenna height
2. The range(distance) of communication can be increased
3. Signals can be multiplexed
4. Bandwidth can be used efficiently
5. Quality of reception can be improved
6. Avoids mixing of the signals

**Height of the antenna:** Minimum height of the antenna for proper transmission and reception is  $\lambda/4$ , where  $\lambda$  is the wavelength. We know that,  $\lambda = c/f$ , where  $c$  is velocity of light and  $f$  is the frequency. At lower frequencies wavelength is high and antenna height is also high. Hence by modulating the message signal using a high frequency carrier, the height of the antenna can be decreased.

**Range of communication:** Since message signal frequency range is low (20 Hz to 20 kHz), the possibility of signal attenuation is more. Modulation increases the frequency and hence the range of communication may be increased.

**Multiplexing:** modulation allows the multiplexing of signals. Multiplexing means two or more message signals are transmitted simultaneously over the same channel. Eg: broadband data services, TV channels operating simultaneously, radio stations in MW and SW band simultaneously.

**Bandwidth utilization:** Bandwidth of the modulated signal can be made smaller or larger than the original signal.

**Quality of reception:** by using specific types of modulation schemes such as FM, noise performance of the receiver can be improved.

**Avoids mixing:** The message signal frequencies are located within the range from 20 Hz to 20 kHz. Simultaneous transmission of multiple message signals may lead to mixing of the signals, which may cause interference in the reception. Instead, if each message signal is modulated separately using different carrier frequencies, then each signal will be located at different portions in the spectrum. The receiver tuned to particular carrier will be able to receive the signal. Therefore modulation avoids mixing of signals.

## 5.4 Telecommunication

There are many applications of communication systems, but telecommunication is the most widely used application as it connects the people around the globe. The communication device used for this communication device is ‘telephone’. If the wireless communication is taking place with the movement of the communication devices, it is referred

to as **mobile communication**. Today the telephone is replaced by a mobile phone and communication is still possible with the movement of the sending or receiving end devices or both.

If the mobile communication involves mobile devices and a coordinator station called base transceiver station or base station within a small geographical area, the communication is **cellular communication**. Each cellular base station is allocated a group of radio channels to be used within a small geographic area called a cell. The scheme started initially for voice transmission. But, today it has been providing internet service, transmission of audio, image and video.

## 5.5 Cellular Communication System

Figure 5.2 shows the block diagram of a cellular communication system in which the hexagon shaped cells are shown. The automobile (mobile user with the mobile device) shown in the figure wirelessly communicate when it moves from one cell to another cell. The base stations of the respective cell connect the mobile devices using Radio Frequency (RF) link. The base stations are controlled by Mobile switching centres (MSC) which are connected to the existing telephone system referred to as Public Switched Telephone Network (PSTN). Base station is provided with a call/data communication handling processor.

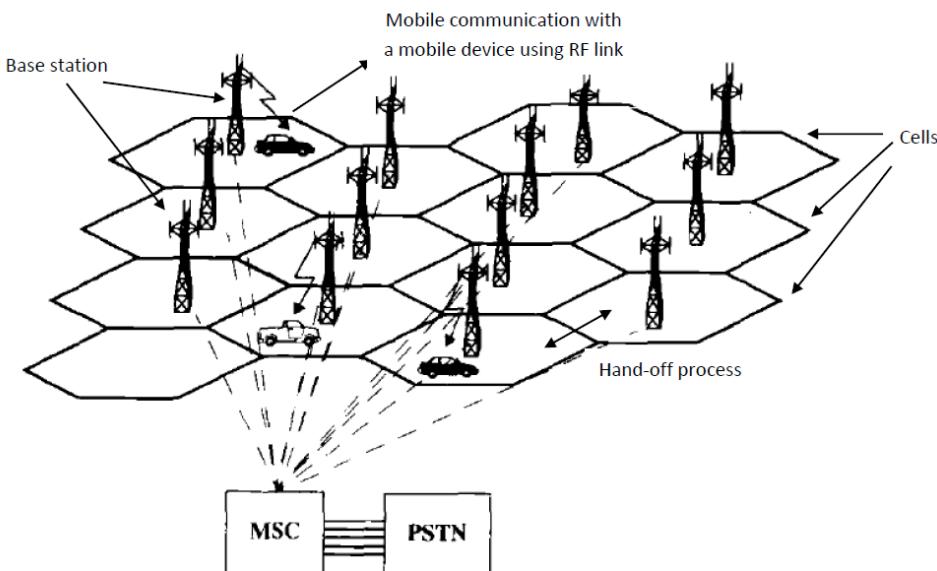


Figure 5.2: Cellular communication system

**RF linkage using Base station and Mobile station:** The entire radio frequency spectrum is divided into small frequency bands. The RF connectivity is established by the MSC with the help of Base station when a call is to be established. It assigns an available frequency band (channel), out of the entire bandwidth to the mobile unit temporarily till the end of the call.

**Hand-off process:** Whenever a mobile user crosses one cell boundary and moves to another cell with an active call, the call is softly handed over to a new frequency band.

the MSC adjusts the transmitted power of the mobile phone and changes the channel of the mobile unit and base stations in order to maintain call quality. This is called a hand-off in mobile communication.

### 5.5.1 Different events between the mobile unit and a cellular system while a phone number is entered

Before the MSC connects to an available frequency band, the initial handshaking is achieved by 4 different frequency bands or channels. They are shown in Table 5.1.

Table 5.1: Channels for initiating the call and voice transmission

Type of Channels	Name of the Channel	Channels used for:
Control channels	Forward Control Channel (FCC)	Initiating mobile calls from the base station to mobiles.
	Reverse Control Channel (RCC)	Initiating mobile calls from the mobiles to base station.
Voice channels	Forward Voice Channel (FVC)	Voice transmission from the base station to mobiles.
	Reverse Voice Channel (RVC)	Voice transmission from mobiles to the base station.

When a mobile originates a call,

1. A call initiation request is sent on the reverse control channel.
2. With this request the mobile unit transmits its telephone number- Mobile Identification Number (MIN), Electronic Serial Number (ESN), and the telephone number of the called party.
3. The mobile also transmits a station class mark (SCM) which indicates what the maximum transmitter power level is for the particular user.
4. The cell base station receives this data and sends it to the MSC.
5. The MSC validates the request, makes connection to the called party through the PSTN,
6. Now, MSC instructs the base station and mobile user to move to an unused forward and reverse voice channel pair to begin the for conversation. Explain

### 5.5.2 Frequency reuse

Cellular systems have grown Figure 3 illustrates the concept of cellular frequency reuse, with the hexagon shaped cells. In the Figure 5.3, cells numbered from A – G forms a group of cells called Cluster. There are 3 such clusters shown in the Figure, with the frequency bands repeated. Cells with the same letter use the same set of frequencies. A cell cluster is outlined in bold and replicated over the coverage area. The N cells which collectively use the complete set of available frequencies is called a cluster.

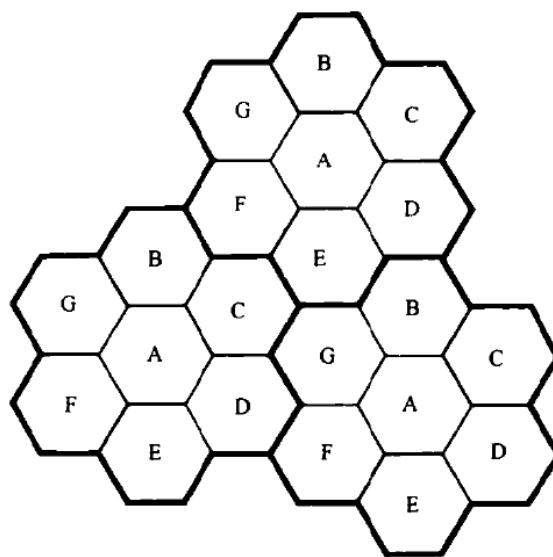


Figure 5.3: Frequency Reuse

From the Figure, it is clear that

1. A cluster uses frequency bands A – G is not repeated in the adjacent cells.
2. The frequency bands are repeated only in the next cluster.

The number of cells in a cluster is cluster size, denoted as ‘N’. Frequency reuse factor is the reciprocal of cluster size. Frequency reuse factor =  $1/N$ . In this example, the cluster size, N, is equal to seven, and the frequency reuse factor is  $1/7$ , since each cell contains one-seventh of the total number of available channels.

### 5.5.3 Why a cell is hexagon in shape?

A cell must be designed to serve the weakest mobiles located at the edge of the cell. The hexagonal cell shape is conceptual. Thus, when considering geometric shapes, the entire region is to be covered without overlap and with equal area. A circle may be thought of to represent the coverage area of a base station, but adjacent circles cannot be overlaid upon a map without leaving gaps creating overlapping regions.

There are three sensible choices:

1. A square;
2. An equilateral triangle;
3. A hexagon.

Theoretically, the radiation zone cannot be represented by a square or triangle. The hexagon permits easy and manageable analysis of a cellular system. For a given distance between the center of a polygon and its farthest perimeter points, the hexagon has the largest area. The hexagon closely approximates a circular radiation pattern. Using this, the fewest number of cells can cover a geographic region, which would occur for an omnidirectional base station antenna.

## 5.6 Embedded Systems

An Electronic/Electro mechanical system which is designed to perform a specific function and is a combination of both hardware and firmware (Software) e.g: Electronic Toys, Mobile Handsets, Washing Machines, Air Conditioners, Automotive Control Units, Set Top Box, DVD Player etc. Embedded Systems are:

- Unique in character and behavior
- With specialized hardware and software

### 5.6.1 Elements of Embedded Systems

An embedded system is a combination of 3 things, Hardware Software Mechanical Components and it is supposed to do one specific task only. The main components of the embedded systems are shown in Figure 5.4:

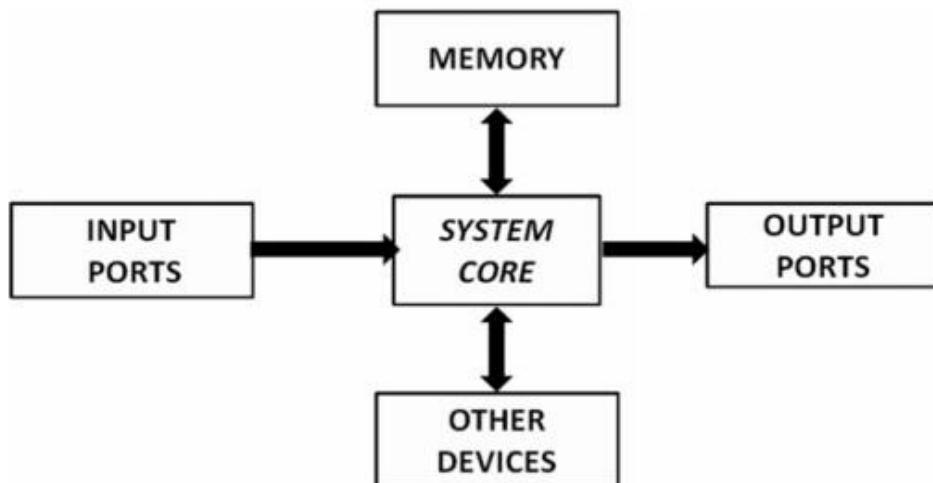


Figure 5.4: Elements of Embedded System

- System core
- Input ports
- Output ports
- Memory
- Other devices

**System core:** A typical embedded system contains a single chip controller which acts as the master brain of the system. The controller can be a Microprocessor or a microcontroller or a Field Programmable Gate Array (FPGA) device or a Digital Signal Processor (DSP) or an Application Specific Integrated Circuit (ASIC)/ Application Specific Standard Product (ASSP).

**Input and Output ports:** Embedded hardware/software systems are basically designed to regulate a physical variable or to manipulate the state of some devices by

sending some control signals to the Actuators or devices connected to the o/p ports of the system, in response to the input signals provided by the end users or Sensors which are connected to the input ports.

Keyboards, push button switches, etc. are examples for common user interface **input devices** whereas LEDs, liquid crystal displays, piezoelectric buzzers, etc. are examples for common user interface **output devices** for a typical embedded system. For example, if the embedded system is designed for any handheld application, such as a mobile handset application, then the system should contain user interfaces like a keyboard for performing input operations and display unit for providing users the status of various activities in progress. The requirement of type of user interface changes from application to application based on domain.

Some embedded systems do not require any manual intervention for their operation. They automatically sense the input parameters from real world through sensors which are connected at input port. The sensor information is passed to the processor after signal conditioning and digitization. The core of the system performs some predefined operations on input data with the help of embedded firmware in the system and sends some actuating signals to the actuator connect connected to the output port of the system.

**Memory:** The memory of the system is responsible for holding the code (control algorithm and other important configuration details). There are two types of memories are used in any embedded system. Fixed memory (ROM) is used for storing code or program. The user cannot change the firmware in this type of memory. The most common types of memories used in embedded systems for control algorithm storage are OTP, PROM, UVEPROM, EEPROM and FLASH.

**Other devices:** The other system components refer to the components which are necessary for the proper functioning of the embedded system. Some of these circuits may be essential for the proper functioning of the processor/controller and firmware execution. Watchdog timer, Reset IC (or passive circuit), brown-out protection IC (or passive circuit), etc. are examples of circuits/ICs which are essential for the proper functioning of the processor/controllers.

### 5.6.2 Difference between Microprocessor and Microcontroller

Table 5.2: Microprocessor Vs Microcontroller

Microprocessor	Microcontroller
It is a heart of computing system	It is a heart of embedded system
Memory and I/O components have to be connected externally	It has internal Memory and I/O components
Due to the external components, power consumption is high	Power consumption is less
Relatively slower	Fast
It has less number of registers, hence more operations are memory-based	It has more number of registers, hence the programs are easier to write.
Program and data are stored in same memory	Program and data are stored in separate memory
Mainly used in the personal computers	Mainly used in washing machine, MP3 players.
cost is high	cost is low

### 5.6.3 Sensors and Actuators

- Embedded system is in constant interaction with the real world
- Controlling/monitoring functions executed by the embedded system is achieved in accordance with the changes happening to the Real World.
- The changes in the system environment or variables are detected by the sensors connected to the input port of the embedded system.
- If the embedded system is designed for any controlling purpose, the system will produce some changes in controlling variable to bring the controlled variable to the desired value.
- It is achieved through an actuator connected to the output port of the embedded system.

#### Sensors:

- A transducer device which converts energy from one form to another for any measurement or control purpose. Sensors acts as input device.
- Example: IR, humidity, PIR(passive infra red) , ultrasonic , piezoelectric , smoke sensors.

#### Actuators:

- A form of transducer device (mechanical or electrical) which converts signals to corresponding physical action (motion). Actuator acts as an output device
- Eg. Electric motor, sliding doors, Escalators, Adjusting the Car Seat.

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