# Department of Computer Science and Engineering In Data Science



# EXPERIMENT NO--5

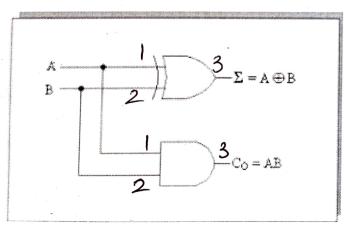
AIM:-To realize half adder and full adder.

RESOURCE REQUIRED: Digital IC trainer kit, AND gate(7408), EX-OR gate (7486), OR gate (7432).

#### THEORY:

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear that a half adder circuit can be easily constructed using one X-OR gate and one AND gate. Half adder is the simplest of all adder circuit, but it has a major disadvantage. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input. So if the input to a half adder have a carry, then it will be neglected it and adds only the A and B bits. That means the binary addition process is not complete and that's why it is called a half adder. The truth table, schematic representation and XOR//AND realization of a half adder are shown in the figure below.

### **Logical Representation**



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# Truth Table - Harf Adder

nput to adder		Output		
Α	В	SUM	CARRY	
0	0	0	0	
0	1	1	0	
1	0	1	0	
1	1	0	1	

From the truth table the expression for sum and carry bits of the output can be obtained as.

Sum, 
$$S = A \times B = A \oplus B$$

Carry,  $C = A \cdot B$ 

#### Full-Adder

A full-adder is a logic circuit having 3 inputs A,B and C (which is the carry from the previous stage) and 2 outputs (Sum and Carry), which will perform according to table 3. The full-adder can handle three binary digits at a time and can therefore be used to add binary numbers in general. The simplest way to construct a full adder is to connect two half- adder and an OR gate as shown in Fig. The full-adder is then the fundamental logic circuit incorporated in digital computers to perform arithmetic functions.

## Logical Representation

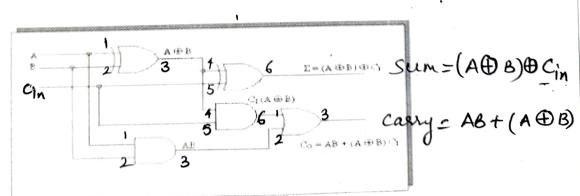


Fig:-Full Addar.

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TRUTH TABLE: - full Adder.

S.No	INPUT			OLITPLIT	OUTPUT	
	Α	В	С	SUM		
1.	0	0	0	0	CARRY	
2.	0	0	1	1	0	
3.	0	1	0	1	0	
4.	0	1	1	0	1	
5.	1	0	0	1	0	
6.	1	0	1	0	1	
7.	1	1	0	0	1	
8.	1	1	1	1	1	

From the truth table the expression for sum and carry bits of the output can be obtained as,

SUM = A'B'C + A'BC' + AB'C' + ABC

CARRY = A'BC + AB'C + ABC' + ABC

- Connections are given as per the circuit diagrams.
- For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
- Apply the inputs and verify the truth table for the half adder and full adder circuits.

#### **CONCLUSION:**

Thus we studied and verified the truth table of half; full adder

## **MCQ QUESTIONS:**

Ι.	How many outputs we get for half adder.							
	a. 1 b. 2 c. 3 , d. 4							
2.	Which Gate we use for making the circuit of half adder							
	a. Ex-OR b. NAND c. NOT d. OR							
3.	We get carry when we add							
	a. 1+0 b. 1+1 c. 0+1 d. 0+0							
4.	A full-adder is a logic circuit having inputs							
	a. 1 b. 2 c. 3 d. 4							
5.	A half adder circuit can be easily constructed using one X-OR gate and one gate							
	a. NOT b. NAND c. NOT d. AND							

#### **REFERENCES:**

1. https://circuitglobe.com/half-adder-and-full-adder-circuit.html