Name - Ameya Barapative Roll No-06 SE-DS

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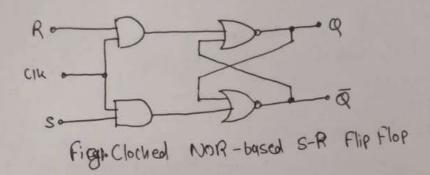
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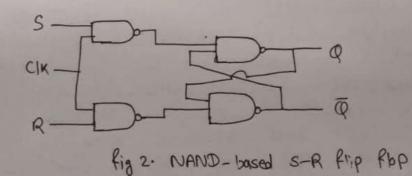
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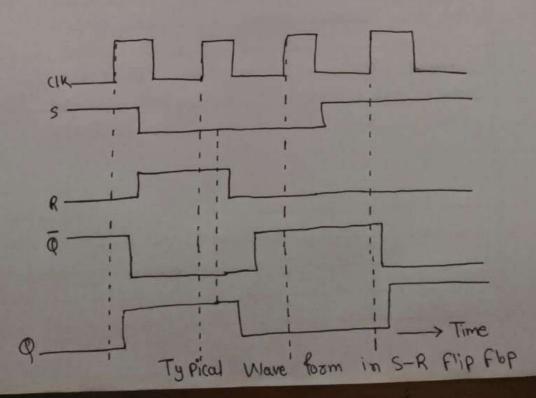
| - | Experiment No-8 |
|---|--|
| | Aim > To fully understand the functionality of S-R flip-flop, J-M flip-flop, D Flip-flop |
| | Theory -> Sequential Circuits: The logic circuits whose output at any matant of time depend not only on the present impresent input but also on the part outputs are called sequential circuit The simplest wind of sequential circuit which is capable of stoning one bit of information is called latch. The operation of basic latch can be modified; by providing an additional control input that determine when the state of the circuit is to be changed. The latch with additional control input is called the flip-flo The additional control input is called the flip-flo clock or chapte input. Different types or flip-flop: There are foor basic types, namely, S-R, J-M, D and T. flipf |
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S-R flip Flop ->

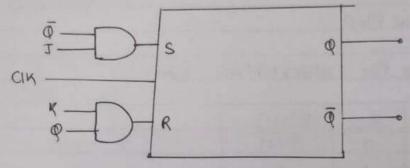




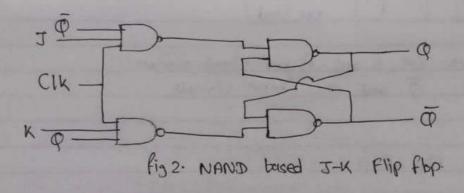


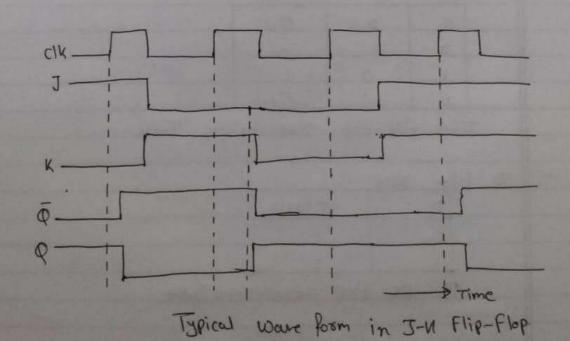
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| | | | | | |
| · S-R | flip f | lop: | | | |
| S-R | Flip f | lop ch | wracteristic | table | |
| | 0 | R (| Q(++1) | TI WIT | Andrew C |
| | S | 0 | Q(t) | | No. of the last of |
| | 0 | 1 | 0 | | |
| | 1 | 0 | 1 | | |
| | 1 | 1 | Not Used | | of Tartial |
| | , ch | 1 6 1 | Rare | input sis | nals. |
| NOT | 3 (1) | 15 00 | 0101 | | |
| | (1) | and | O: COHN | signals | |
| | (9 | and | Q: OHAN | Signale | |
| | | and | Q: COHINT | Signals | |
|). Z-K | 765 | | CO : COHWY | Signals | |
|). J-k | Aip | -f10P | | Signals | |
|). Z-k | Alip | -F10P | Q(th) | Signals | |
|). J-K | Flip | -f10P | | Signals | |
|). J-k | Alip | -F10P | Q(th) | Signals | |
|). J-k | Flip | -F10P | Q(t) Q(t) | Sigrae | |
| | Flip | -F10P | Q(t) Q(t) | Sigrae | |
| | Flip | -F10P | Q(t+1) Q(t) | Sigrae | |
| | Flip | -F10P X 0 1 F15P-F10 | Q(t) Q(t) | Sigrae | |
| | Flip Flip | -F10P | Q(th) Q(t) Q(t) Q(t) | Sigrae | |
| | Flip | -F10P X 0 1 F15P-F10 | Q(t) Q(t) | Sigrae | |
| | Flip D | -F10P K O I F17P-F10 F10P | Q(th) Q(t) Q(t) Q(t) | Sigras Herestic | Table. |

J-K Flip Flop-

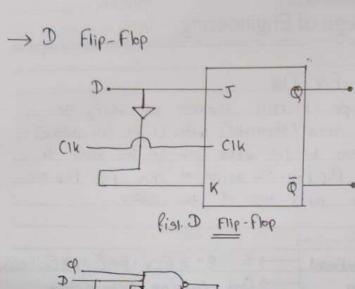


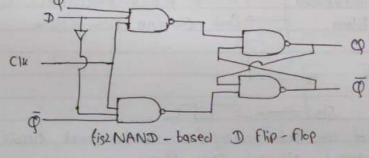
fist J-K Flip-Plop using S-R flip flop.





SARASWATI Education Society's SARASWATI College of Engineering DATE: PAGE NO.: -> Synthesis using Flip-Flop As a simple exertise students can verify the operation of a serial (sequential) order (1 bit Pul) odder) Carry adopt of a one bit full adder can be led back to the input of a D flip flop. The output of this flip flop run be fell beck to the carry import of that adder. → S S= ABCin+ABCin+ABCin+ABCin Combinational -> Cout Cout = AB + ACin + BCin Rloch CinT Verification of the functionality of a combinational circuit using sequential element (Flip-Flop). Cout Cin Truth table of 1 bit full adder. Conclusion - We have fully understood the concept and functionality of S-R, J-M and D frip (log.





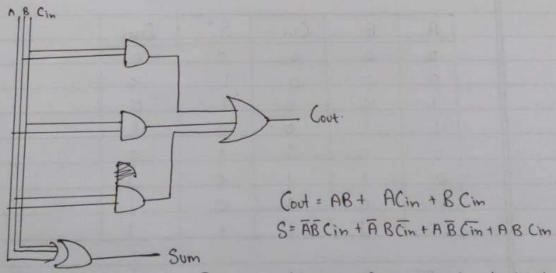


Fig-Chate diagram of combinational circuit (1 bit full adder)