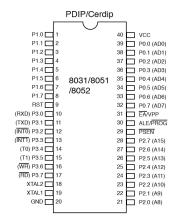
## 8051 Microcontroller:

# Ports



## Virendra Singh

Computer Architecture and Dependable Systems Lab
Department of Electrical Engineering
Indian Institute of Technology Bombay
http://www.ee.iitb.ac.in/~viren/

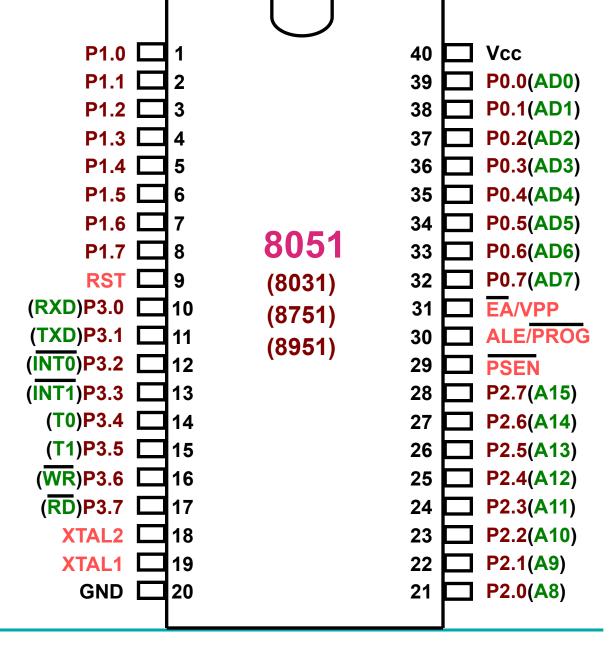
E-mail: viren@ee.iitb.ac.in

EE-309: Microprocessors











CADSL

2

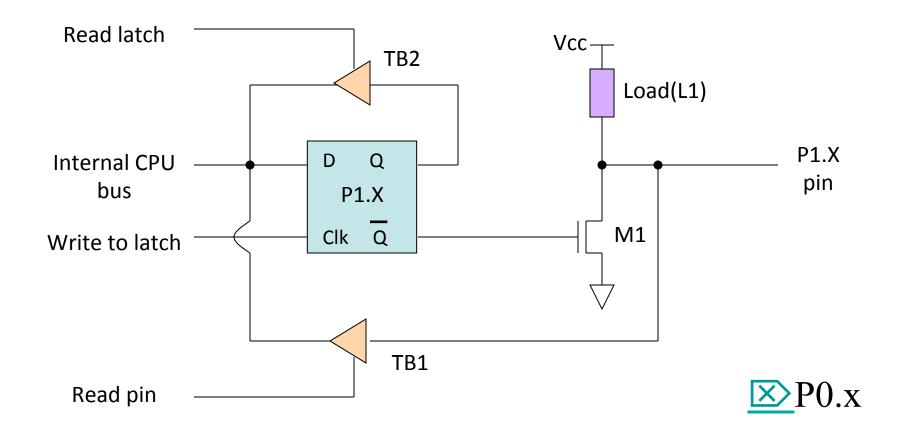
#### 8051 Microcontroller

- Limited by the number of pins
- Pins are used for multiple functionality





#### A Pin of Port 1





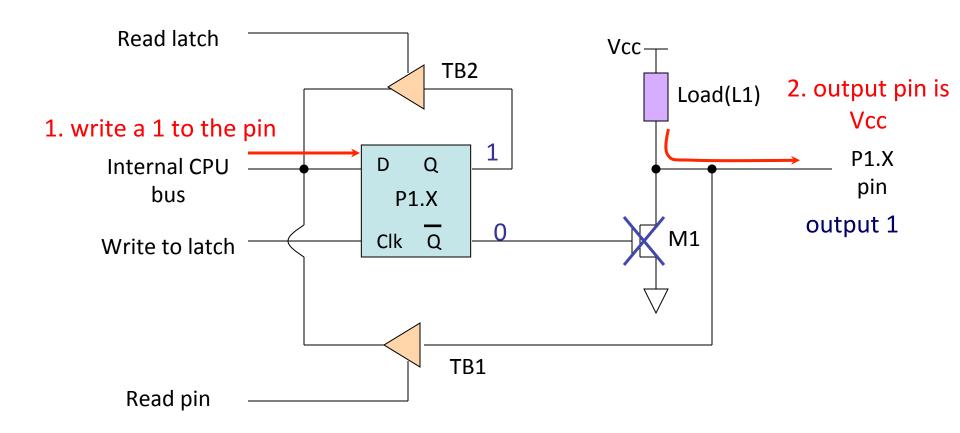
#### Hardware Structure of I/O Pin

- Each pin of I/O ports
  - Internal CPU bus: communicate with CPU
  - A D latch store the value of this pin
    - D latch is controlled by "Write to latch"
      - Write to latch = 1: write data into the D latch
  - 2 Tri-state buffer :
    - TB1: controlled by "Read pin"
      - Read pin = 1: really read the data present at the pin
    - TB2: controlled by "Read latch"
      - Read latch = 1: read value from internal latch
  - A transistor M1 gate
    - Gate=0: open
    - Gate=1: close



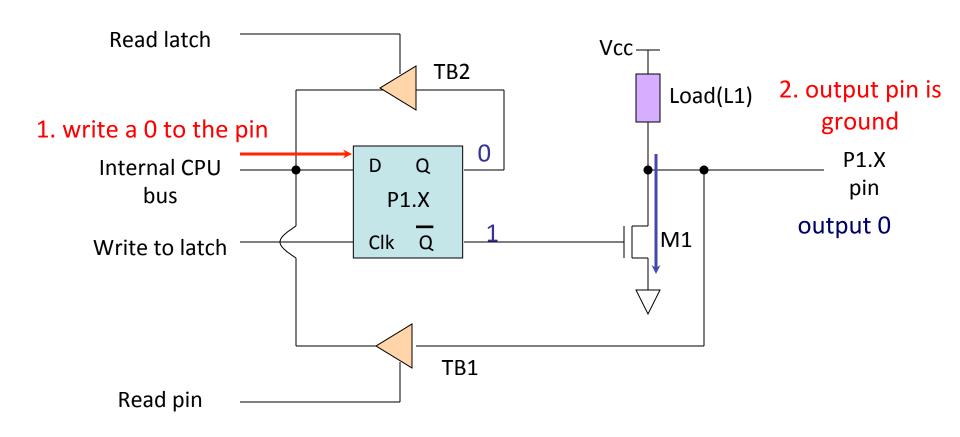


## Writing "1" to Output Pin P1.X





## Writing "0" to Output Pin P1.X





## Port 1 as Output (Write to a Port)

Send data to Port 1:

MOV A,#55H

BACK: MOV P1,A

**ACALL DELAY** 

CPL A

SJMP BACK

- Let P1 toggle.
- You can write to P1 directly.





## Reading Input vs Port Latch

- When reading ports, there are two possibilities:
  - Read the status of the input pin. (from external pin value)
    - MOV A, PX
    - JNB P2.1, TARGET ; jump if P2.1 is not set
    - JB P2.1, TARGET ; jump if P2.1 is set
  - Read the *internal latch* of the output port.
    - ANL P1, A

; P1  $\leftarrow$  P1 AND A

• ORL P1, A

; P1 ← P1 OR A

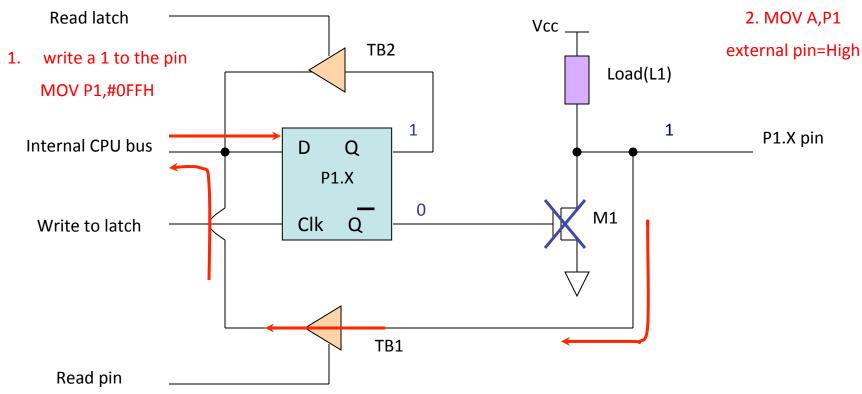
• INC P1

; increase P1





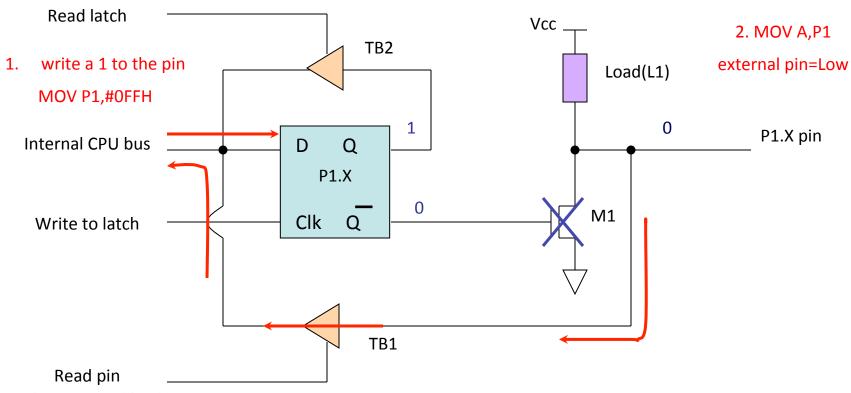
## Reading "High" at Input Pin







## Reading "Low" at Input Pin



3. Read pin=1 Read latch=0



#### Port 1 as Input (Read from Port)

• In order to make P1 an input, the port must be programmed by writing 1 to all the bit.

```
MOV A,#0FFH ;A=11111111B

MOV P1,A ;make P1 an input port

BACK: MOV A,P1 ;get data from P1

MOV P2,A ;send data to P2

SJMP BACK
```

To be an input port, P0, P1, P2 and P3 have similar methods.





#### Instructions For Reading an Input Port

| Mnemonics  | Examples        | Description                      |
|------------|-----------------|----------------------------------|
| MOV A,PX   | MOV A,P2        | Bring into A the data at P2 pins |
| JNB PX.Y,  | JNB P2.1,TARGET | Jump if pin P2.1 is low          |
| JB PX.Y,   | JB P1.3,TARGET  | Jump if pin P1.3 is high         |
| MOV C,PX.Y | MOV C,P2.4      | Copy status of pin P2.4 to CY    |





#### Reading Latch

Exclusive-or the Port 1:

```
MOV P1,#55H ;P1=01010101
ORL P1,#0F0H ;P1=11110101
```

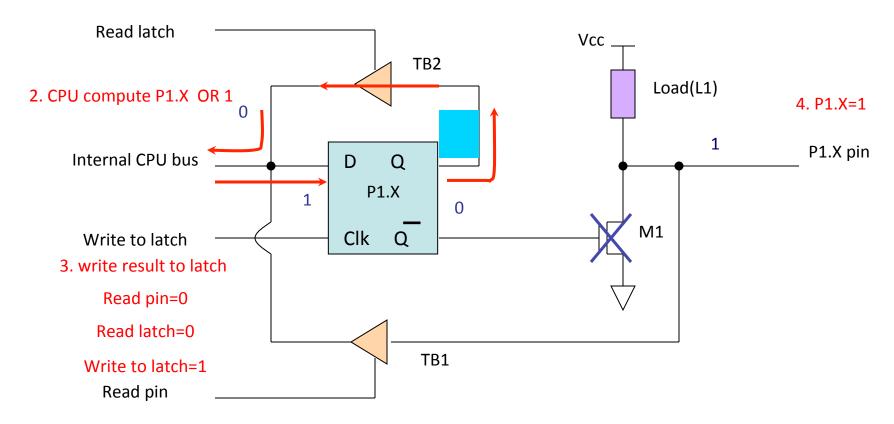
- 1. The read latch activates TB2 and bring the data from the Q latch into CPU.
  - Read P1.0=0
- 2. CPU performs an operation.
  - This data is ORed with bit 1 of register A. Get 1.
- 3. The latch is modified.
  - D latch of P1.0 has value 1.
- 4. The result is written to the external pin.
  - External pin (pin 1: P1.0) has value 1.





## Reading the Latch

1. Read pin=0 Read latch=1 Write to latch=0 (Assume P1.X=0 initially)





### Read-Modify-Write Instructions

| Mnemonics        | Example          |  |
|------------------|------------------|--|
| ANL              | ANL P1,A         |  |
| ORL              | ORL P1,A         |  |
| XRL              | XRL P1,A         |  |
| JBC PX.Y, TARGET | JBC P1.1, TARGET |  |
| CPL              | CPL P1.2         |  |
| INC              | INC P1           |  |
| DEC              | DEC P1           |  |
| DJNZ PX, TARGET  | DJNZ P1,TARGET   |  |
| MOV PX.Y,C       | MOV P1.2,C       |  |
| CLR PX.Y         | CLR P1.3         |  |
| SETB PX.Y        | SETB P1.4        |  |





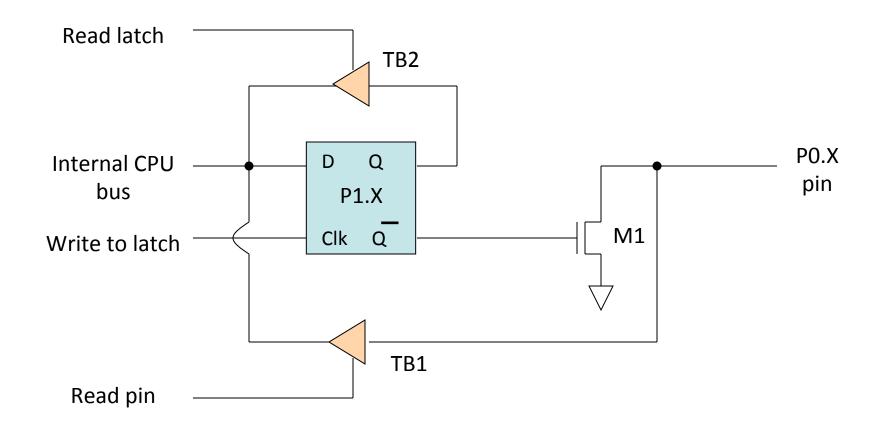
#### Other Pins

- P1, P2, and P3 have internal pull-up resisters.
  - P1, P2, and P3 are not open drain.
- P0 has no internal pull-up resistors and does not connects to Vcc inside the 8051.
  - P0 is open drain.
- However, for a programmer, it is the same to program P0, P1,
   P2 and P3.
- All the ports upon RESET are configured as output.



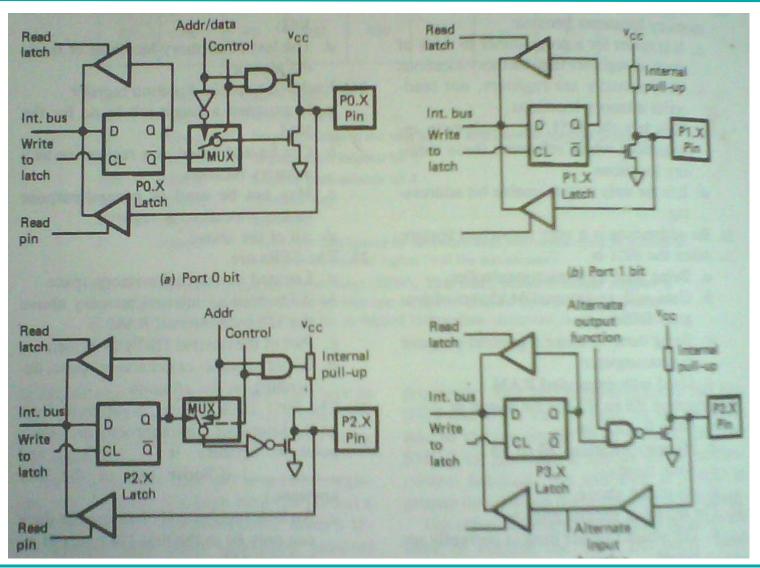


## A Pin of Port 0





#### I/O Ports of 8051





19

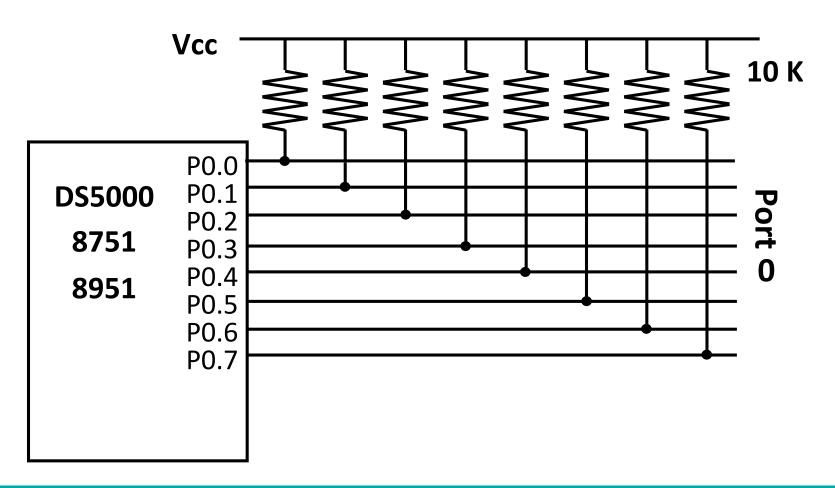
### Port 0 (pins 32-39)

- P0 is an open drain.
  - Open drain is a term used for MOS chips in the same way that open collector is used for TTL chips.
- When P0 is used for simple data I/O we must connect it to external pull-up resistors.
  - Each pin of P0 must be connected externally to a 10K ohm pull-up resistor.
  - With external pull-up resistors connected upon reset, port
     0 is configured as an output port.





#### Port 0 with Pull-Up Resistors





# Thank You



