CISC Design

Clocking and Interrupt

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EE-309: Microprocessors

Lecture 28 (29 Sep 2015)

CADSL

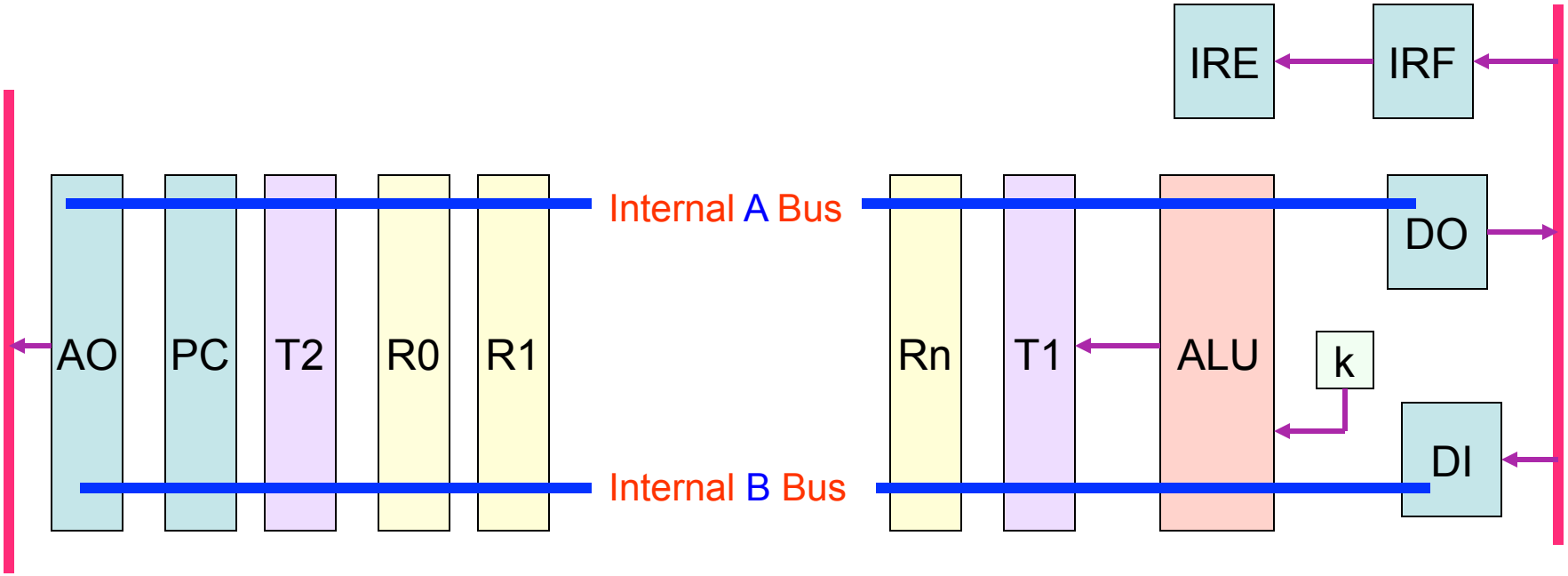
Internal Clocking

- Four phase clocking
  - P1 – source register is gated to internal bus
  - P2 – the signal on internal bus is amplified and broadcast the length of bus
  - P3 – the signal on internal bus is gated to the destination
  - P4 – the bus is returned to the neutral state

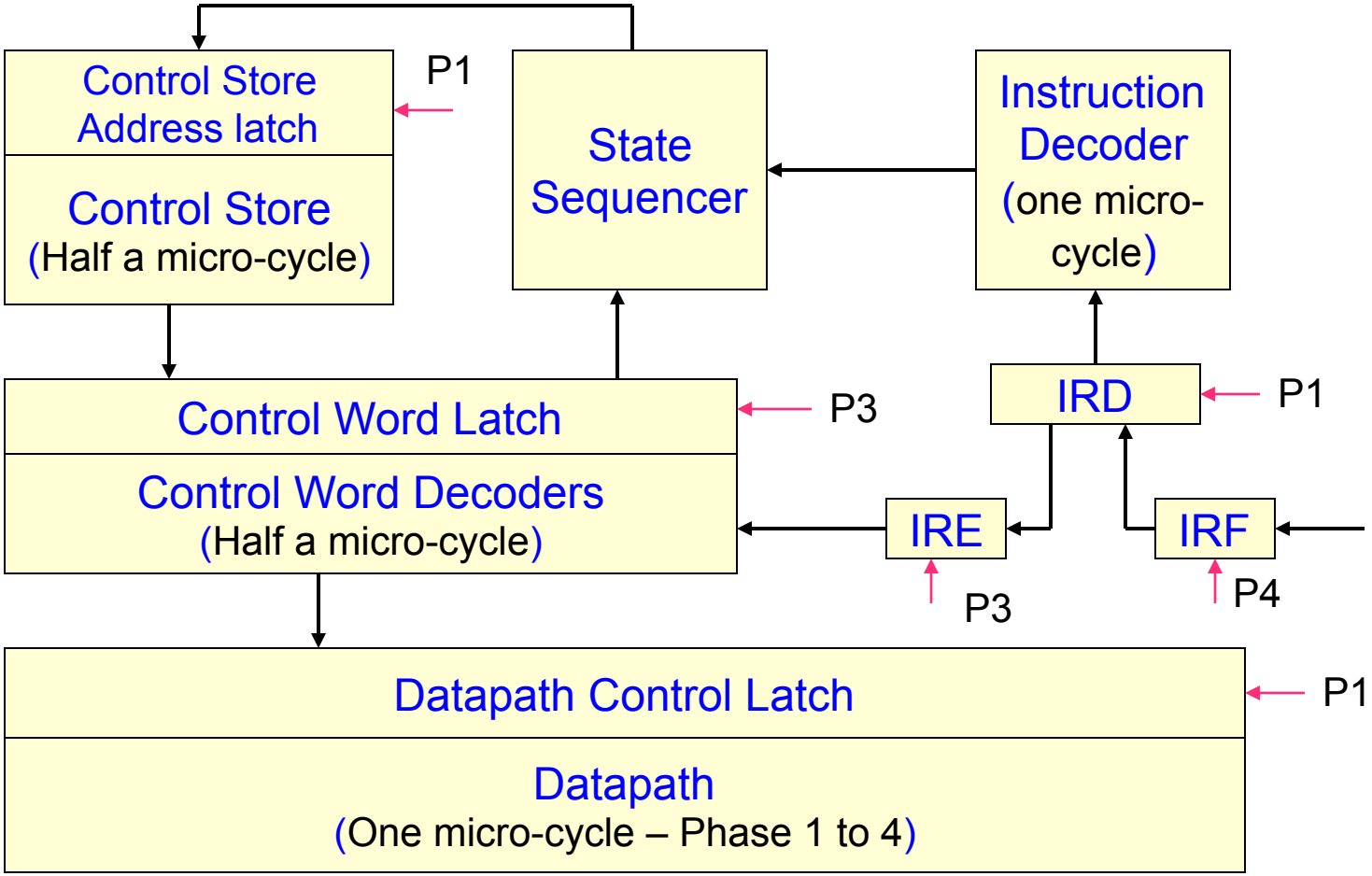
Internal Clocking

- The clocking on chip has to allow for delay from the external bus
- Add new clock phase P4 prime
- Split cycle (2 internal state in one external bus cycle)

MIN Datapath



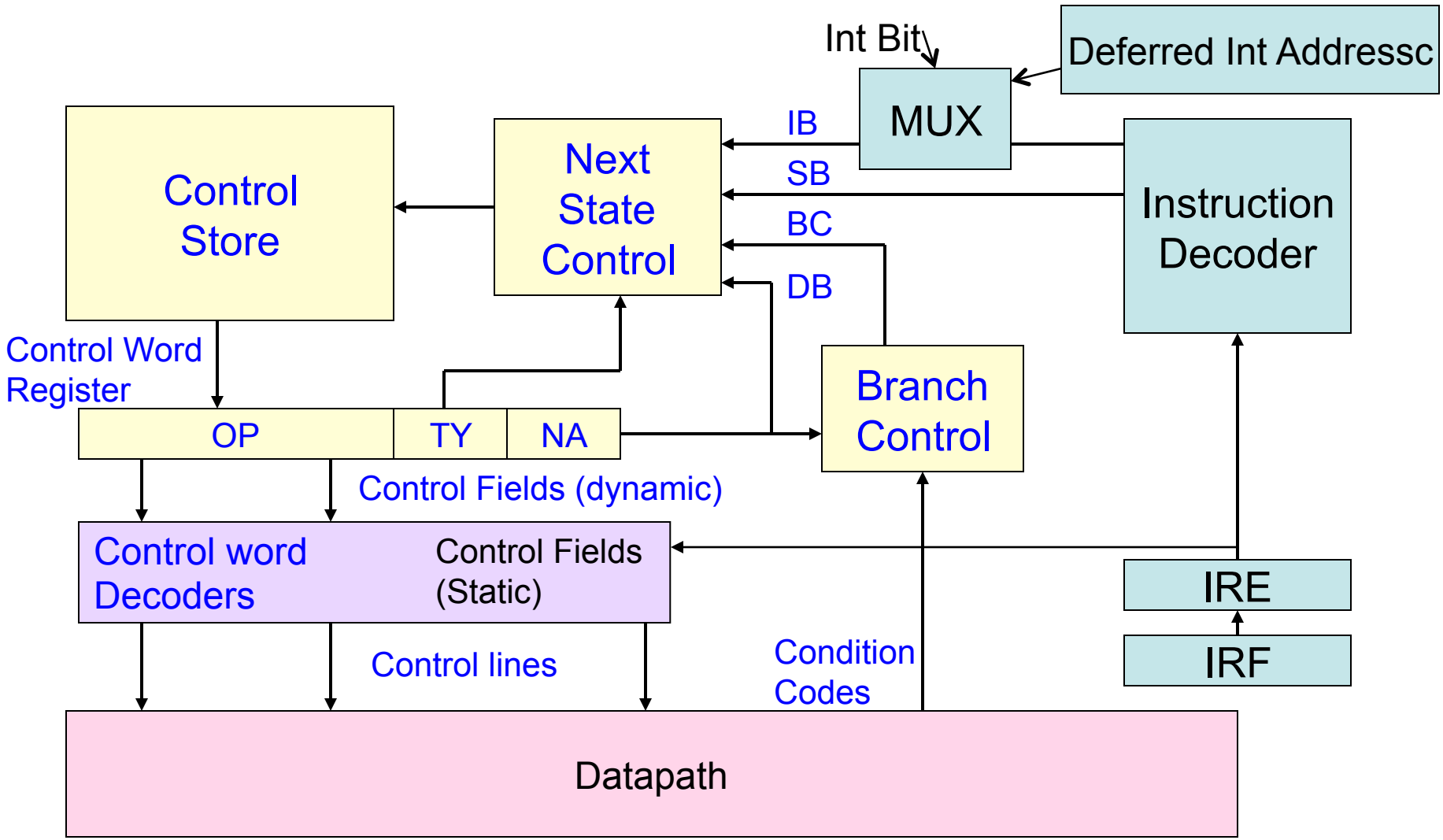
Internal Timing



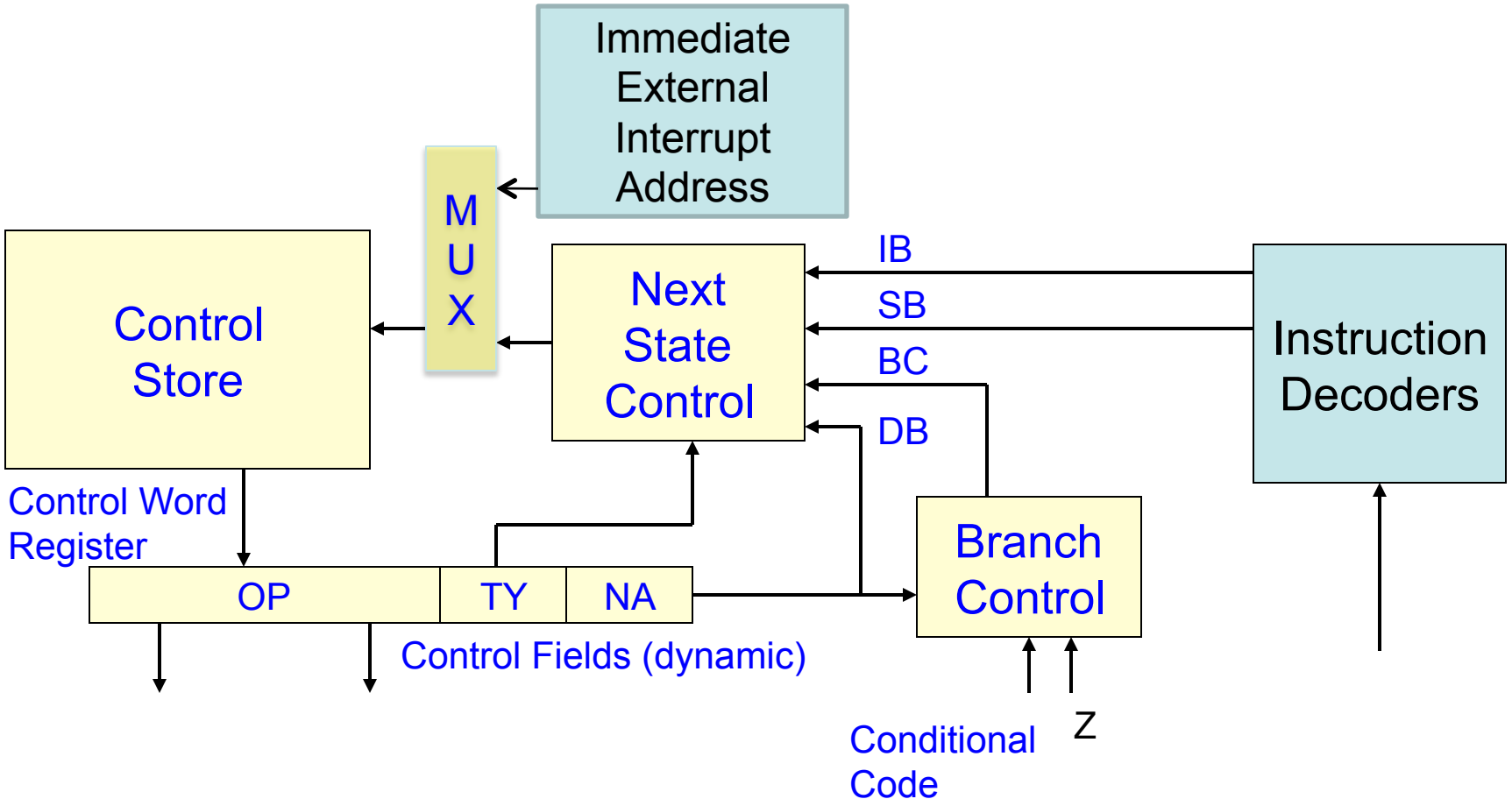
Exceptions/Interrupt

- Interrupts
  - Internal
    - Fixed point overflow
    - Divide by zero
    - Trace
  - External
    - Bus error
    - Peripheral service request
    - Reset request
    - Power on

Deferred Interrupt



Immediate Interrupt



Thank You