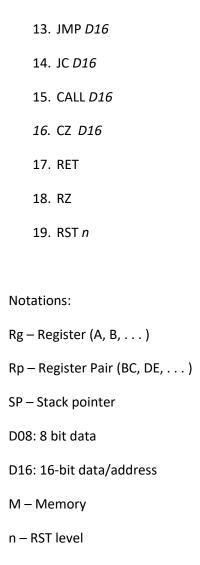# Assignment 1

Submission Deadline: 18 October 2019 (Friday) 23:55 Hrs (**Firm**)

Statement: Design a scaled down version of 8085 microprocessor, say Mini-8085 which is suppose to implement the following instructions. Hardware flow chart method is a well-structured method to design microprocessors. Therefore, use hardware flow chart method to design Mini-8085. It should be microcode-based architecture, i.e., use control store (CS) to store encoded control signals. Provide level 2 flow chart, Datapath organization and controller organization including the layout of control store and complete control words along with decode logic.

It should be submitted as *hand written document*.

Instruction Set

1. MOV *Rg, Rg*

2. MOV *Rg, M*

3. MOV *M, Rg*

4. MVI *Rg, D08*

5. LXI *Rp/SP, D16*

6. LDA *D16*

7. STA *D16*

8. ADC *Rg*

9. ACI *D08*

10. SBB *Rg*

11. ANA *Rg*

12. CMP *Rg*

13. JMP *D16*

14. JC *D16*

15. CALL *D16*

16. CZ *D16*

17. RET

18. RZ

19. RST *n*

Notations:

Rg – Register (A, B, . . .)

Rp – Register Pair (BC, DE, . . .)

SP – Stack pointer

D08: 8 bit data

D16: 16-bit data/address

M – Memory

n – RST level

Please refer to the following book for the further details of these instructions and encoding of the instructions

Ramesh Gaonkar, *Microprocessor Architecture, Programming, and Applications with 8085*, **PRI Publisher**