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Assignment 7

Part 1:

Register	Assembly Name	Register	Assembly Name
r0	$zero	r24-r25	Always 0
r1	$at	r26-r27	$k0-$k1
r2, r3	$v0, $v1	r28	$gp
r4 - r7	$a0 - $a3	r29	$sp
r8 - r15	$t0 - $t7	r30	$fp
r16 - r23	$s0-$s7	r31	$ra

Part 2:

Size of memory:

➔ **INSTRUCTION** Memory : **256 X 8** (word length)
➔ **DATA** Memory : **256 X 8** (word length)

Part 3:

The instruction layout used is the same as that used in MIPS.

Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, imm. format
J-format	op	target address					Jump instruction format

Class	Instruction	Function/Opcode
Arithmetic	add r0, r1, r2	100000
	sub r0, r1, r2	100010
	addu r0, r1, r2	100001
	subu r0,r1,r2	100011
	addi r0,r1,1000	001000
	addiu r0,r1, 1000	001001
Logical	and r0,r1,r2	100100
	or r0,r1,r2	100101
	andi r0,r1, 1000	001100
	ori r0,r1, 1000	001101
	sll r0, r1, 10	000000
	srl r0, r1, 10	000010
Data transfer	lw r0,10(r1)	100011
	sw r0,10(r1)	101011

Conditional Branch	**beq r0,r1,10**	**000100**
	bne r0,r1,10	**000101**
	bgt r0,r1,10	**000111**
	bgte r0,r1, 10	**011000**
	ble r0,r1, 10	**000110**
	bleq r0,r1, 10	**011001**
Unconditional Branch	**j 10**	**111111**
	jr r0	**111110**
	jal 10	**111101**
Comparison	**slt r0,r1,r2**	**101010**
	slti 1,2,100	**101010**