Nirma University

Institute of Technology

Semester End Examination (IR/RPR), May 2019

B.Tech. in Computer Engineering/Information Technology, Semester – IV

CE402 COMPUTER ORGANIZATION

Roll/ Exam No		Supervisor's initial with date	

Time : 3 Hours Max Marks: 100

Instructions:
1. Attempt all questions.
2. Figures to the right indicate full marks.
3. Draw neat sketches wherever necessary.
4. Use section-wise separate answer sheet.
5. Assume suitable data wherever necessary and specify them.

SECTION - I

Q.1 Do as directed. **[22]**

A. CO3, BL3 Assume that the following changes are made in the basic computer: [10]
11-bit addresses are used to access any memory location of the main memory; The width of opcode field is 4-bits; The hardwired control unit is replaced by the microprogrammed control unit; The size of control memory is 128X20. There are two registers SBR and CAR available in the control unit; A microprogram can use eight consecutive memory locations in the control memory; The microinstruction is of 20 bits and contains the following fields:

F1 (3 bits)	F2 (3 bits)	F3 (3 bits)	CD (2 bits)	BR (2 bits)	AD (7 bits)

i) Formulate the correct mapping procedure for this computer and give the symbolic routine for the following instruction of the basic computer (The content of AC should not be changed unless it is specified in the instruction):

SUBM: if (AC>0) then M[EA] <- AC - (M[EA])'

ii) Give the correct symbolic routines for FETCH and INDRCT (for reading effective address) for the above computer configuration. Assume the necessary values for the fields of a microinstruction. State your assumptions clearly.

B. CO3, BL3 Give the sequence of microoperations for executing the following instructions in the basic computer: [06]

XCH: AC ← M[AR] , M[AR] ← AC

SOQ: If (AC = M[AR]) then PC ← PC + 1 (AC doesn't change)

The computer supports AC ← AC ex-OR DR microoperation.

C. **CO3, BL3** An indirect instruction at address 053 in the basic computer has an operation code of the AND instruction and an address part equal to 0AB. The memory word at address 0AB contains CF25. The content of the memory word at address F25 is A620. The content of the memory word at address 620 is BC00. The content of the memory word at address C00 is A921. The content of AC is 986B. Go over the instruction cycle and determine the contents of the following registers at the end of the execute phase: AR, IR, PC, DR, AC. Repeat the problem six more times starting with an operation code of another memory reference instruction. Assume that all numbers are in hexadecimal. [06]

OR

C. **CO3, BL3** Derive the gate structure associated with the control inputs of the Data Register DR in the basic computer. [06]

Q.2 **Answer the following.** **[14]**

A. **CO4, BL3** A pipelined system has four stages and each stage takes 20 ns. 20% of the instructions are branch instructions. Each branch instruction introduces a delay of 3 stall cycles. What is the speed up factor compared to the same non pipelined environment, if there are 10000 instructions to be executed? [06]

B. **CO4, BL6** Design a pipeline for evaluating the following expression for a stream of numbers: [08]

$$A_i + (B_i / C_i - (D_i * E_i)), \text{ for } i = 1, 2, 3, \ldots, 10$$

Draw a block diagram and a space-time diagram. Show the contents of registers for each pipeline segment and clock cycle.

Q.3 **Do as directed.** **[14]**

A. **CO1, BL2** A digital computer has three registers: A, B and C. Four flip-flops provide the control functions for the computer: S is a flip-flop that is enabled by an external signal to start the system's operation; L and R are used for sequencing the microoperations; A fourth flip-flop T is set by the computer when the operation is completed. The function of the system is described by the following register transfer statements: [04]

$$S: C \leftarrow 0, S \leftarrow 0, T \leftarrow 0, L \leftarrow 1$$
$$L: L \leftarrow 0, \text{ if } (A = 0) \text{ then } (T \leftarrow 1) \text{ else } (R \leftarrow 1)$$
$$R: C \leftarrow C + B, A \leftarrow A - 1, R \leftarrow 0, L \leftarrow 1$$

Describe the function that the system performs.

B. **CO1, BL6** Show the hardware that implements the following conditional control statements: [04]

If (P=1) then (R1←R2)
else if (Q=1) then (R1←R1-R2)
else R1←R1 + R3

C. **CO1, BL3** Suppose, we want to execute the following operations in the basic computer: [06]

i) Circular Shift Right
ii) Selective Complement

What should be the sequence of the program instructions to get the result of the above operations? How many clock cycles are needed to generate the result of each of these operations?

OR

C. **CO1, BL3** In the basic computer, the control is currently executing a direct load instruction, available at address 185. The next instruction is available at address 186. Assume that an interrupt would be generated in the next clock cycle. For handling this interrupt, the required I/O routine is available in memory at address 789. All values are in hexadecimal. Give the necessary microoperations associated with interrupt cycle. Also state the values of registers, flip-flops, memory locations and counters involved in the operation. Give the list of program instructions which are needed to call the interrupt and return from the interrupt with the correct memory locations. [06]

SECTION - II

Q.4 **Do as directed.** **[18]**

A. **CO1, BL2** Differentiate between RISC and CISC architectures. [04]

B. **CO1, BL3** Give the assembly code to evaluate the following arithmetic expression: [04]

$$X = A + (B * C / (D + E) - F)$$

i) Using a general register computer with three-address instructions
ii) Using RISC instructions

C. **CO1, BL2** Describe the following with appropriate examples: [04]

i) Internal Interrupts
ii) External Interrupts
iii) Software Interrupts

D. **CO1, BL3** A computer employs RAM chips of 256X8 and ROM chips of 1024X8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. [06]

i) How many RAM and ROM chips are needed?
ii) Draw a memory-address map for the system.
iii) Give the address range in hexadecimal for RAM, ROM and interface.

OR

D. A four-way set associative cache memory has four words in each set. A replacement procedure based on the least recently used (LRU) [06]

CO1, BL3 algorithm is implemented by means of 2-bit counters associated with each word in the set. A value in the range 0 to 3 is thus recorded for each word. When a hit occurs, the counter associated with the referenced word is set to 0, those counters with values originally lower than the referenced one are incremented by 1, and all others remain unchanged. If a miss occurs, the word with counter value 3 is removed, the new word is put in its place, and its counter is set to 0. The other counters are incremented by 1. Show that this procedure works for the following sequence of word reference: A, B, C, D, C, E, D, A, B, C, E, A, C. Start with A, B, C, D as the initial four words, with word A being the least recently used.

Q.5 Do as directed. **[18]**

A. CO2, BL3 The access time of a cache memory is 105 ns and that of main memory 1200 ns. It is estimated that 75% of the memory requests are for read and the remaining 25% for write. The hit ratio for read accesses only is 0.8. A write-through procedure is used. [06]

i) What is the average access time of the system considering only memory read cycles?

ii) What is the average access time of the system for both memory read and write requests?

iii) What is the hit ratio taking into consideration the write cycles?

B. CO2, BL2 Differentiate between the following: [06]

i) Memory-mapped I/O and I/O mapped I/O

ii) Strobe and Handshaking

C. CO2, BL2 Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs? [06]

OR

C. CO2, BL1 Explain the importance and working of daisy chaining mechanism. [06]

Q.6 Answer the following. **[14]**

A. CO2, BL3 Show the multiplication of (+19) X (-15) using Booth's multiplication algorithm. For each step, give the content of all registers and counters involved in the process. [07]

B. CO2, BL3 Show the contents of registers E, A, Q, B and SC during the process of division (Restoring method) of (-124) by (+9). [07]