CS220: Assignment 7

Shrey Bansal (210997)
Narendra Singh (210649)

1 [PDS1]

We will use 30 registers for the CSE-BUBBLE Processor

$\$0$: Constant value 0
$\$1 - \$2$: Values for function results
$\$3 - \$7$: Arguments
$\$8 - \$18$: Temporary Registers
$\$19 - \$26$: Saved Temporaries
$\$27$: Program Counter
$\$28$: Stack Pointer
$\$29$: Return Address

2 [PDS2]

The sizes of memories are:

Register Memory : 30×32 bits
Data Memory : $2^{16} \times 32$ bits
Instruction Memory : $2^{16} \times 32$ bits

3 [PDS3]

3.1 Instruction Layout for R-type instructions

- Bits $0 - 5$ will store function code
- Bits $6 - 10$ will store the shift amount
- Bits $11 - 15$ will store the destination register code
- Bits $16 - 20$ will store the second source register code
- Bits $21 - 25$ will store the first source register code
- Bits $26 - 31$ will store the opcode for the instruction

3.2 Instruction Layout for I-type instructions

- Bits $0 - 15$ will store the address / constant value
- Bits $16 - 20$ will store the second source register code
- Bits $21 - 25$ will store the first source register code
- Bits $26 - 31$ will store the opcode for the instruction

3.3 Instruction Layout for J-type instructions

- Bits $0 - 25$ will store the address
- Bits $26 - 31$ will store the opcode for the instruction

3.4 Encoding Methodologies for Instruction Set

Instructions	op	rs	rt	rd	shamt	add./const.	funct
add	0	reg	reg	reg	reg	NA	0
sub	0	reg	reg	reg	reg	NA	1
addu	0	reg	reg	reg	reg	NA	2
subu	0	reg	reg	reg	reg	NA	3
addi	1	reg	reg	NA	NA	constant	NA
addiu	2	reg	reg	NA	NA	constant	NA
and	0	reg	reg	reg	reg	NA	4
or	0	reg	reg	reg	reg	NA	5
andi	3	reg	reg	NA	NA	constant	NA
ori	4	reg	reg	NA	NA	constant	NA
sll	0	0	reg	reg	reg	NA	6
srl	0	0	reg	reg	reg	NA	7
lw	5	reg	reg	NA	NA	address	NA
sw	6	reg	reg	NA	NA	address	NA
beq	7	reg	reg	NA	NA	address	NA
bne	8	reg	reg	NA	NA	address	NA
bgt	9	reg	reg	NA	NA	address	NA
bgte	10	reg	reg	NA	NA	address	NA
ble	11	reg	reg	NA	NA	address	NA
bleq	12	reg	reg	NA	NA	address	NA
j	13	NA	NA	NA	NA	address	NA
jr	14	NA	NA	NA	NA	address	NA
jal	15	NA	NA	NA	NA	address	NA
slt	0	reg	reg	reg	reg	NA	8
slti	16	reg	reg	NA	NA	constant	NA

Table 1: Instruction Set for CSE-BUBBLE