Logic Gates

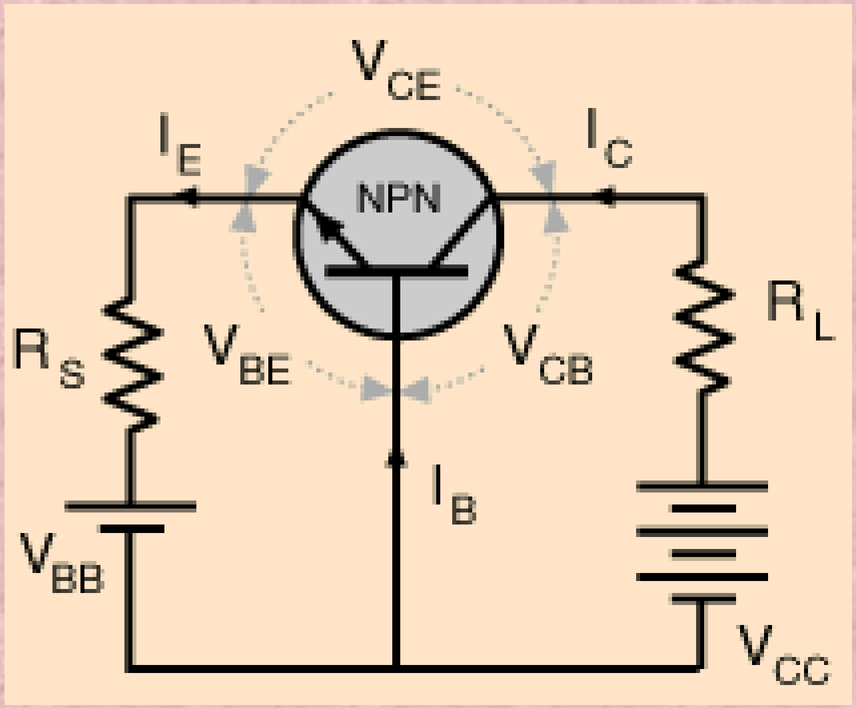
- A logic gate is a small transistor circuit, basically a type of amplifier, which is implemented in different forms within an integrated circuit. Each type of gate has one or more (most often two) inputs and one output.

- The principle of operation is that the circuit operates on just two voltage levels, called logic 0 and logic 1. When either of these voltage levels is applied to the inputs, the output of the gate responds by assuming a 1 or a 0 level, depending on the particular logic of the gate. The logic rules for each type of gate can be described in different ways, by a written description of the action, by a truth table, or by a Boolean algebra statement.

- Boolean statements use letters from the beginning of the alphabet, such as A, B, C etc. to indicate inputs, and letters from the second half of the alphabet, very commonly X or Y and sometimes Q or P to label an output. The letters have no meaning in themselves, other than just to label the various points in the circuit. The letters are then linked by a symbol indicating the logical action of the gate.

Transistors as Switches

- V_{BB} voltage controls whether the transistor conducts in a common base configuration.



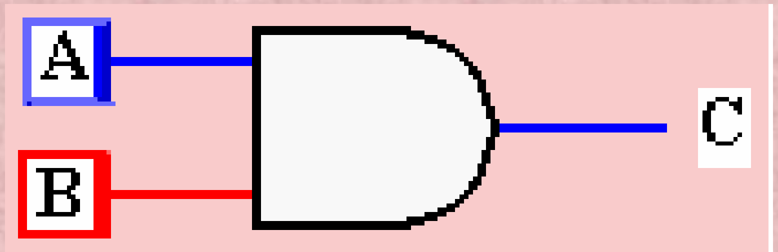
- Logic circuits can be built using transistors

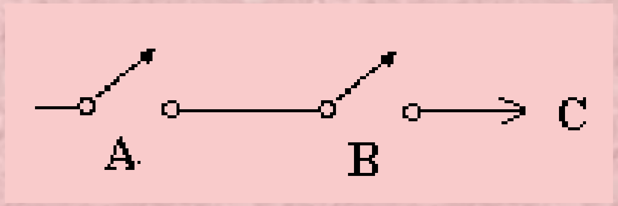
Boolean Algebra

AND

- In order for current to flow, both switches must be closed
  - Logic notation A•B = C

    (Sometimes AB = C)

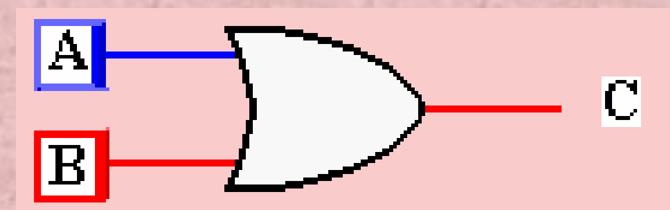


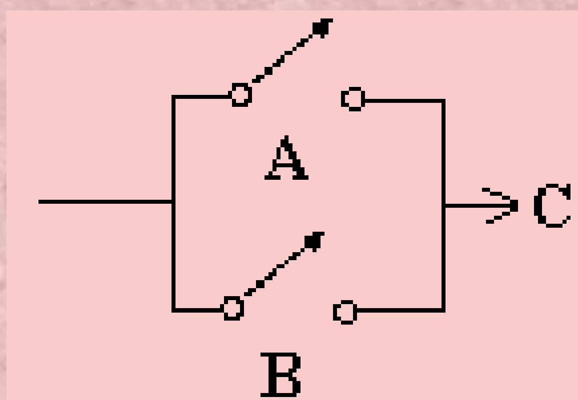


A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

OR

- Current flows if either switch is closed
  - Logic notation A + B = C

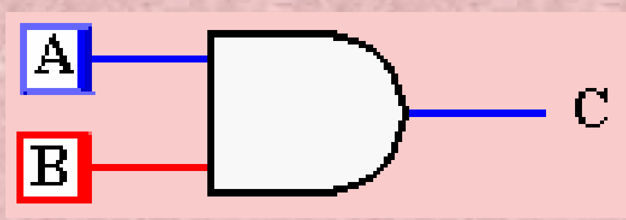




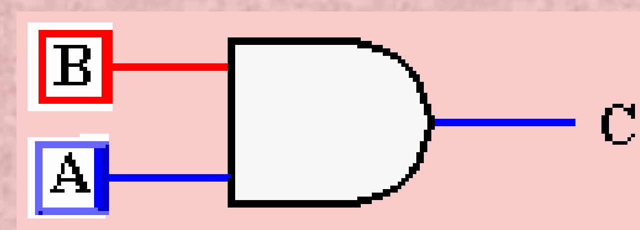
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

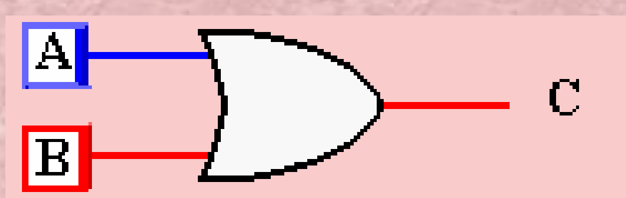
Properties of AND and OR

- Commutation
  - A + B = B + A
  - A • B = B • A

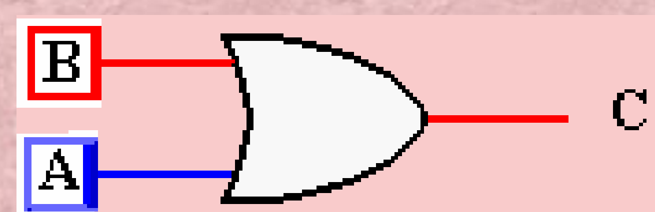


Same as

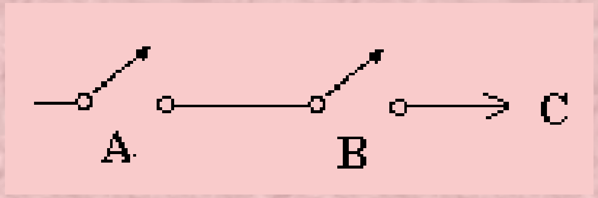




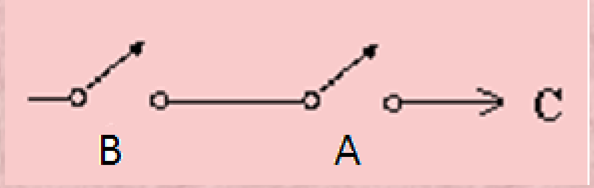
Same as



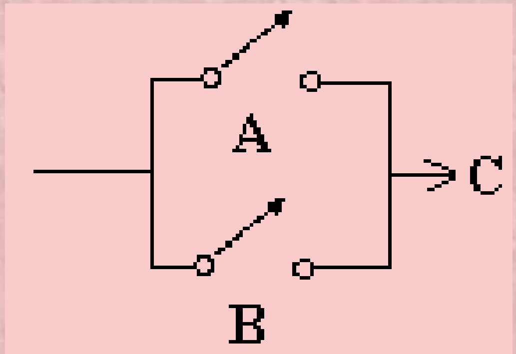
Commutation Circuit



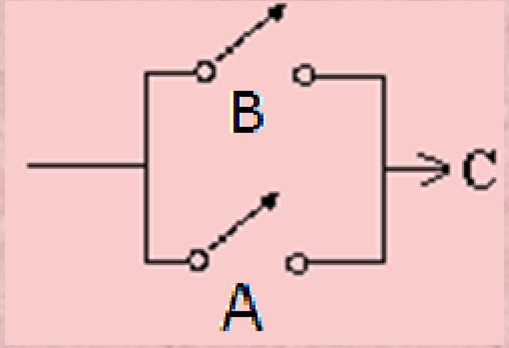
A • B



B • A



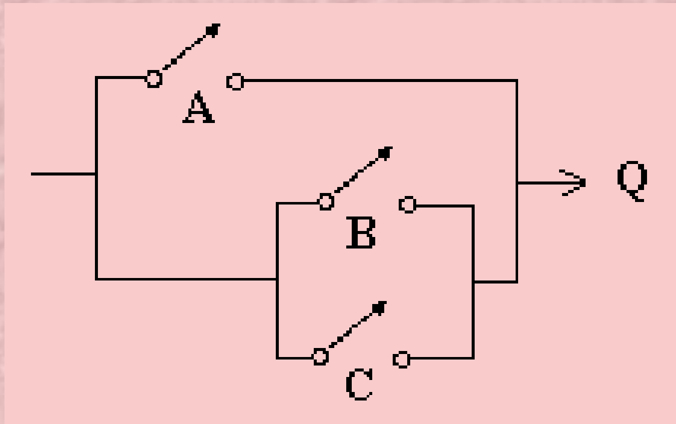
A + B



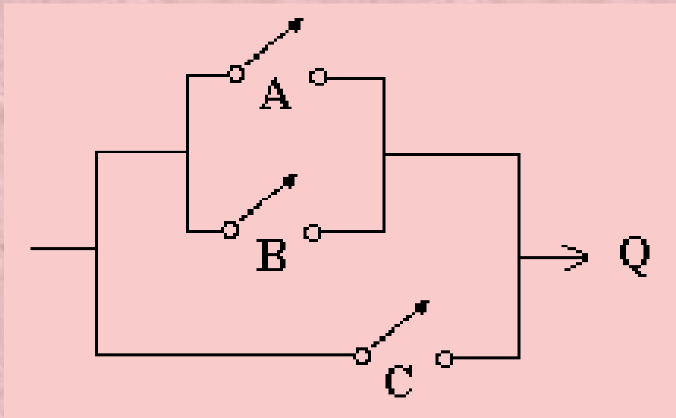
B + A

Properties of AND and OR

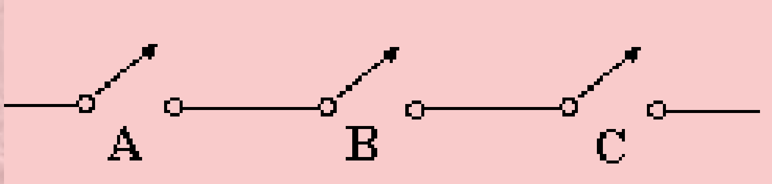
- Associative Property
  - A + (B + C) = (A + B) + C



=



  - A • (B • C) = (A • B) • C

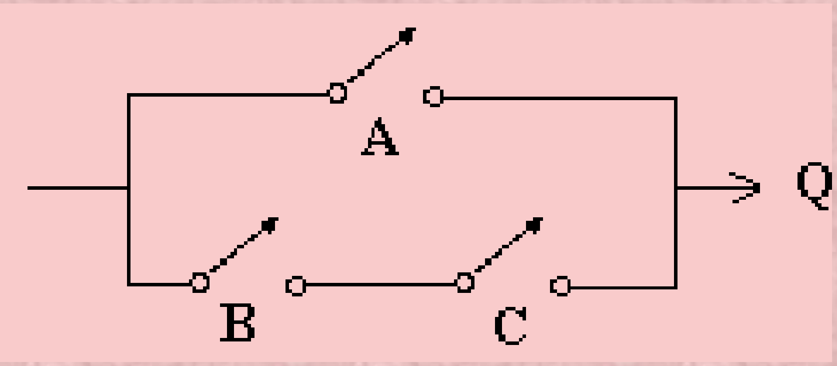


Properties of AND and OR

Distributive Property

A + B • C = (A + B) • (A + C)

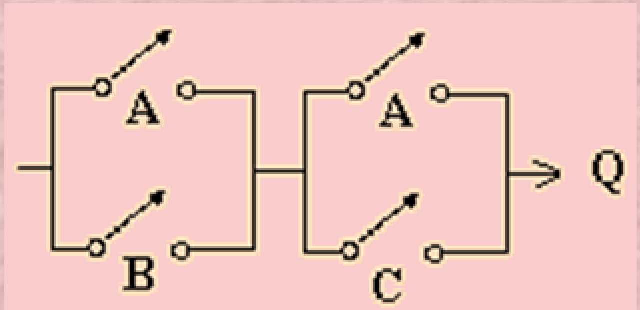
A + B • C



A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Distributive Property

(A + B) • (A + C)



A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

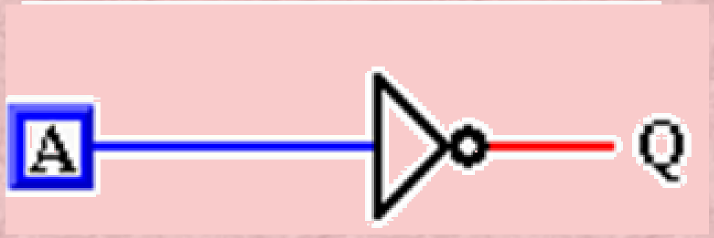
Binary Addition

A	B	S	C(arry)
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Notice that the carry results are the same as AND

$$C = A \bullet B$$

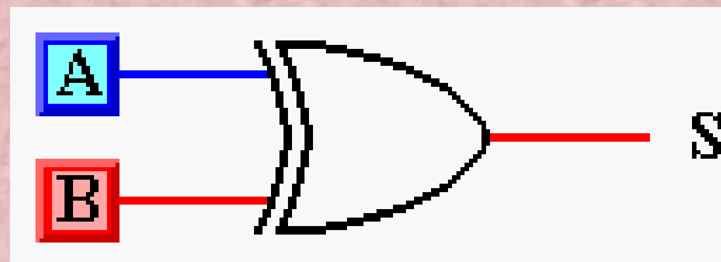
Inversion (NOT)



Logic: $Q = \overline{A}$

A	Q
0	1
1	0

Exclusive OR (XOR)



Either A or B, but not both

This is sometimes called the **inequality detector**, because the result will be 0 when the inputs are the same and 1 when they are different.

The truth table is the same as for S on Binary Addition. $S = A \oplus B$

A	B	S
0	0	0
1	0	1
0	1	1
1	1	0

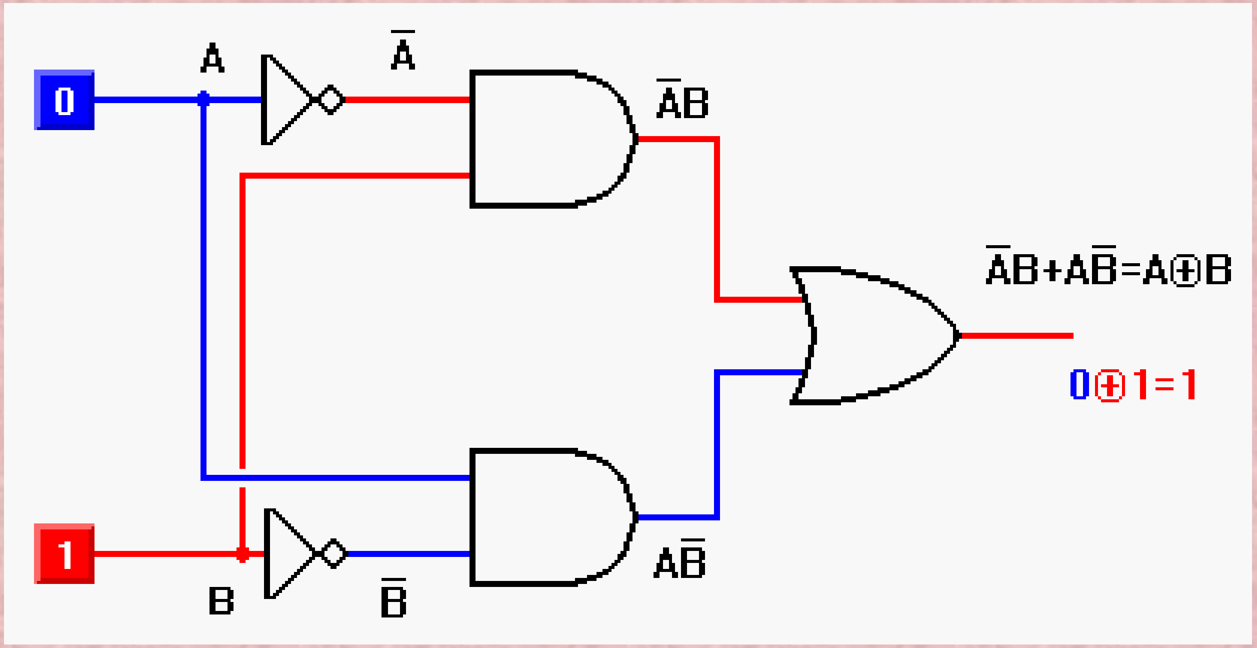
Getting the XOR

Two ways of getting S = 1

$$A \cdot \overline{B} \text{ or } \overline{A} \cdot B$$

A	B	S
0	0	0
1	0	1
0	1	1
1	1	0

Circuit for XOR



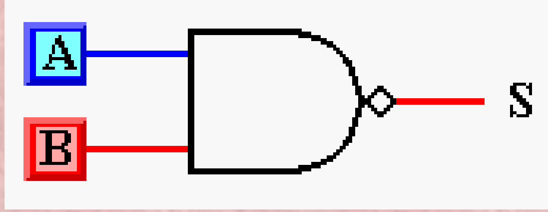
$$A \oplus B = \overline{A} \cdot B + A \cdot \overline{B}$$

Accumulating our results: Binary addition is the result of XOR plus AND

Counting in Binary

1	1	11	1011	21	10101
2	10	12	1100	22	10110
3	11	13	1101	23	10111
4	100	14	1110	24	11000
5	101	15	1111	25	11001
6	110	16	10000	26	11010
7	111	17	10001	27	11011
8	1000	18	10010	28	11100
9	1001	19	10011	29	11101
10	1010	20	10100	30	11110

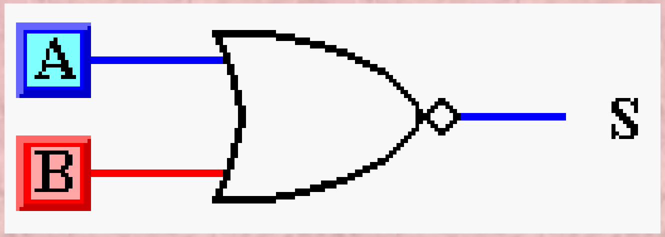
NAND (NOT AND)



$$Q = \overline{A \cdot B}$$

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

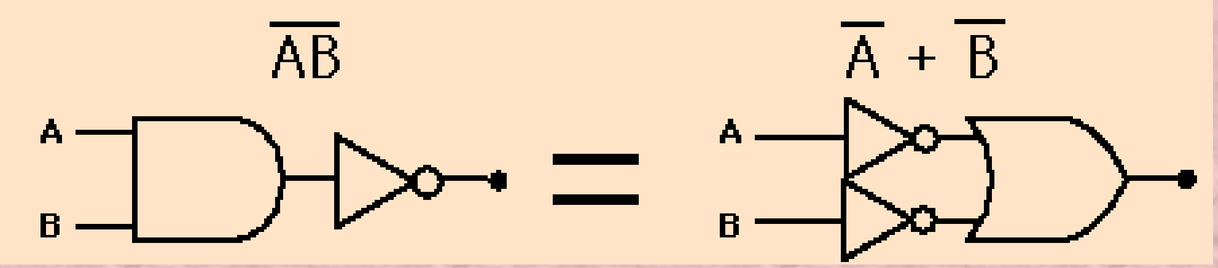
NOR (NOT OR)



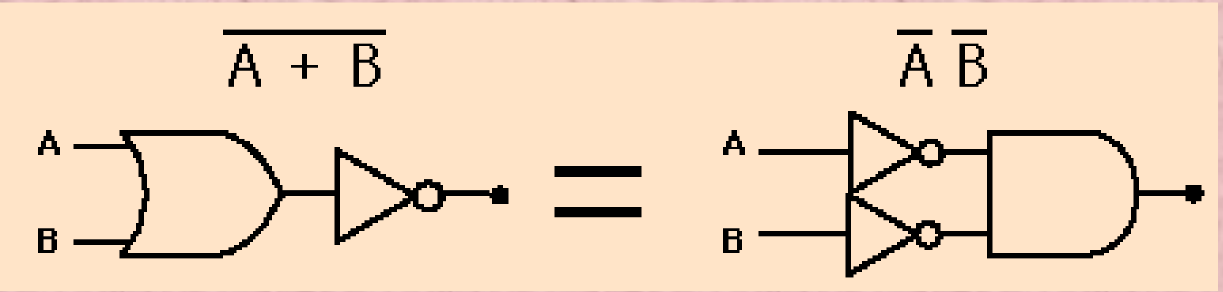
$$Q = \overline{A + B}$$

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

DeMorgan's Theorem



A NAND gate is equivalent to an inversion followed by an OR



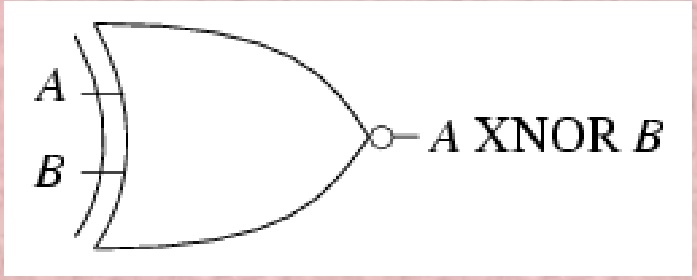
A NOR gate is equivalent to an inversion followed by and AND

DeMorgan Truth Table

A	B	$\overline{AB}$	$\overline{A}+\overline{B}$	$\overline{A+B}$	$\overline{A}\,\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	0
1	0	1	1	0	0
1	1	0	0	0	0

NAND NOR

Exclusive NOR



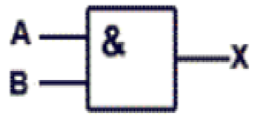
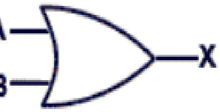
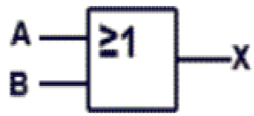
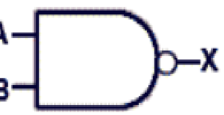
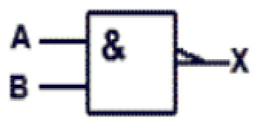
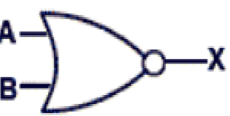
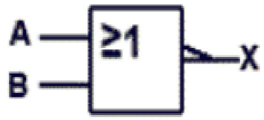
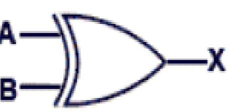
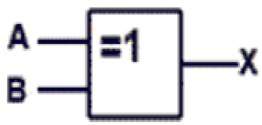
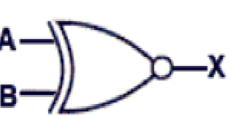
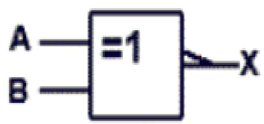
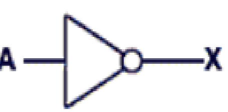
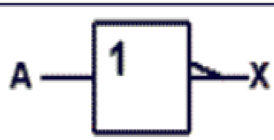
$$Q = \overline{A \oplus B}$$

Equality Detector

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Summary

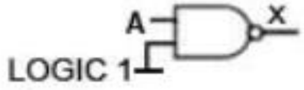
Summary for all 2-input gates							
Inputs		Output of each gate					
A	B	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

ANSI Symbol	IEC Symbol	Description	Boo
		The AND gate output is at logic 1 when, and only when all its inputs are at logic 1, otherwise the output is at logic 0.	X =
		The OR gate output is at logic 1 when one or more of its inputs are at logic 1. If all the inputs are at logic 0, the output is at logic 0.	X =
		The NAND Gate output is at logic 0 when, and only when all its inputs are at logic 1, otherwise the output is at logic 1.	X =
		The NOR gate output is at logic 0 when one or more of its inputs are at logic 1. If all the inputs are at logic 0, the output is at logic 1.	X =
		The XOR gate output is at logic 1 when one and ONLY ONE of its inputs is at logic 1. Otherwise the output is logic 0.	X =
		The XNOR gate output is at logic 0 when one and ONLY ONE of its inputs is at logic 1. Otherwise the output is logic 1. (It is similar to the XOR gate, but its output is inverted).	X =
		The NOT gate output is at logic 0 when its only input is at logic 1, and at logic 1 when its only input is at logic 0. For this reason it is often called an INVERTER.	X =

a. 

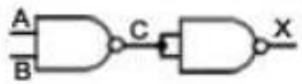
A	B	X
0	0	1
1	1	0

NOT

b. 

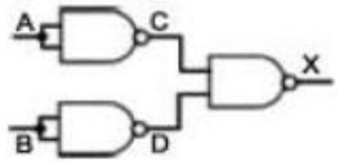
A	B	X
0	1	1
0	1	1
1	1	0
1	1	0

AND

c. 

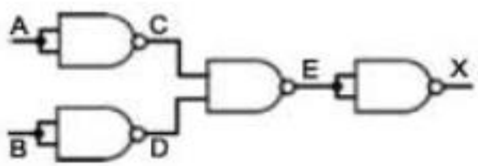
A	B	C	X
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

OR

d. 

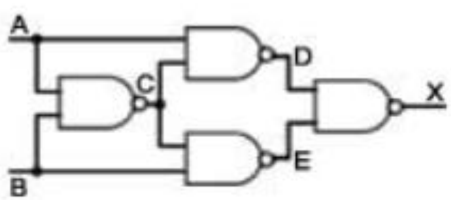
A	B	C	D	X
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

NOR

e. 

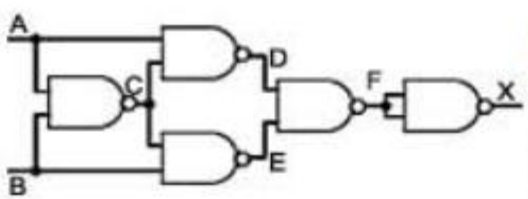
A	B	C	D	E	X
0	0	1	1	0	1
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	1	0

XOR

f. 

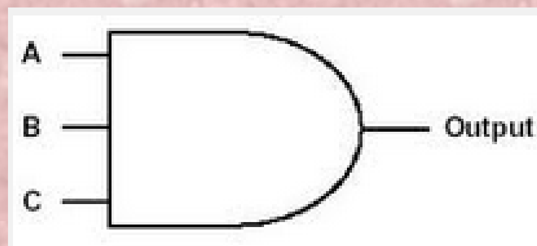
A	B	C	D	E	X
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

XNOR

g. 

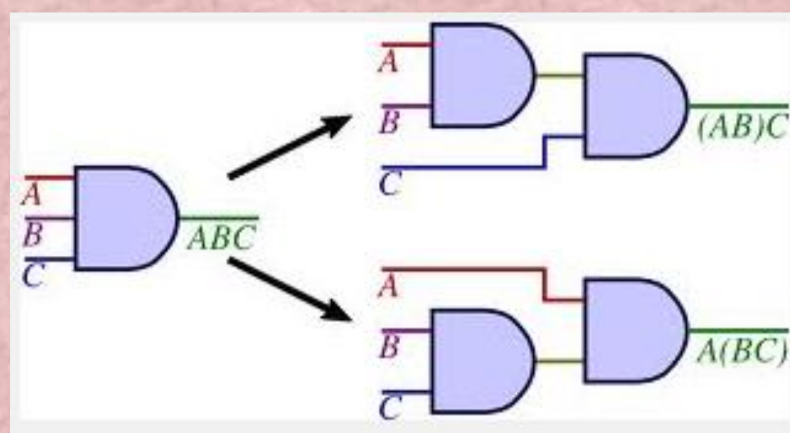
A	B	C	D	E	F	X
0	0	1	1	1	0	1
0	1	1	1	0	1	0
1	0	1	0	1	1	0
1	1	0	1	1	0	1

Multi-input Gates

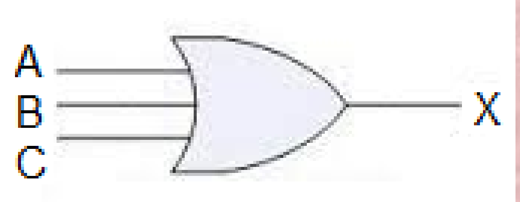


3 Input AND gate

A	B	C	A.B.C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



Three input OR



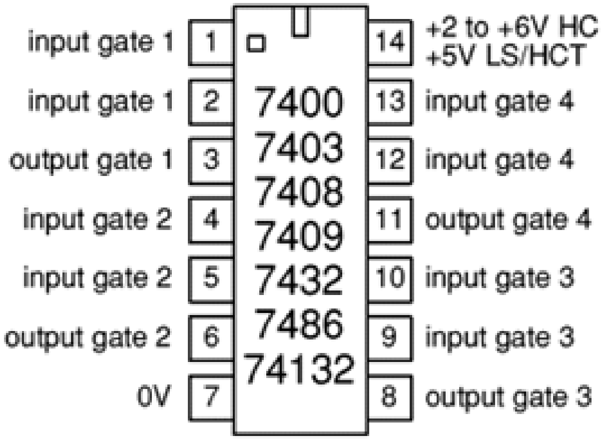
A	B	C	X = A+B+C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Logic Gate ICs

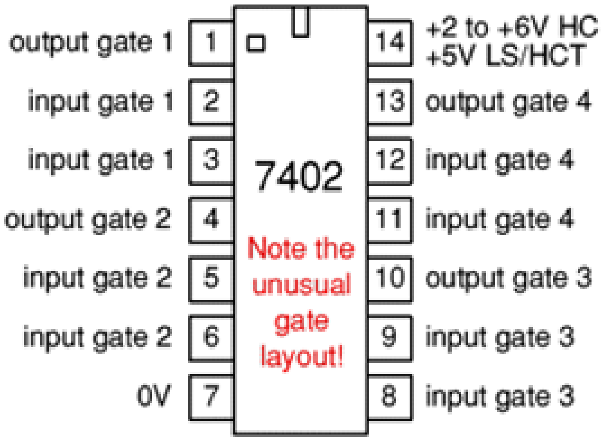
Quad 2-input gates

- 7400 quad 2-input NAND
- 7403 quad 2-input NAND with open collector outputs
- 7408 quad 2-input AND
- 7409 quad 2-input AND with open collector outputs
- 7432 quad 2-input OR
- 7486 quad 2-input EX-OR
- 74132 quad 2-input NAND with Schmitt trigger inputs

The 74132 has Schmitt trigger inputs to provide good noise immunity.
They are ideal for slowly changing or noisy signals.



- 7402 quad 2-input NOR
  Note the unusual gate layout.



Example 7400