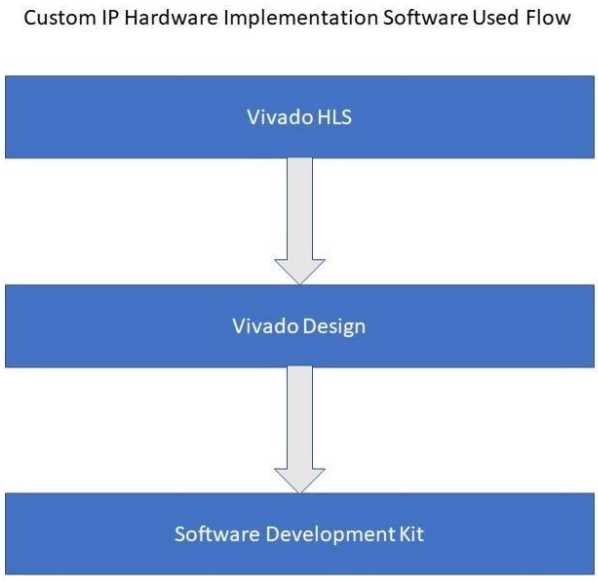
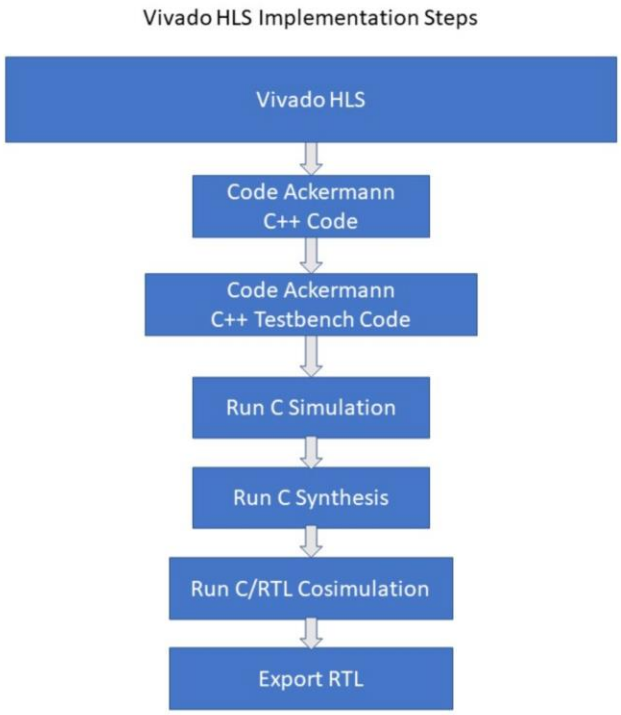
Group: Panduranga-Sood

Custom Logic IP Implementation on Hardware

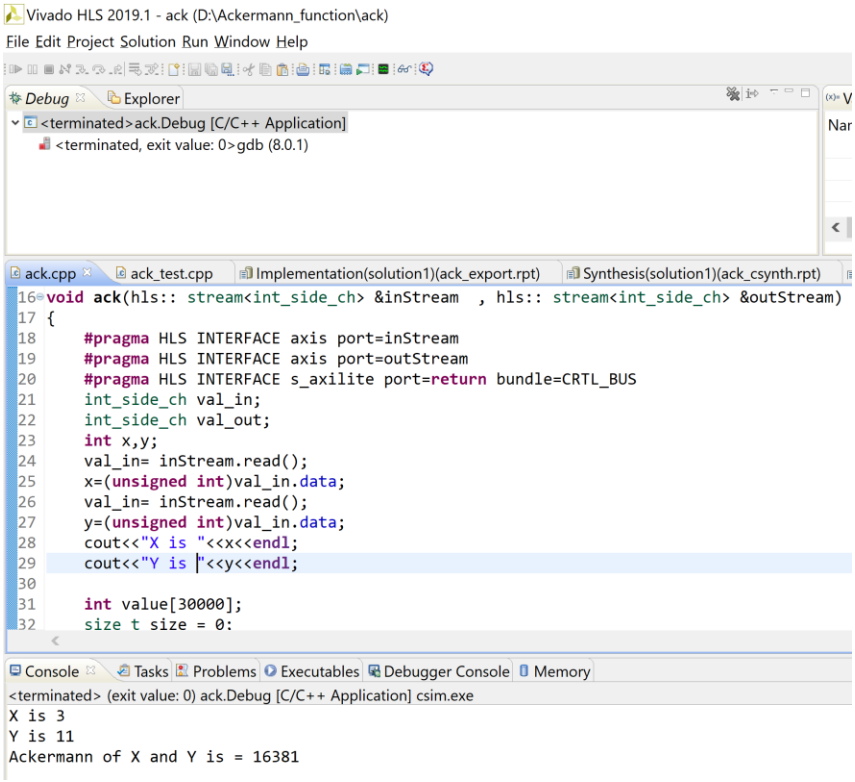


Vivado HLS



Vivado HLS Outputs

- C Simulation:



- C Synthesis:

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	6.774	1.25

Latency (clock cycles)

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	356	-
FIFO	-	-	-	-	-
Instance	0	-	36	40	-
Memory	64	-	0	0	0
Multiplexer	-	-	-	270	-
Register	-	-	290	-	-
Total	64	0	326	666	0
Available	100	66	28800	14400	0
Utilization (%)	64	0	1	4	0

- C/RTL Cosimulation:

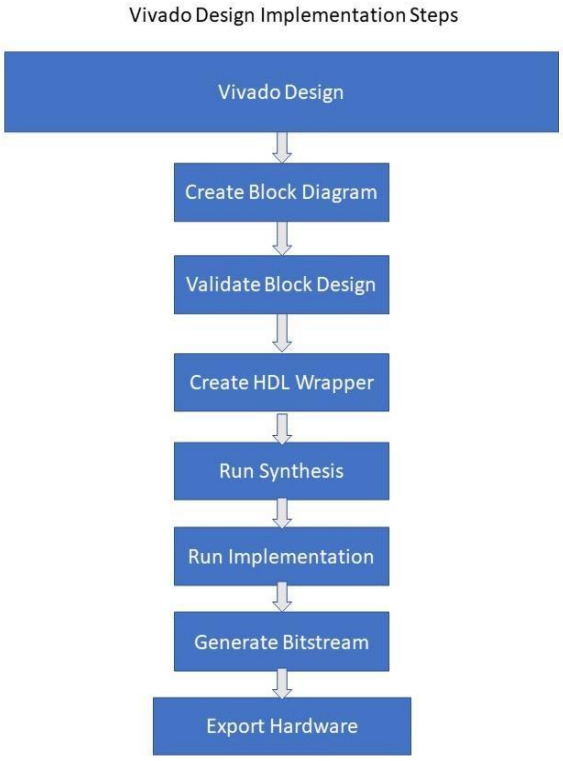
Cosimulation Report for 'ack'

Result

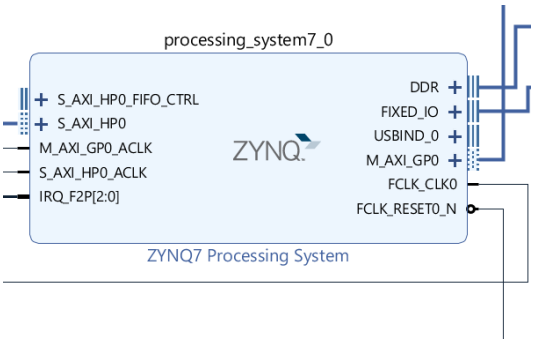
		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	89396668	89396668	89396668	NA	NA	NA

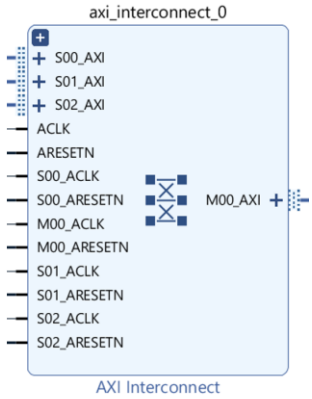
Export the report(.html) using the Export Wizard

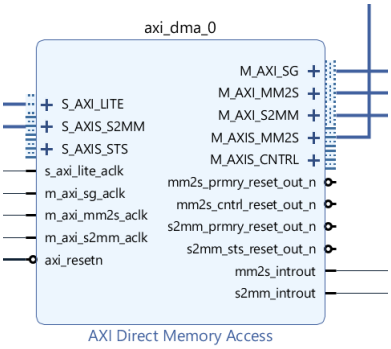
Vivado Design

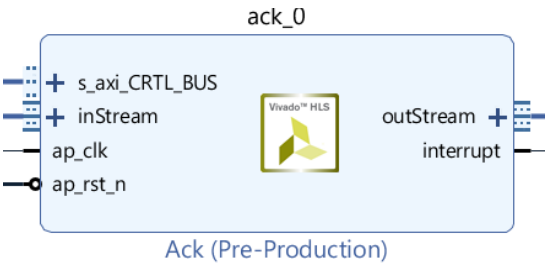


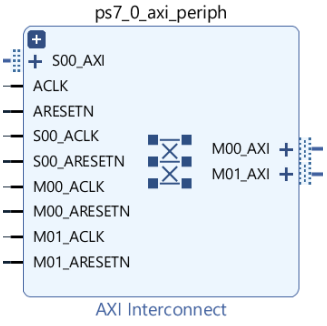
Vivado Design design blocks

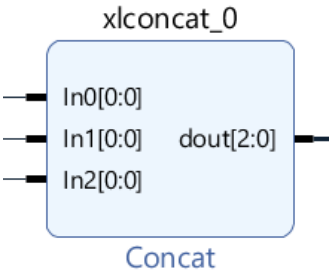


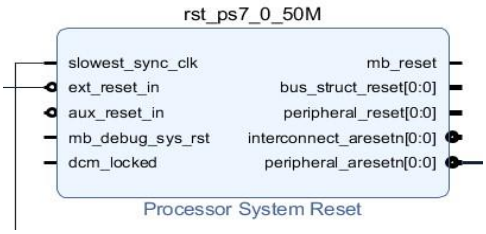

axi_interconnect_0
S00_AXI
S01_AXI
S02_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
S01_ACLK
S01_ARESETN
S02_ACLK
S02_ARESETN
M00_AXI
AXI Interconnect


axi_dma_0
S_AXI_LITE
S_AXIS_S2MM
S_AXIS_STS
s_axi_lite_aclk
m_axi_sg_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_SG
M_AXI_MM2S
M_AXI_S2MM
M_AXIS_MM2S
M_AXIS_CNTRL
mm2s_prmry_reset_out_n
mm2s_cntrl_reset_out_n
s2mm_prmry_reset_out_n
s2mm_sts_reset_out_n
mm2s_introut
s2mm_introut
AXI Direct Memory Access

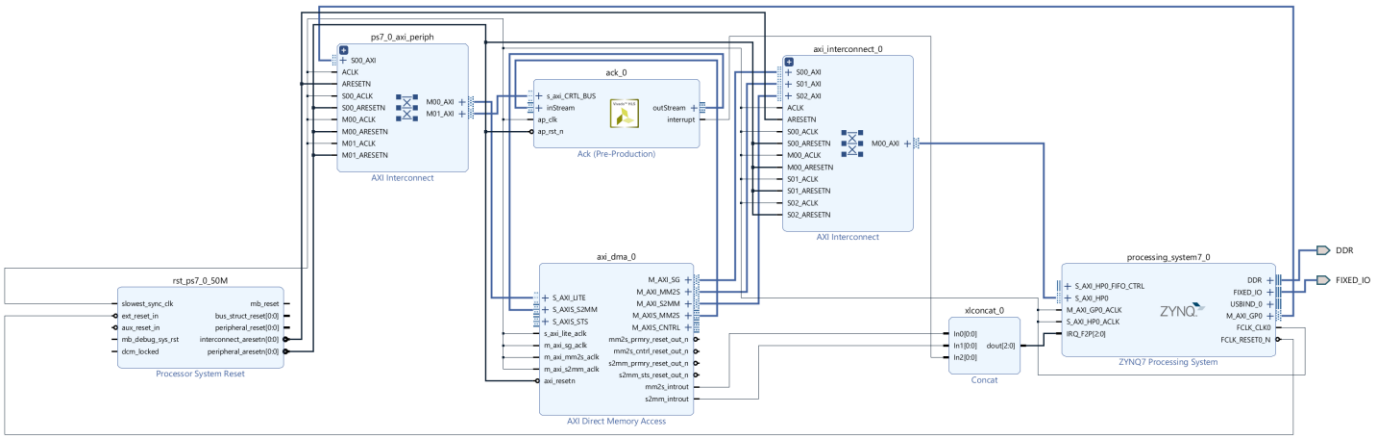

ack_0
s_axi_CRTL_BUS
inStream
ap_clk
ap_rst_n
Vivado™ HLS
outStream
interrupt
Ack (Pre-Production)


ps7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect

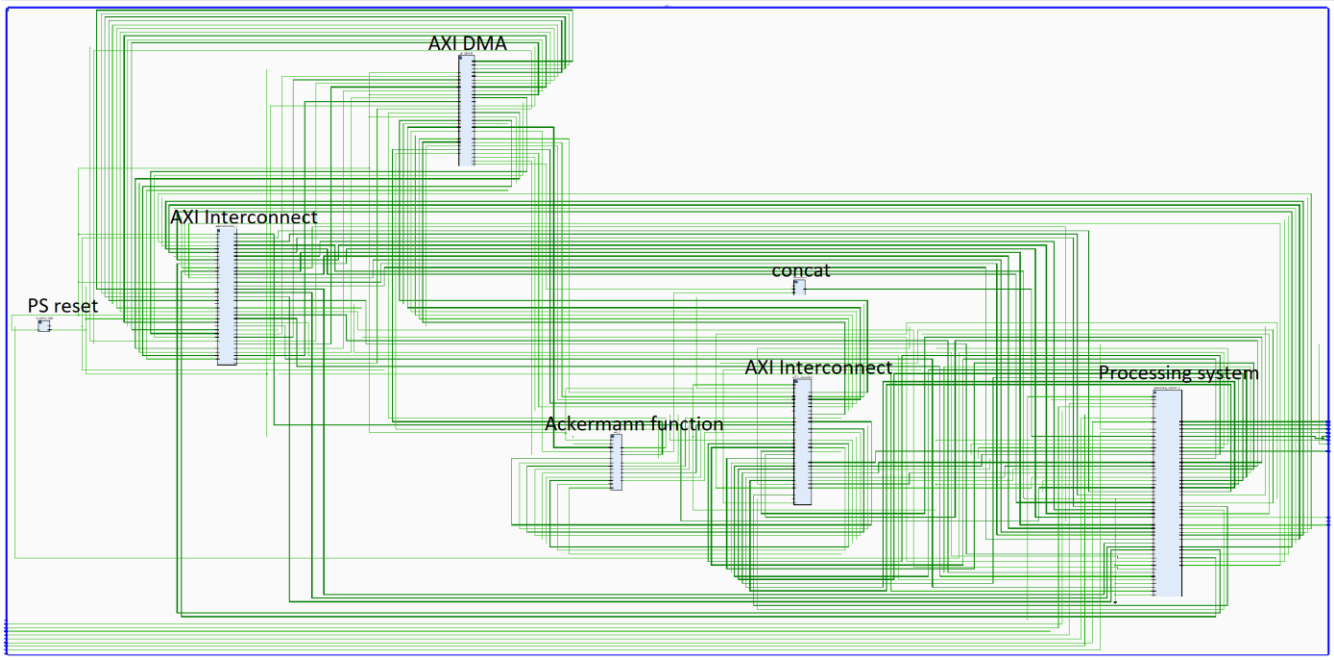




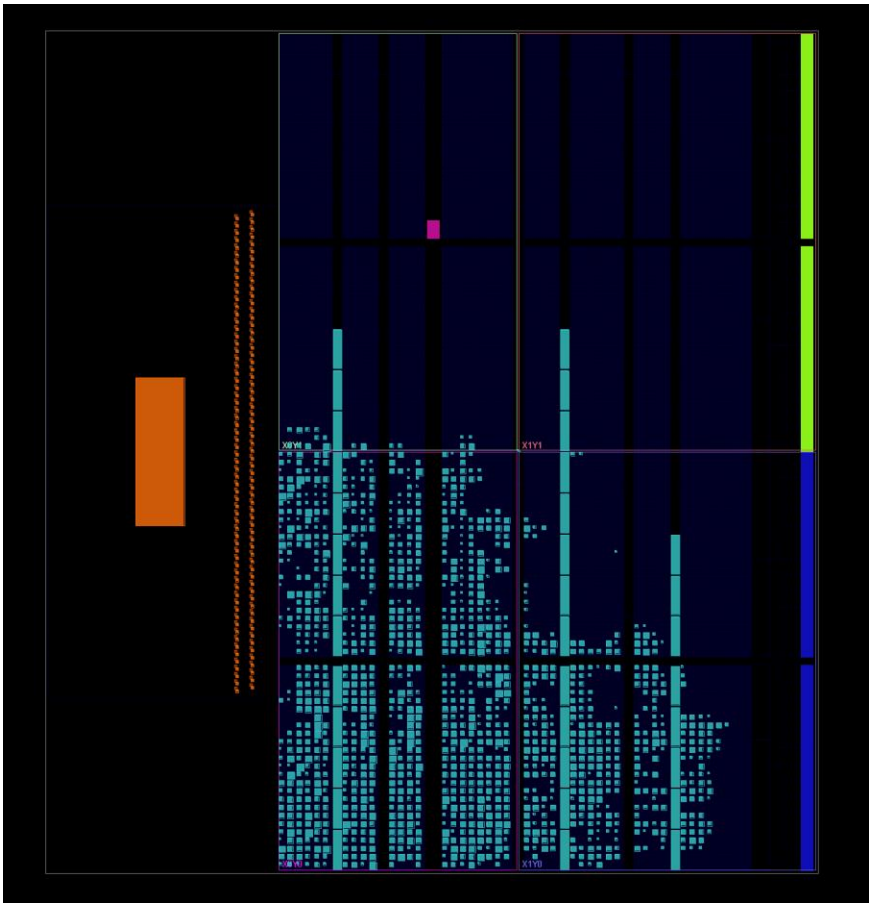
Block Design



Schematic Design



LUTs used in the Design



Vivado Design Outputs

- Timing Report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.153 ns	Worst Hold Slack (WHS):	0.010 ns	Worst Pulse Width Slack (WPWS):	8.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	11096	Total Number of Endpoints:	11096	Total Number of Endpoints:	4281

All user specified timing constraints are met.

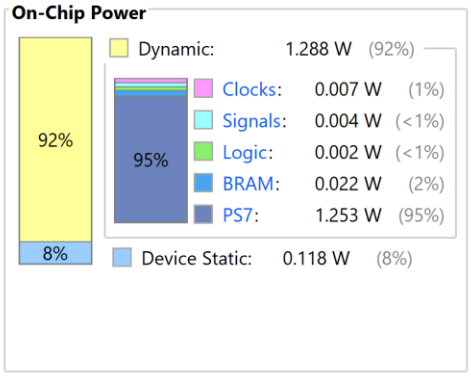
- Power Summary:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.407 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**41.2°C**
Thermal Margin:	43.8°C (3.7 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

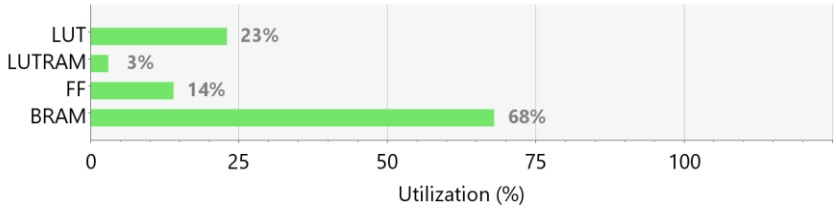
Launch Power Constraint Advisor to find and fix invalid switching activity



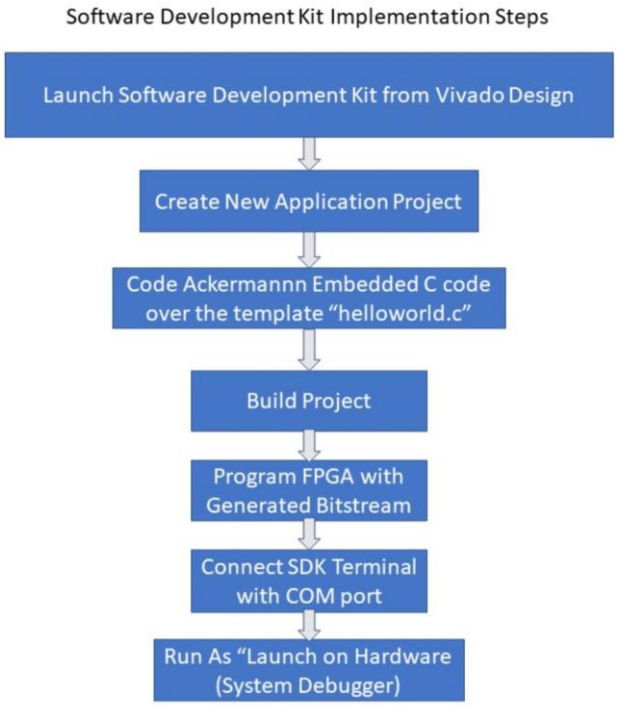
- Utilization Report:

Summary

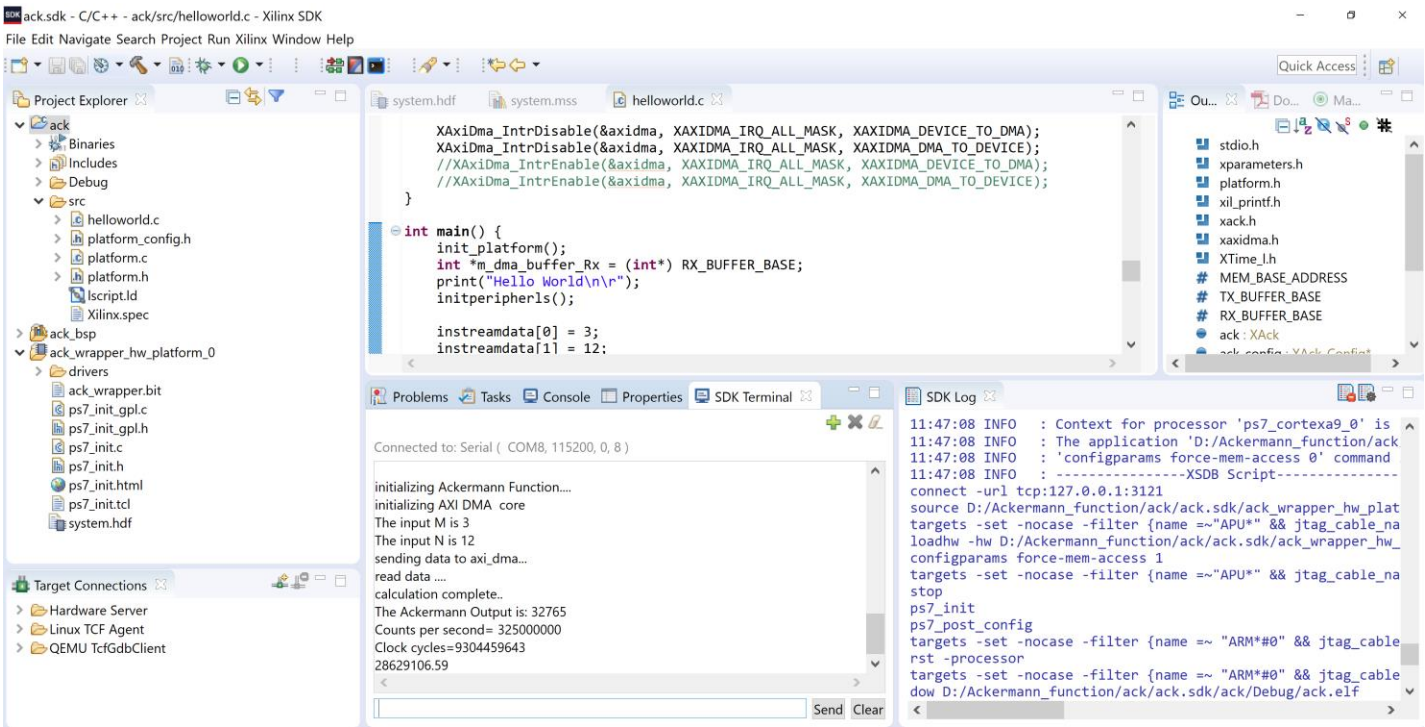
Resource	Utilization	Available	Utilization %
LUT	3327	14400	23.10
LUTRAM	206	6000	3.43
FF	3948	28800	13.71
BRAM	34	50	68.00



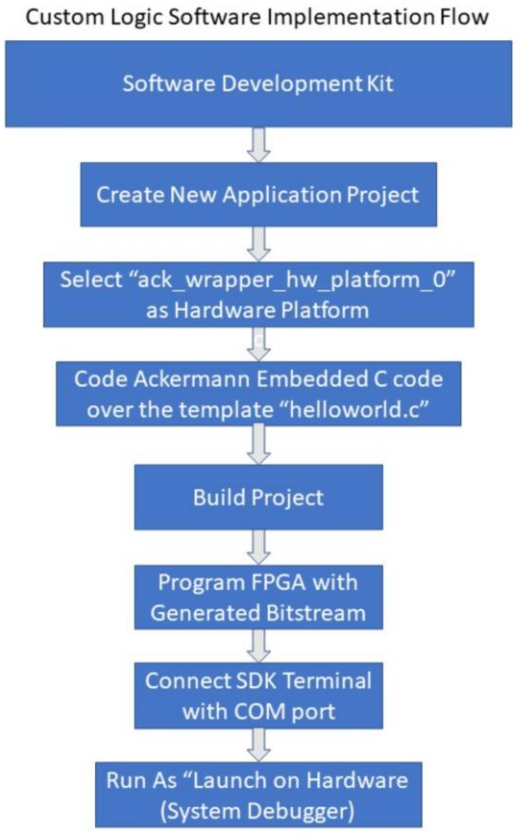
Software Development Kit



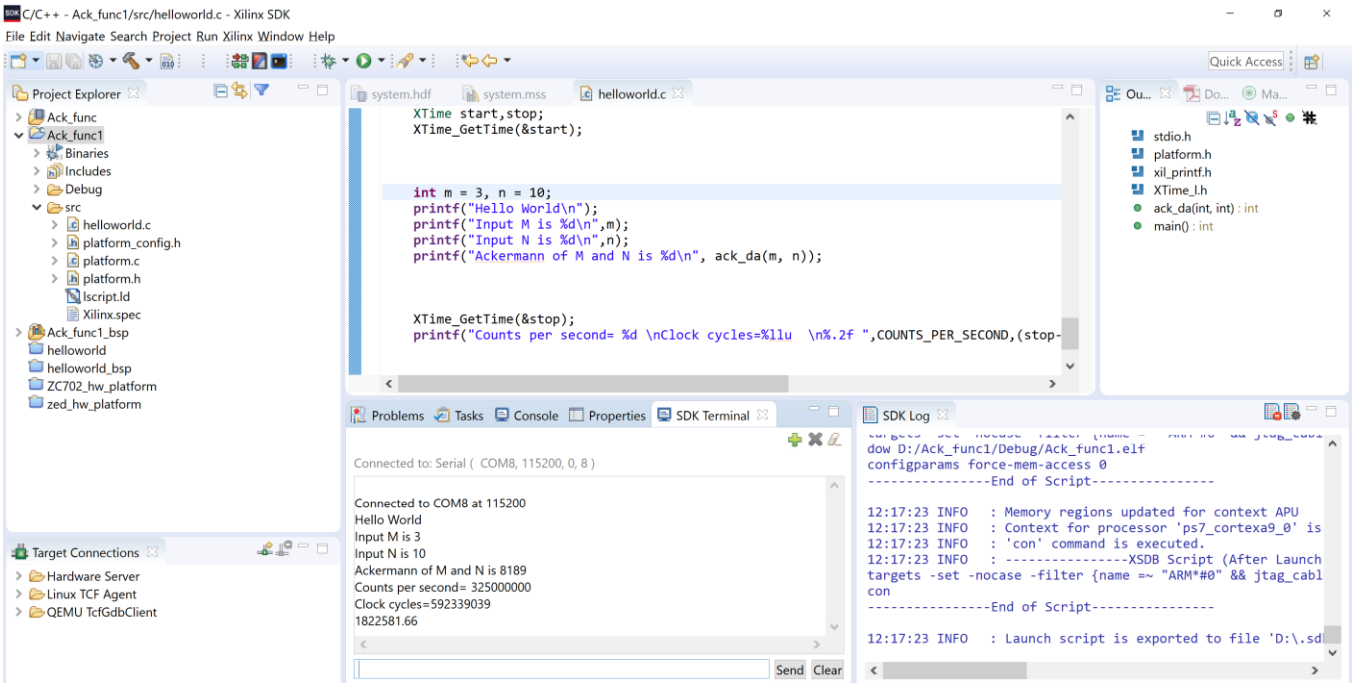
Software Development Kit Output



Custom Logic Implementation on Software



Software Development Kit Output



Hardware vs Software Performance Comparison

Clock cycles taken by Hardware: 9304459643

Clock cycles taken by Software: 592339039

Zybo Board Clock Period: 10ns

Therefore,

Time taken by Hardware Implementation: 9304459643 * 10ns = 93044.59643 ms

Time taken by Software Implementation: 592339039* 10ns = 5923.39039 ms

Hence,

Hardware is slower than Software by a factor of ~83 for the Ackermann logic implementation