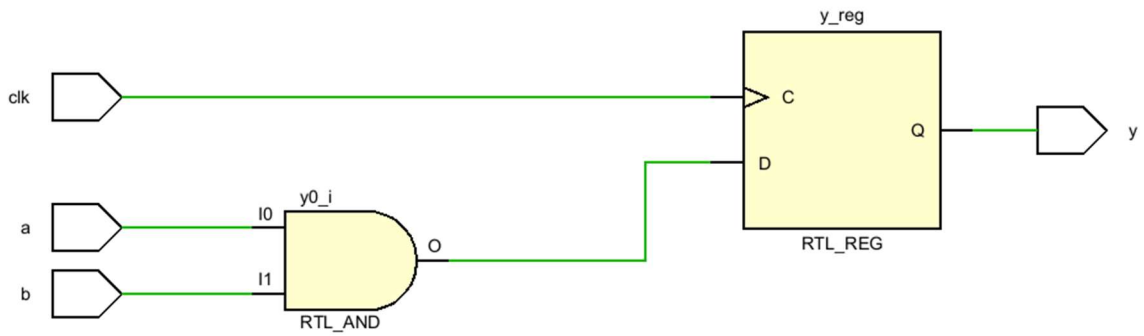
AND GATE WITH D FLIP FLOP

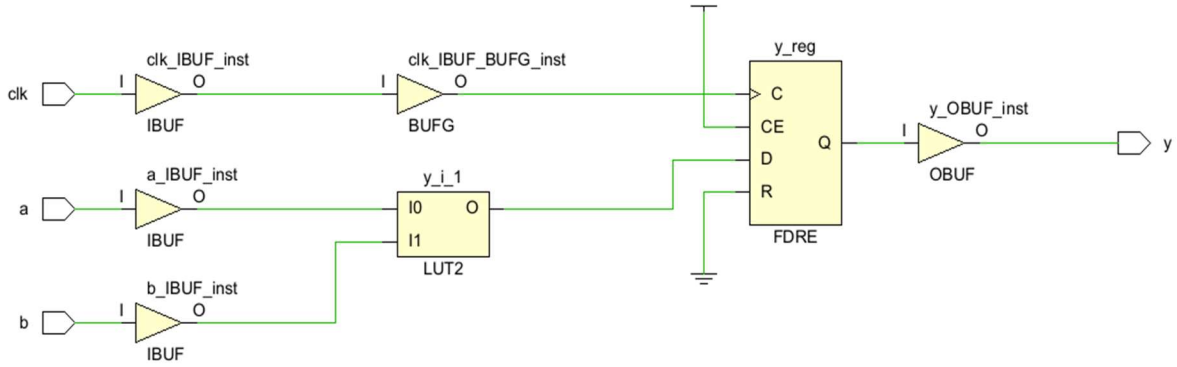
Verilog code:

```
module and_gate_d(input wire clk,
   input wire a,
   input wire b,
   output reg y
);
always @(posedge clk) begin
   y <= a & b;
end
endmodule
```

RTL analysis schematic:



Synthesis schematic:



Look Up Table:

Cell Properties

y_i_1

I1	I0	O=I0 ...
0	0	0
0	1	0
1	0	0
1	1	1