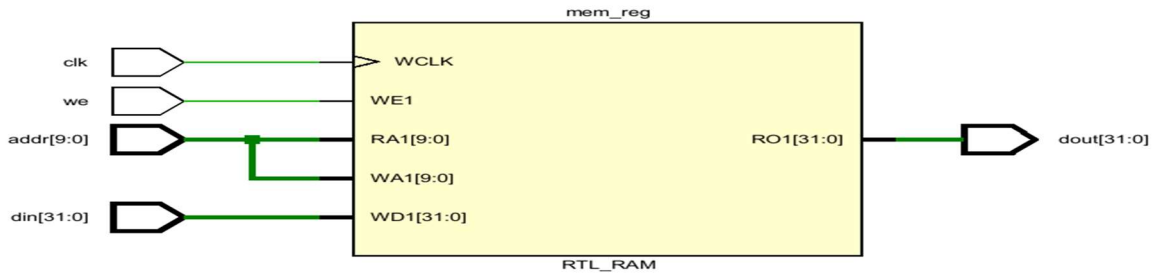
BRAM(PARAMETERIZED)

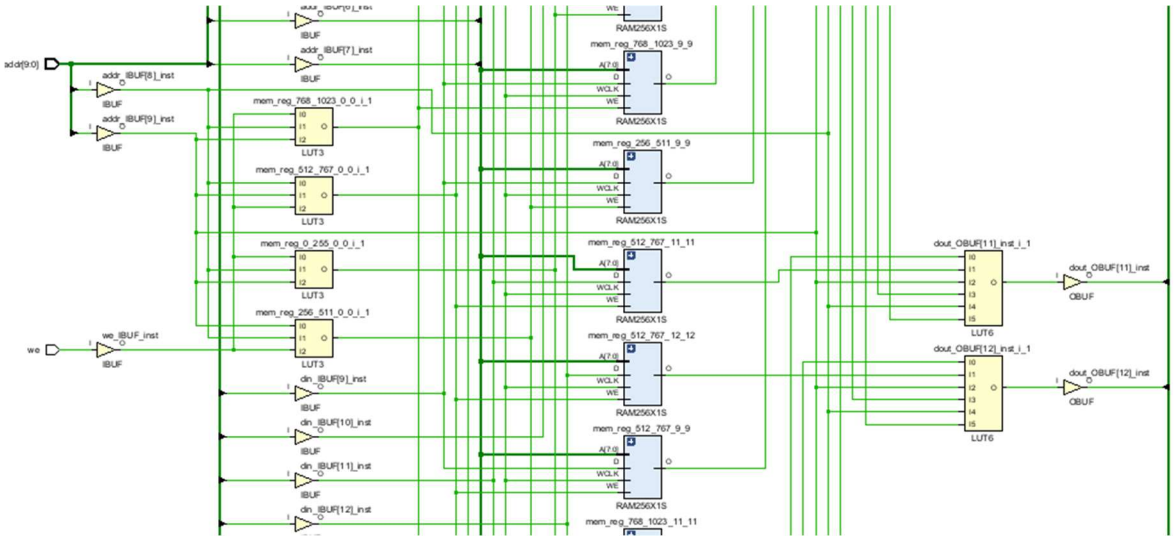
Verilog code:

```
module BRAM_para #(
   parameter WIDTH = 32,
   parameter DEPTH = 1024,
   parameter ADDR_WIDTH = 10
)(
   input clk,
   input we,
   input [ADDR_WIDTH-1:0] addr,
   input [WIDTH-1:0] din,
   output [WIDTH-1:0] dout
);
   reg [WIDTH-1:0] mem [0:DEPTH-1]
   always @(posedge clk) begin
      if (we) begin
         mem[addr] <= din;
      end
   end
   assign dout = mem[addr];
endmodule
```

RTL schematic:



Synthesis schematic:



1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	548	0	0	53200	1.03
LUT as Logic	36	0	0	53200	0.07
LUT as Memory	512	0	0	17400	2.94
LUT as Distributed RAM	512	0			
LUT as Shift Register	0	0			
Slice Registers	0	0	0	106400	0.00
Register as Flip Flop	0	0	0	106400	0.00
Register as Latch	0	0	0	106400	0.00
F7 Muxes	256	0	0	26600	0.96
F8 Muxes	128	0	0	13300	0.96