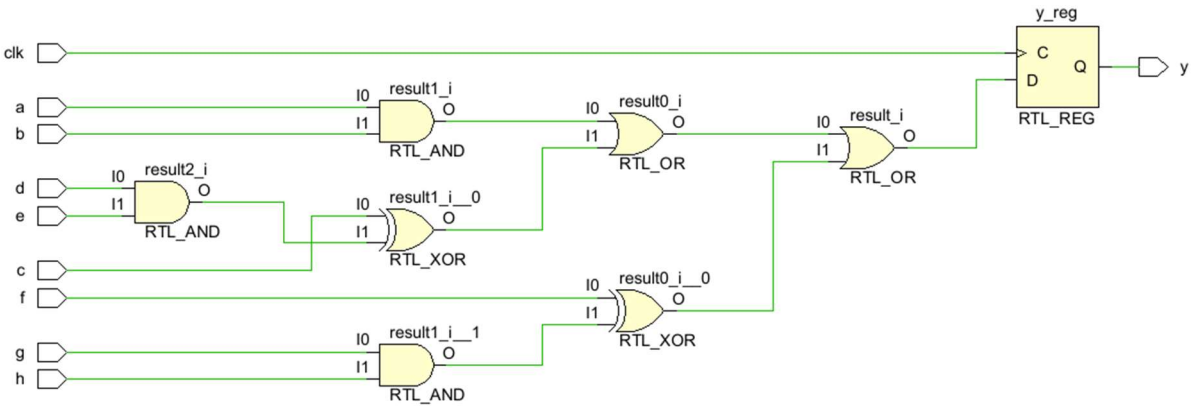
8 INPUT FUNCTION

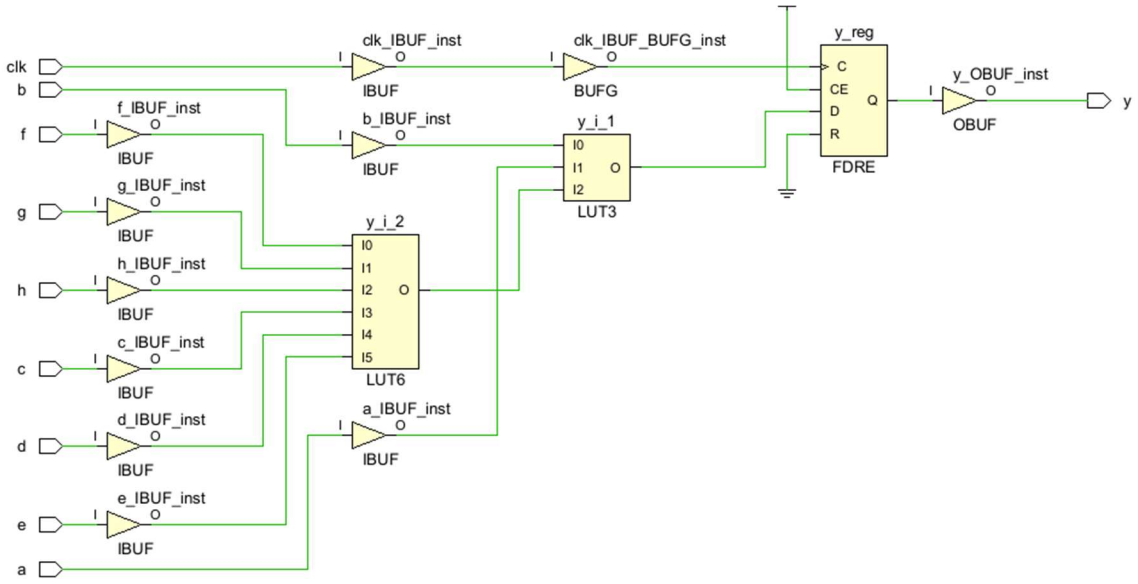
Verilog code:

```
module function_8bit(
    input  wire a, b, c, d, e, f, g, h,
    input  wire clk,
    output reg y
);
    wire result;
    assign result = (a & b) | (c ^ (d & e)) | (f ^ (g & h));
    always @(posedge clk) begin
        y <= result;
    end
endmodule
```

RTL schematic analysis:



Synthesis schematic:



Look Up Tables:

Cell Properties

y_i_2

I5	I4	I3	I2	I1	I0	O=!I0 & I1 & I2 + !I3 & I4 & I5 + I0 & !I2 + I3 & !I5 + I0 & !I1 & I2 + I3 & !I4 & I5
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	0
0	0	0	0	1	1	1
0	0	0	1	0	0	0
0	0	0	1	0	1	1
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	1	0	0	0	1
0	0	1	0	0	1	1
0	0	1	0	1	0	1
0	0	1	0	1	1	1
0	0	1	1	0	0	1
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	0	1	1
0	1	0	0	1	0	0
0	1	0	0	1	1	1
0	1	0	1	0	0	0
0	1	0	1	0	1	1
0	1	0	1	1	0	1
0	1	0	1	1	1	0
0	1	1	0	0	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	1
0	1	1	0	1	1	1
0	1	1	1	0	0	1
0	1	1	1	0	1	1
0	1	1	1	1	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	0	0	1	1
1	0	0	0	1	0	0
1	0	0	0	1	1	1

1	0	0	1	0	0	0
1	0	0	1	0	1	1
1	0	0	1	1	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	0	1	0	0	1	1
1	0	1	0	1	0	1
1	0	1	0	1	1	1
1	0	1	1	0	0	1
1	0	1	1	0	1	1
1	0	1	1	1	0	1
1	0	1	1	1	1	1
1	1	0	0	0	0	1
1	1	0	0	0	1	1
1	1	0	0	1	0	1
1	1	0	0	1	1	1
1	1	0	1	0	0	1
1	1	0	1	0	1	1
1	1	0	1	1	0	1
1	1	0	1	1	1	1
1	1	1	0	0	0	0
1	1	1	0	0	1	1
1	1	1	0	1	0	0
1	1	1	0	1	1	1
1	1	1	1	0	0	0
1	1	1	1	0	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Figure 1: LUT6

Cell Properties

y_i_1

I2	I1	I0	O=I0 & I1 + I2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Figure 2: LUT3

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	2	0	0	53200	<0.01
LUT as Logic	2	0	0	53200	<0.01
LUT as Memory	0	0	0	17400	0.00
Slice Registers	1	0	0	106400	<0.01
Register as Flip Flop	1	0	0	106400	<0.01
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00