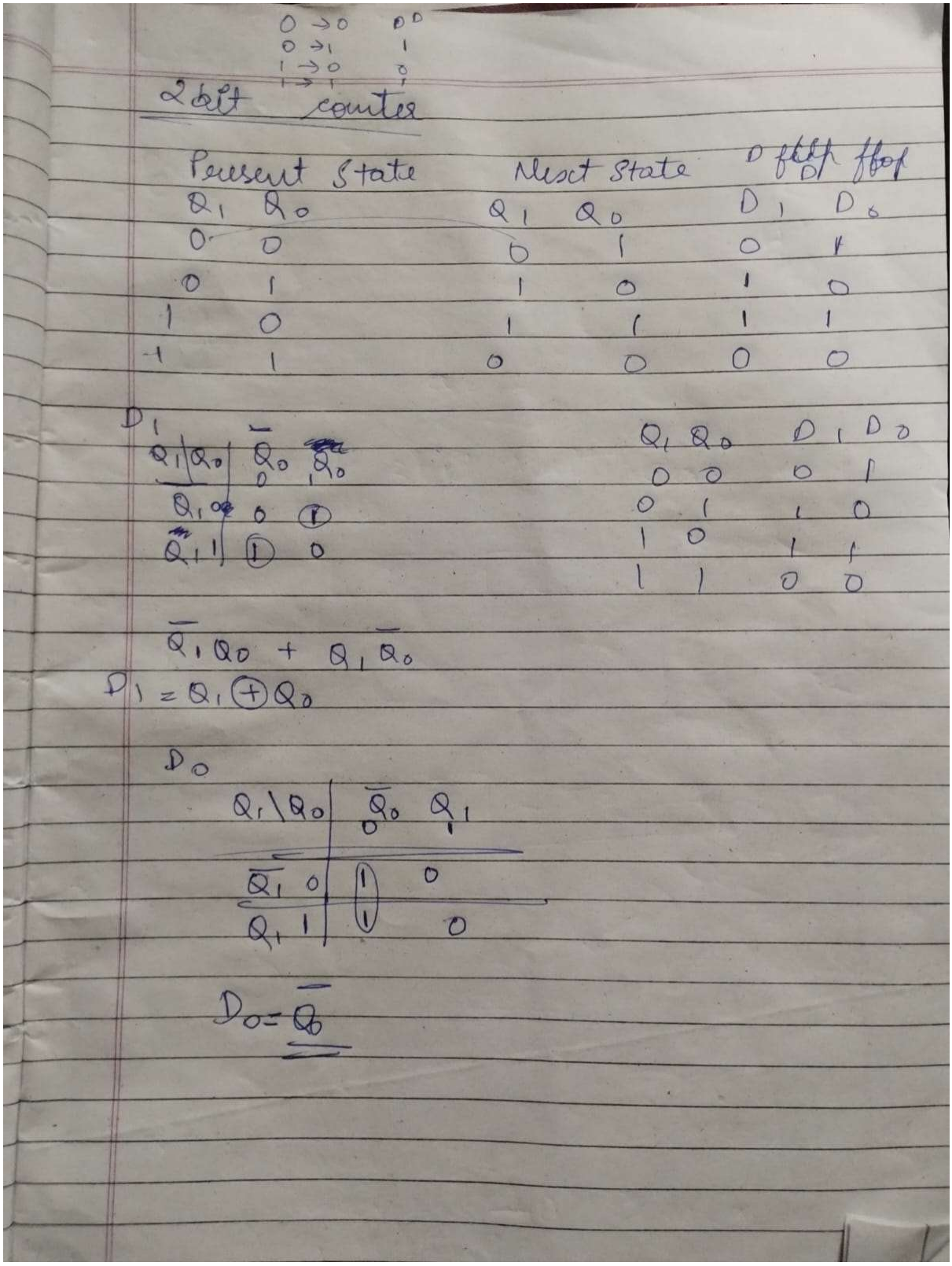
2 BIT COUNTER

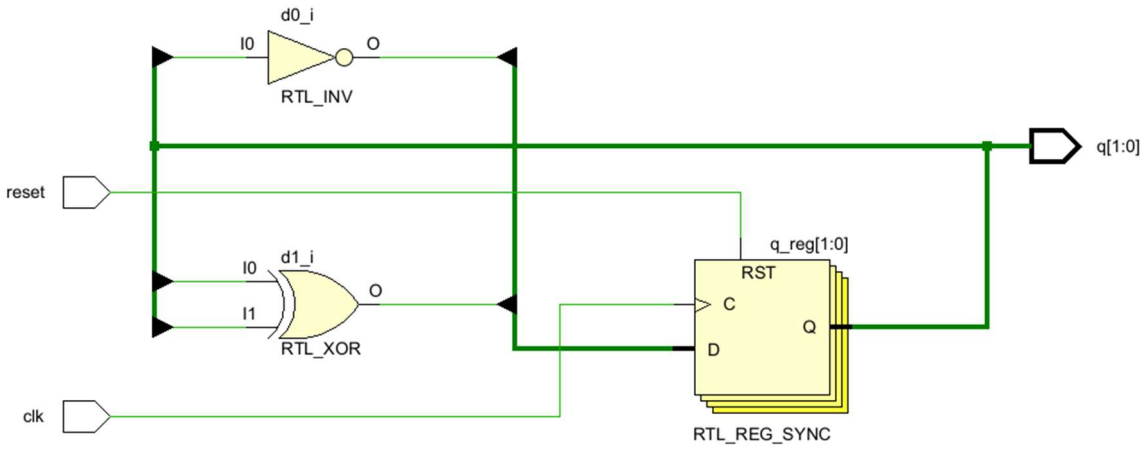


Verilog code:

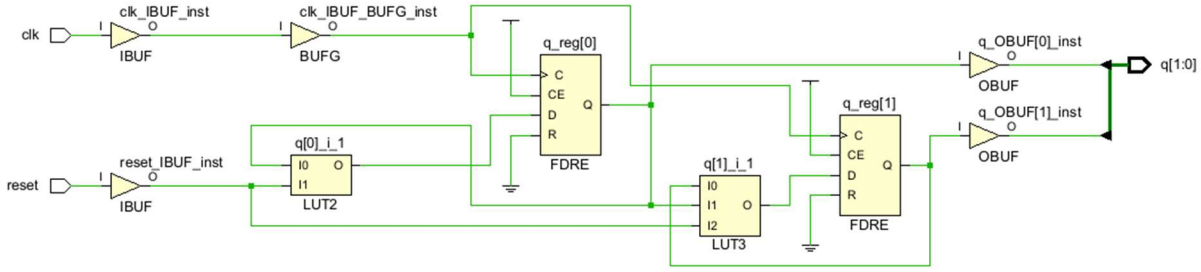
```
module counter_2bit (clk, reset, q);
   input wire clk;
   input wire reset;
   output reg [1:0]q;
   wire d0, d1;

   assign d0 = ~q[0];
   assign d1 = q[1] ^ q[0];
   always @(posedge clk) begin
      if (reset)
         q <= 2'b00;
      else
         q <= {d1, d0};
   end
   endmodule
```

RTL analysis schematic:



Synthesis analysis schematic:



Look Up Tables:

Cell Properties

q[0]_i_1

I1	I0	O=!I0 & !I1
0	0	1
0	1	0
1	0	0
1	1	0

Figure 1: LUT for q[0]

Cell Properties

q[1]_i_1

I2	I1	I0	O=I0 & !I1 & !I2 + !I0 & I1 & !I2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 2: LUT for q[1]