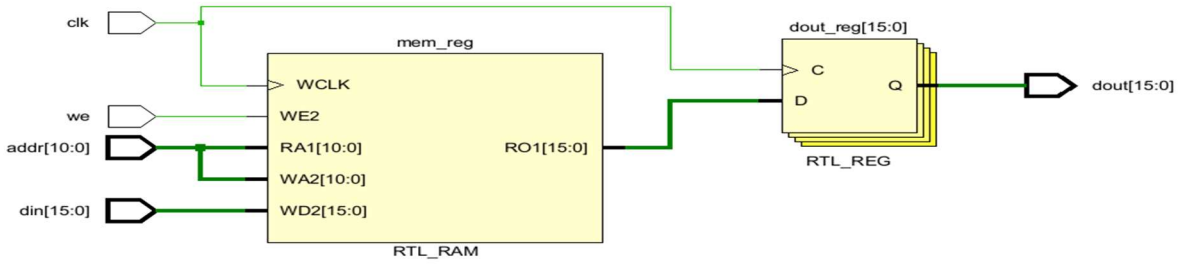
MEMORIES

Single port BRAM (16 X 2048)

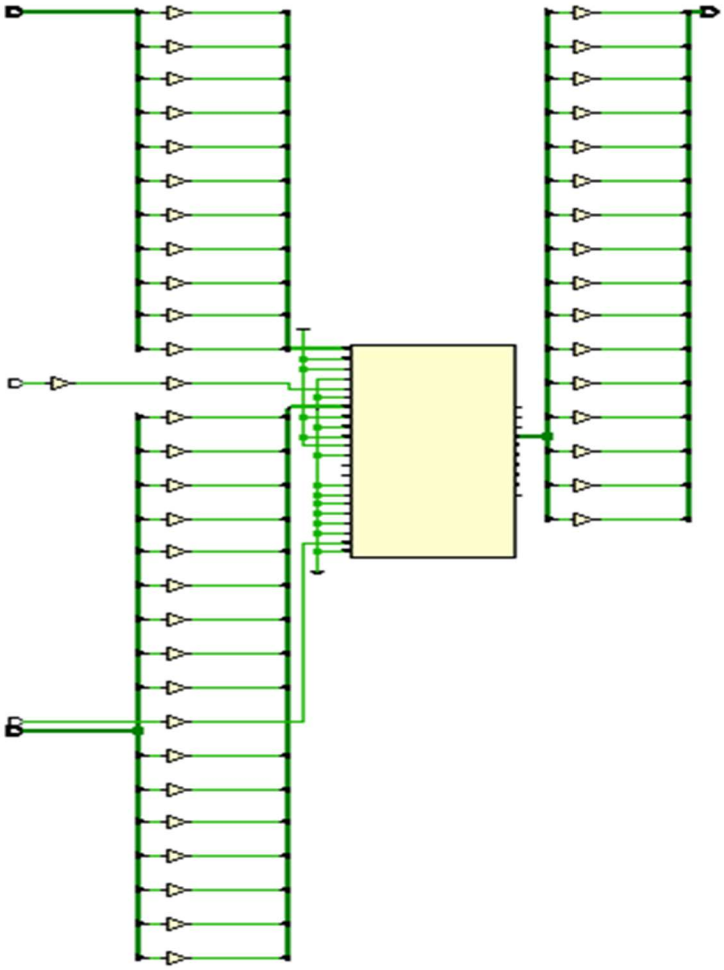
Verilog code:

```
module singleport_BRAM(
   input clk,
   input we,
   input [10:0] addr,
   input [15:0] din,
   output reg [15:0] dout
);
   (* ram_style = "block" *)
   reg [15:0] mem [0:2047];
   always @(posedge clk) begin
      if (we) begin
         mem[addr] <= din;
      end
      dout <= mem[addr];
   end
endmodule
```

RTL schematic:



Synthesis schematic:



2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	1	0	0	140	0.71
RAMB36/FIFO*	1	0	0	140	0.71
RAMB36E1 only	1				
RAMB18	0	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accomm

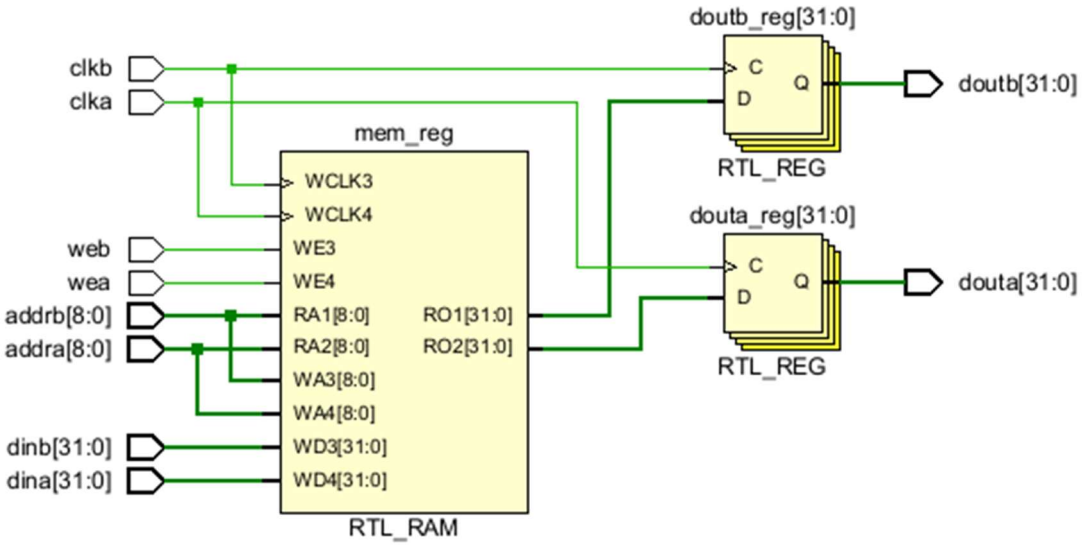
ONE 36K BRAM is needed since (16x2048 =32768) less than 36K = 36x1024 = 36864 of RAMB36E1

True dual port BRAM (32X16K)

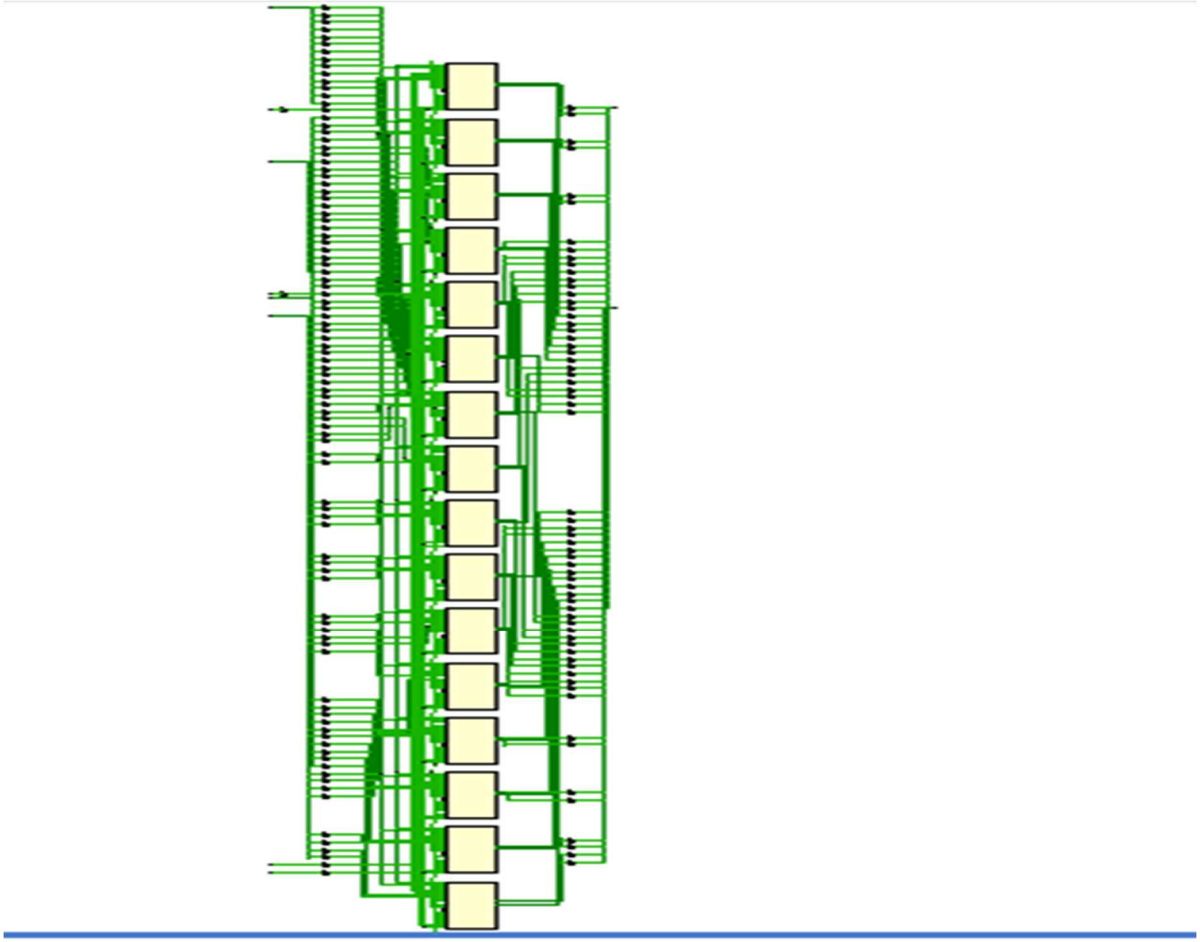
Verilog code:

```
module truedualport_BRAM (
   input clka,
   input clkb,
   input wea,
   input web,
   input [8:0] addra,
   input [8:0] addrb,
   input [31:0] dina,
   input [31:0] dinb,
   output reg [31:0] douta,
   output reg [31:0] doutb
);
   (* ram_style = "block" *)
   reg [31:0] mem [0:511];     // locations   ( 16K = 16384) 16384 /32 = 512 words
   always @(posedge clka) begin
      if (wea)
         mem[addra] <= dina;
      douta <= mem[addra];
   end
   always @(posedge clkb) begin
      if (web)
         mem[addrb] <= dinb;
      doutb <= mem[addrb];
   end
endmodule
```

RTL schematic:



Synthesis schematic:

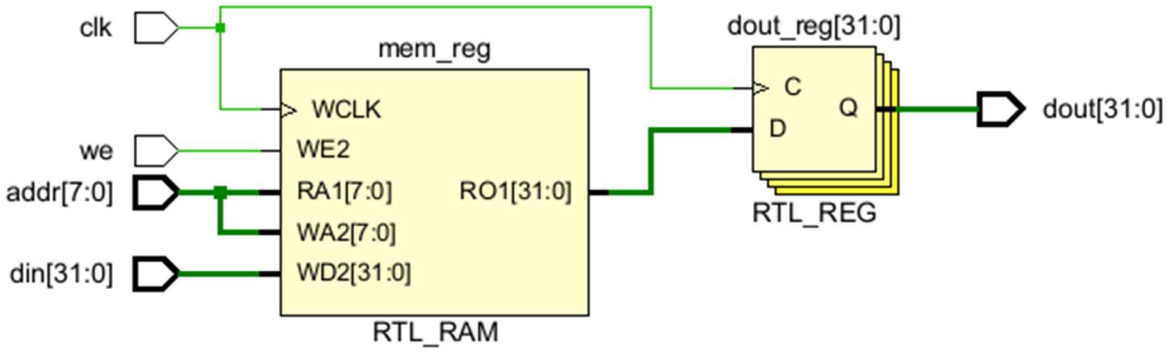


Distributed BRAM (256 X 32)

Verilog code:

```
module distributed_BRAM (
   input clk,
   input we,
   input [7:0] addr,
   input [31:0] din,
   output reg [31:0] dout
);
   (* ram_style = "distributed" *)
   reg [31:0] mem [0:255];
   always @(posedge clk) begin
      if (we)
         mem[addr] <= din;
      dout <= mem[addr];
   end
endmodule
```

RTL schematic:



2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	128	0	0	53200	0.24
LUT as Logic	0	0	0	53200	0.00
LUT as Memory	128	0	0	17400	0.74
LUT as Distributed RAM	128	0			
LUT as Shift Register	0	0			
Slice Registers	32	0	0	106400	0.03
Register as Flip Flop	32	0	0	106400	0.03
Register as Latch	0	0	0	106400	0.00
F7 Muxes	64	0	0	26600	0.24
F8 Muxes	32	0	0	13300	0.24