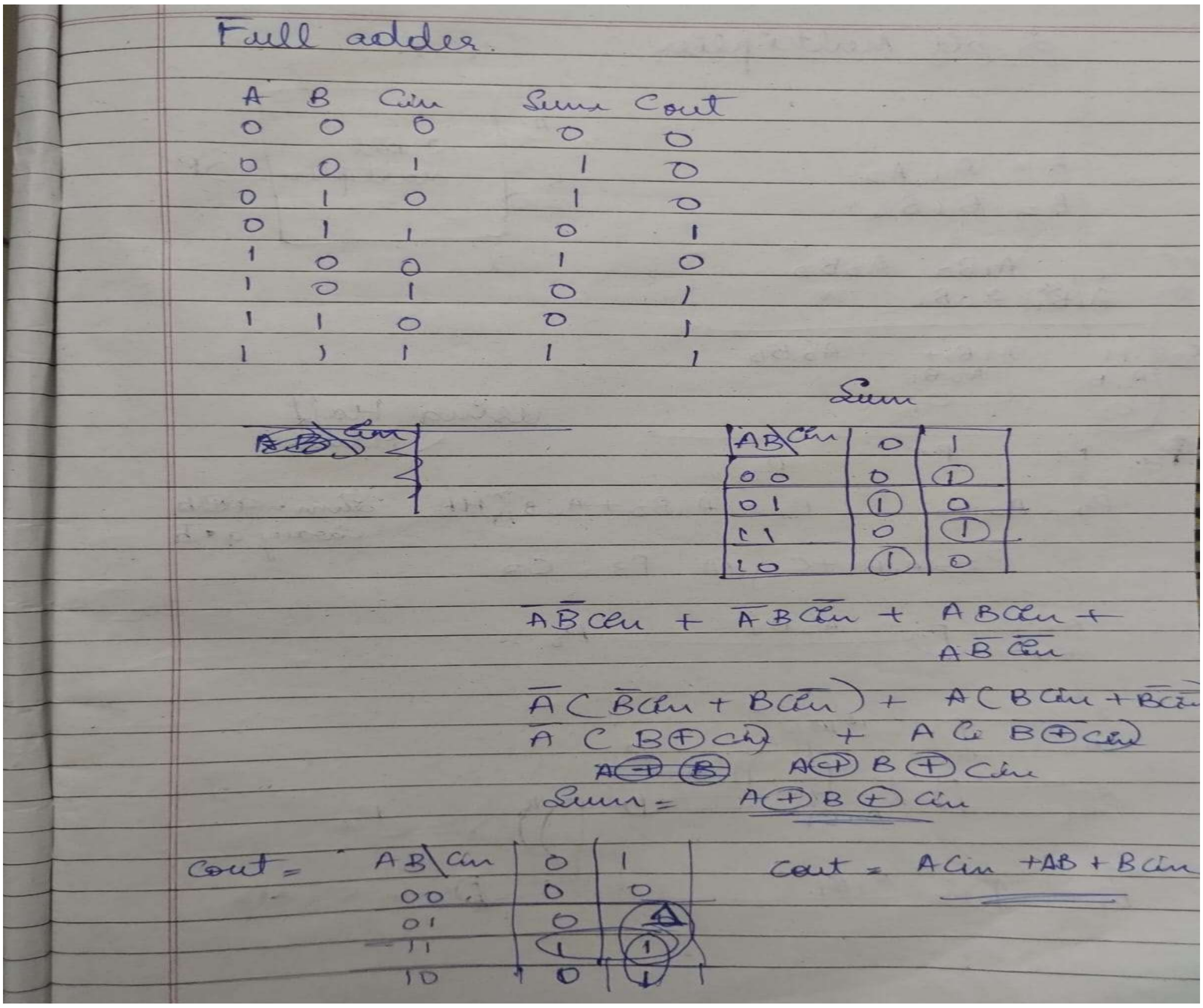
Full Adder



Full adder.

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

~~AB~~ Cin

Sum

AB\Cin	0	1
00	0	1
01	1	0
11	0	1
10	1	0

$\bar{A}\bar{B}Cin + \bar{A}B\overline{Cin} + ABCin + A\bar{B}\overline{Cin}$

$\bar{A}(\bar{B}Cin + B\overline{Cin}) + A(BCin + \bar{B}\overline{Ci}$

$\bar{A}(B \oplus Cin) + A(\overline{B \oplus Cin})$

~~$A \oplus B$~~ $A \oplus B \oplus Cin$

Sum = $\underline{A \oplus B \oplus Cin}$

Cout =

AB\Cin	0	1
00	0	0
01	0	1
11	1	1
10	0	1

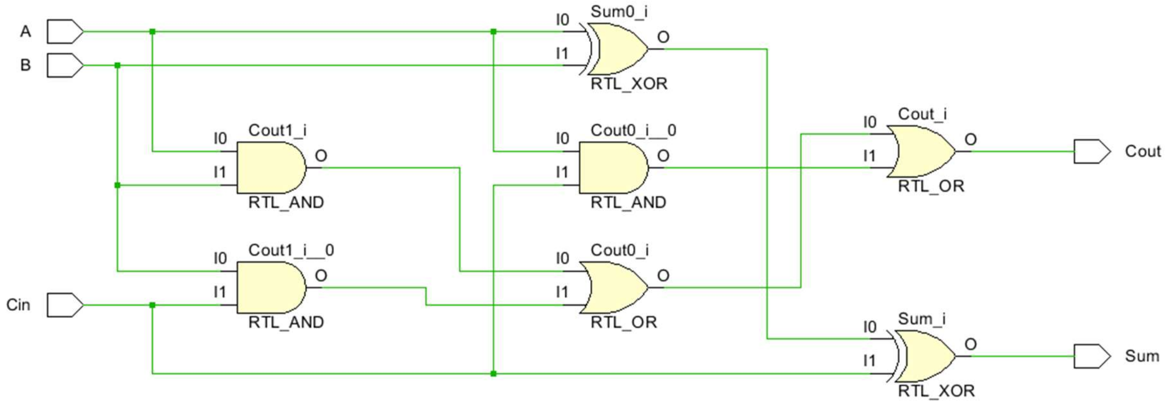
Cout = $\underline{ACin + AB + BCin}$

Verilog Code

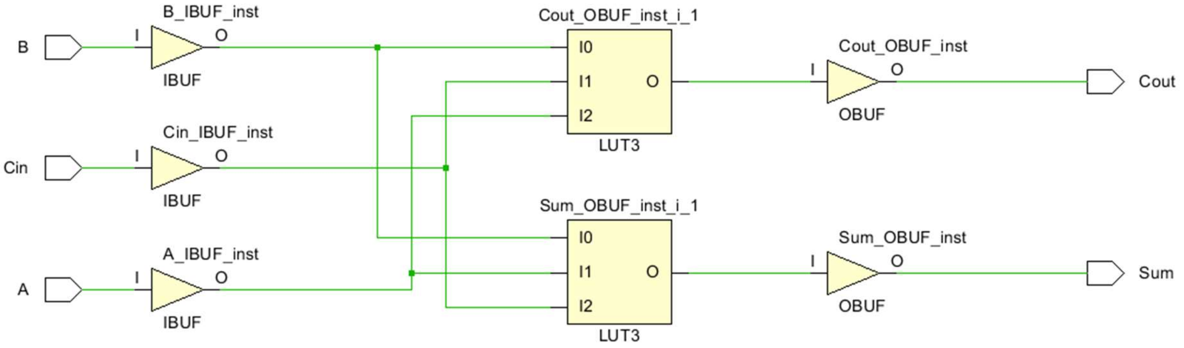
```
module fulladder(A, B, Cin, Sum, Cout);
 input wire A, B, Cin;
 output wire Sum, Cout;

 assign Sum = A ^ B ^ Cin;
 assign Cout = (A & B) | (B & Cin) | (A & Cin);
endmodule
```

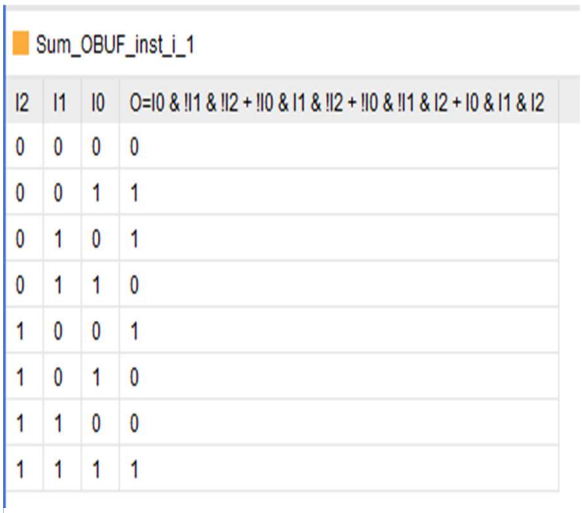
RTL analysis schematic:



Synthesis schematic:



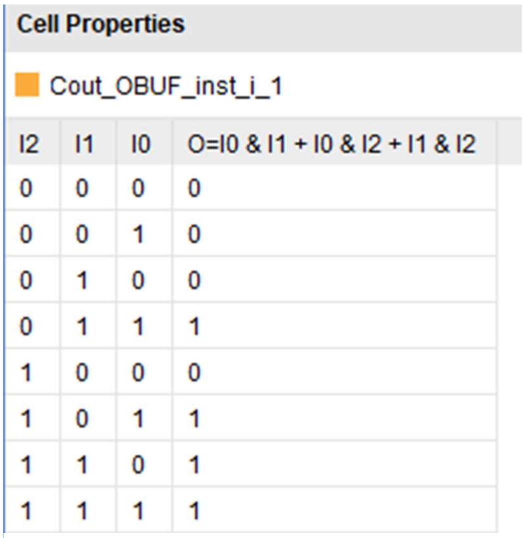
Look Up Table:



Sum_OBUF_inst_i_1

I2	I1	I0	O=I0 & !I1 & !I2 + !I0 & I1 & !I2 + !I0 & !I1 & I2 + I0 & I1 & I2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure 1:LUT Sum



Cell Properties

Cout_OBUF_inst_i_1

I2	I1	I0	O=I0 & I1 + I0 & I2 + I1 & I2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 2: LUT Carry