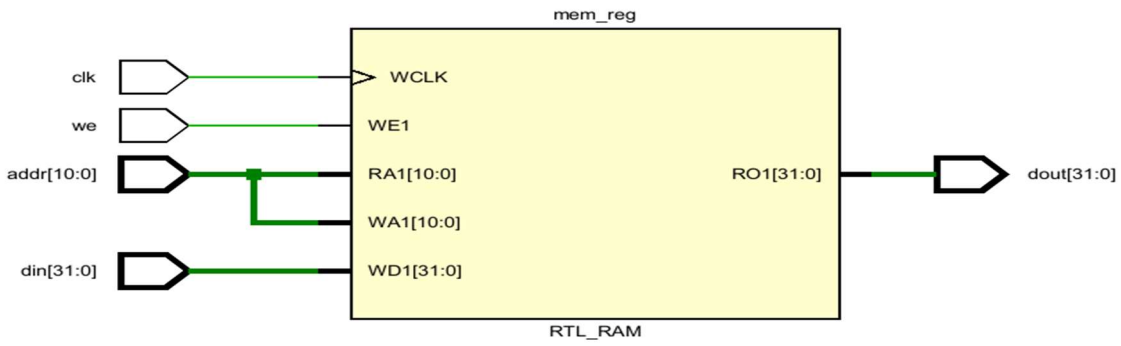
BRAM (50K bits LUT)

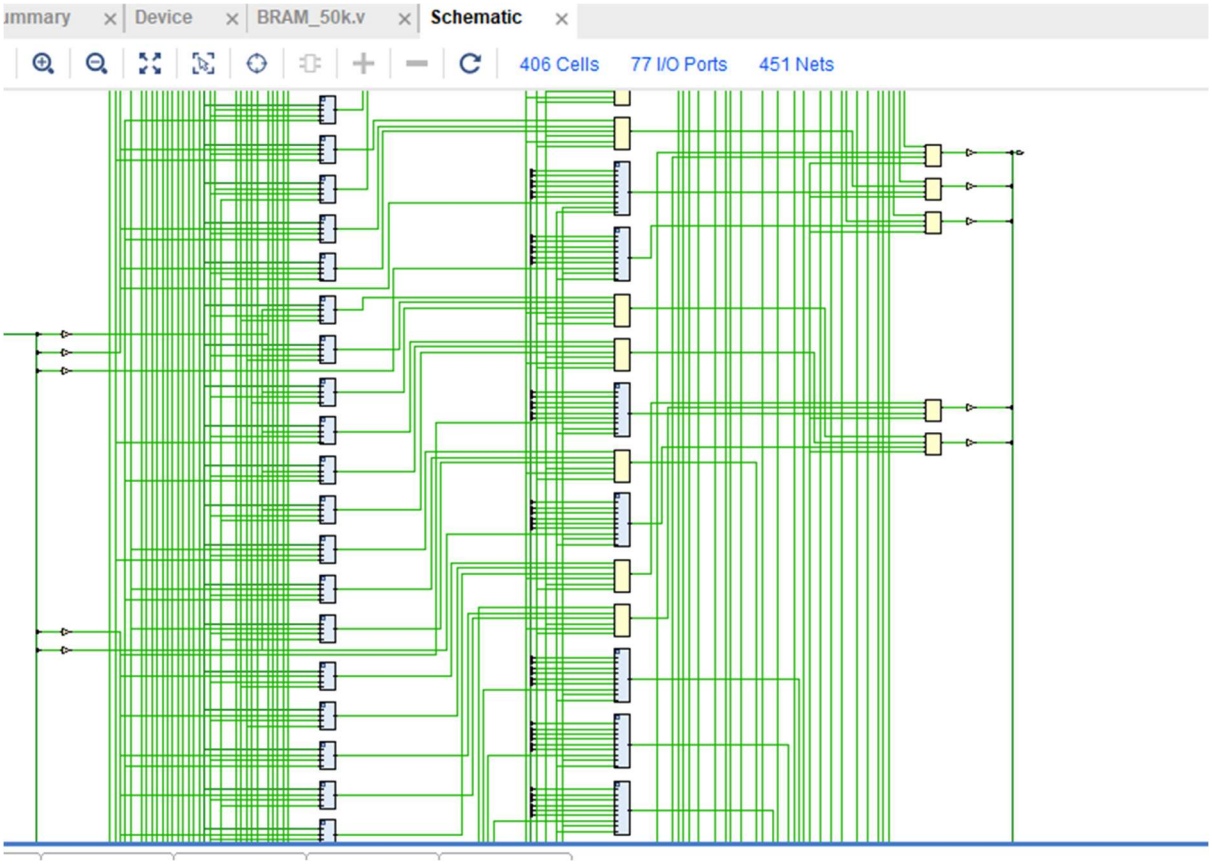
Verilog code:

```
module BRAM_50K #(
   parameter WIDTH = 32,
   parameter DEPTH = 1600,
   parameter ADDR_WIDTH = 11
)(
   input clk,
   input we,
   input [ADDR_WIDTH-1:0] addr,
   input [WIDTH-1:0] din,
   output [WIDTH-1:0] dout
);
   reg [WIDTH-1:0] mem [0:DEPTH-1];
   always @(posedge clk) begin
      if (we)
         mem[addr] <= din;
   end
   assign dout = mem[addr];
endmodule
```

RTL schematic:



Synthesis schematic:



1. Slice Logic

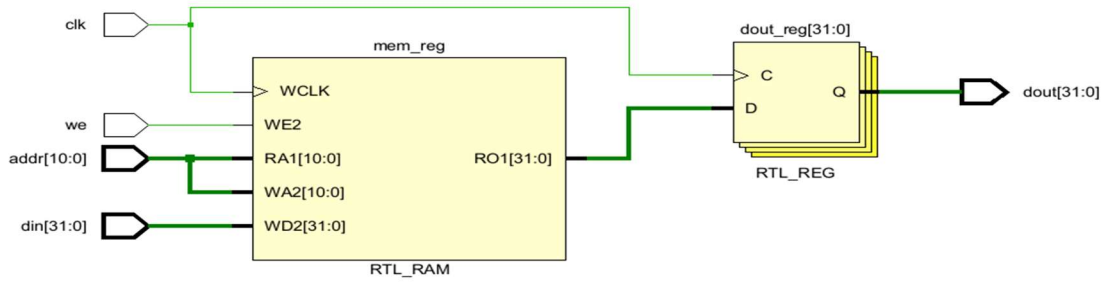
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	904	0	0	53200	1.70
LUT as Logic	104	0	0	53200	0.20
LUT as Memory	800	0	0	17400	4.60
LUT as Distributed RAM	800	0			
LUT as Shift Register	0	0			
Slice Registers	0	0	0	106400	0.00
Register as Flip Flop	0	0	0	106400	0.00
Register as Latch	0	0	0	106400	0.00
F7 Muxes	384	0	0	26600	1.44
F8 Muxes	192	0	0	13300	1.44

BRAM (50K bits uses block memory)

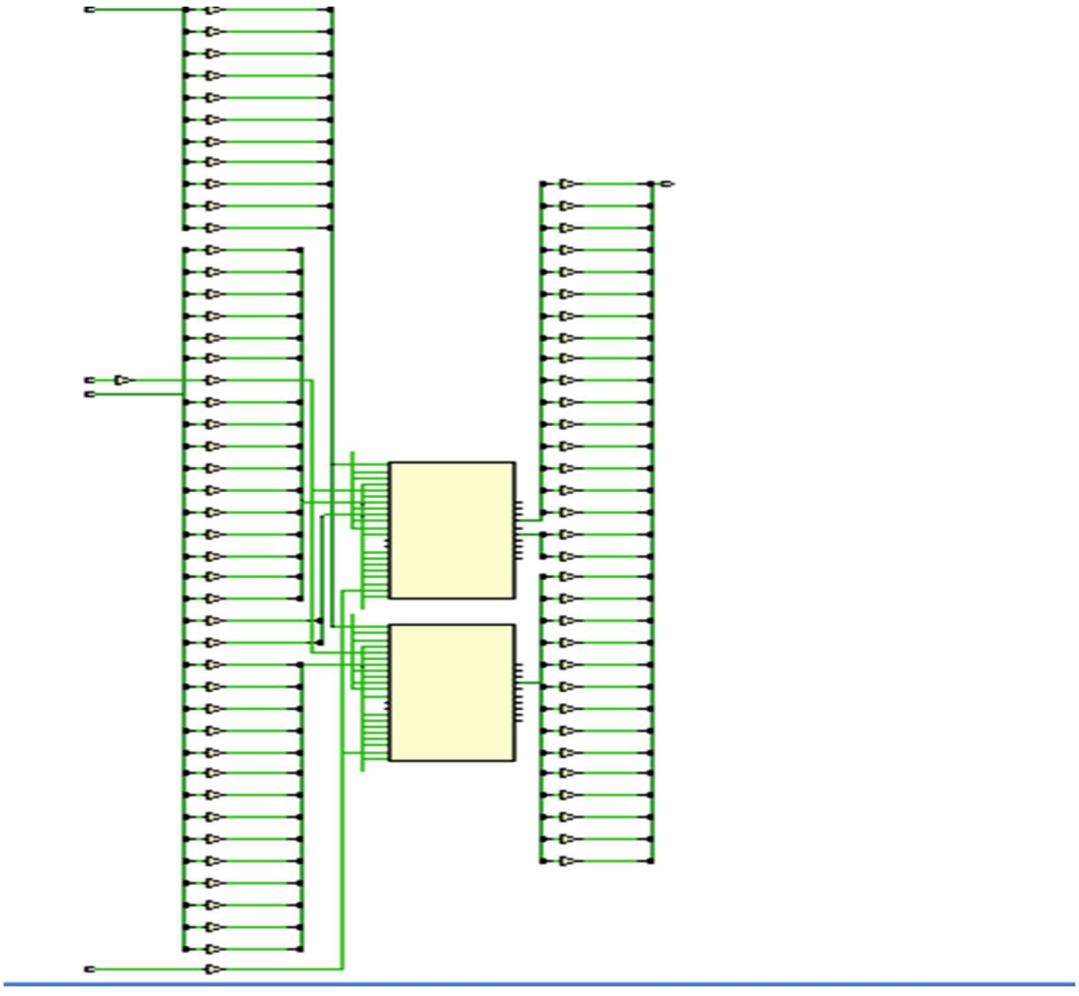
Verilog code:

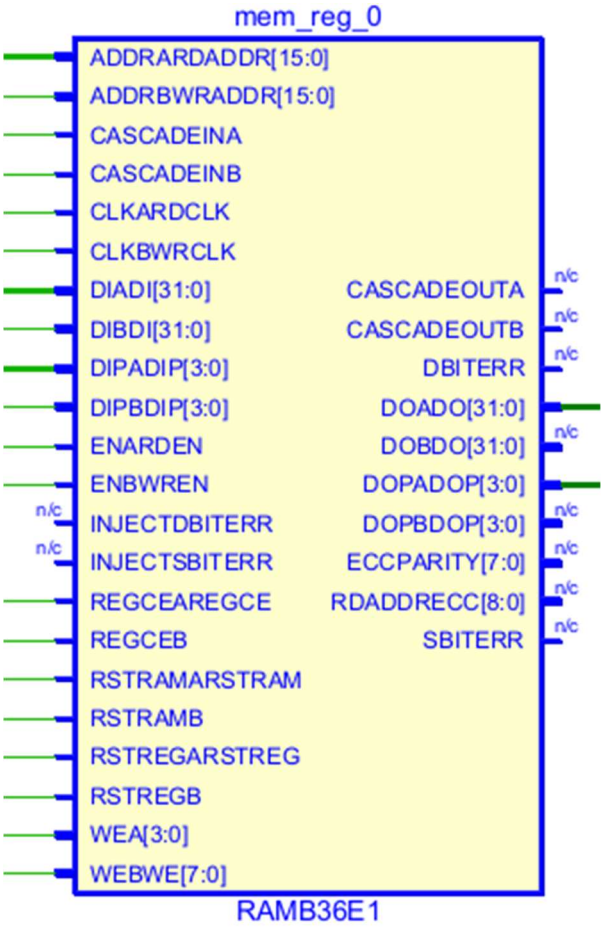
```
module BRAM_2 #(
    parameter WIDTH = 32,
    parameter DEPTH = 1600,
    parameter ADDR_WIDTH = 11
)(
    input clk,
    input we,
    input [ADDR_WIDTH-1:0] addr,
    input [WIDTH-1:0] din,
    output reg [WIDTH-1:0] dout
);
    (* ram_style = "block" *)
    reg [WIDTH-1:0] mem [0:DEPTH-1];
    always @(posedge clk) begin
        if (we) begin
            mem[addr] <= din;
        end
        dout <= mem[addr];
    end
endmodule
```

RTL schematic:



Synthesis schematic:





2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	2	0	0	140	1.43
RAMB36/FIFO*	2	0	0	140	1.43
RAMB36E1 only	2				
RAMB18	0	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefo