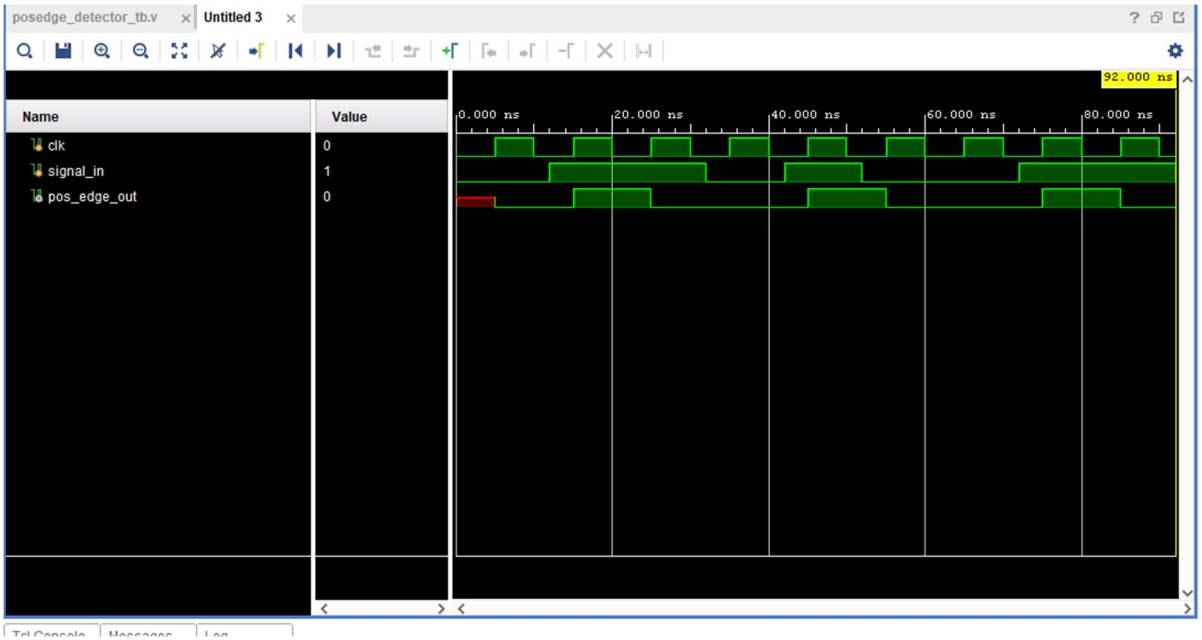
EDGE DETECTOR

Positive edge detector:

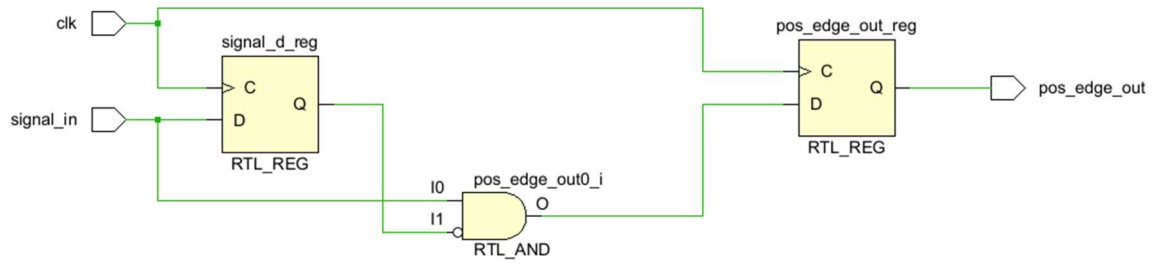
Verilog code:

```
module posedge_detector(
   input  wire clk,
   input  wire signal_in,
   output reg  pos_edge_out
);
   reg signal_d;
   always @(posedge clk) begin
      signal_d <= signal_in;
      pos_edge_out <= signal_in & ~signal_d;
   end
endmodule
```

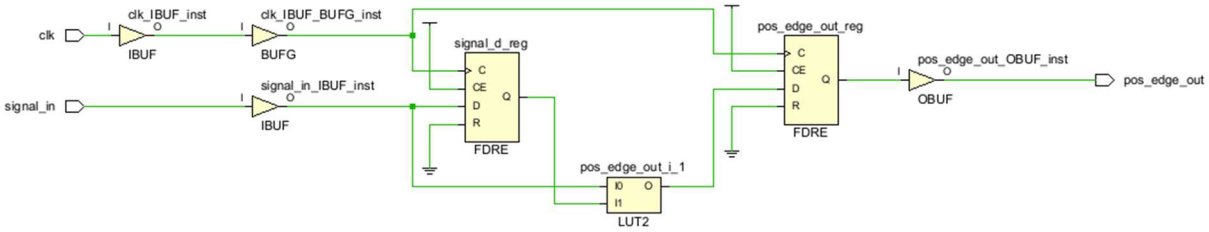
Waveform:



RTL analysis:



Synthesis schematic:



Look Up Table:

Cell Properties

pos_edge_out_i_1

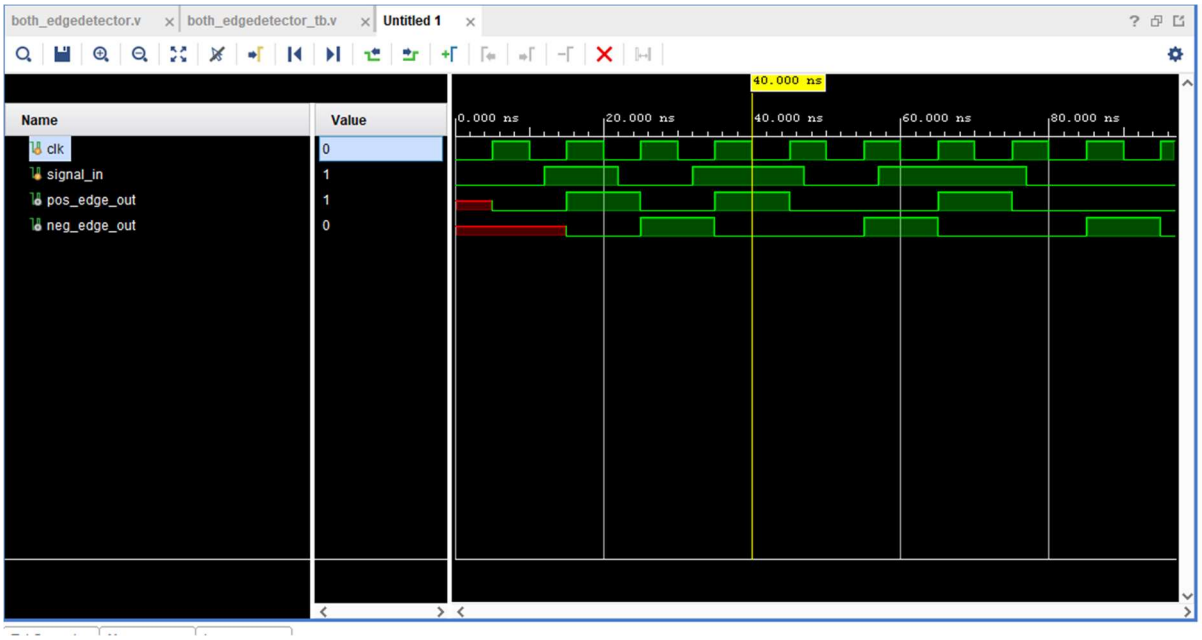
I1	I0	O=I0 & !I1
0	0	0
0	1	1
1	0	0
1	1	0

Both edge detector:

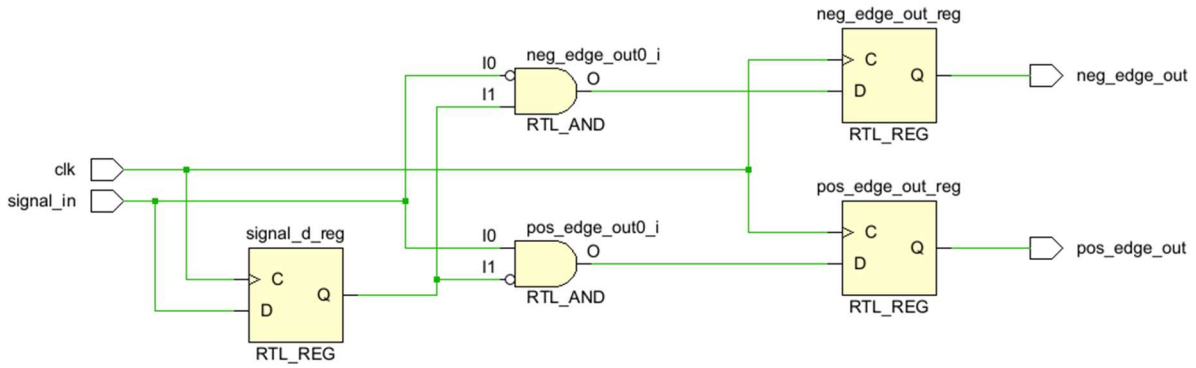
Verilog code:

```
module both_edgedetector (
    input  wire clk,
    input  wire signal_in,
    output reg  pos_edge_out,
    output reg  neg_edge_out
);
    reg signal_d;
    always @(posedge clk) begin
        signal_d     <= signal_in;
        pos_edge_out <=  signal_in & ~signal_d;
        neg_edge_out <= ~signal_in &  signal_d;
    end
endmodule
```

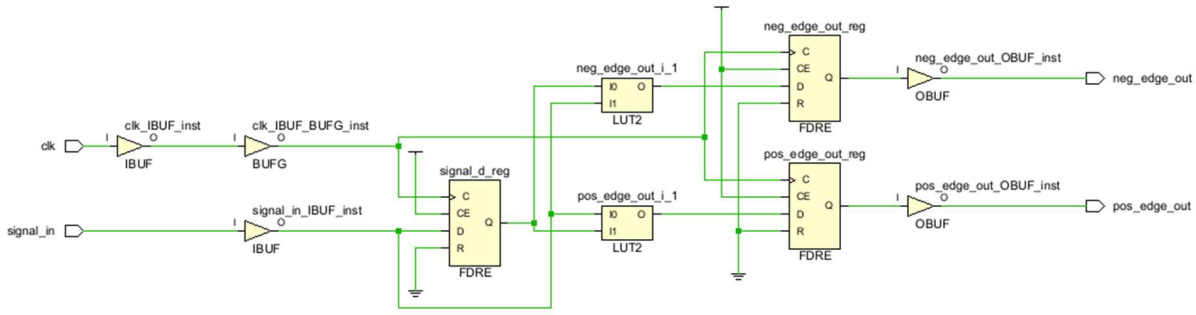
Waveform:



RTL schematic:



Synthesis schematic:



Look Up Table:

Cell Properties

pos_edge_out_i_1

I1	I0	O=I0 & !I1
0	0	0
0	1	1
1	0	0
1	1	0

Cell Properties

neg_edge_out_i_1

I1	I0	O=I0 & !I1
0	0	0
0	1	1
1	0	0
1	1	0