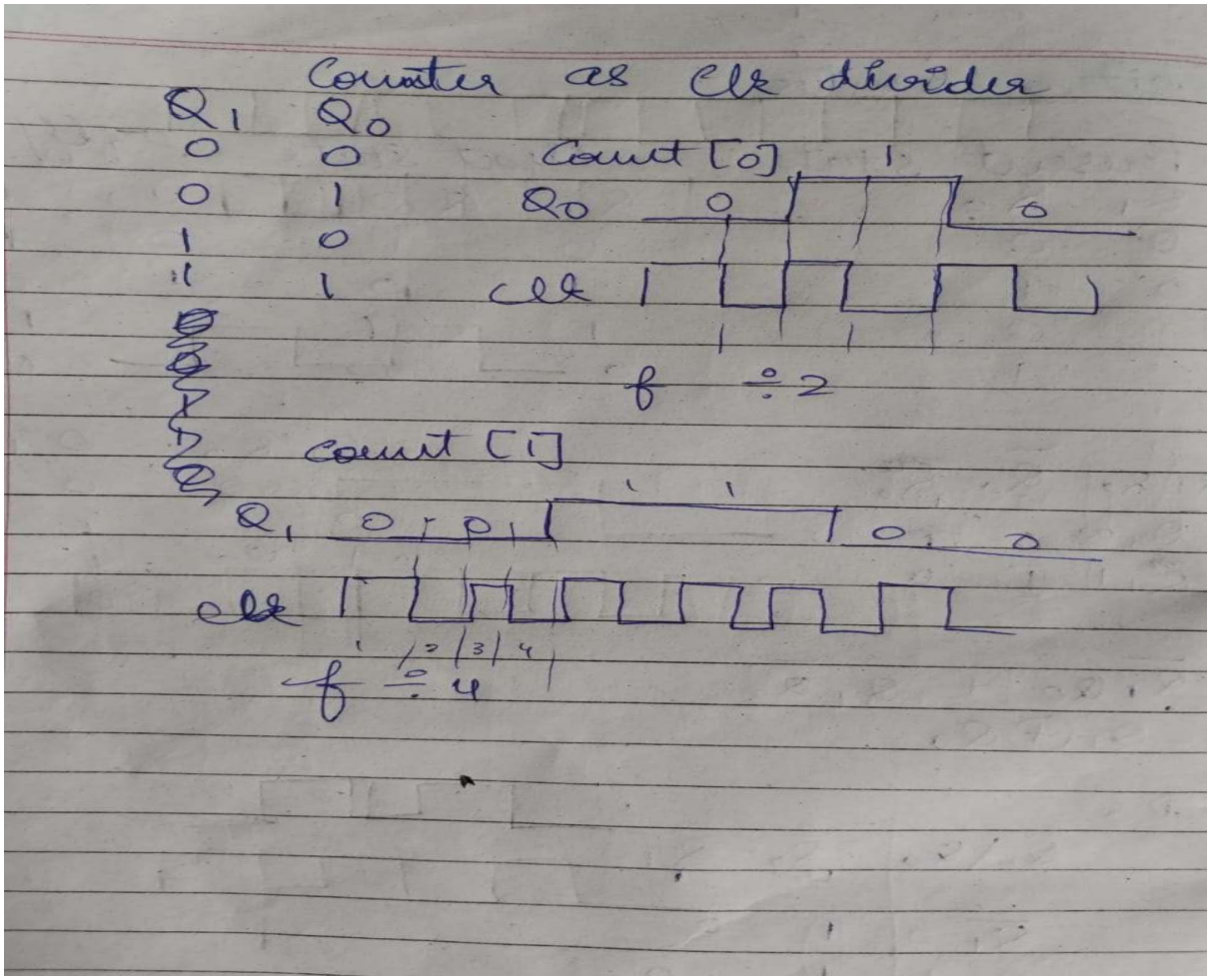
COUNTER AS CLOCK DIVIDER

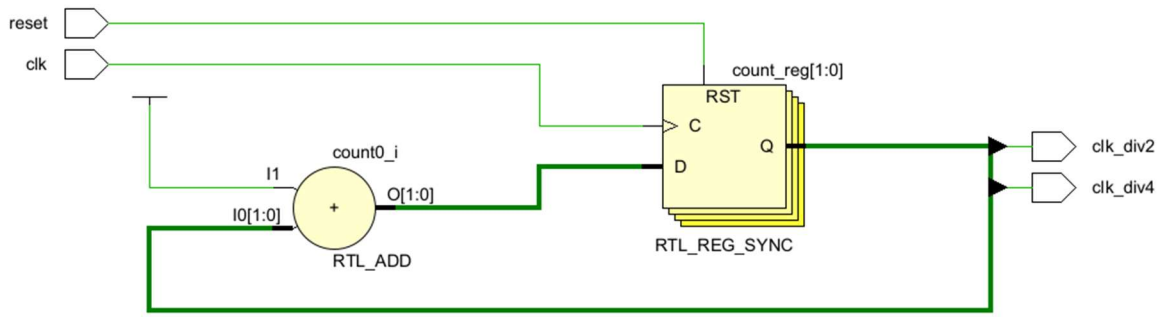


Verilog code:

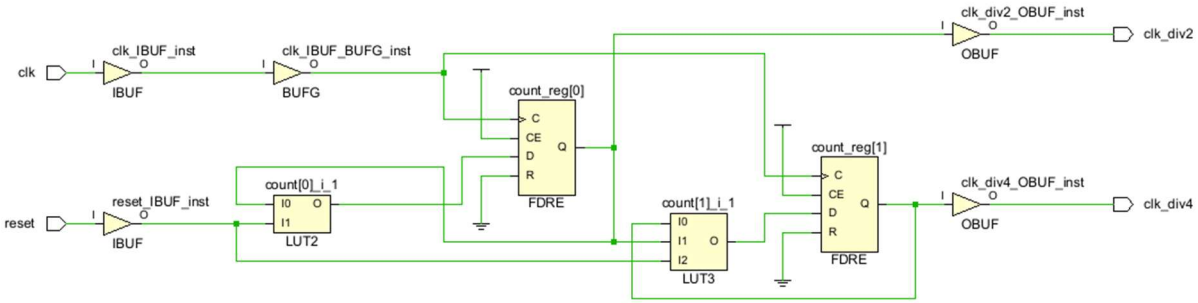
```
module couter_clkdivider(
    input wire clk,
    input wire reset,
    output wire clk_div2,
    output wire clk_div4
);
    reg [1:0] count;
    always @(posedge clk) begin
```

```
        if (reset)
            count <= 2'b00;
        else
            count <= count + 1;
    end
    assign clk_div2 = count[0];
    assign clk_div4 = count[1];
endmodule
```

RTL analysis schematic:



Synthesis schematic:



Look Up Tables:

Cell Properties

count[0]_i_1

I1	I0	O=!I0 & !I1
0	0	1
0	1	0
1	0	0
1	1	0

Figure 1: LUT FOR COUNT[0]

Cell Properties

count[1]_i_1

I2	I1	I0	O=I0 & !I1 & !I2 + !I0 & I1 & !I2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 2: LUT FOR COUNT[1]