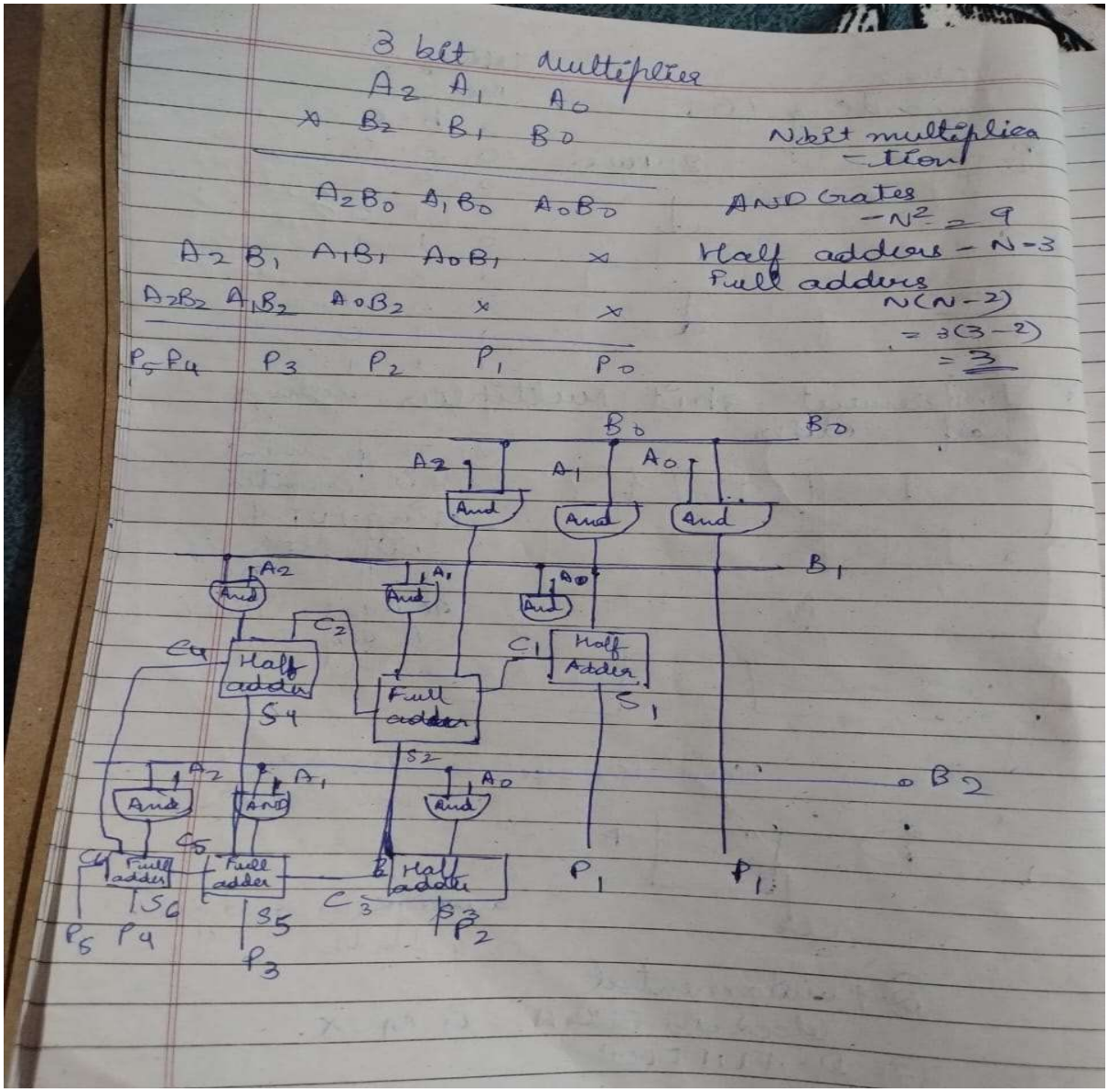
3 BIT MULTIPLIER



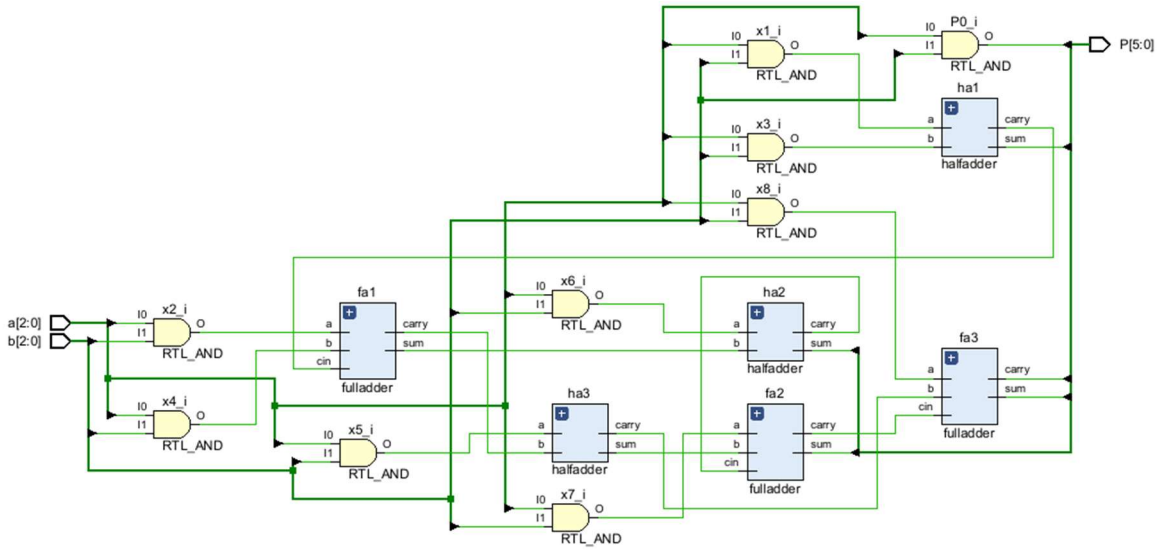
Verilog code:

```
module halfadder(input a, input b, output sum, output carry);
   assign sum = a ^ b;
   assign carry = a & b;
endmodule
```

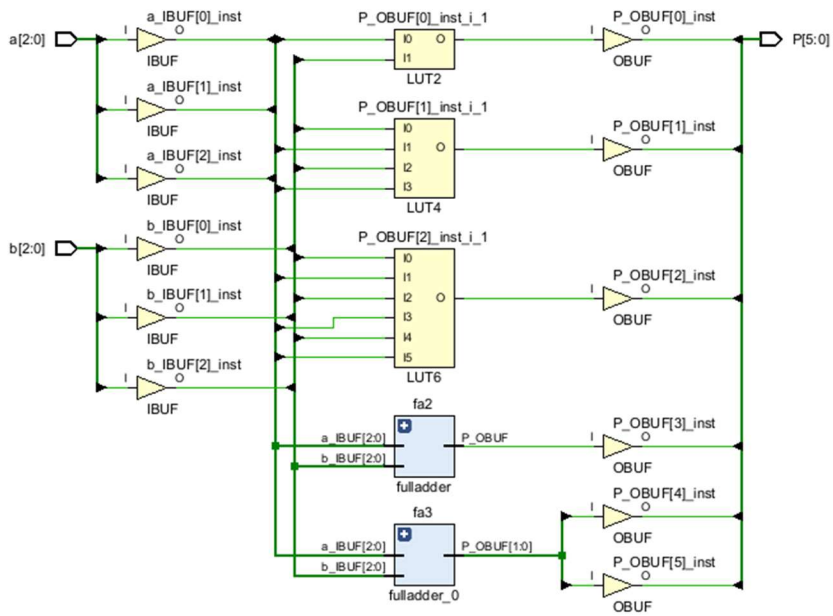
```
module fulladder(input a, input b, input cin, output sum, output carry);
   assign sum = a ^ b ^ cin;
   assign carry = (a & b) | (b & cin) | (a & cin);
endmodule

module multiplier_3bit (
   input [2:0] a,
   input [2:0] b,
   output [5:0] P
);
 wire x1, x2, x3, x4, x5, x6, x7, x8;
 wire c1, c2, c3, c4, c5, c6;
 wire s1, s2, s3, s4, s5, s6;
assign P[0]= a[0] & b[0];
   assign x1 = a[1] & b[0];
   assign x2 = a[2] & b[0];
   assign x3 = a[0] & b[1];
   assign x4 = a[1] & b[1];
   assign x5 = a[2] & b[1];
   assign x6 = a[0] & b[2];
   assign x7 = a[1] & b[2];
   assign x8 = a[2] & b[2];
  halfadder ha1(x1, x3, s1, c1);
   assign P[1] = s1;
   fulladder fa1(x2, x4, c1, s2, c2);
   halfadder ha2(x6, s2, s3, c3);
   assign P[2] = s3;
   halfadder ha3(x5, c2, s4, c4);
   fulladder fa2(x7, s4, c3, s5, c5);
```

```
    assign P[3] =s5;
    fulladder fa3(x8, c4, c5, s6, c6);
    assign P[4] = s6;
    assign P[5] = c6;
endmodule
```

RTL analysis schematic:



Synthesis analysis schematic:



Look Up Tables:

Cell Properties

P_OBUF[0]_inst_i_1

I1	I0	O=I0 & I1
0	0	0
0	1	0
1	0	0
1	1	1

Figure 1: LUT2

Cell Properties

P_OBUF[1]_inst_i_1

I3	I2	I1	I0	O=I0 & I1 & !I3 + I0 & I1 & !I2 + !I1 & I2 & I3 + !I0 & I2 & I3
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Figure 2: LUT4

Cell Properties

P_OBUF[2]_inst_i_1

I5	I4	I3	I2	I1	I0	O=I0 & I1 & I13 & I15 + I11 & I2 & I3 & I15 + I2 & I3 & I14 & I5 + I11 & I13 & I4 & I5 + I0 & I1 & I12 & I14 + I10 & I2 & I3 & I15 + I10 & I13 & I4 & I5 + I11 & I12 & I4 & I5 + I0 & I1 & I12 & I15 + I0 & I1 & I2 & I13 & I4 + I10 & I1 & I12
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	1
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	1
0	0	1	0	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	0	0
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0	1	0	0	0	1	0
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1	1	0	0	1	0	1

1	1	0	0	1	1	0
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1	1	0	1	1	1	1
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1	1	1	0	1	1	0
1	1	1	1	0	0	0
1	1	1	1	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	1	0

Figure 3: LUT6