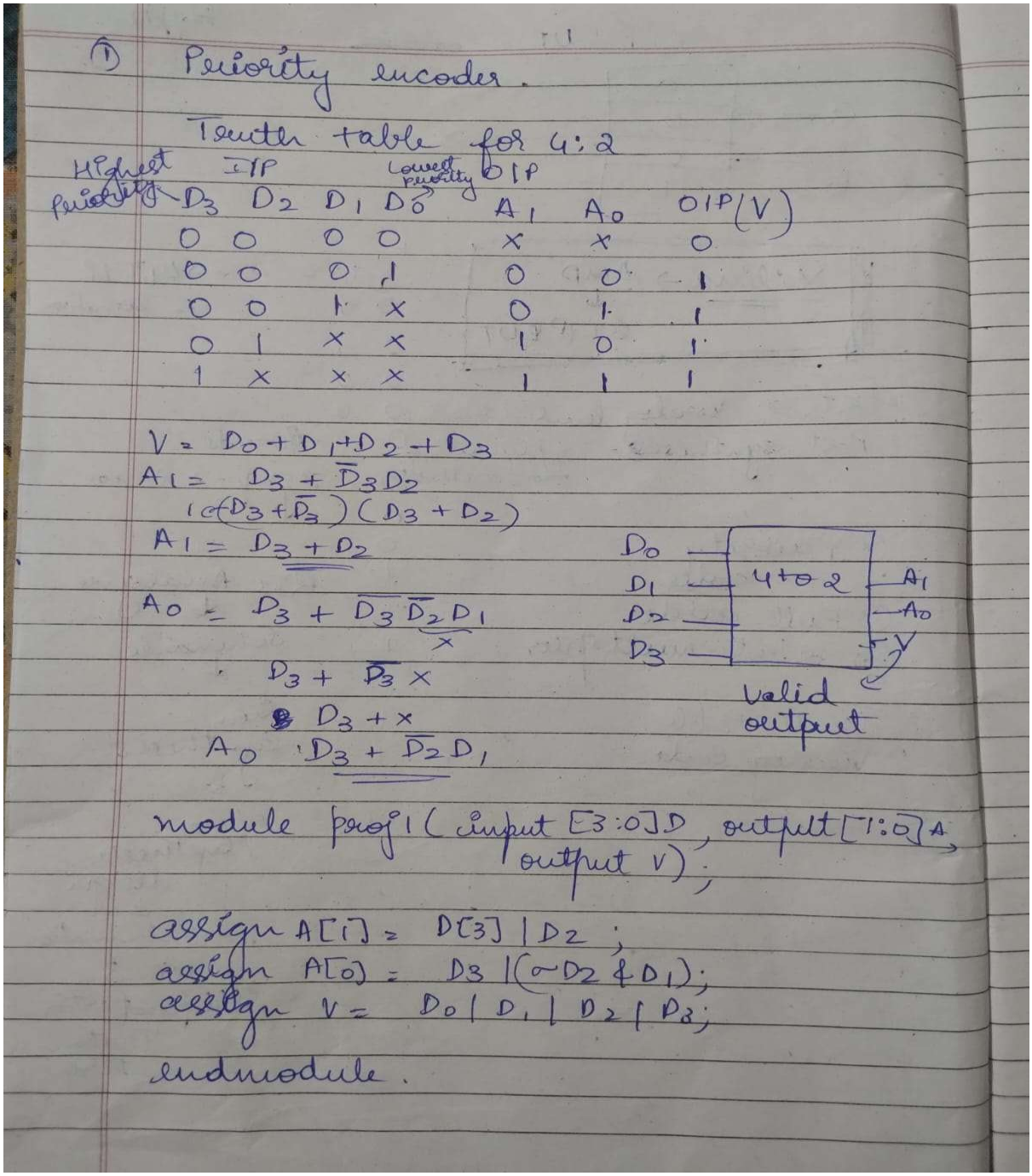
4: 2 Priority Encoder



① Priority encoder.

Truth table for 4:2

Highest priority I/P D_3	D_2	D_1	Lowest priority I/P D_0	O/P A_1	A_0	O/P (V)
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

$V = D_0 + D_1 + D_2 + D_3$

$A_1 = D_3 + \bar{D}_3 D_2$

$(D_3 + \bar{D}_3)(D_3 + D_2)$

$A_1 = D_3 + D_2$

$A_0 = D_3 + \bar{D}_3 \bar{D}_2 D_1$

$D_3 + \bar{D}_3 x$

$D_3 + x$

$A_0 = D_3 + \bar{D}_2 D_1$

module proj1 (input [3:0] D, output [1:0] A, output V);

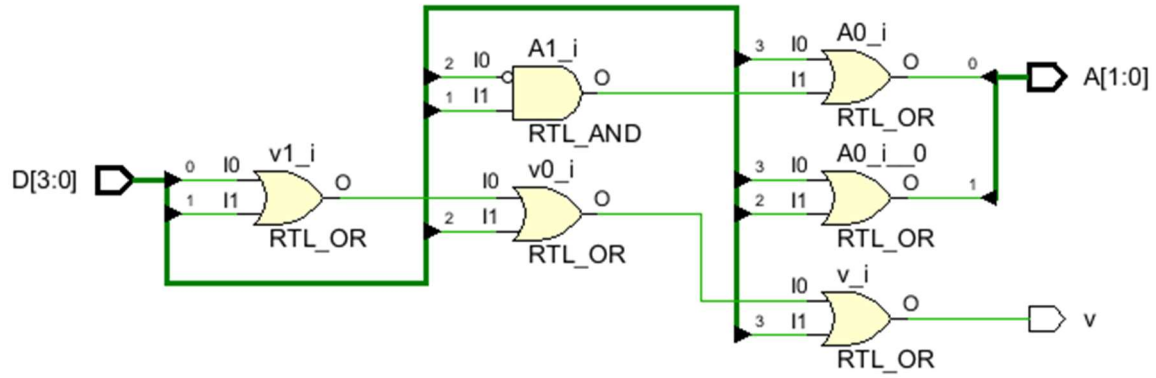
assign A[1] = D[3] | D2 ;
assign A[0] = D3 | (~D2 & D1);
assign V = D0 | D1 | D2 | D3;

endmodule.

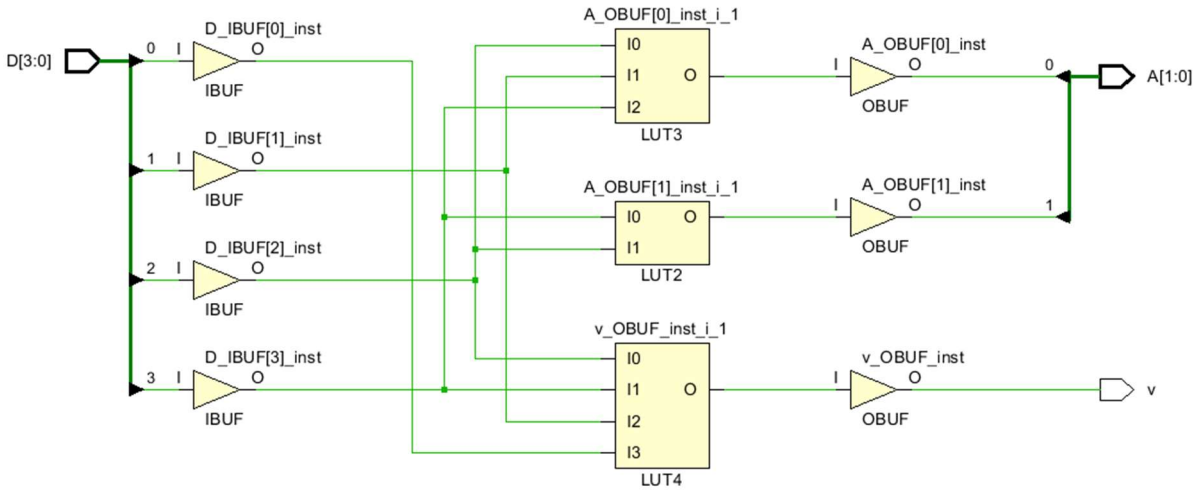
Verilog code:

```
module proj1(input[3:0]D, output[1:0]A, output v);
assign A[1] = D[3]|D[2];
assign A[0] = D[3]|(~D[2]&D[1]);
assign v = D[0]|D[1]|D[2]|D[3];
endmodule
```

RTL synthesis schematic:



Synthesis schematic:



Look Up Table:

Cell Properties

A_OBUF[1]_inst_i_1

I1	I0	O=I0 + I1
0	0	0
0	1	1
1	0	1
1	1	1

Figure 1: LUT 22

Cell Properties

A_OBUF[0]_inst_i_1

I2	I1	I0	O=!I0 & I1 + I2
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Figure 2: LUT 3

Cell Properties

v_OBUF_inst_i_1

I3	I2	I1	I0	O=I0 + I1 + I2 + I3
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Figure 3: LUT 4