Inferences from PERF analysis of Locks and Barriers:

Locks:

1. Latency/Time required for the same load:

In terms of latency, the TAS and TTAS locks show the lowest uncontended latency. This is because of it’s relatively simple design. The ticket and mcs lock show comparable times when the number of threads and iterations are low, at higher number of threads and iterations the time required for execution bumps up exponentially. However the pthread mutex lock shows a consistent timing in all aspects even if the number of threads or iterations are high.

1. Cache Misses:

In ideal scenario, Tas causes significant cache misses. The TTAS alleviates this issue. However since both TAS and TTAS are LIFO locks, they have more cache hits than FIFO locks like ticket lock and MCS lock.

1. L1 cache hit rate

The hit rate for LIFO locks like TAS and TTAS are significantly higher than FIFO locks like ticket and MCS. Out of which ticket has the lowest hit rate, lower than MCS. Mutex locks however show lower hit rate according to the analysis.

1. Branch prediction hit rate

Similar to L1 cache hit rate.

1. Starvation and wait traffic:

The TAS and TTAS have been known to create starvation of processes waiting to get into the critical section. The lock which released the critical section has more chances of re-acquiring the critical section again depriving other process. This may lead to good cache hit rate but poor fairness and more starving.

On the other hand, ticket and MCS have more overhead of processing and switching as well as take up more space but allow all processes to acquire the lock on the basis of their order of arrival.

1. Fairness

MCS and ticket lock show more fairness as compared to tas and ttas. This can be seen from the fact that they are lower cache hit rates and have higher page faults.

1. Page Faults

TAS and TTAS how lower page faults than MCS and Ticket.

Barriers:

The pthread barrier shows more latency than sense reversal barrier in my implementation. The hit rate of sense reveral barrier is significantly higher than pthread as can be seen from the analysis. The page faults should ideally be lower for sense reveral barrier.

Conclusion:

The best primitive for situation where fairness is more important than timing requirements and space requirements is MCS lock or ticket lock which MCS lock having lesser timing over head but more spatial overhead and vice versa for ticket lock.

The best primitive for lower timing requirement where fairness of the process is not required is TTAS over TAS as this reduces the cache invalidation and contention misses.

The pthread mutex lock can be chosen in ideal scenarios as it provides linear timings and cache and hit rate even as the number of threads and functionalities increase.