Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 7 = 14**

Q no.	Question	Marks	CO
a.	What is the difference between binary, decimal, and hexadecimal number systems?	2	1
b.	What is a don't-care condition in Karnaugh maps?	2	1
c.	Explain the function of a magnitude comparator.	2	2
d.	Differentiate between synchronous and asynchronous counters.	2	3
e.	Explain the concept of a ring counter.	2	3
f.	What are the advantages of synchronous counters over asynchronous counters?	2	4
g.	Differentiate between RAM and ROM.	2	5

SECTION B

2. Attempt any *three* of the following: **7 x 3 = 21**

a.	Explain the SOP and POS forms in Boolean algebra. How are they derived?	7	1
b.	Describe the operation of half and full adders. Provide truth tables and circuit diagrams.	7	2
c.	Define storage elements and discuss the characteristics of latches and flip-flops.	7	3
d.	Explain the concept of hazards in digital circuits and methods to eliminate them.	7	4
e.	Compare and contrast different digital logic families such as DTL, DCTL, TTL, ECL, and CMOS in terms of their characteristics.	7	5

SECTION C

3. Attempt any *one* part of the following: **7 x 1 = 7**

a.	Minimize the Boolean function F(A, B, C, D) = Σ(0, 1, 2, 4, 6, 7, 9, 12, 14) using the Karnaugh map method.	7	1
b.	Implement the Boolean function F = AB + AC + BC using only NAND gates.	7	1

4. Attempt any *one* part of the following: **7 x 1 = 7**

a.	Discuss the operation of BCD adders and their significance.	7	2
b.	Implement a 4-to-1 multiplexer using basic logic gates.	7	2

5. Attempt any *one* part of the following: **7 x 1 = 7**

a.	Explain the concept of ripple counters and synchronous counters.	7	3
b.	Convert a JK flip-flop to a T flip-flop and demonstrate its operation with characteristic equations.	7	3

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BTECH
(SEM III) THEORY EXAMINATION 2023-24
DIGITAL ELECTRONICS

TIME: 3HRS **M.MARKS: 70**

6.	**Attempt any *one* part of the following:**	**7 x 1 = 7**	
a.	Describe the process of state reduction and assignments in sequential circuit design.	7	4
b.	Discuss the concept of race-free state assignment and how it is achieved.	7	4

7.	**Attempt any *one* part of the following:**	**7 x 1 = 7**	
a.	Describe the working principles of PLA and PAL and their applications.	7	5
b.	Explain the concepts of fan-out, fan-in, and noise margin in digital circuits.	7	5

ROLL NO.

G.L. BAJAJ INSTITUTE OF TECHNOLOGY & MANAGEMENT
GREATER NOIDA
B. TECH (III[rd]) - (CSE-AIML, CSE-DS, AI-DS & AIML)
SESSIONAL TEST (ODD SEM 2023-24)
Digital Electronics (BOE 310)

Faculty Name: Dr. Vinay Kumar, Dr. Krishanu Kundu & Ms. Deeksha Sankrit

Time: 2:00 Hrs Max. Marks: 50

Note:
(i) No student will be allowed to leave the examination Room before end of exam.
(ii) Diagram should be neat and clean.
(iii) Mention Question number/section correctly.
(iv) Be precise in your answer.
(v) Do not write anything on question paper except Roll number.

Course Outcomes:

Following are the course outcomes of the subject

CO Code	Course Outcome (CO)	Bloom's Level
BOE-310.1	Apply concepts of Digital Binary System and implementation of Gates.	K3
BOE-310.2	Analyze and design of Combinational logic circuits.	K4
BOE-310.3	Analyze and design of Sequential logic circuits with their applications.	K4
BOE-310.4	Implement the Design procedure of Synchronous & Asynchronous Sequential Circuits.	K3
BOE-310.5	Apply the concept of Digital Logic Families with circuit implementation.	K3

Section: A

1. Attempt all questions. (2*5= 10)

Q.No.	Questions	Marks	CO	BL
a)	Show the how do you convert a decimal number into other number with base 'b' ?	2	BOE310.1	K3
b)	Illustrate the meaning of 'sign-magnitude' form of representation?	2	BOE310.1	K3
c)	The value of base 'b' if $(121)_b = (144)_8$ is ---------	2	BOE310.1	K3
d)	Convert the following numbers into Gray & BCD Code Numbers (i) $(110110010)_2$ (ii) $(ECE)_{16}$	2	BOE310.1	K3
e)	Demonstrate the Implicant, Prime Implicant and Essential Prime Implicant ?	2	BOE310.1	K3

Section: B

2. Attempt any four of the following: (5*4 = 20)

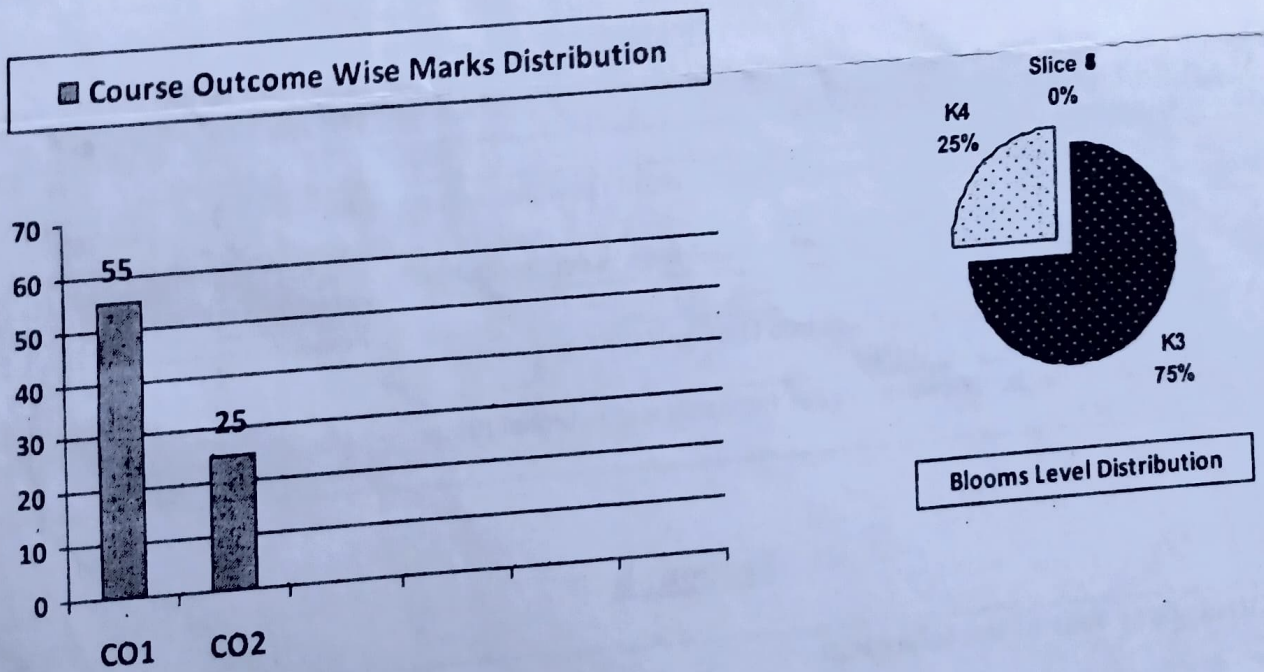
Q. No.	Questions	Marks	CO	BL
a)	Convert the following (i) $(5162)_{10} = (\ldots)_2$, (ii) $(11011001)_2 = (\ldots)_{10}$ (iii) $(6273)_{10} = (\ldots)_8$, (iv) $(7860)_{10} = (\ldots)_{16}$, (v) $(A23B8)_{16} = (\ldots)_{10}$	5	BOE310.1	K3
b)	Implement the function by using K-Map (i) $F(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 10, 11, 12)$ (ii) $F(W, X, Y, Z) = \sum m(0, 2, 6, 10, 11, 12, 13) + \sum d(3, 4, 5, 14, 15)$	5	BOE310.1	K3
c)	Explain the difference between SOP and POS form.	5	BOE310.1	K3
d)	Convert the following into SOP form (i) $F(A, B, C, D) = ABC+AB+DC+D'$	5	BOE310.1	K3

	(ii) F (A, B, C, D, E) = ABCDE+ABE'+ACD			
e)	Iplement of Full Adder by using universal logic.	5	BOE310.2	K3
f)	Simplify the Boolean Function using K map and implement it in NOR logic F(A, B,C,D) = ΠM(1,4,5,9,13,14)	5	BOE310.1	K3

Section: C

3. Attempt any one question		(10 *1 = 10)		
Q. No.	Questions	Marks	CO	BL
a)	Simplify the Boolean function using K-map and implement it in NAND logic F = ∑m(0, 1, 2, 4, 7, 8, 12, 14, 15, 16, 17, 18, 20, 24, 28, 30, 31)	10	BOE310.1	K3
b)	Using the Tabular method, obtain the minimal expression for F=∑m(2, 3, 8, 12, 13)+ ∑d(10,14) and implement it in universal logic.	10	BOE310.1	K3

4. Attempt any one question		(10 *1 = 10)		
Q. No.	Questions	Marks	CO	BL
a)	Design 4-bit BCD adder.	10	BOE310.2	K4
b)	Realize the logic expression given below using a (i) 8:1 MUX &(ii) 16:1 MUX F =∑m(0, 1, 3, 5, 8, 11, 12, 14, 15)	10	BOE310.2	K4



Checked By
(Head of Department)