BIRLA VISHVAKARMA MAHAVIDYALAY

(AN AUTONOMOUS INSTITUTION)

ELECTRONICS ENGINNERING DEPARTMENT

A.Y. 2023-2024

DIGITAL SYSTEM DESIGN: -50 VERILOG CODES

NAME: **SHREYA VERMA**

ID NO.: **21EL001**

SEMESTER: **5TH**

BATCH: **A – BATCH**

BRANCH: **ELECTRONICS ENGINEERING**

SR. NO.	LIST
1.	CLOCK DIVIDER
2.	JOHNSON COUNTER
3.	RING COUNTER
4.	5 INPUT MAJORITY CIRCUIT
5.	PARITY GENERATOR
6.	BINARY TO ONE HOT ENCODER
7.	4-BIT BCD SYNCHRONOUS COUNTER
8.	4-BIT CARRY LOOKAHEAD ADDER
9.	N-BIT COMPARATOR
10.	SERIAL IN SERIAL OUT SHIFT REGISTER
11.	SERIAL IN PARALLEL OUT SHIFT REGISTER
12.	PARALLEL IN PARALLEL OUT REGISTER
13.	PARALLEL IN SERIAL OUT REGISTER
14.	BIDIRECTION SHIFT REGISTER
15.	PRBS SEQUENCE GENERATOR
16.	8-BIT SUBTRACTOR
17.	8-BIT ADDER/SUBTRACTOR
18.	4-BIT MULTIPLIER
19.	FIXED POINT DIVISION
20.	MASTER SLAVE JK FLIP FLOP
21.	POSITIVE EDGE DETECTOR

22.	BCD ADDER
23.	4-BIT CARRY SELECT ADDER
24.	MOORE FSM 1010 SEQUENCE DETECTOR
25.	N:1 MUX
26.	BCD TIMECOUNT
27.	3-1 MUX
28.	BCD TO SEVEN SEGMENT DISPLAY
29.	D LATCH USING 2:1 MUX
30.	8-BIT BARREL SHIFTER
31.	1-BIT COMPARATOR USING 4X1 MUX
32.	LOGICAL, ALGEBRAIC, AND ROTATE SHIFT OPERATIONS
33.	ALU
34.	4-BIT ASYNCHRONOUS DOWN COUNTER
35.	MOD-N UPDOWN COUNTER
36.	UNIVERSAL BINARY COUNTER
37.	UNIVERSAL SHIFT REGISTER
38.	CN(CHANGE-NO CHANGE FLIPFLOP) USING 2:1 MUX
39.	FREQUENCY DIVIDER BY ODD NUMBERS
40.	GREATEST COMMON DIVISOR USING BEHAVIOURAL MODELLING
41.	GREATEST COMMON DIVISOR VIA FSM

42.	SINGLE PORT RAM
43.	DUAL PORT RAM
44.	CLOCK BUFFER
45.	SYNCHRONOUS FIFO
46.	PRIORITY ENCODER
47.	SEVEN SEGMENT DISPLAY USING ROM
48.	SERIAL ADDER
49.	FIXED PRIORITY ARBITER
50.	ROUND ROBIN ARBITER

CODE-1: CLOCK DIVIDER

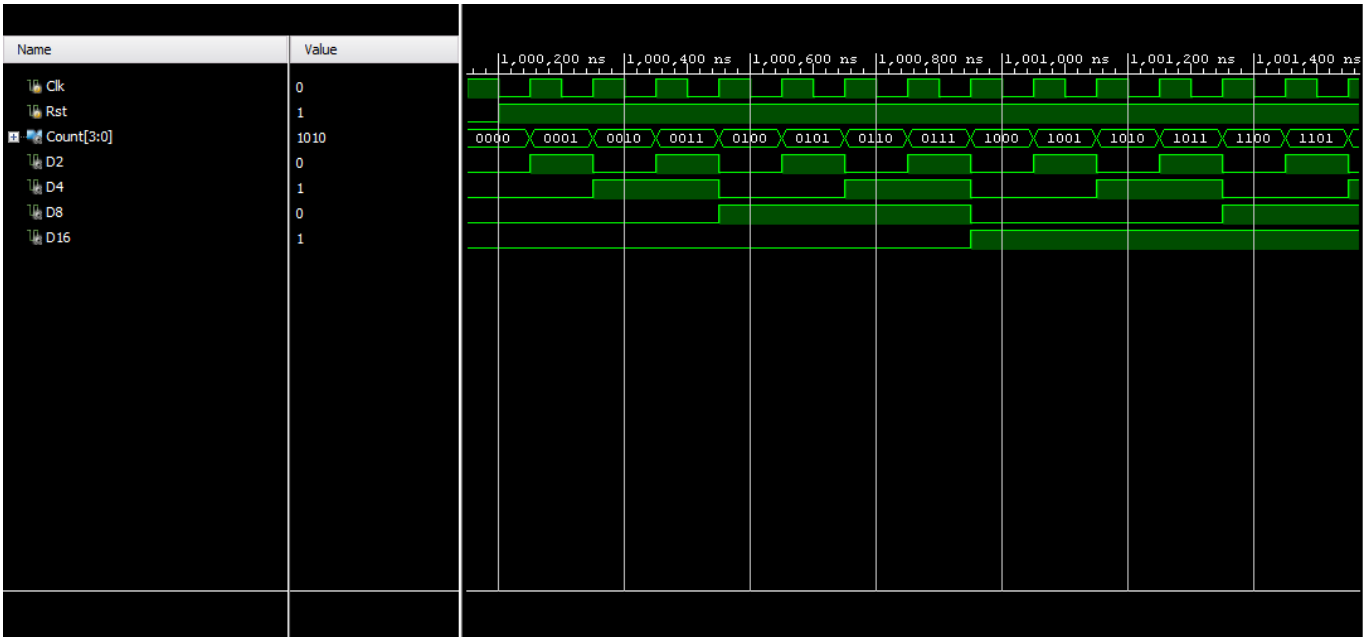
CODE FOR TESTBENCH:

```
module testbench;
reg Clk,Rst;
wire [3:0] Count;
wire D2,D4,D8,D16;

Clock_Divider dut(Clk,Rst,Count,D2,D4,D8,D16);
initial
begin
$monitor("Clk=%b Rst=%b Count=%b D2=%b D4=%b D8=%b D16=%b",Clk,Rst,Count,D2,D4,D8,D16);
end
 always
  begin
  #50   Clk = ~Clk;
  end
initial
begin
      #100 Rst = 1;
      #100 Rst = 0;


      $finish;
    end
endmodule
```

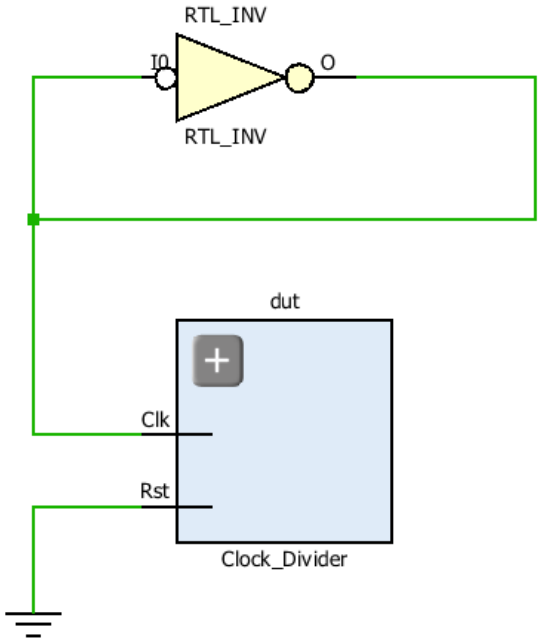
VERILOG CODE:

```
module Clock_Divider(
    input Clk,
    input Rst,
    output reg [3:0] Count,
    output reg D2,D4,D8,D16
    );
    always@(posedge Clk)
    begin
    if (Rst==0)
    Count=4'b0000;
    else
    Count=Count+1;
    D2=Count[0];
    D4=Count[1];
    D8=Count[2];
    D16=Count[3];
    end

endmodule
```

SIMULATION:



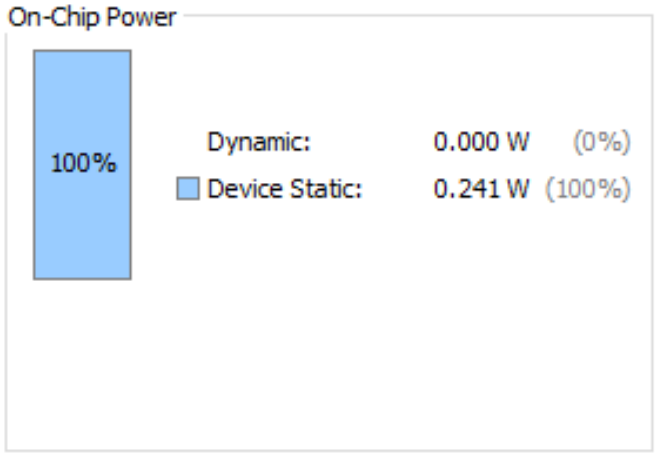
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-2: JOHNSON COUNTER

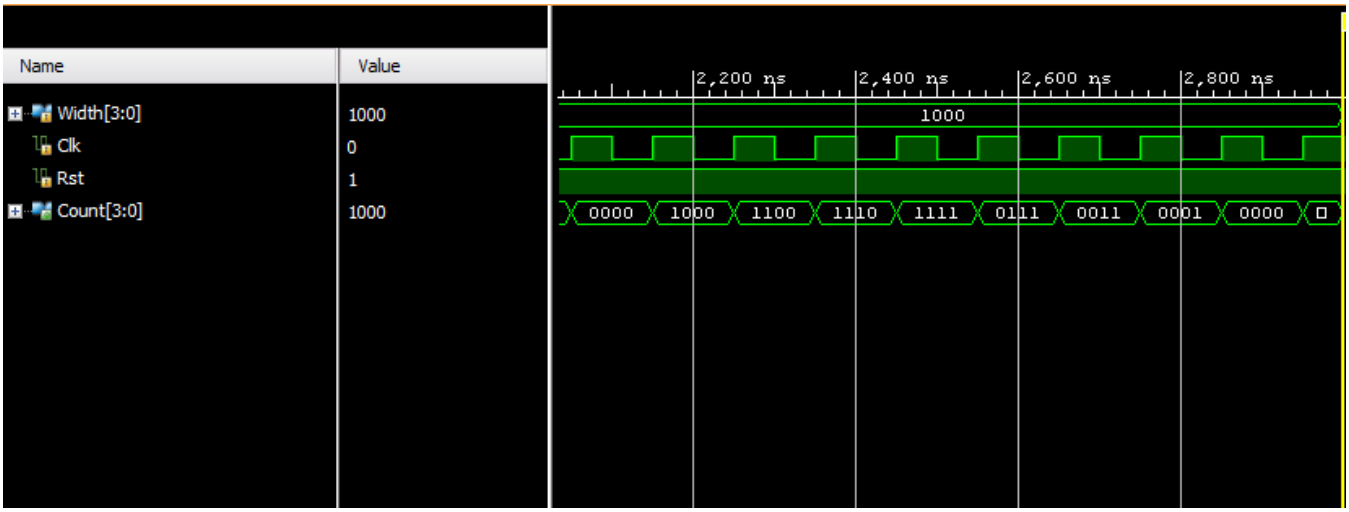
CODE FOR TESTBENCH:

```
module testbench;
reg Clk,Rst;
reg [3:0] Width;
wire [3:0] Count;


JOHNSON_COUNTER dut(Clk,Rst,Width,Count);
initial
begin
$monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
end
 always
  begin
  #50   Clk = ~Clk;
  end
initial
begin
      #100 Rst = 1;
      #100 Rst = 0;


      $finish;
    end
endmodule
```

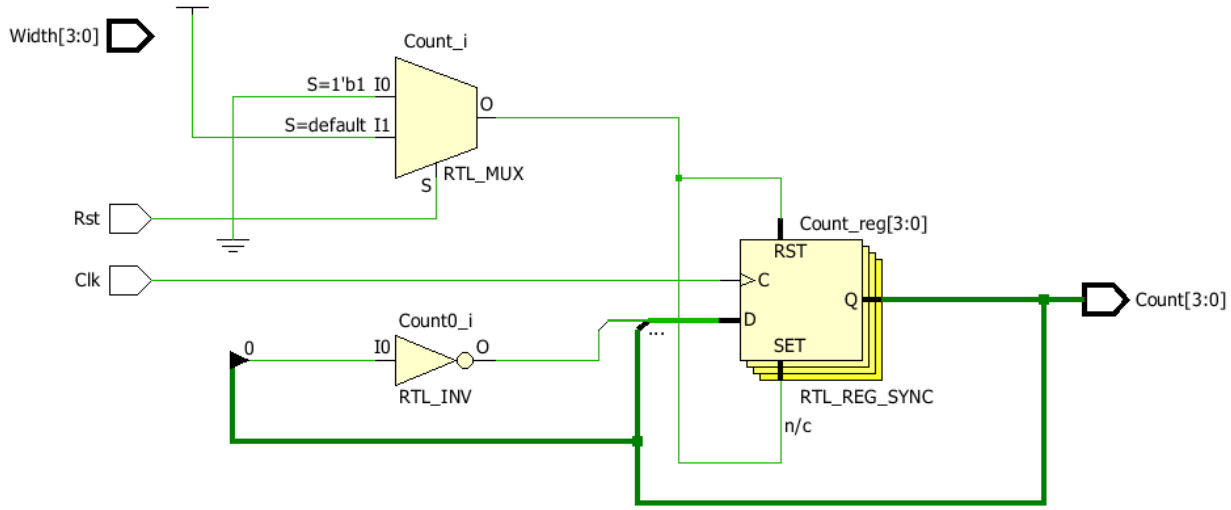
VERILOG CODE:

```
module JOHNSON_COUNTER(
    input [3:0] Width,
    input Clk,
    input Rst,
    output reg [3:0] Count
    );

    always@(posedge Clk)
    begin
    if(Rst)
    Count={~Count[0],Count[3:1]};
    else
    Count=4'b0001;
    end
endmodule
```

SIMULATION:



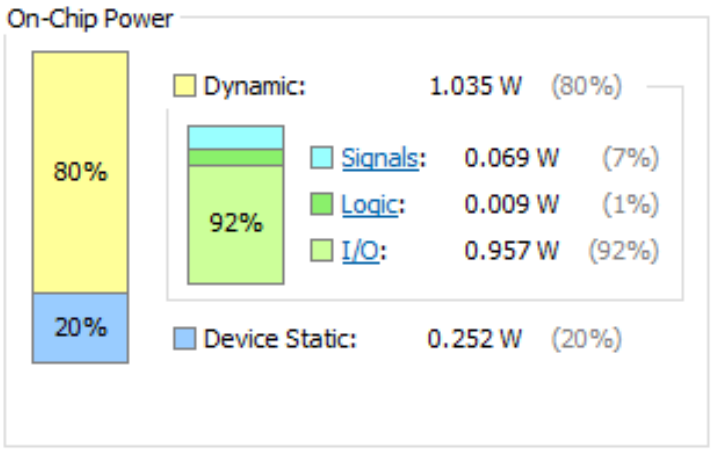
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.287 W**
Junction Temperature:	**26.8 °C**
Thermal Margin:	58.2 °C (40.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-3: RING COUNTER

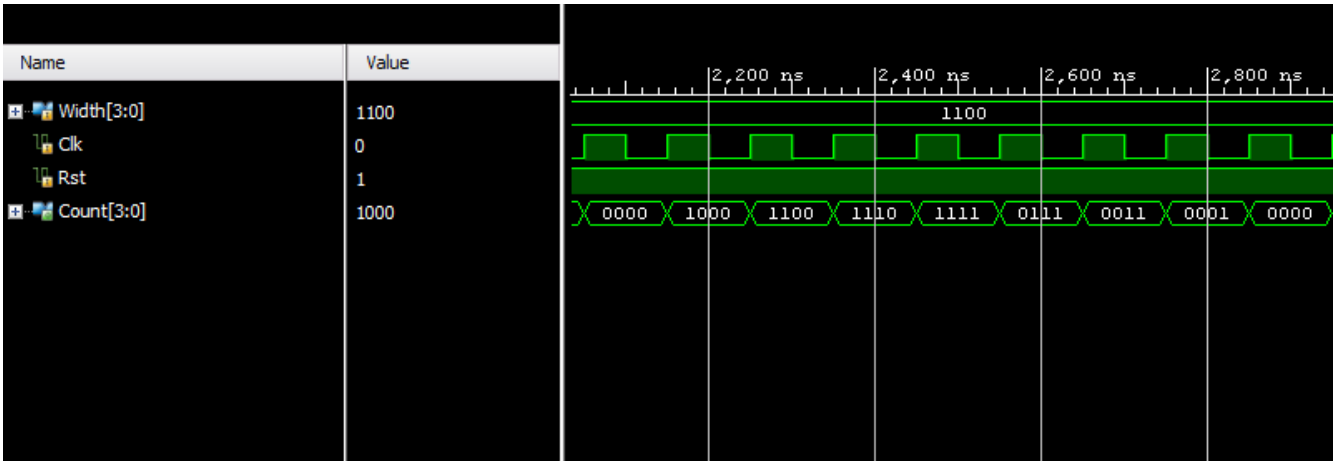
CODE FOR TESTBENCH:

```
module testbench;
reg [3:0] Width;
reg Clk,Rst;
wire [3:0] Count;

RING_COUNTER dut(Clk,Rst,Width,Count);

initial
begin
$monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
end
  always
  begin
   #50 Clk=~Clk;
   end
   initial
   begin
   #100 Rst=1;
   #100 Rst=0;
   $finish;
   end
   endmodule
```

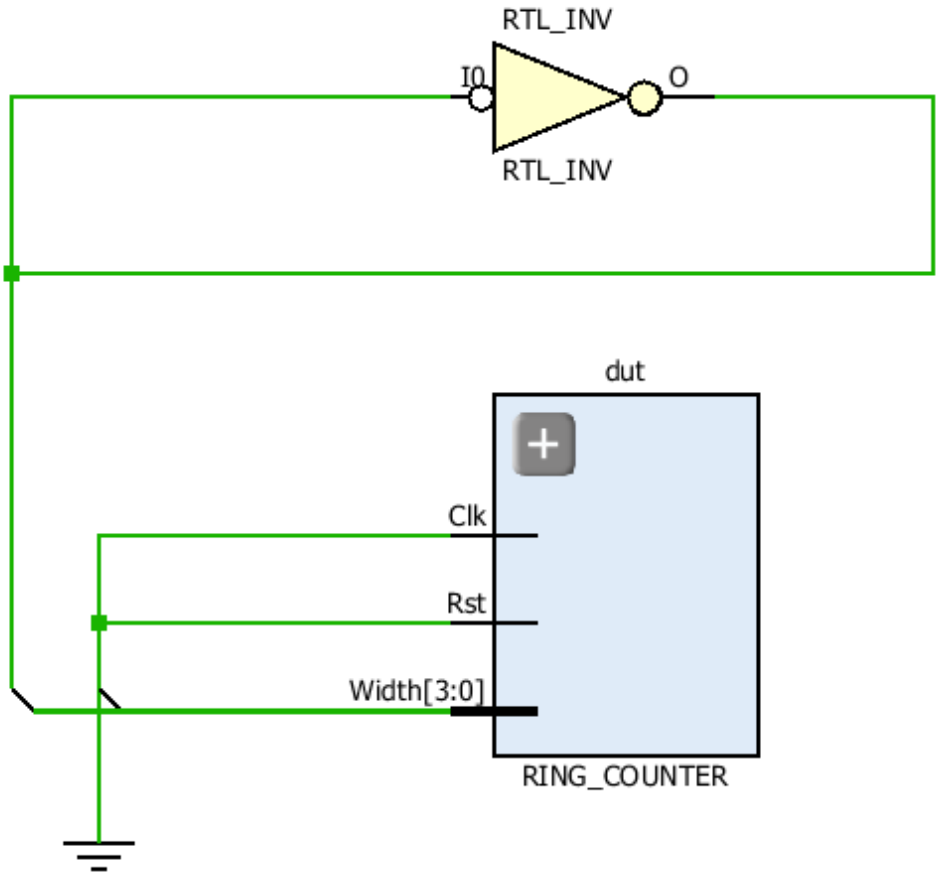
VERILOG CODE:

```
module RING_COUNTER(
    input [3:0] Width,
    input Clk,
    input Rst,
    output reg [3:0] Count
    );

    always@(posedge Clk)
    begin
    if(Rst)
    Count={~Count[0],Count[3:1]};
    else
    Count=4'b0001;
    end
endmodule
```

SIMULATION:



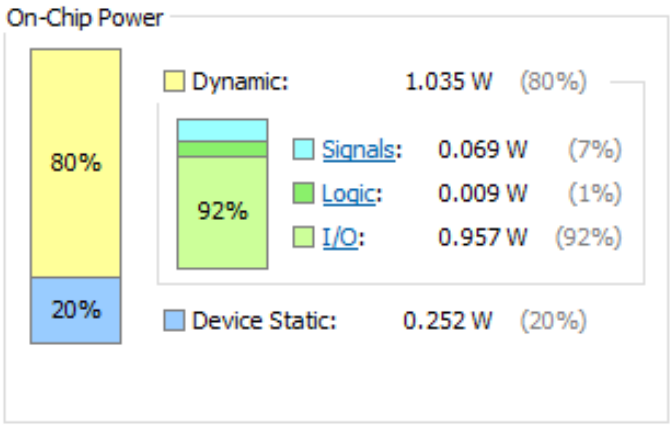
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.287 W**
Junction Temperature:	**26.8 ℃**
Thermal Margin:	58.2 ℃ (40.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-4: 5 INPUT MAJORITY CIRCUIT

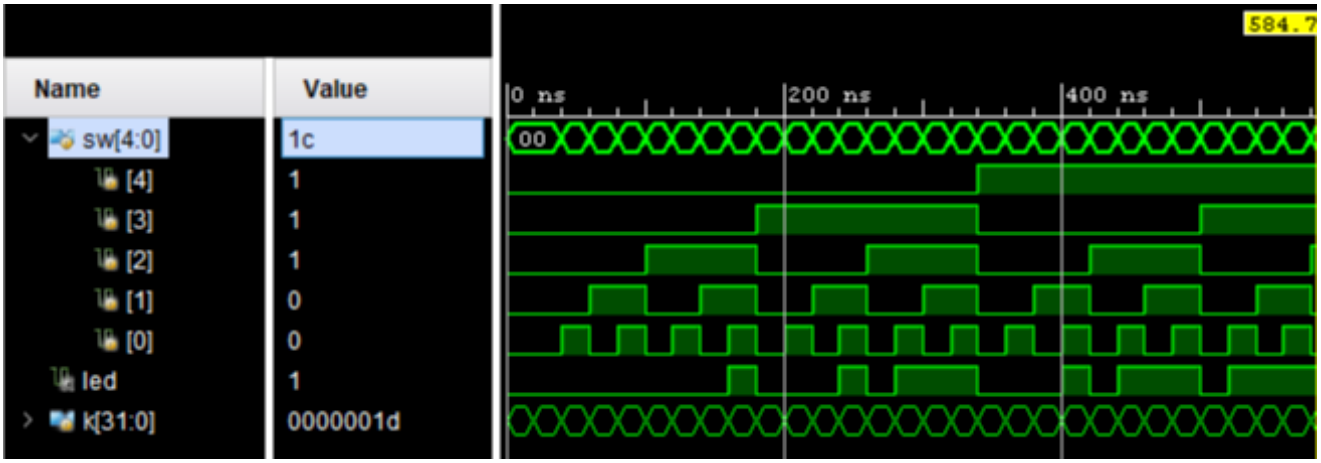
CODE FOR TESTBENCH:

```
module testbench;
reg [4:0] x;
wire z;
INPUT_MAJORITY_CIRCUIT dut(x[0],x[1],x[2],x[3],x[4],z);
initial
begin
$monitor("x[0]=%b x[1]=%b x[2]=%b x[3]=%b x[4]=%b z=%b",x[0],x[1],x[2],x[3],x[4],z);
  #2 x[0]=0; x[1]=0; x[2]=0; x[3]=0; x[4]=0;
  #3 x[0]=0; x[1]=0; x[2]=0; x[3]=0; x[4]=1;
  #4 x[0]=0; x[1]=0; x[2]=0; x[3]=1; x[4]=0;
  #5 x[0]=0; x[1]=0; x[2]=0; x[3]=1; x[4]=1;
  #6 x[0]=0; x[1]=0; x[2]=1; x[3]=0; x[4]=0;
  #7 x[0]=0; x[1]=0; x[2]=1; x[3]=0; x[4]=1;
  #8 x[0]=0; x[1]=0; x[2]=1; x[3]=1; x[4]=0;
  #9 x[0]=0; x[1]=1; x[2]=1; x[3]=1; x[4]=1;
  #10 x[0]=0; x[1]=1; x[2]=0; x[3]=0; x[4]=0;
  #11 x[0]=0; x[1]=1; x[2]=0; x[3]=0; x[4]=1;
  #12 x[0]=0; x[1]=1; x[2]=0; x[3]=1; x[4]=0;
  #13 x[0]=0; x[1]=1; x[2]=0; x[3]=1; x[4]=1;
  #14 x[0]=0; x[1]=1; x[2]=1; x[3]=0; x[4]=0;
  #15 x[0]=0; x[1]=1; x[2]=1; x[3]=0; x[4]=1;
  #16 x[0]=0; x[1]=1; x[2]=1; x[3]=1; x[4]=0;
  #17 x[0]=0; x[1]=1; x[2]=1; x[3]=1; x[4]=1;
  #18 x[0]=1; x[1]=0; x[2]=0; x[3]=0; x[4]=0;
  #19 x[0]=1; x[1]=0; x[2]=0; x[3]=0; x[4]=1;
  end
endmodule
```

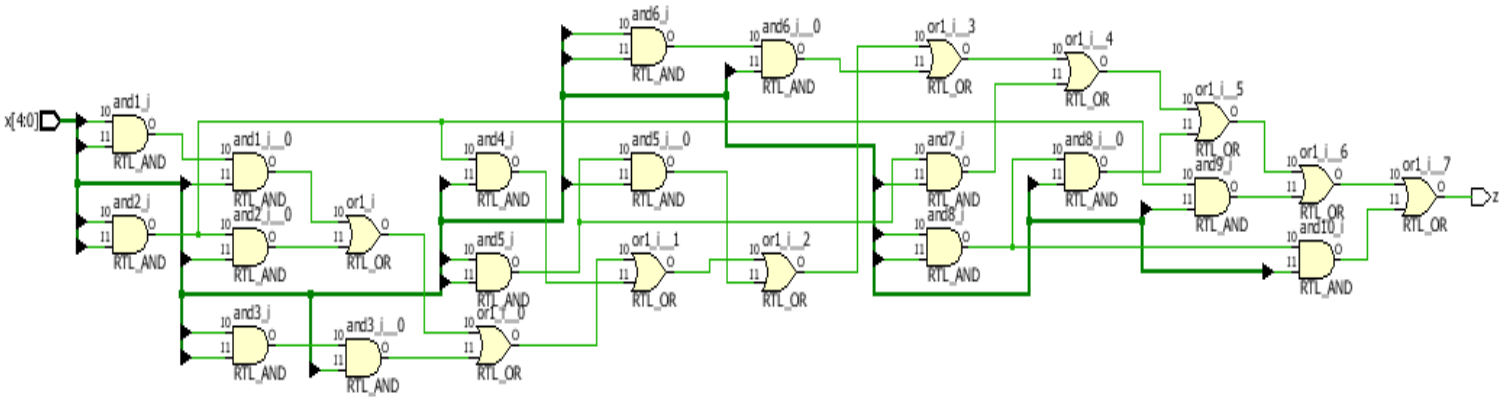
VERILOG CODE:

```
module INPUT_MAJORITY_CIRCUIT(
    input [4:0] x,
    output z
    );
    wire [9:0] w;
    and and1(w[0],x[2],x[3],x[4]);
    and and2(w[1],x[1],x[3],x[4]);
    and and3(w[2],x[1],x[2],x[4]);
    and and4(w[3],x[1],x[3],x[2]);
    and and5(w[4],x[0],x[3],x[4]);
    and and6(w[5],x[0],x[2],x[4]);
    and and7(w[6],x[0],x[3],x[2]);
    and and8(w[7],x[1],x[0],x[4]);
    and and9(w[8],x[1],x[3],x[0]);
    and and10(w[9],x[1],x[0],x[2]);
    or or1(z,w[0],w[1],w[2],w[3],w[4],w[5],w[6],w[7],w[8],w[9]);
endmodule
```

SIMULATION:



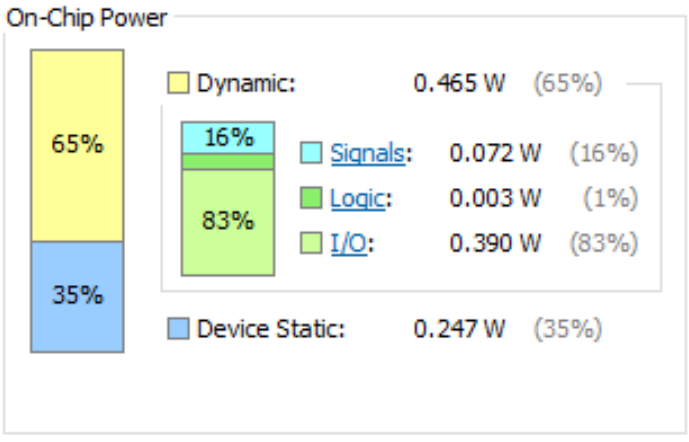
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.712 W**
Junction Temperature:	**26.0 ℃**
Thermal Margin:	59.0 ℃ (40.6 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-5: PARITY GENERATOR

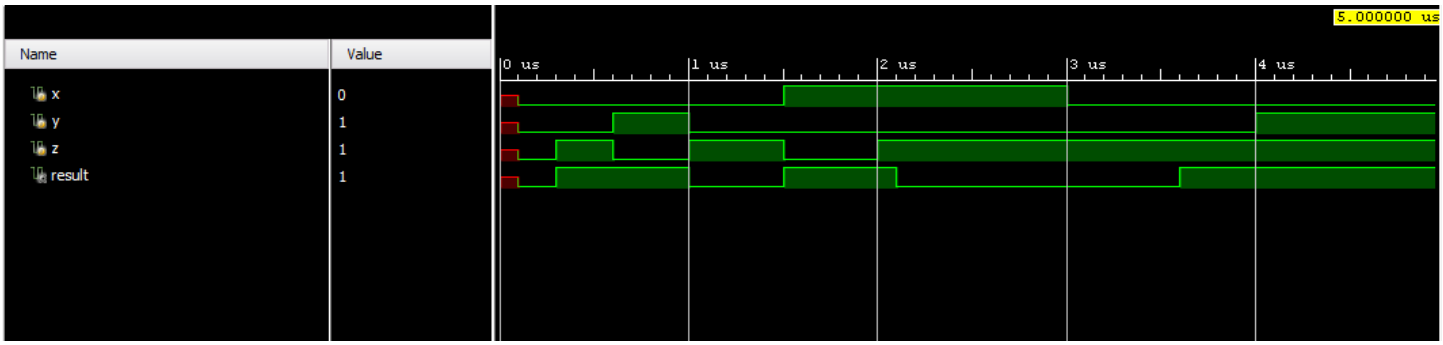
CODE FOR TESTBENCH:

```
module testbench;
reg x,y,z;
wire result;

 PARITY_GENERATOR dut(x,y,z,result);

 initial
 begin
 $monitor("x=%b y=%b z=%b result=%b",x,y,z,result);

  #100 x=0; y=0; z=0;
  #200 x=0; y=0; z=1;
  #300 x=0; y=1; z=0;
  #400 x=0; y=1; z=1;
  #500 x=1; y=0; z=0;
  #600 x=1; y=0; z=1;
  #700 x=1; y=1; z=0;
  #800 x=1; y=1; z=1;

 end
 endmodule
```

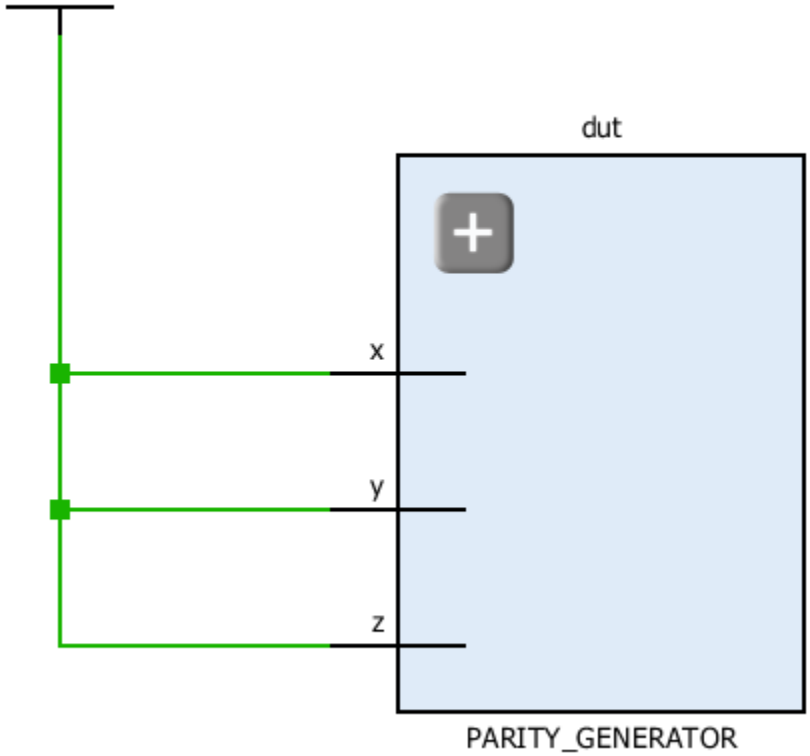
VERILOG CODE:

```
module PARITY_GENERATOR(
    input x,
    input y,
    input z,
    output result
    );
    assign result= x^y^z;
endmodule
```

SIMULATION:



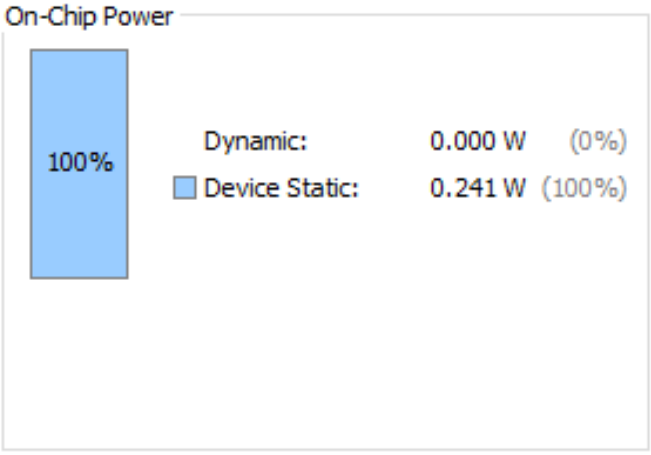
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-6: BINARY TO ONE HOT ENCODER

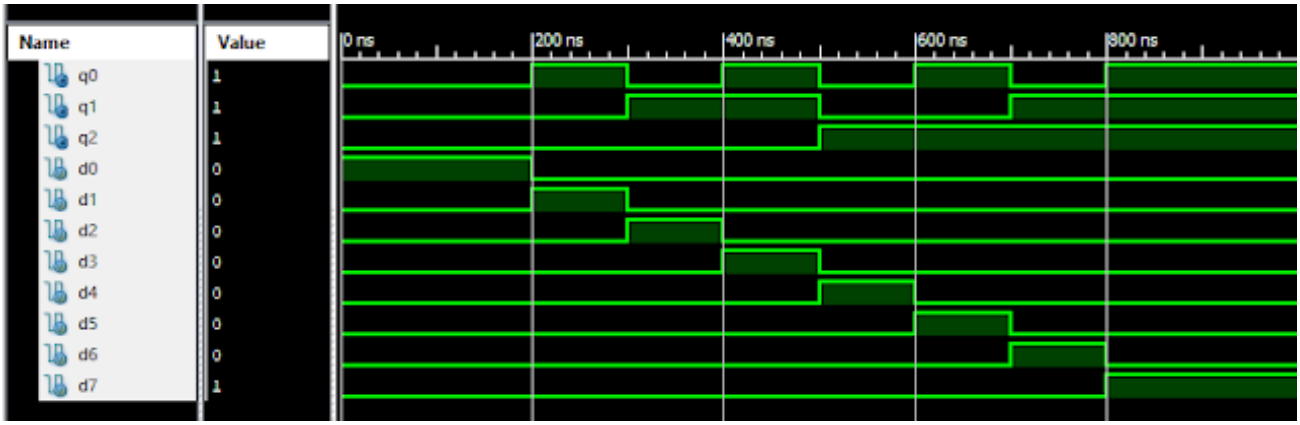
CODE FOR TESTBENCH:

```
module testbench;
reg [1:0] bin_i;
wire [1:0] one_hot_o;

BINARY_TO_ONE_HOT_ENCODER dut(bin_i,one_hot_o);

initial
begin
$monitor("bin_i=%b one_hot_o=%b",bin_i,one_hot_o);

#100 bin_i[0]=0; bin_i[1]=0;
#200 bin_i[0]=0; bin_i[1]=1;
#300 bin_i[0]=1; bin_i[1]=0;
#400 bin_i[0]=1; bin_i[1]=1;

end
endmodule
```

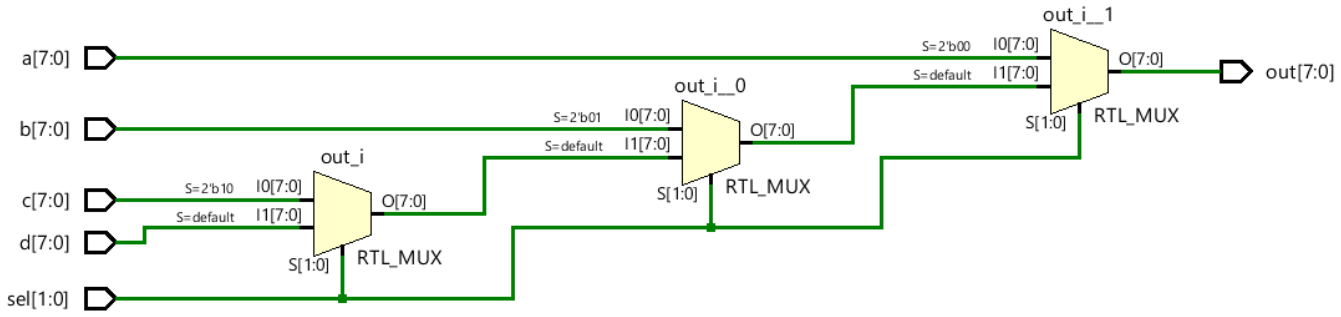
VERILOG CODE:

```
module BINARY_TO_ONE_HOT_ENCODER(
    input [2:0] bin_i,
    output [7:0] one_hot_o
    );
    parameter bin_w=4;
    parameter one_hot_w=16;
    input [1:0] bin_i;
    output reg [1:0] one_hot_o;

    assign one_hot_o = (1<<bin_i);
endmodule
```

SIMULATION:



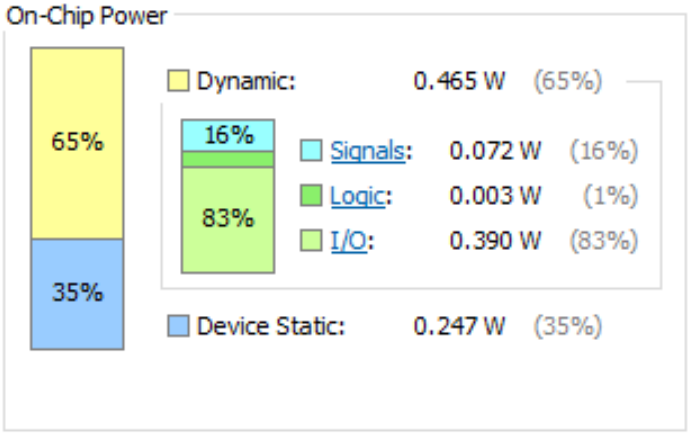
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.712 W**
Junction Temperature:	**26.0 ℃**
Thermal Margin:	59.0 ℃ (40.6 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-7: 4 BIT BCD SYNCHRONOUS COUNTER

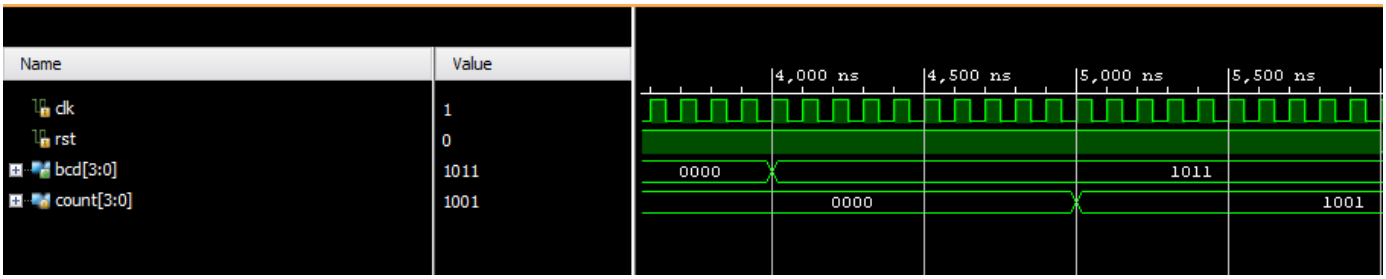
CODE FOR TESTBENCH:

```
module bcd_counter(
  input wire clk,         // Clock input
  input wire rst,         // Reset input
  output wire [3:0] bcd // 4-bit BCD output
);

reg [3:0] count;          // 4-bit counter

always @(posedge clk or posedge rst) begin
  if (rst) begin
    count <= 4'b0000;   // Reset the counter to 0
  end else begin
    // Increment the counter
    if (count == 4'b1001) begin
      count <= 4'b0000; // Reset to 0 when it reaches 9 (BCD)
    end else begin
      count <= count + 1;
    end
  end
end

assign bcd = count;     // Output BCD

endmodule
```

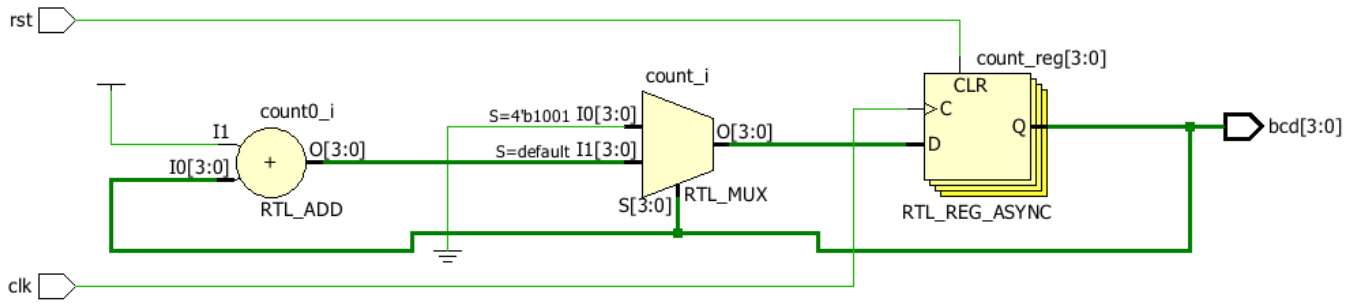
VERILOG CODE:

```
module BCD_COUNTER(
    input Clk,
    input Clear,
    output [3:0] Count
    );
      reg [3:0] t;
      always@(posedge Clk)
      begin
      if(Clear)
      t <= 4'b0000;
      Count <= 4'b0000;
      end
      else
      begin
      t <= t+1;
      if(t==4'b1001)
      begin
      t <= 4'b0000;
      end
      Count <=t;
      end
      end
endmodule
```

SIMULATION:



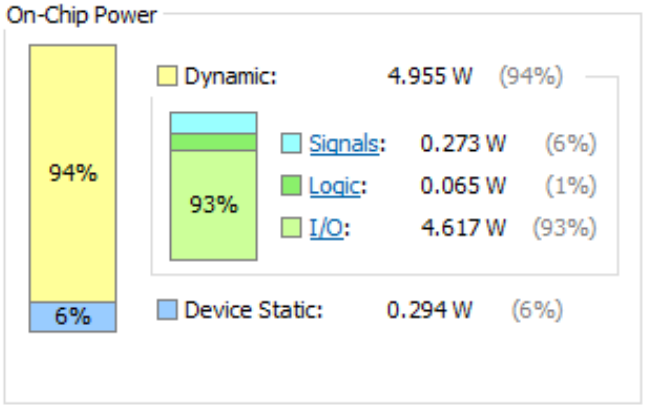
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**5.248 W**
Junction Temperature:	**32.3 °C**
Thermal Margin:	52.7 °C (36.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-8: 4 - BIT CARRY LOOK AHEAD ADDER

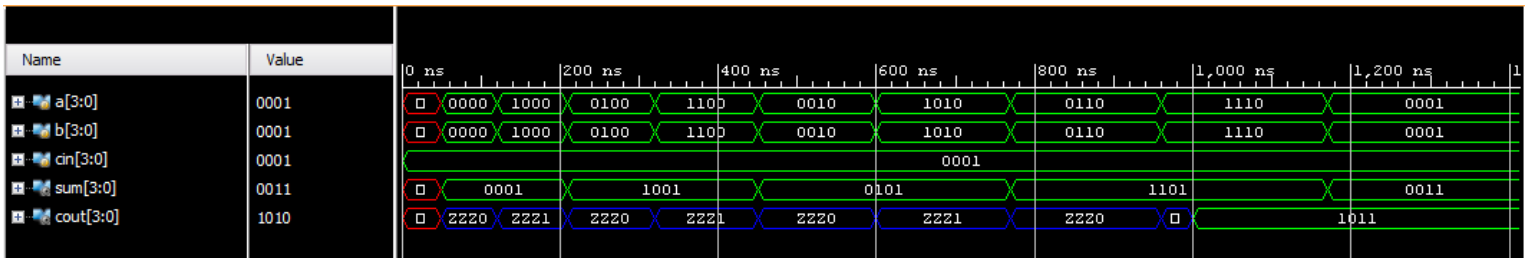
CODE FOR TESTBENCH:

```
module testbench;
reg [3:0] a, b,cin;
wire [3:0] sum,cout;
CARRY_LOOK_AHEAD_ADDER dut(a,b,cin,sum,cout);
initial
begin
$monitor("a=%b b=%b cin=%b sum=%b cout=%b",a,b,cin,sum,cout);
     cin=1;
#50 a[0]=0; a[1]=0; a[2]=0; a[3]=0;
     b[0]=0; b[1]=0; b[2]=0; b[3]=0;
#70 a[0]=0; a[1]=0; a[2]=0; a[3]=1;
     b[0]=0; b[1]=0; b[2]=0; b[3]=1;
#90 a[0]=0; a[1]=0; a[2]=1; a[3]=0;
     b[0]=0; b[1]=0; b[2]=1; b[3]=0;
#110 a[0]=0; a[1]=0; a[2]=1; a[3]=1;
     b[0]=0; b[1]=0; b[2]=1; b[3]=1;
#130 a[0]=0; a[1]=1; a[2]=0; a[3]=0;
     b[0]=0; b[1]=1; b[2]=0; b[3]=0;
#150 a[0]=0; a[1]=1; a[2]=0; a[3]=1;
     b[0]=0; b[1]=1; b[2]=0; b[3]=1;
#170 a[0]=0; a[1]=1; a[2]=1; a[3]=0;
     b[0]=0; b[1]=1; b[2]=1; b[3]=0;
#190 a[0]=0; a[1]=1; a[2]=1; a[3]=1;
     b[0]=0; b[1]=1; b[2]=1; b[3]=1;
#210 a[0]=1; a[1]=0; a[2]=0; a[3]=0;
     b[0]=1; b[1]=0; b[2]=0; b[3]=0;
     end
     endmodule
```

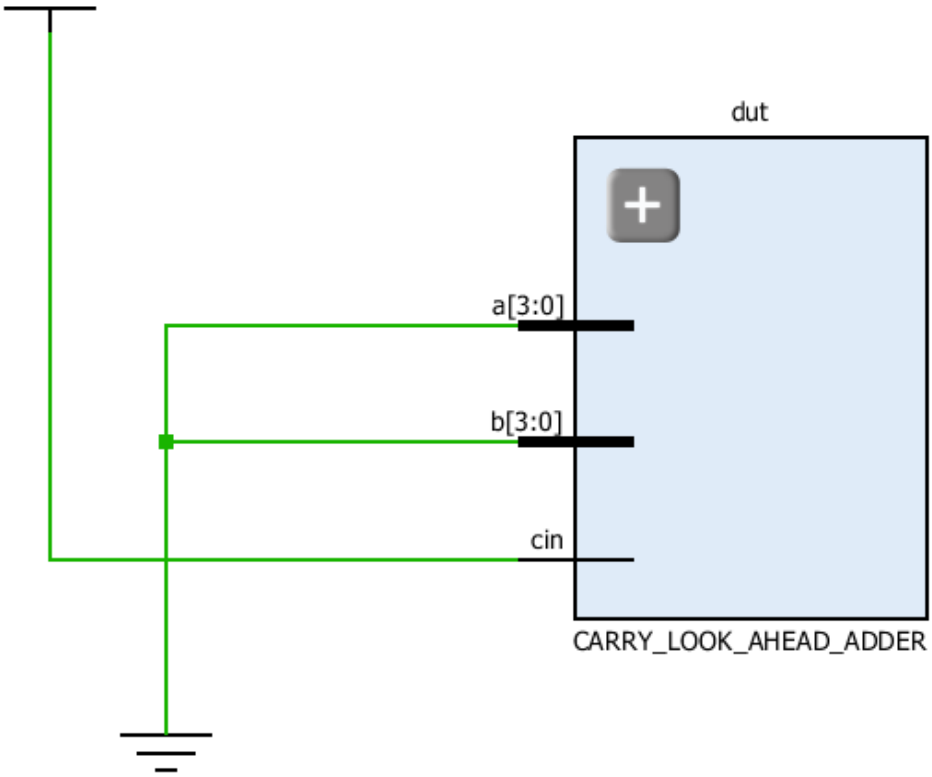
VERILOG CODE:

```
module CARRY_LOOK_AHEAD_ADDER(
    input [3:0] a,
    input [3:0] b,
    input cin,
    output [3:0] sum,
    output cout
    );
    and (g0,a[0],b[0]),
    (g1,a[1],b[1]),
    (g2,a[2],b[2]),
    (g3,a[3],b[3]);
    xor (p0,a[0],b[0]),
    (p1,a[1],b[1]),
    (p2,a[2],b[2]),
    (p3,a[3],b[3]);
    xor (sum[0],p0,cin),
        (sum[1],p1,c0),
        (sum[2],p2,c1),
        (sum[3],p3,c2);
        assign c0= g0 | (p0 & cin),
        c1= g1 | (p1 & g0) | (p1 & p0 & cin),
        c2= g2 | (p2 & g1) | (p2 & p1 & g0) | (p2 & p1 & p0 & cin),
        c3= g3 | (p3 & g2) | (p3 & p2 & g1) | (p3 & p2 & p1 & g0) | (p3 & p2 & p1 & p0 & cin);
        assign cout=c3;

endmodule
```

SIMULATION:



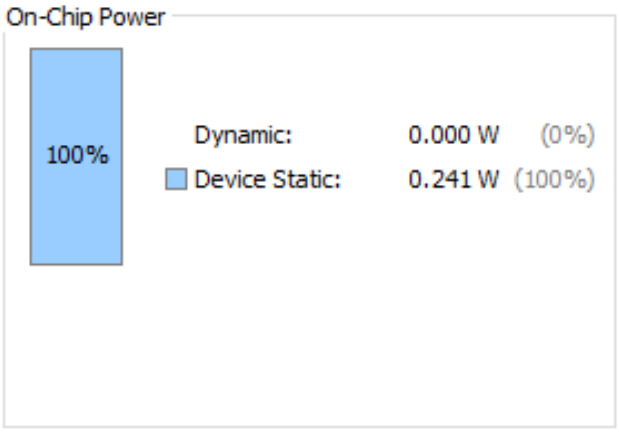
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-9: N - BIT COMPARATOR

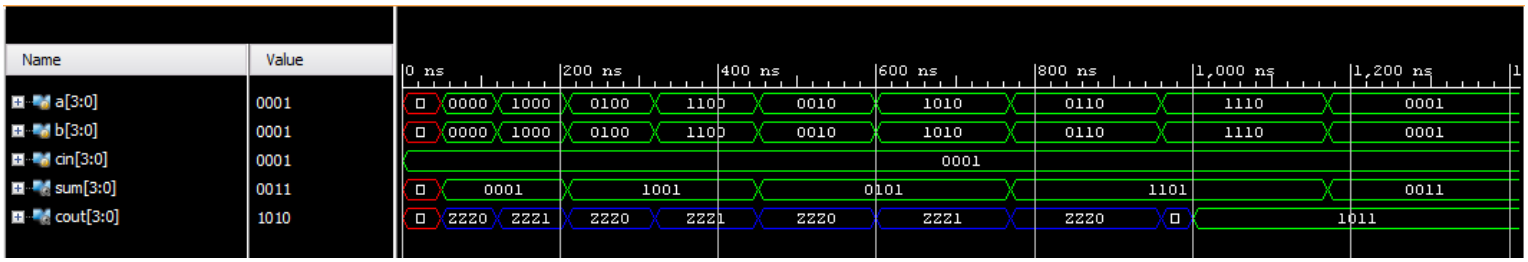
CODE FOR TESTBENCH:

```
module testbench;
reg [1:0] a,b;
wire L,E,G;
N_BIT_COMPARATOR dut(a,b,L,E,G);
initial
begin
$monitor("a=%b b=%b L=%b E=%b G=%b",a,b,L,E,G);
#100 a[0]=0; a[1]=0;
     b[0]=0; b[1]=0;
#200 a[0]=0; a[1]=1;
     b[0]=0; b[1]=1;
#300 a[0]=1; a[1]=0;
     b[0]=1; b[1]=0;
#400 a[0]=1; a[1]=1;
     b[0]=1; b[1]=1;
#500 a[0]=0; a[1]=0;
     b[0]=0; b[1]=0;
#600 a[0]=0; a[1]=1;
     b[0]=0; b[1]=1;
     end
     endmodule
```

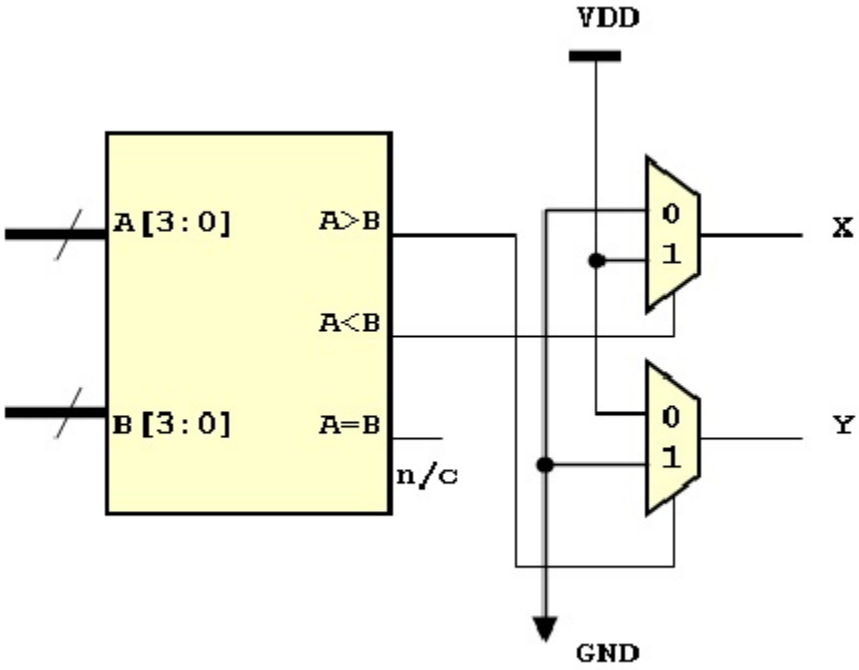
VERILOG CODE:

```
module N_BIT_COMPARATOR(
    input [1:0]a,
    input [1:0] b,
    output L,
    output G,
    output E
    );
   parameter n=32;
    input [1:0]a,b;
    output L,G,E;
    reg L=0, G=0, E=0;
    always@(a,b)
    begin
    if(a>b)
    begin
    L=0; E=0; G=1;
    end
    else if (a<b)
    begin
    L=1; E=0; G=0;
    end
    else
    begin
    L=0; E=1; G=0;
    end
    end
endmodule
```

SIMULATION:



RTL SCHEMATIC:

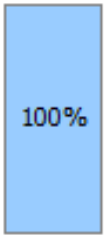


POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power



Dynamic:	0.000 W	(0%)
Device Static:	0.241 W	(100%)

CODE-10: SERIAL IN SERIAL OUT SHIFT REGISTER

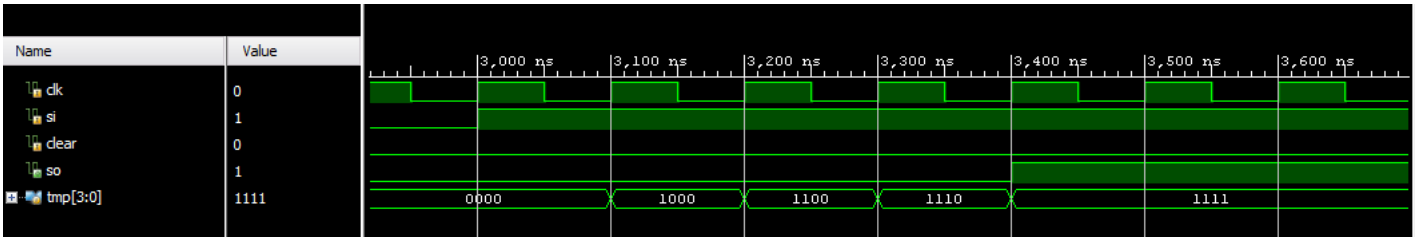
CODE FOR TESTBENCH:

```
module testbench;
reg [3:0] Width;
reg Clk,Rst;
wire [3:0] Count;

RING_COUNTER dut(Clk,Rst,Width,Count);

initial
begin
$monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
end
  always
  begin
   #50 Clk=~Clk;
   end
   initial
   begin
   #100 Rst=1;
   #100 Rst=0;
   $finish;
   end
   endmodule
```

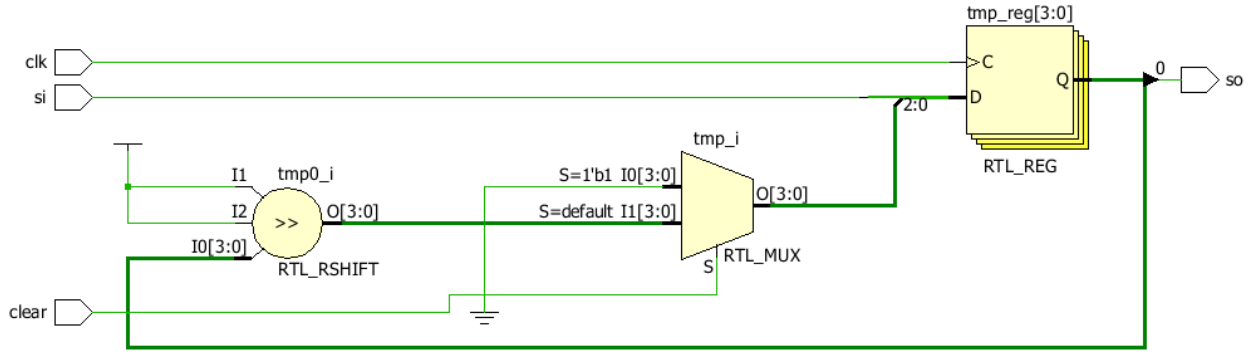
VERILOG CODE:

```
module SISO_REG(
    input clk,
    input si,
    input clear,
    output so
    );
    reg [3:0] tmp;
    always@(posedge clk)
    begin
    if(clear)
    tmp <=4'b0000;
    else
    tmp <= tmp >>1;
    tmp[3] <= si;
    end
    assign so = tmp;
endmodule
```

SIMULATION:



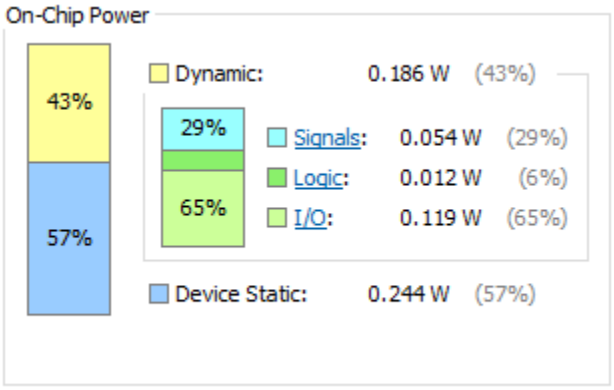
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.43 W**
Junction Temperature:	**25.6 ℃**
Thermal Margin:	59.4 ℃ (40.9 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-11: SERIAL IN PARALLEL OUT SHIFT REGISTER

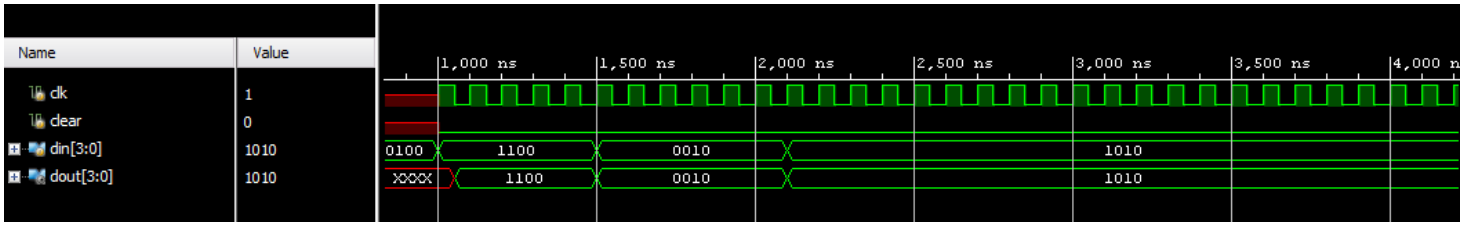
CODE FOR TESTBENCH:

```
module testbench;
reg clk,clear;
reg [3:0] din;
wire [3:0] dout;

SIPO_REG dut(clk,clear,din,dout);
initial
begin
$monitor("clk=%b clear=%b din=%b dout=%b",clk,clear,din,dout);

#100 din[0]=0; din[1]=0; din[2]=0; din[3]=0;
#200 din[0]=0; din[1]=0; din[2]=0; din[3]=1;
#300 din[0]=0; din[1]=0; din[2]=1; din[3]=0;
#400 din[0]=0; din[1]=0; din[2]=1; din[3]=1;
#500 din[0]=0; din[1]=1; din[2]=0; din[3]=0;
#600 din[0]=0; din[1]=1; din[2]=0; din[3]=1;
end
endmodule
```

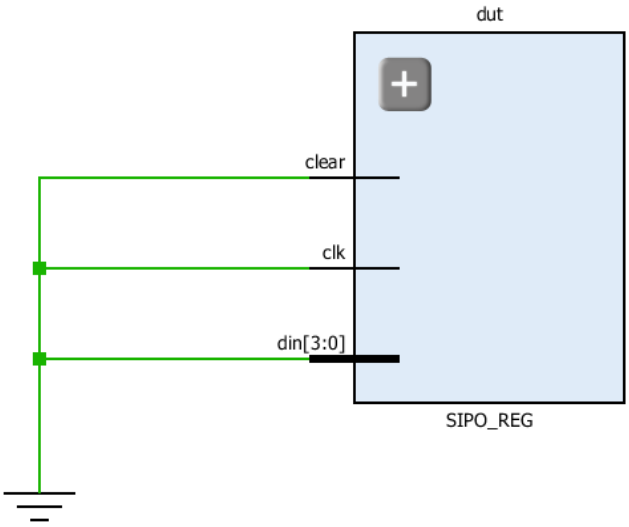
VERILOG CODE:

```
module SIPO_REG(
    input clk,
    input clear,
    input [3:0] din,
    output reg [3:0] dout
    );
    always@(posedge clk)
    begin
    if(clear)
    dout <= 4'b0000;
    else
    dout <= din;
    end
endmodule
```

SIMULATION:



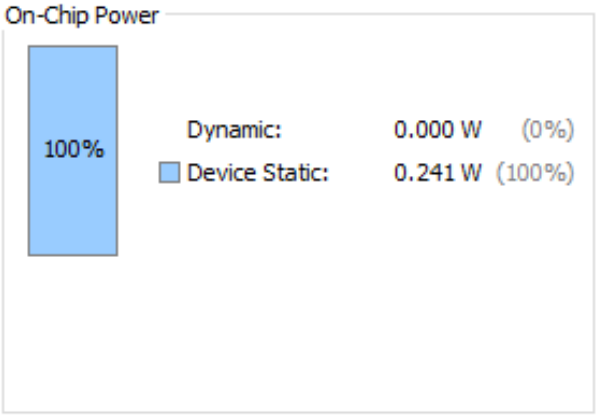
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-12: PARALLEL IN PARALLEL OUT SHIFT REGISTER

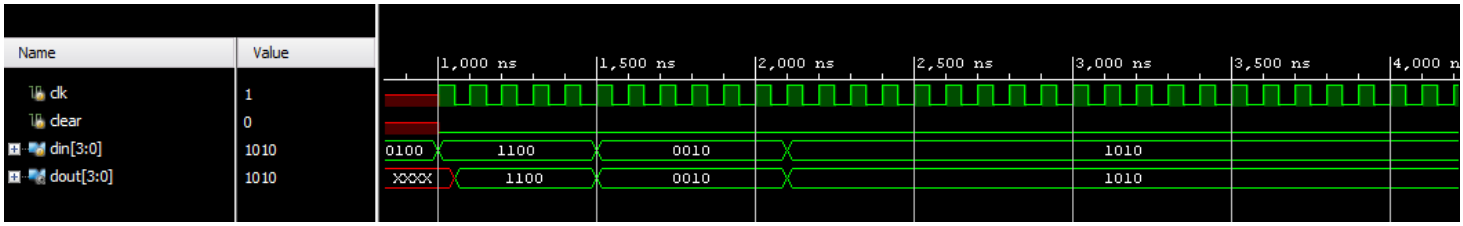
CODE FOR TESTBENCH:

```
module testbench;
reg clk,clear;
reg [3:0] din;
wire [3:0] dout;

PIPO_REG dut(clk,clear,din,dout);
initial
begin
$monitor("clk=%b clear=%b din=%b dout=%b",clk,clear,din,dout);

#100 din[0]=0; din[1]=0; din[2]=0; din[3]=0;
#200 din[0]=0; din[1]=0; din[2]=0; din[3]=1;
#300 din[0]=0; din[1]=0; din[2]=1; din[3]=0;
#400 din[0]=0; din[1]=0; din[2]=1; din[3]=1;
#500 din[0]=0; din[1]=1; din[2]=0; din[3]=0;
#600 din[0]=0; din[1]=1; din[2]=0; din[3]=1;
end
endmodule
```

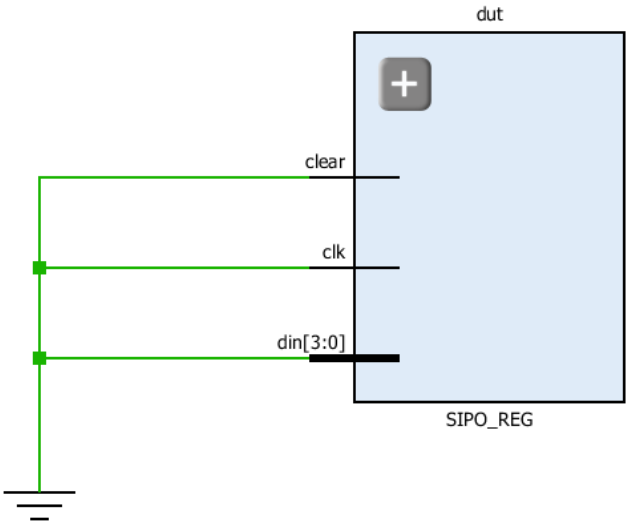
VERILOG CODE:

```
module PIPO_REG(
    input clk,
    input clear,
    input [3:0] din,
    output reg [3:0] dout
    );
    always@(posedge clk)
    begin
    if(clear)
    dout <= 4'b0000;
    else
    dout <= din;
    end
endmodule
```

SIMULATION:



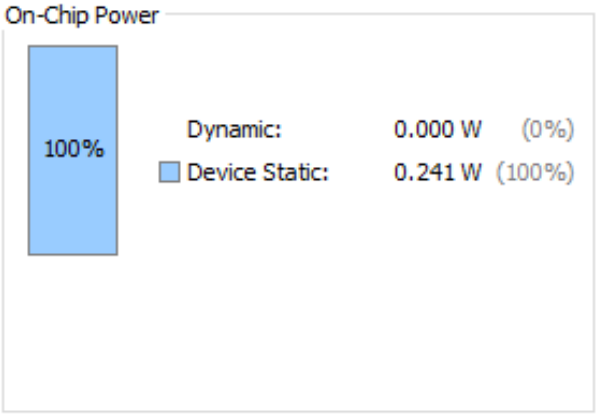
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-13: PARALLEL IN SERIAL OUT SHIFT REGISTER

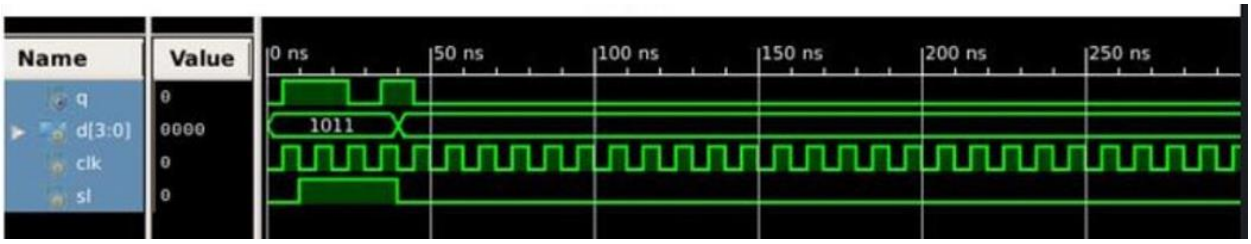
CODE FOR TESTBENCH:

```
module s1(
input a,b,s1,
output q
);
assign q = (~s1&b) | (s1&a);
endmodule

module dff(
input d,clk,
output q
);
reg q=0;
always@(posedge clk)
begin
q <= d;
end
endmodule

module PISO_REG(
    input [3:0] d,
    input clk,
    input s1,
    output q
    );
    wire q1,q2,q3,d1,d2,d3;
    dff a(d[3],clk,q1);
    s1 a1(q1,d[2],s1,d1);
    diff b(d1,clk,q2);
    s1 b1(q2,d[1],s1,d2);
    dff c(d2,clk,q3);
    s1 c1(q3,d[0],s1,d3);
    dff dd(d3,clk,q);
endmodule
```

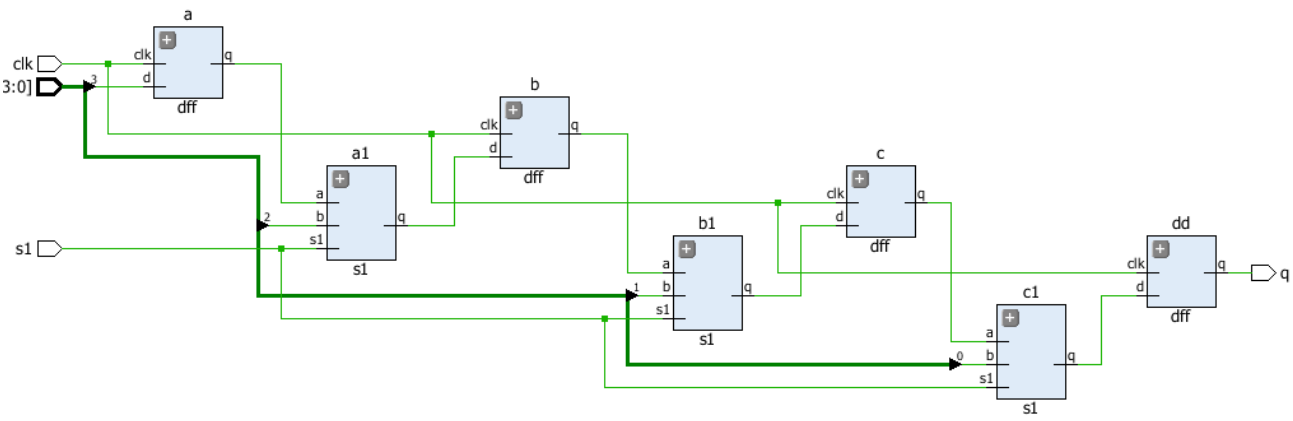
VERILOG CODE:

```
module s1(
input a,b,s1,
output q
);
assign q = (~s1&b) | (s1&a);
endmodule

module dff(
input d,clk,
output q
);
reg q=0;
always@(posedge clk)
begin
q <= d;
end
endmodule
```

SIMULATION:



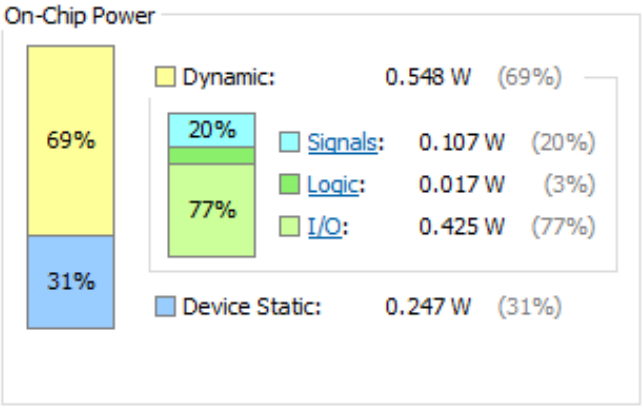
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.796 W**
Junction Temperature:	**26.1 ℃**
Thermal Margin:	58.9 ℃ (40.6 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-14: BIDIRECTIONAL SHIFT REGISTER

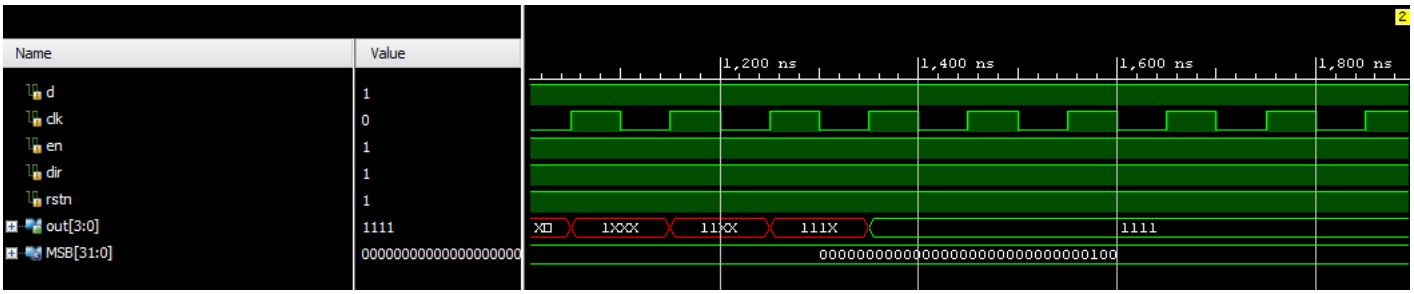
CODE FOR TESTBENCH:

```
module testbench;
reg [3:0] Width;
reg Clk,Rst;
wire [3:0] Count;

RING_COUNTER dut(Clk,Rst,Width,Count);

initial
begin
$monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
end
  always
  begin
   #50 Clk=~Clk;
   end
   initial
   begin
   #100 Rst=1;
   #100 Rst=0;
   $finish;
   end
   endmodule
```

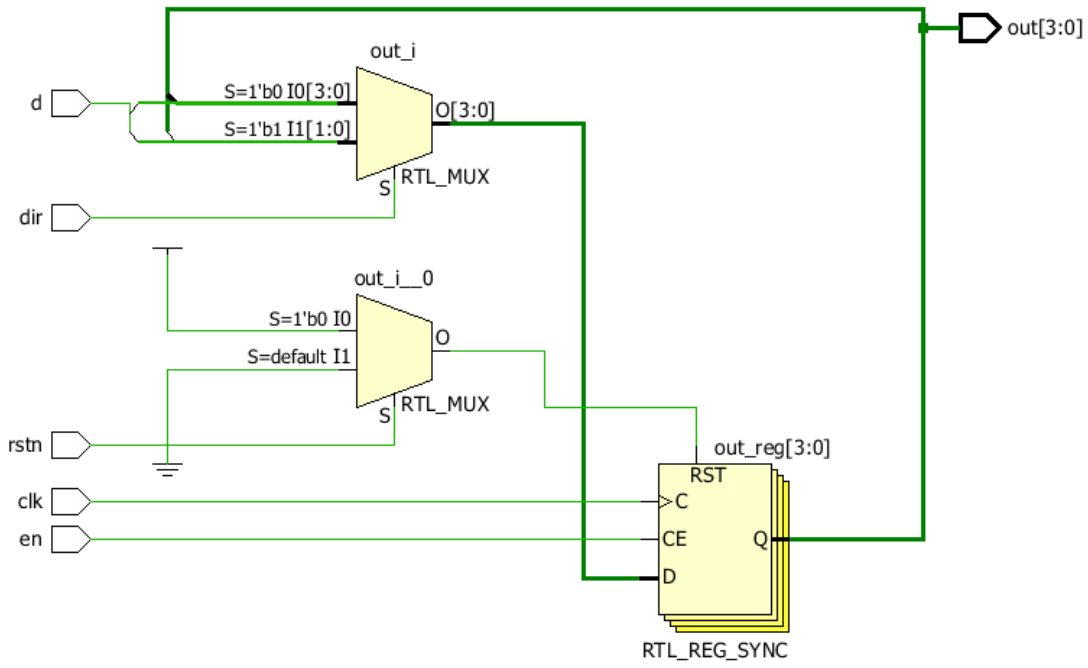
VERILOG CODE:

```
module BIDIRECTIONAL_SHIFT_REG
#(parameter MSB=4)
(
    input d,
    input clk,
    input en,
    input dir,
    input rstn,
    output reg [MSB-1:0] out
    );
    always@(posedge clk)
    if(!rstn)
    out <= 0;
    else
    begin
    if(en)
    case (dir)
    0: out <= {out[MSB-2:0],d};
    1: out <= {d,out[MSB-1:1]};
    endcase
    else
        out <= out;
        end
endmodule
```

SIMULATION:



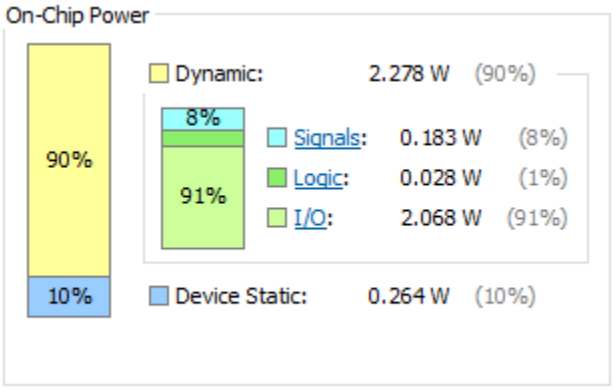
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.542 W**
Junction Temperature:	**28.6 ℃**
Thermal Margin:	56.4 ℃ (38.8 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-15: PRBS SEQUENCE GENERATOR

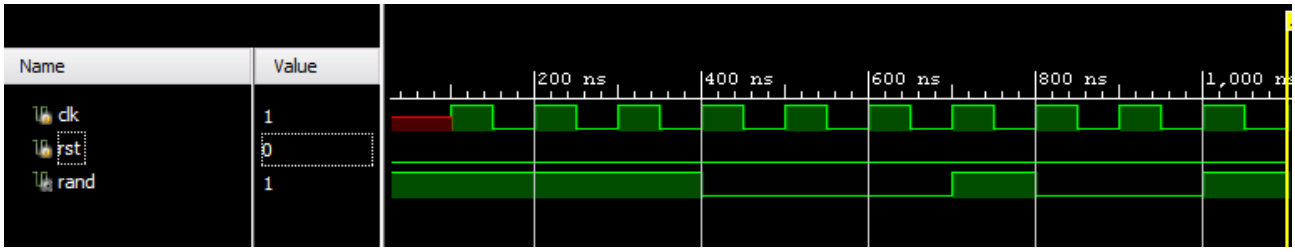
CODE FOR TESTBENCH:

```
module tb_PRBS_SEQUENCE_GENERATOR;
  reg clk;
  reg rst;
  wire rand;
  PRBS_SEQUENCE_GENERATOR uut (
    .clk(clk),
    .rst(rst),
    .rand(rand)
  );
    always begin
    #5 clk = ~clk;
  end
    initial begin
    rst = 1;
    #10 rst = 0;
  end
    initial begin
    $display("Time\tPRBS Output");
    $monitor("%d\t%b", $time, rand);
    #100;
    $finish;
  end
endmodule
```

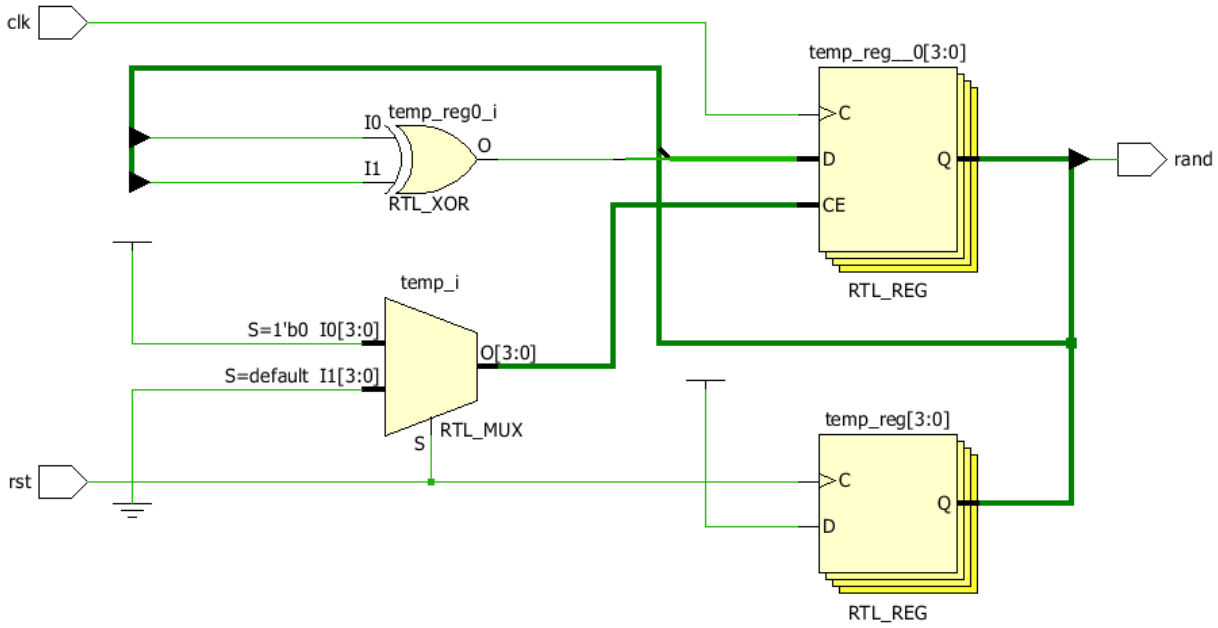
VERILOG CODE:

```
module PRBS_SEQUENCE_GENERATOR(
input clk,rst,
output rand
);

reg [3:0] temp;
always@(posedge rst)
begin
temp <= 4'hf;
end
always@(posedge clk)
begin
if (~rst)
begin
temp <= {temp[0]^temp[1],temp[3],temp[2],temp[1]};
end
end
assign rand = temp[0];
endmodule
```

SIMULATION:



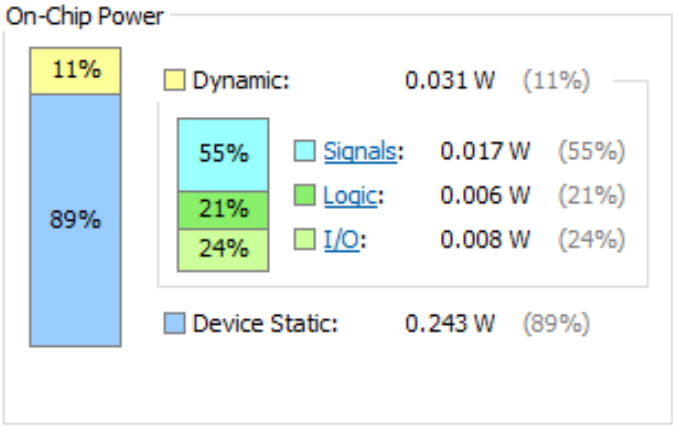
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.274 W**
Junction Temperature:	**25.4 °C**
Thermal Margin:	59.6 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-16: 8 – BIT SUBTRACTOR

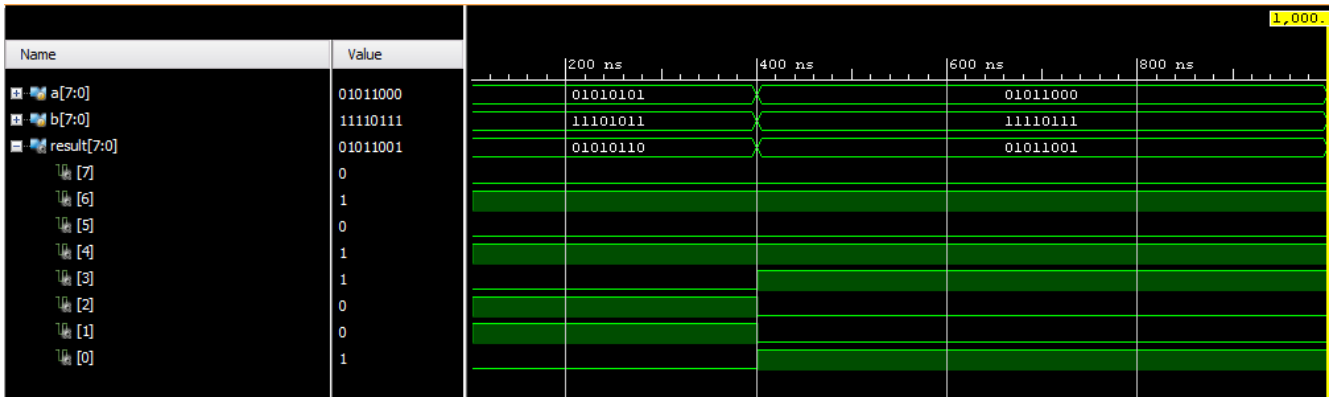
CODE FOR TESTBENCH:

```
module testbench;
reg [7:0] a,b;
wire [7:0] result;
SUBTRACTOR_8_BIT dut(a,b,result);

initial
begin
$monitor("a=%b b=%b result=%b",a,b,result);
#100 a[0]=1; a[1]=0; a[2]=1; a[3]=0; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
     b[0]=1; b[1]=1; b[2]=0; b[3]=1; b[4]=0; b[5]=1; b[6]=1; b[7]=1;
#300 a[0]=0; a[1]=0; a[2]=0; a[3]=1; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
     b[0]=1; b[1]=1; b[2]=1; b[3]=0; b[4]=1; b[5]=1; b[6]=1; b[7]=1;
     end
     endmodule
```

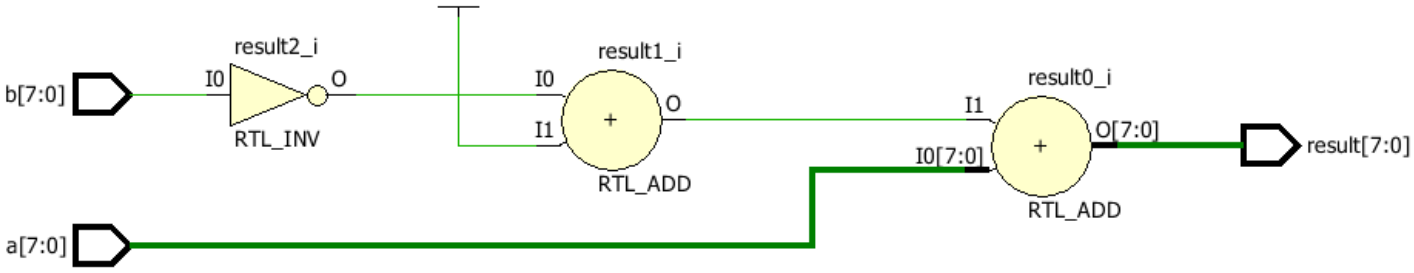
VERILOG CODE:

```
module SUBTRACTOR_8_BIT(
    input [7:0] a,
    input [7:0] b,
    output reg [7:0] result
    );

    reg neg_b;
    always@(a or b)
    begin
    neg_b = ~ b + 1;
    result = a + neg_b;
    end
endmodule
```

SIMULATION:



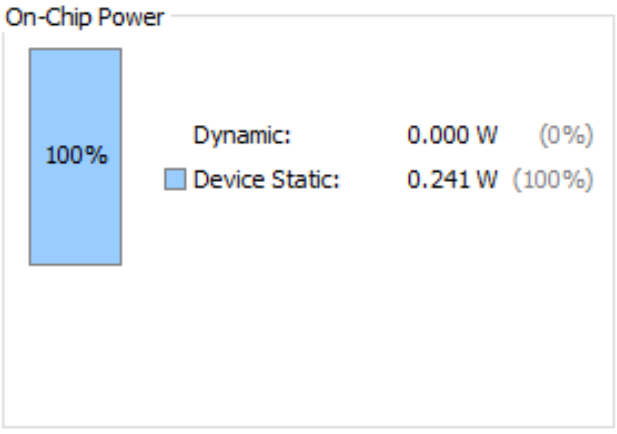
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-17: 8 – BIT ADDER SUBTRACTOR

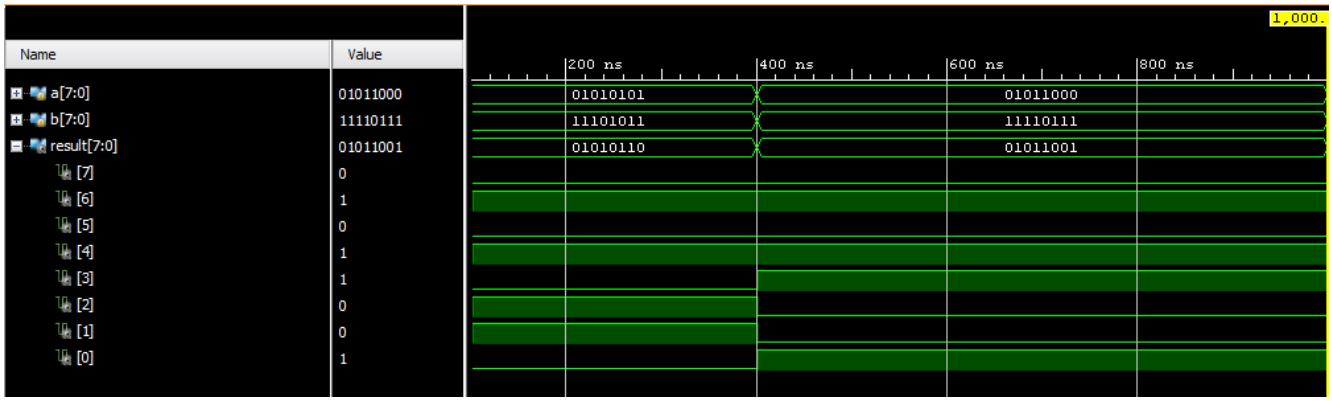
CODE FOR TESTBENCH:

```
module testbench;
reg [7:0] a,b;
wire [7:0] result;
SUBTRACTOR_8_BIT dut(a,b,result);

initial
begin
$monitor("a=%b b=%b result=%b",a,b,result);
#100 a[0]=1; a[1]=0; a[2]=1; a[3]=0; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
     b[0]=1; b[1]=1; b[2]=0; b[3]=1; b[4]=0; b[5]=1; b[6]=1; b[7]=1;
#300 a[0]=0; a[1]=0; a[2]=0; a[3]=1; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
     b[0]=1; b[1]=1; b[2]=1; b[3]=0; b[4]=1; b[5]=1; b[6]=1; b[7]=1;
     end
     endmodule
```

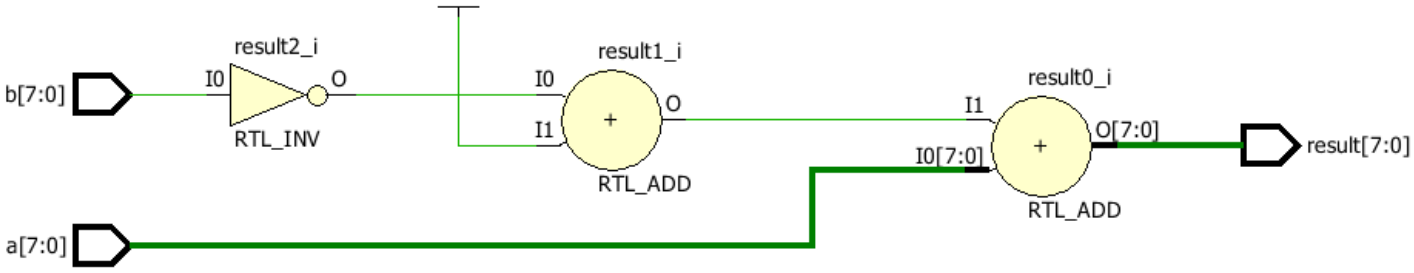
VERILOG CODE:

```
module ADDER_SUBTRACTOR_8_BIT(
    input [7:0] a,
    input [7:0] b,
    input mode,
    output reg [7:0] result,
    output reg ovfl
    );
    wire [7:0] a,b;
    wire mode;
    reg [7:0] neg_b;
    always@(a or b or mode)
    begin
    if(mode==0)
    begin
    result = a+b;
    ovfl = (a[7] & b[7] & ~result[7]) | (~a[7] & ~b[7] & result[7]);
    end
    else
    begin
    neg_b = ~b+1;
    result = a + neg_b;
    ovfl = (a[7] & neg_b[7] & ~result[7]) | (~a[7] & ~neg_b[7] & result[7]);
    end

endmodule
```

SIMULATION:



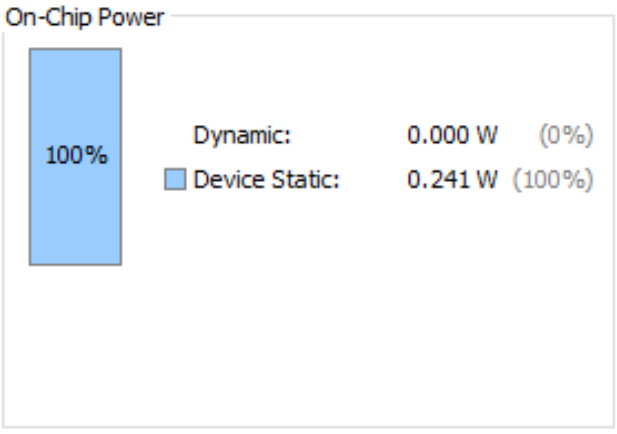
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-18: 4 – BIT MULTIPLYER

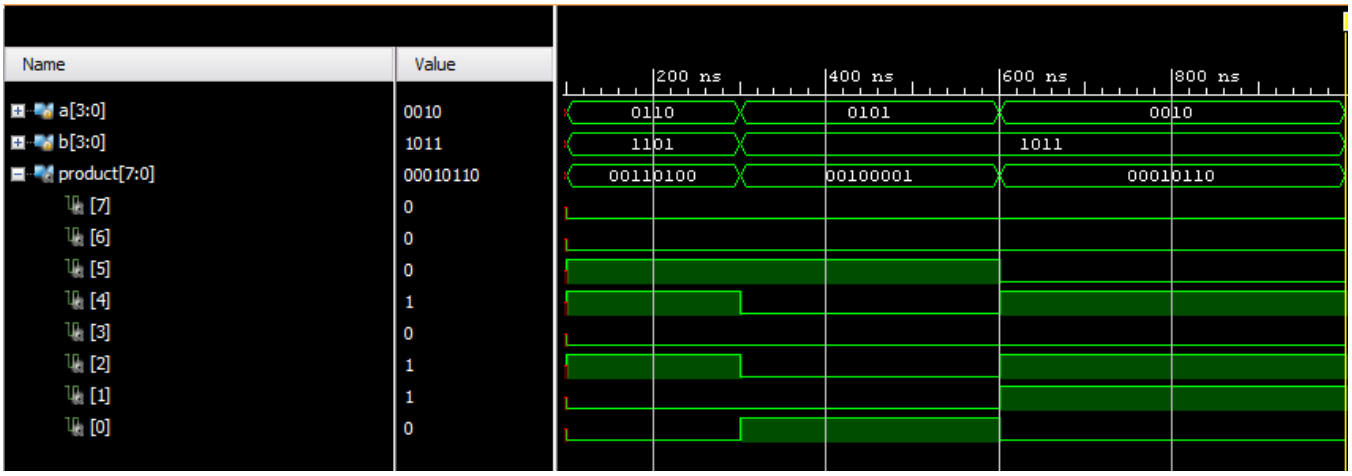
CODE FOR TESTBENCH:

```
module testbench;
reg [3:0]a,b;
wire [7:0] product;

    MULTIPLYER dut(a,b,product);
    initial
    begin
    $monitor("a=%b b=%b product=%b",a,b,product);

    #100 a[0]=0; a[1]=1; a[2]=1; a[3]=0;
         b[0]=1; b[1]=0; b[2]=1; b[3]=1;
    #200 a[0]=1; a[1]=0; a[2]=1; a[3]=0;
         b[0]=1; b[1]=1; b[2]=0; b[3]=1;
    #300 a[0]=0; a[1]=1; a[2]=0; a[3]=0;
         b[0]=1; b[1]=1; b[2]=0; b[3]=1;
         end
         endmodule
```

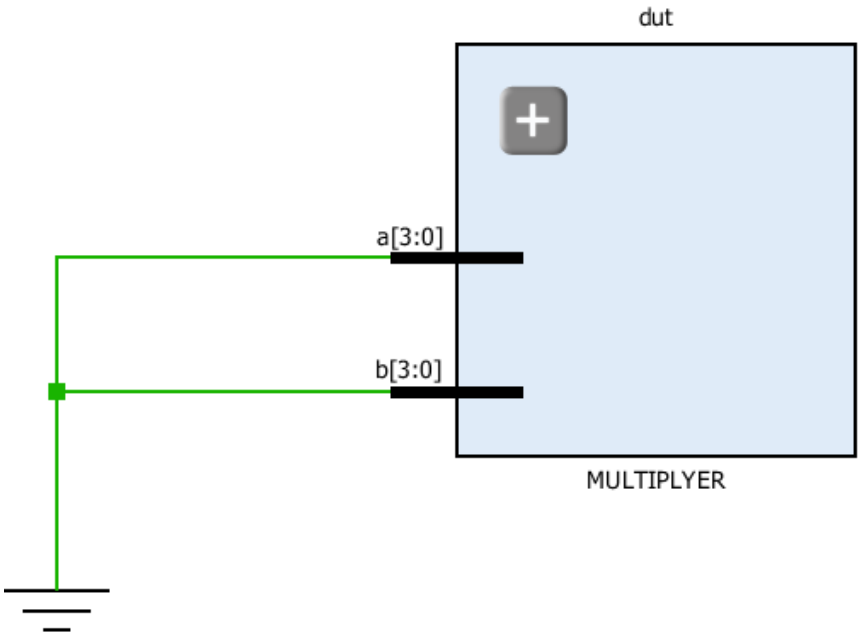
VERILOG CODE:

```
module MULTIPLYER(
    input [3:0] a,
    input [3:0] b,
    output [7:0] product
    );
    wire [3:0] m0;
    wire [4:0] m1;
    wire [5:0] m2;
    wire [6:0] m3;
    wire [7:0] s1,s2,s3;
    assign m0={4{a[0]}}&b[3:0];
    assign m1={4{a[1]}}&b[3:0];
    assign m2={4{a[2]}}&b[3:0];
    assign m3={4{a[3]}}&b[3:0];

    assign s1=m0+(m1<<1);
    assign s2=s1+(m2<<1);
    assign s3=s2+(m3<<1);
    assign product= s3;
endmodule
```

SIMULATION:



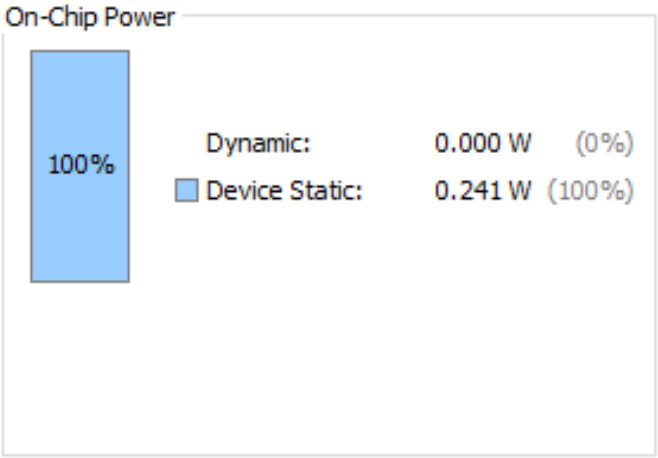
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-19: FIXED POINT DIVISION

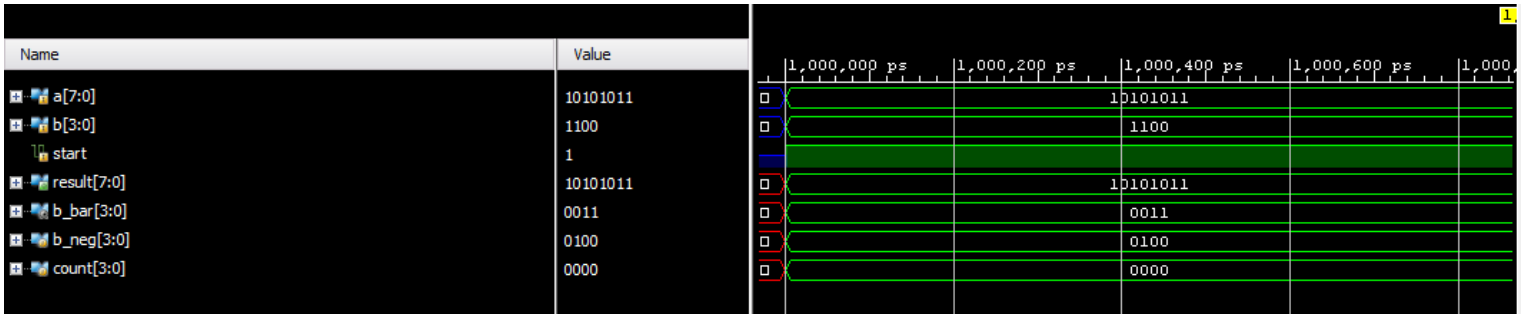
CODE FOR TESTBENCH:

```
module testbench;
reg [7:0]a;
reg [3:0]b;
reg start;
wire [7:0] result;

    FIXED_POINT_DIVISION dut(a,b,start,result);
    initial
    begin
    $monitor("a=%b b=%b start=%b result=%b",a,b,start,result);

    #100 a[0]=0; a[1]=1; a[2]=1; a[3]=0; a[4]=1; a[5]=0; a[6]=1; a[7]=1;
         b[0]=1; b[1]=0; b[2]=1; b[3]=1;
    #200 a[0]=1; a[1]=0; a[2]=1; a[3]=0; a[4]=0; a[5]=1; a[6]=0; a[7]=0;
         b[0]=1; b[1]=1; b[2]=0; b[3]=1;
    #300 a[0]=0; a[1]=1; a[2]=0; a[3]=0; a[4]=1; a[5]=1; a[6]=1; a[7]=1;
         b[0]=1; b[1]=1; b[2]=0; b[3]=1;
         end
         endmodule
```

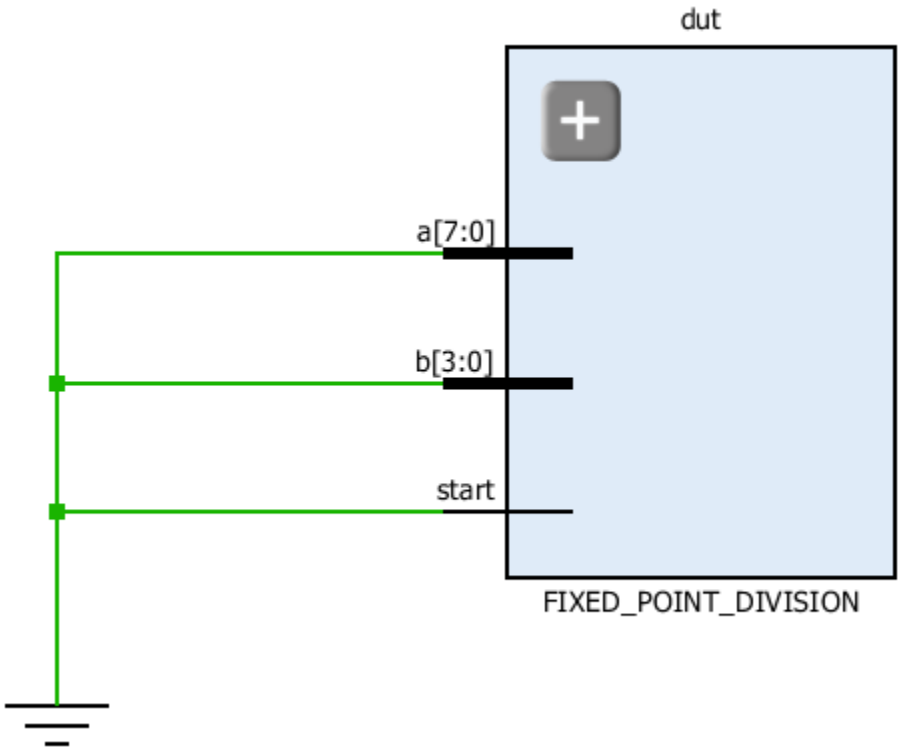
VERILOG CODE:

```
module FIXED_POINT_DIVISION(
    input [7:0] a,
    input [3:0] b,
    input start,
    output reg [7:0] result
    );
    wire[3:0] b_bar;
    reg [3:0] b_neg;

    reg [3:0] count;
    assign b_bar=~b;
    always@(b_bar)
    b_neg=b_bar+1;
    always@(posedge start)
    begin
    result=a;
    count=4'b0000;
    if((a!=0) &&  (b!=0))
    while (count)
    begin
    result=result<<1;
    result={(result[7:4] + b), result[3:1],1'b0};
    count=count-1;
    end
    else
    begin
    result={result[7:1],1'b1};
    count=count-1;
    end
    end

endmodule
```

SIMULATION:



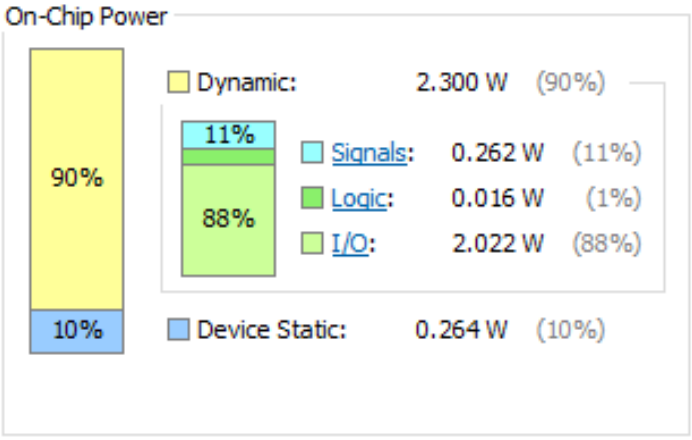
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.564 W**
Junction Temperature:	**28.6 ℃**
Thermal Margin:	56.4 ℃ (38.8 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-20: MASTER SLAVE JK FLIP FLOP

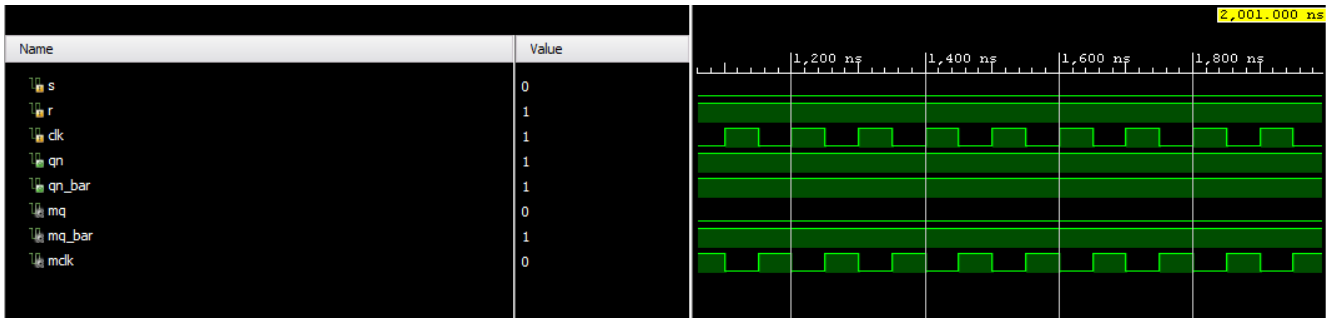
CODE FOR TESTBENCH:

```
module master_slave(
    input s,r,clk,
    output qn,qn_bar
    );
    wire mq;
    wire mq_bar;
    wire mclk;
    assign mclk=~clk;
    JK_FF master(s,r,clk,mq,mq_bar);
    JK_FF slave(mq,mq_bar,mclk,qn,qn_bar);
   endmodule
```

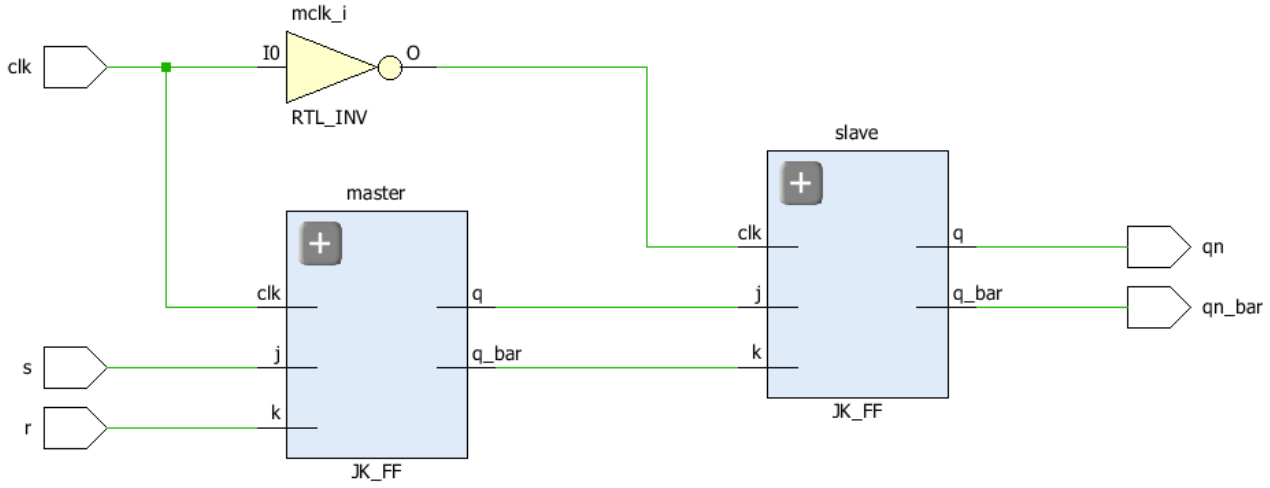
VERILOG CODE:

```
module JK_FF(
    input j,
    input k,
    input clk,
    output reg q,
    output q_bar
    );
    assign q_bar=~q;
    always@(posedge clk)
    begin
    case({j,k})
    2'b00: q<=q;
    2'b01: q<=0;
    2'b10: q<=1;
    2'b11: q<=~q;
    endcase
    end
endmodule

module master_slave(
    input s,r,clk,
    output qn,qn_bar
    );
    wire mq;
    wire mq_bar;
    wire mclk;
    assign mclk=~clk;
    JK_FF master(s,r,clk,mq,mq_bar);
    JK_FF slave(mq,mq_bar,mclk,qn,qn_bar);
   endmodule
```

SIMULATION:



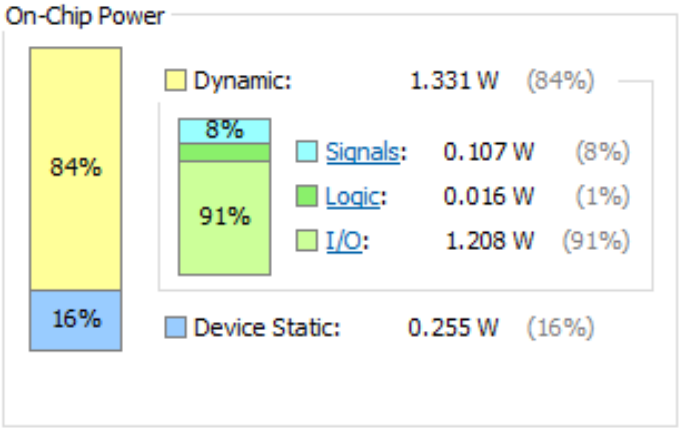
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.586 W**
Junction Temperature:	**27.2 ℃**
Thermal Margin:	57.8 ℃ (39.8 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-21: POSITIVE EDGE DETECTOR

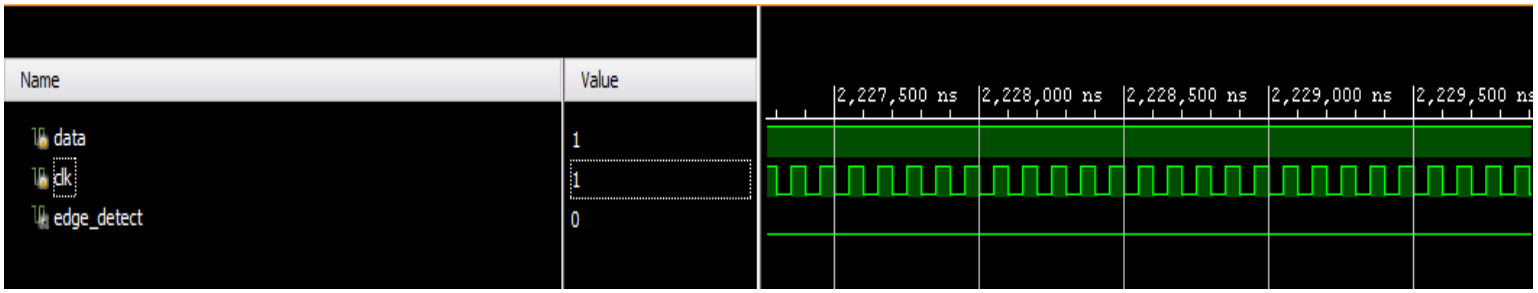
CODE FOR TESTBENCH:

```
module testbench;
reg data,clk;
wire edge_detect;
    EDGE_DETECTOR dut(data,clk,edge_detect);
    initial
    begin
    $monitor("data=%b clk=%b edge_detect=%b",data,clk,edge_detect);
    end
     always
      begin
      #50   clk = ~clk;



        end
    endmodule
```

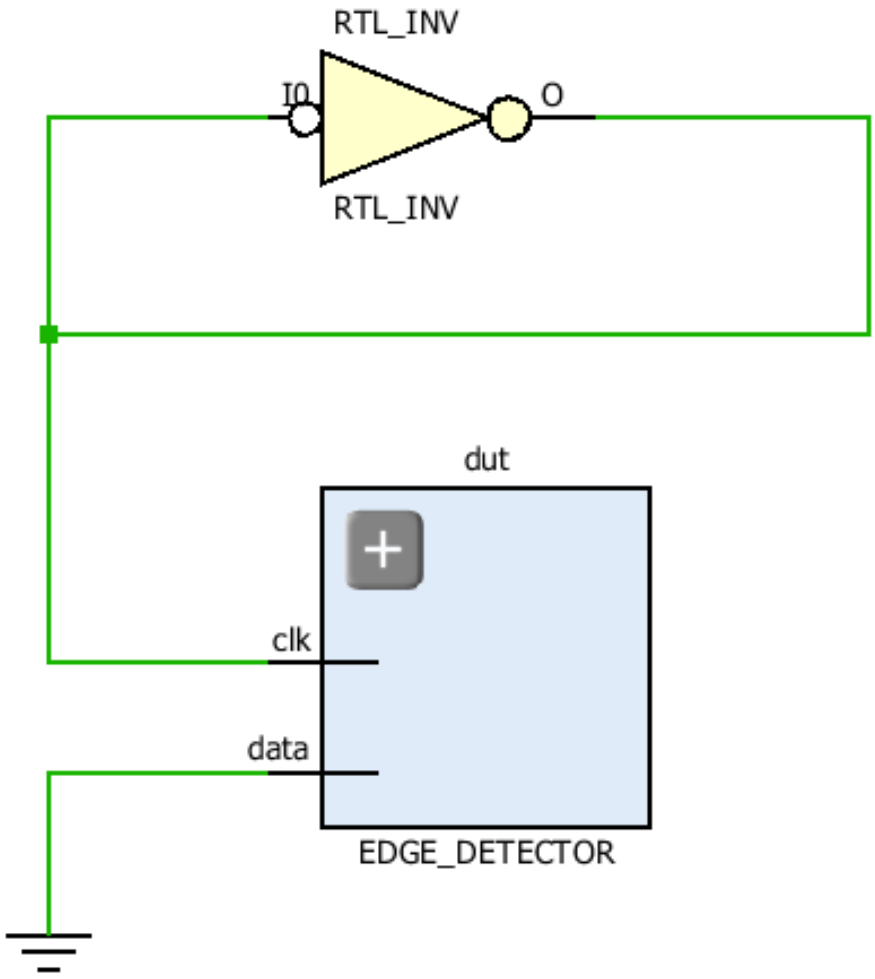
VERILOG CODE:

```
module EDGE_DETECTOR(
    input data,
    input clk,
    output edge_detect
    );
    reg data_d;
    always@(posedge clk)
    begin
    data_d <= data;
    end
    assign edge_detect= data & ~data_d;
endmodule
```

SIMULATION:



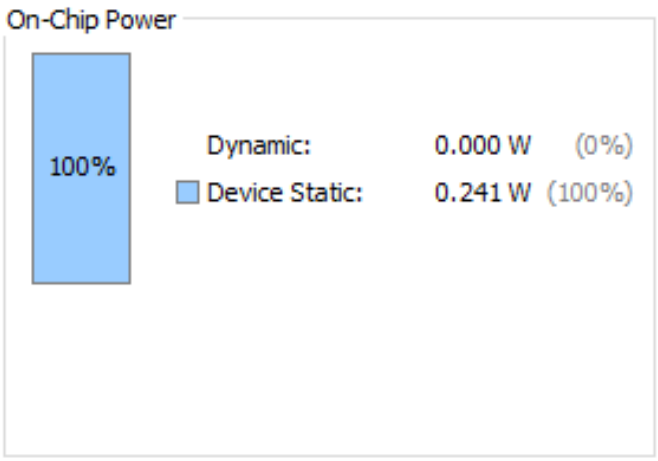
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-22: BCD ADDER

CODE FOR TESTBENCH:

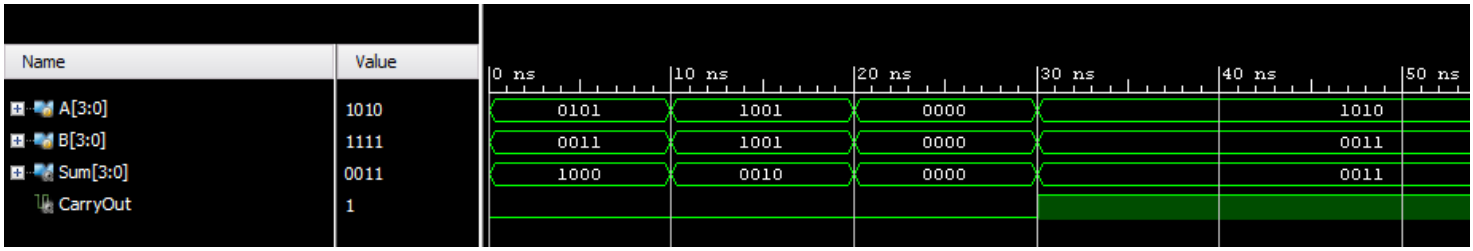
```
module BCD_Adder_Testbench;
reg [3:0] A, B;
wire [3:0] Sum;
wire CarryOut;
BCD_Adder uut(
    .A(A),
    .B(B),
    .Sum(Sum),
    .CarryOut(CarryOut)
);
initial begin
    $display("Testing BCD Adder");


    A = 4'b0101;
    B = 4'b0011;
    #10 $display("A = %b, B = %b, Sum = %b, CarryOut = %b", A, B, Sum, CarryOut);

    A = 4'b1001;
    B = 4'b1001;
    #10 $display("A = %b, B = %b, Sum = %b, CarryOut = %b", A, B, Sum, CarryOut);

    A = 4'b0000;
    B = 4'b0000;
    #10 $display("A = %b, B = %b, Sum = %b, CarryOut = %b", A, B, Sum, CarryOut);

    $finish;
end
endmodule
```

CODE

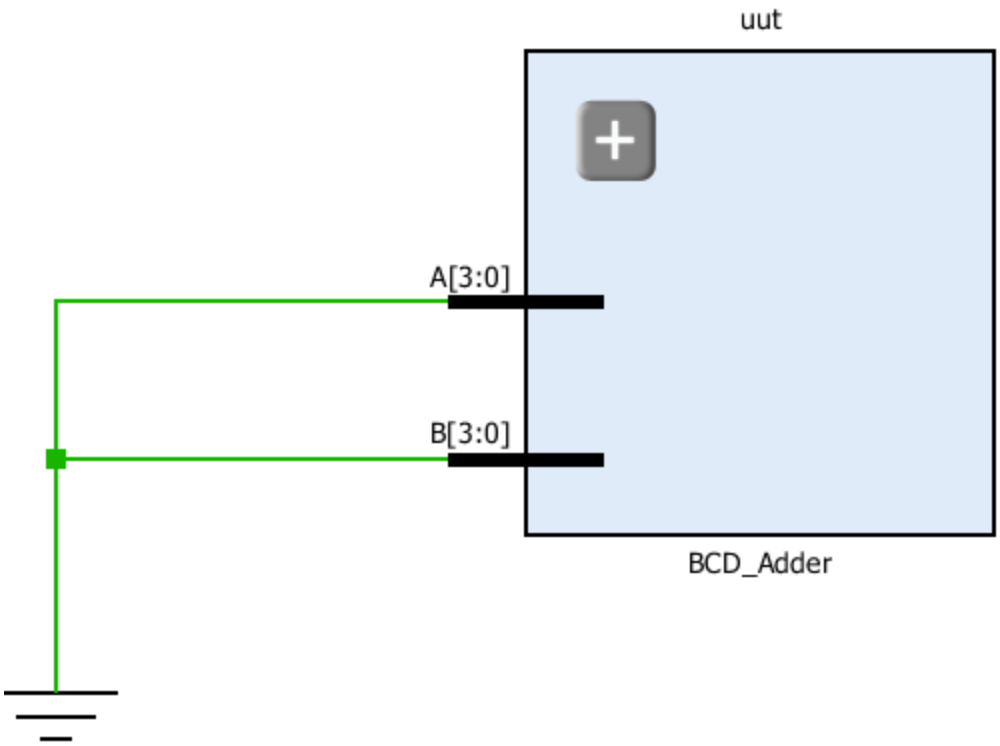
VERILOG CODE:

```
module BCD_Adder(
    input [3:0] A,
    input [3:0] B,
    output reg [3:0] Sum,
    output reg CarryOut
);

always @(*) begin
    Sum = A + B;
    if (Sum >= 10) begin
        Sum = Sum - 10;
        CarryOut = 1;
    end else begin
        CarryOut = 0;
    end
end

endmodule
```

SIMULATION:



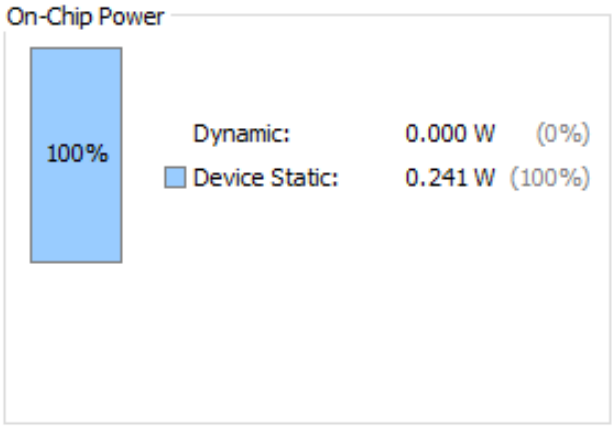
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-23: 4-BIT CARRY SELECT ADDER

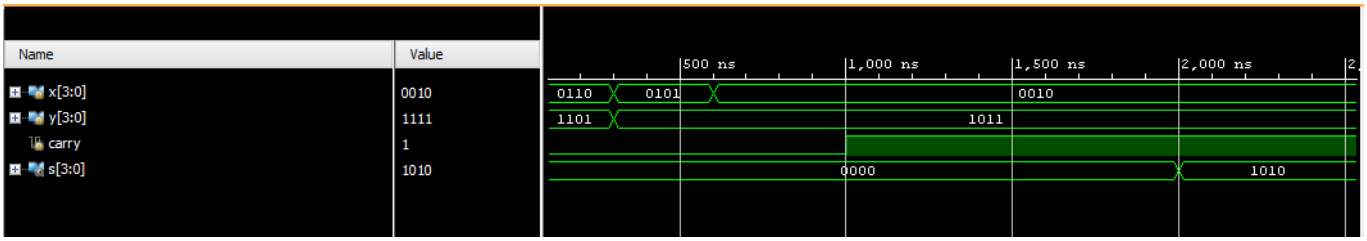
CODE FOR TESTBENCH:

```
module testbench;
reg [3:0]x,y;
reg carry;
wire [3:0] s;

    CARRY_SELECT dut(x,y,carry,s);
    initial
    begin
    $monitor("x=%b y=%b carry=%b s=%b",x,y,carry,s);
     carry = 1;
     carry = ~carry;
    #100 x[0]=0; x[1]=1; x[2]=1; x[3]=0;
         y[0]=1; y[1]=0; y[2]=1; y[3]=1;
    #200 x[0]=1; x[1]=0; x[2]=1; x[3]=0;
         y[0]=1; y[1]=1; y[2]=0; y[3]=1;
    #300 x[0]=0; x[1]=1; x[2]=0; x[3]=0;
         y[0]=1; y[1]=1; y[2]=0; y[3]=1;
         end
         endmodule
```

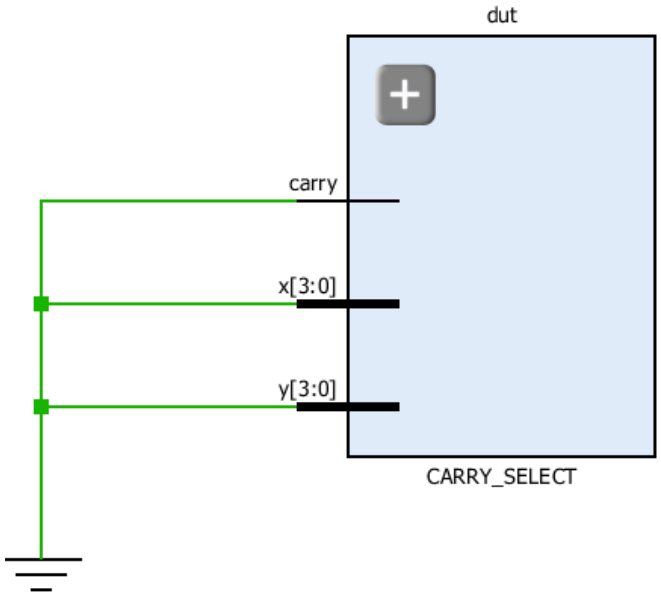
VERILOG CODE:

```
module FULL_ADDER(
    input a,
    input b,
    input cin,
    output reg S,cout
    );
    always@(a or b or cin)
    begin
    S = a^b^cin;
    cout = a&b | b&cin | cin&a;
    end
    endmodule

    module mux(
    input a,b,
    input S,
    output reg y
    );
    always@(a,b,S)
    begin
    y = S&a | S&b;
    end
    endmodule

module CARRY_SELECT(
    input [3:0] x,
    input [3:0] y,
    input carry,
    output [3:0] s,
    output cout
    );
    wire w1,w2,w3,w4,w5,w6,w7,w8,w9,w10,w11,w12,w13,w14,w15,w16;
    FULL_ADDER fa0(x[0],y[0],1'b0,w1,w2);
    FULL_ADDER fa1(x[1],y[1],w2,w3,w4);
    FULL_ADDER fa2(x[2],y[2],w4,w5,w6);
    FULL_ADDER fa3(x[3],y[3],w6,w7,w8);
    FULL_ADDER fa4(x[0],y[0],1'b1,w9,w10);
    FULL_ADDER fa5(x[1],y[1],w10,w11,w12);
    FULL_ADDER fa6(x[2],y[2],w12,w13,w14);
    FULL_ADDER fa7(x[3],y[3],w14,w15,w16);
    mux mu0(w1,w9,carry,s[0]);
    mux mu1(w3,w11,carry,s[1]);
    mux mu2(w5,w13,carry,s[2]);
    mux mu3(w7,w15,carry,s[3]);
    mux mu4(w8,w16,carry,cout);
endmodule
```

SIMULATION:



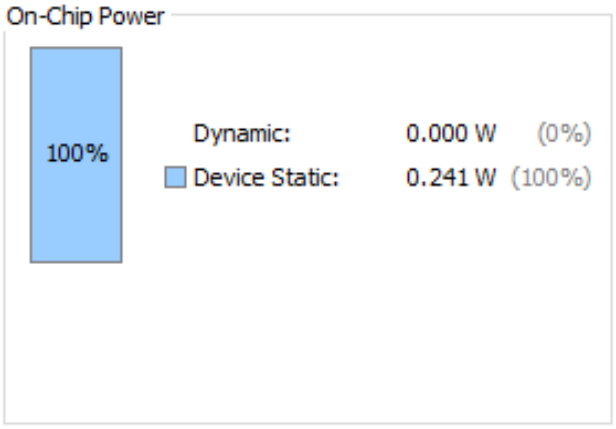
RTL SCHEMATIC:



POWER REPORT

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-24: MOORE FSM 1010 SEQUENCE DETECTOR

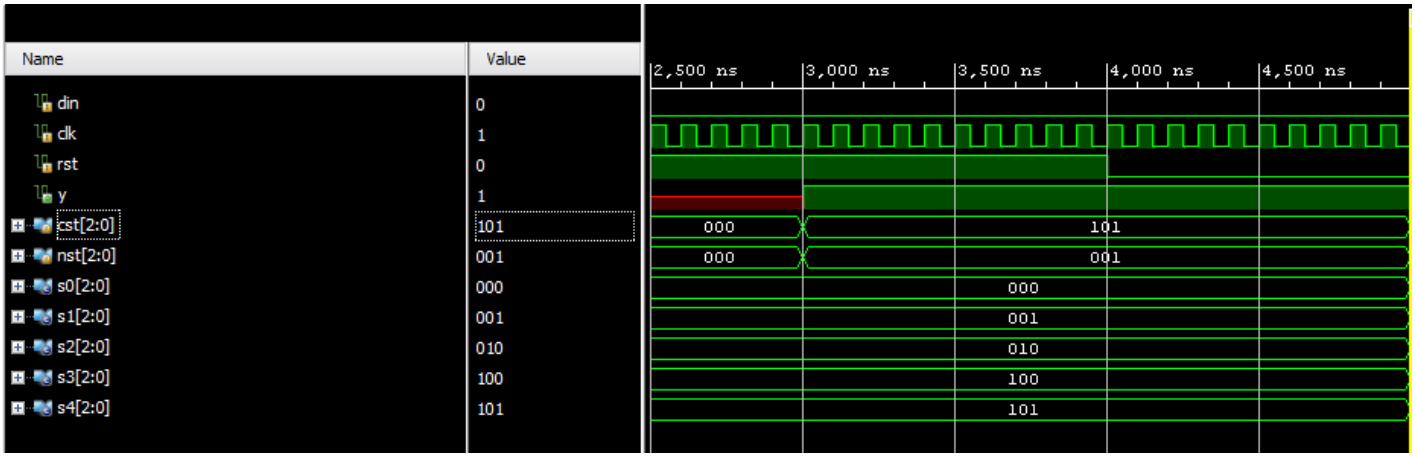
CODE FOR TESTBENCH:

```
module testbench;
reg din,clk,rst;
wire y;
    MOORE_FSM dut(din,clk,rst,y);
    initial
    begin
    $monitor("din=%b clk=%b rst=%b y=%b",din,clk,rst,y);
    end
     always
      begin
      #50   clk = ~clk;



        end
    endmodule
```

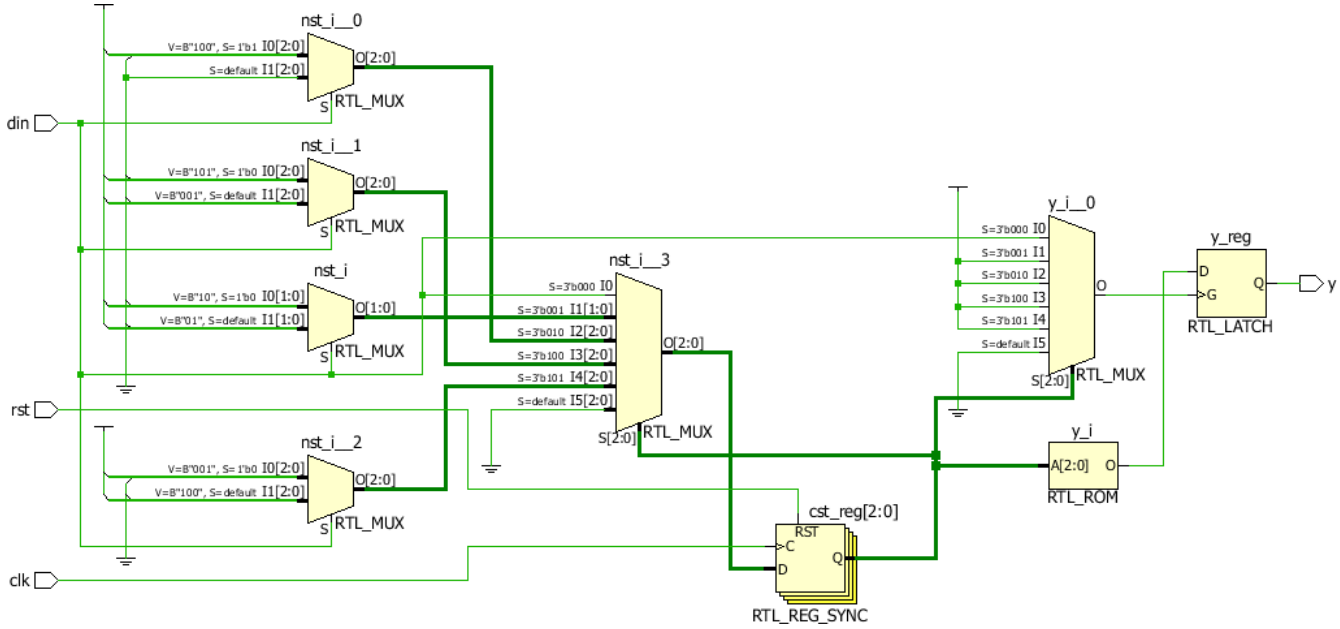
VERILOG CODE:

```
module MOORE_FSM(
    input din,
    input clk,
    input rst,
    output reg y
    );
    reg [2:0] cst,nst;
    localparam s0=3'b000,
               s1=3'b001,
               s2=3'b010,
               s3=3'b100,
               s4=3'b101;
    always@(cst or din)
    begin
    case(cst)
    s0 : if(din==1'b1)
        begin
        nst = s1;
        y=1'b0;
        end
      else nst = cst;
      s1 : if(din==1'b0)
              begin
              nst = s2;
              y=1'b0;
              end
      else
      begin
      nst = cst;
      y=1'b0;
      end
       s2 : if(din==1'b1)
                   begin
                   nst = s3;
                   y=1'b0;
                   end
            else
```

SIMULATION:



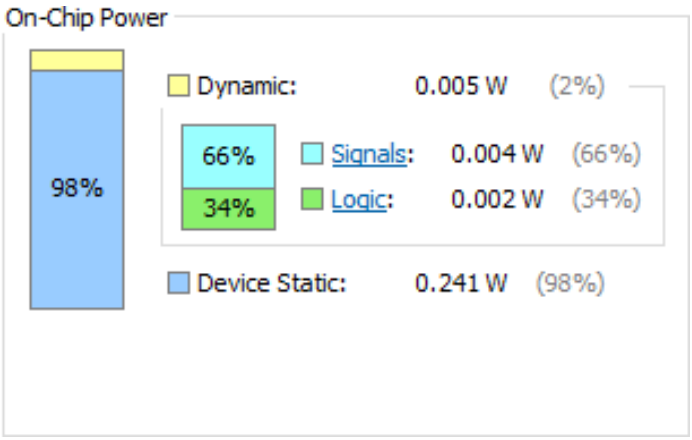
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.246 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-25: N:1 MUX

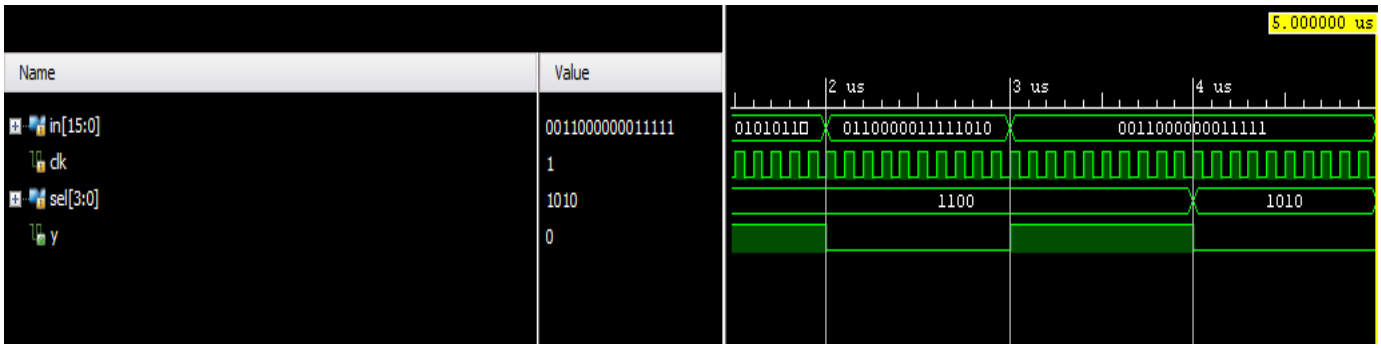
CODE FOR TESTBENCH:

```
module testbench;

   N_MUX uut (
    .data_inputs({16'b00000001, 16'b00000010, 16'b00000100, 16'b00001000,
                  16'b00010000, 16'b00100000, 16'b01000000, 16'b10000000,
                  16'b00000001, 16'b00000010, 16'b00000100, 16'b00001000,
                  16'b00010000, 16'b00100000, 16'b01000000, 16'b10000000}),
    .sel(sel),
    .y(y)
  );
  reg [15:0] in;
  reg [3:0] sel;
  wire y;
  reg clk = 0;
  always #5 clk = ~clk;
   initial begin
    sel = 4'b0000;
    #10;

    sel = 4'b0101;
    #10;

    sel = 4'b1111;
    #10;
     $finish;
  end

  always @(posedge clk)
   begin
    $monitor("sel = %b in = %b y=%b", sel, in, y);
  end

endmodule
```

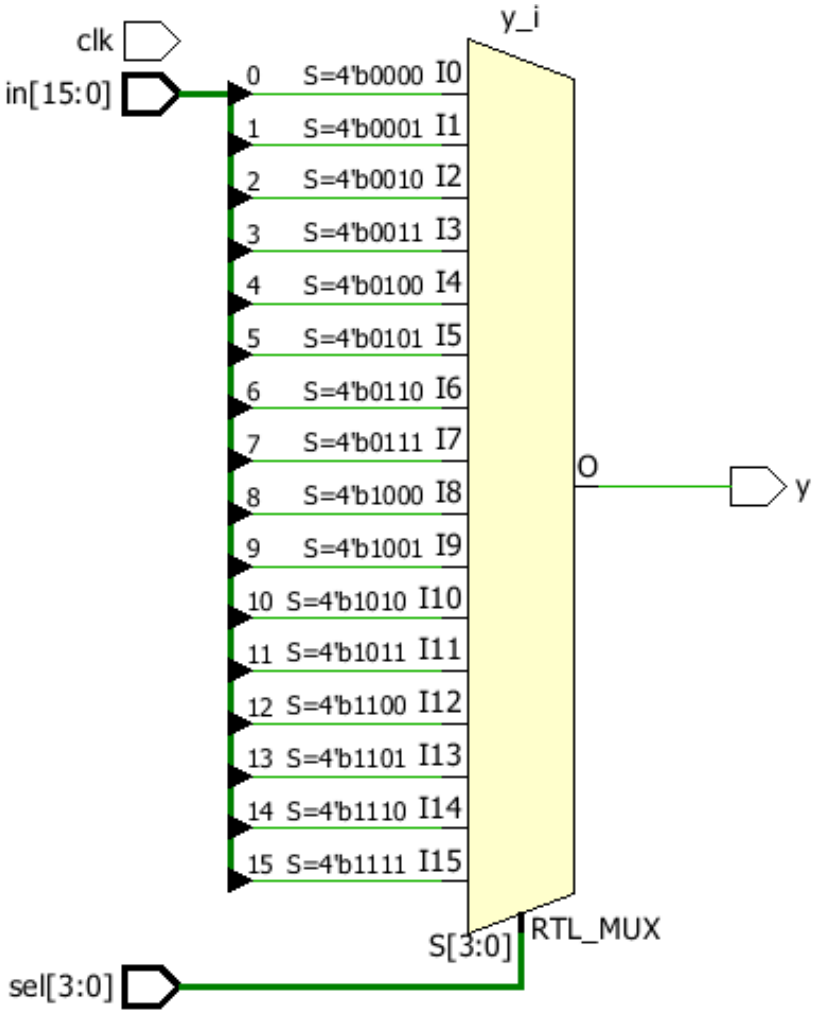
VERILOG CODE:

```
module N_MUX(
    input [15:0] in,
    input clk,
    input [3:0] sel,
    output reg y
    );

    always@(in or sel)
    begin
    case(sel)
    4'b0000 : y  = in[0];
    4'b0001 : y  = in[1];
    4'b0010 : y  = in[2];
    4'b0011 : y  = in[3];
    4'b0100 : y  = in[4];
    4'b0101 : y  = in[5];
    4'b0110 : y  = in[6];
    4'b0111 : y  = in[7];
    4'b1000 : y  = in[8];
    4'b1001 : y  = in[9];
    4'b1010 : y  = in[10];
    4'b1011 : y  = in[11];
    4'b1100 : y  = in[12];
    4'b1101 : y  = in[13];
    4'b1110 : y  = in[14];
    4'b1111 : y  = in[15];
    default : y  = 4'b0000;
    endcase
    end
endmodule
```

SIMULATION:



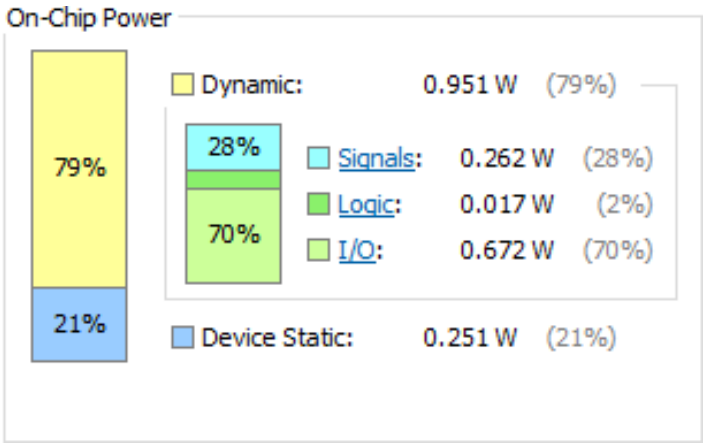
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.202 W**
Junction Temperature:	**26.7 ℃**
Thermal Margin:	58.3 ℃ (40.2 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-26: BCD TIMECOUNT

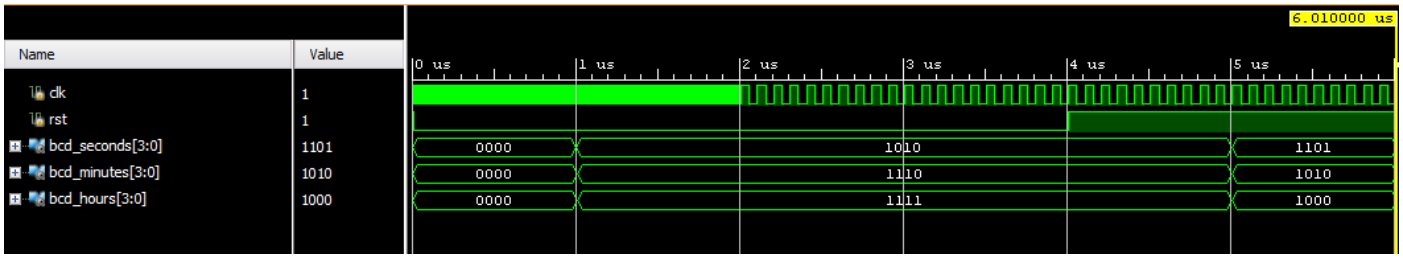
CODE FOR TESTBENCH:

```
module testbench;

reg clk;
reg rst;
wire [3:0] bcd_seconds;
wire [3:0] bcd_minutes;
wire [3:0] bcd_hours;


BCD_TIMECOUNT uut (
    .clk(clk),
    .rst(rst),
    .bcd_seconds(bcd_seconds),
    .bcd_minutes(bcd_minutes),
    .bcd_hours(bcd_hours)
);


always begin
    #5 clk = ~clk;
end

initial begin
    clk = 0;
    rst = 1;
    #10 rst = 0;
    #1000 $finish;

end
always @(posedge clk) begin
    $display("Time: %d%d:%d%d:%d%d", bcd_hours, bcd_hours, bcd_minutes, bcd_minutes, bcd_seconds, bcd_seconds);
end

endmodule
```

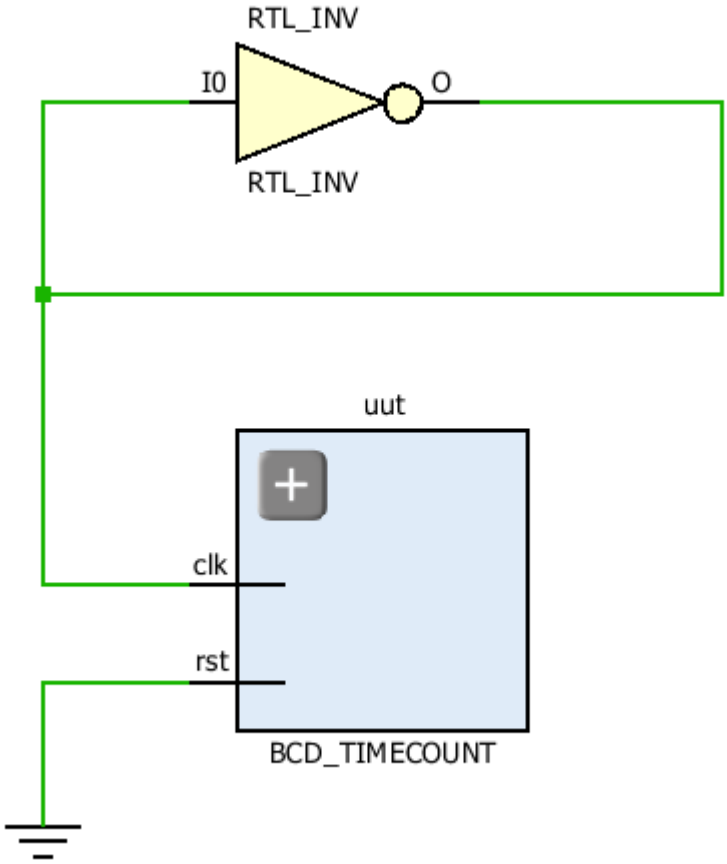
VERILOG CODE:

```
module BCD_TIMECOUNT (
    input wire clk,
    input wire rst,
    output wire [3:0] bcd_seconds,
    output wire [3:0] bcd_minutes,
    output wire [3:0] bcd_hours
);
reg [3:0] seconds_reg = 4'b0000;
reg [3:0] minutes_reg = 4'b0000;
reg [3:0] hours_reg   = 4'b0000;
reg [23:0] count = 0;
always @(posedge clk or posedge rst) begin
    if (rst) begin
        seconds_reg <= 4'b0000;
        minutes_reg <= 4'b0000;
        hours_reg   <= 4'b0000;
        count <= 0;
    end else if (count == 1000000) begin
        seconds_reg <= seconds_reg + 1;
        count <= 0;
    end else if (seconds_reg == 10) begin

        seconds_reg <= 4'b0000;
        minutes_reg <= minutes_reg + 1;
    end else if (minutes_reg == 10) begin

        minutes_reg <= 4'b0000;
        hours_reg   <= hours_reg + 1;
    end else begin

        count <= count + 1;
    end
end
assign bcd_seconds = seconds_reg;
assign bcd_minutes = minutes_reg;
assign bcd_hours   = hours_reg;
endmodule
```

SIMULATION:



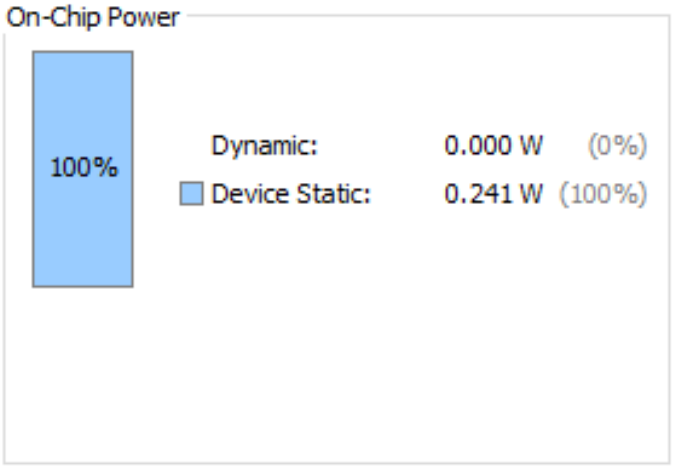
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-27: 3:1 MUX

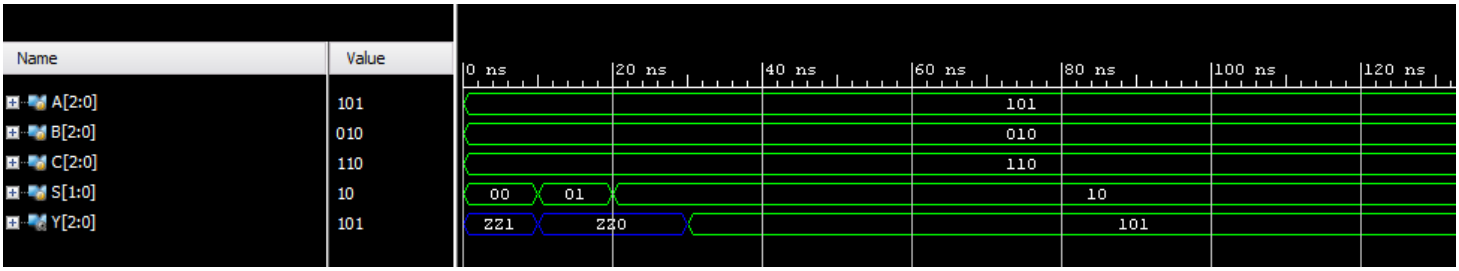
CODE FOR TESTBENCH:

```
module tb_MUX_3_1;
    reg [2:0] A;
    reg [2:0] B;
    reg [2:0] C;
    reg [1:0] S;
    wire [2:0] Y;
    MUX_3_1 uut (
        .A(A),
        .B(B),
        .C(C),
        .S(S),
        .Y(Y));
    initial begin
        $display("Testing 3-to-1 Multiplexer");
        A = 3'b101;
        B = 3'b010;
        C = 3'b110;
        S = 2'b00;
        #10;
        if (Y !== A)
            $display("Test case 1 failed");
        A = 3'b101;
        B = 3'b010;
        C = 3'b110;
        S = 2'b01;
        #10;
        if (Y !== B)
            $display("Test case 2 failed");
        A = 3'b101;
        B = 3'b010;
        C = 3'b110;
        S = 2'b10;
        #10;
        if (Y !== C)
            $display("Test case 3 failed");
 $finish;
    end
endmodule
```

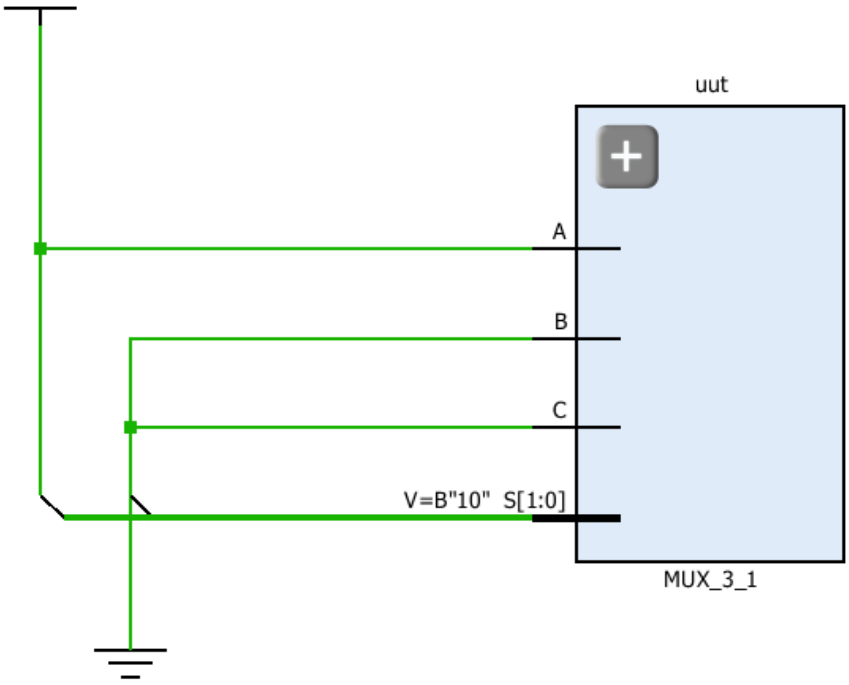
VERILOG CODE:

```
module MUX_3_1(
    input A,
    input B,
    input C,
    input [1:0] S,
    output reg Y
    );
    always@(A or B or C or S)
    begin
    if(S==2'b00)
    Y=A;
    else if (S==2'b01)
    Y=B;
    else if (S==2'b10)
    Y=C;
    else
    Y=C;
    end
endmodule
```

SIMULATION:



RTL SCHEMATIC:

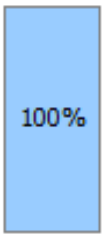


POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power



Dynamic:	0.000 W	(0%)
Device Static:	0.241 W	(100%)

CODE-28: BCD TO SEVEN SEGMENT DISPLAY

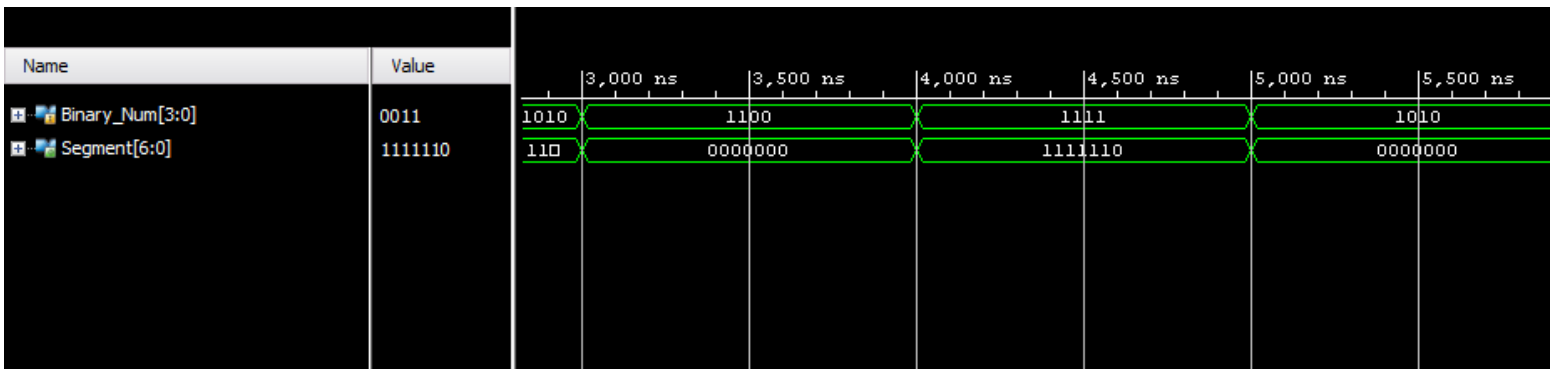
CODE FOR TESTBENCH:

```
module tb_BINARY_7_SEGMENT;
  reg [3:0] Binary_Num;
  wire [6:0] Segment;
  wire [6:0] anodes;
  wire cathode;

  BINARY_7_SEGMENT uut (
    .bcd_input(bcd_input),
    .seg_output(seg_output),
    .anodes(anodes),
    .cathode(cathode)
  );
  initial begin
    bcd_input = 4'b0000;
    $display("BCD Input | 7-Segment Output");
    $display("---------------------------------");
    for (int i = 0; i <= 9; i = i + 1) begin
      bcd_input = i;
      #10;
      $display("%b         | %b", bcd_input, seg_output);
    end
    $finish;
  end
  initial begin
    $monitor("Anodes: %b, Cathode: %b", anodes, cathode);
  end
endmodule
```

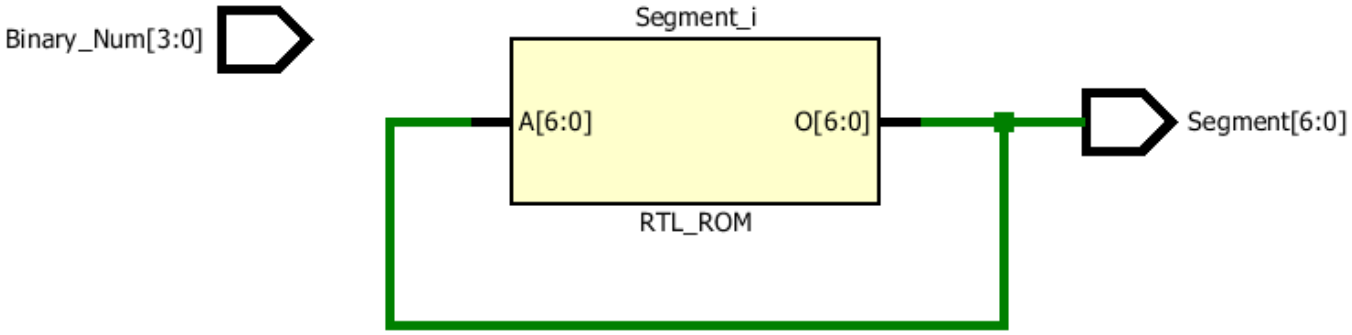
VERILOG CODE:

```
module BINARY_7_SEGMENT(
    input [3:0] Binary_Num,
    output reg [6:0] Segment
    );

    always@(Binary_Num)
    begin
    case(Segment)
     0: Segement = 7'b1111110;
     1: Segement = 7'b0110000;
     2: Segement = 7'b1101101;
     3: Segement = 7'b1111001;
     4: Segement = 7'b0110011;
     5: Segement = 7'b1011011;
     6: Segement = 7'b1011111;
     7: Segement = 7'b1110000;
     8: Segement = 7'b1111111;
     9: Segement = 7'b1111011;
     default : Segment = 7'b0000000;
     endcase
     end
endmodule
```

SIMULATION:



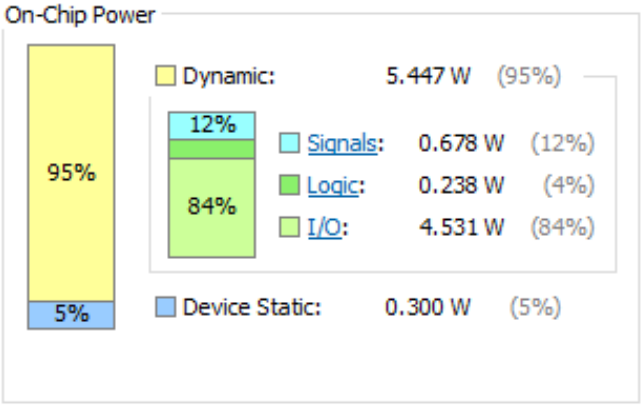
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**5.746 W**
Junction Temperature:	**33.0 ℃**
Thermal Margin:	52.0 ℃ (35.7 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-29: D LATCH USING 2:1 MUX

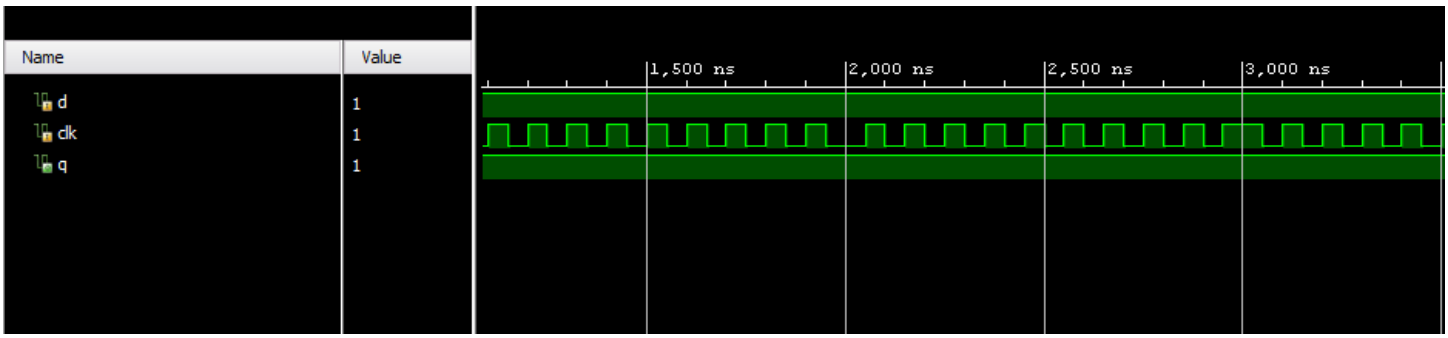
CODE FOR TESTBENCH:

```
module tb_D_LATCH;
  reg a;
  reg b;
  wire y;
  D_LATCH uut (
    .a(a),
    .b(b),
    .y(y)
  );
  initial begin
    a = 0;
    b = 1;
     $display("Time | a | b | y");
    $display("------------------");
    for (int i = 0; i <= 1; i = i + 1) begin
      a = i;
      #10;
      $display("%t | %b | %b | %b", $time, a, b, y);
    end
    a = 0;
    b = 1;
    #10;
    $display("%t | %b | %b | %b", $time, a, b, y);
    a = 0;
    #10;
    $display("%t | %b | %b | %b", $time, a, b, y);
    a = 1;
    b = 1;
    #10;
    $display("%t | %b | %b | %b", $time, a, b, y);
    $finish;
  end
endmodule
```

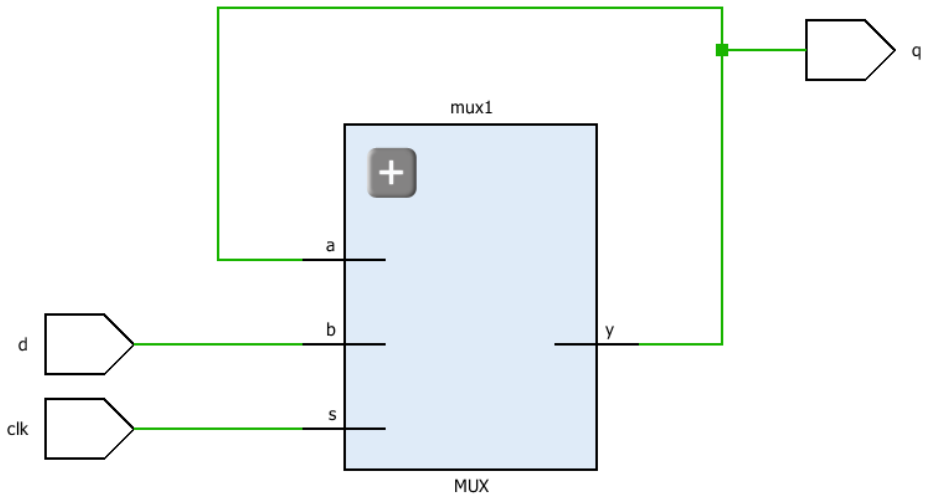
VERILOG CODE:

```
module MUX(
    input a,
    input b,
    input s,
    output reg y
    );
    always@(a or b or s)
    begin
    y= (~s&a) | (s&b);
    end
    endmodule
    module D_LATCH(
    input d,clk,
    output q
    );
    MUX mux1(.a(q),.b(d),.s(clk),.y(q));

endmodule
```

SIMULATION:



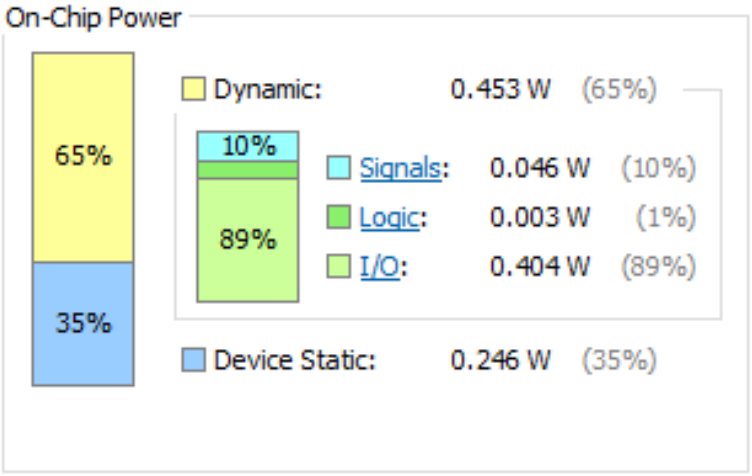
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.699 W**
Junction Temperature:	**26.0 ℃**
Thermal Margin:	59.0 ℃ (40.7 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-30: 8 BIT BARALLEL SHIFTER

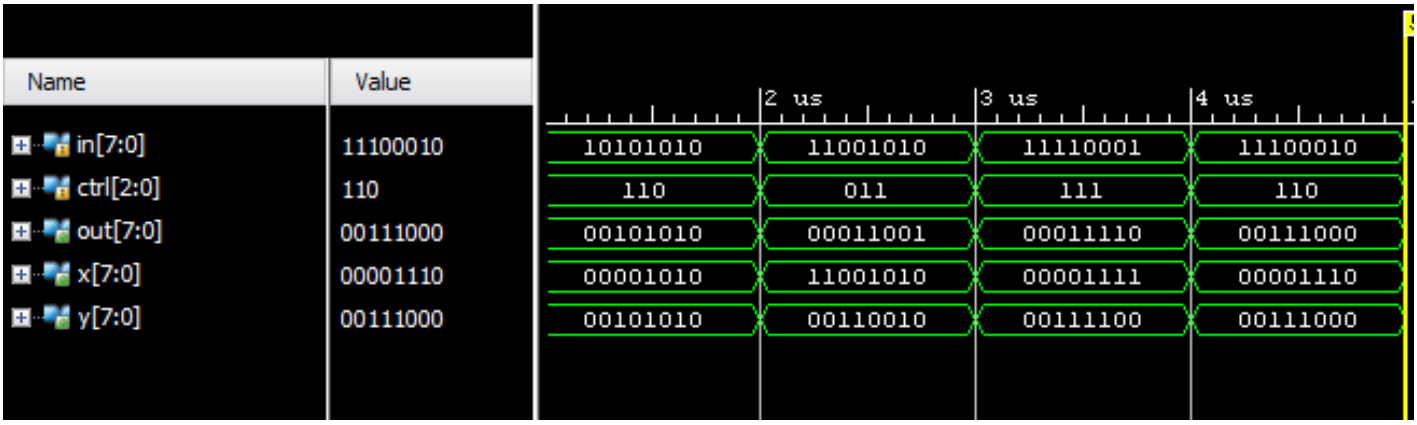
CODE FOR TESTBENCH:

```
module barrel_shifter_tb;
  parameter DATA_WIDTH = 8;
  reg [DATA_WIDTH-1:0] data_in;
  reg [2:0] shift_amount;
  reg enable;
  wire [DATA_WIDTH-1:0] data_out;
  barrel_shifter_8bit uut (
    .data_in(data_in),
    .shift_amount(shift_amount),
    .enable(enable),
    .data_out(data_out)
  );
  reg clk;
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    data_in = 8'b11011010;
    shift_amount = 3'b001;
    enable = 1;
    $display("Time\tData_In\tShift_Amount\tEnable\tData_Out");
    shift_amount = 3'b001;
    $monitor("%d\t%b\t%b\t%b\t%b", $time, data_in, shift_amount, enable, data_out);
    #10;
    shift_amount = 3'b010;
    $monitor("%d\t%b\t%b\t%b\t%b", $time, data_in, shift_amount, enable, data_out);
    #10;
    $finish;
  end
endmodule
```

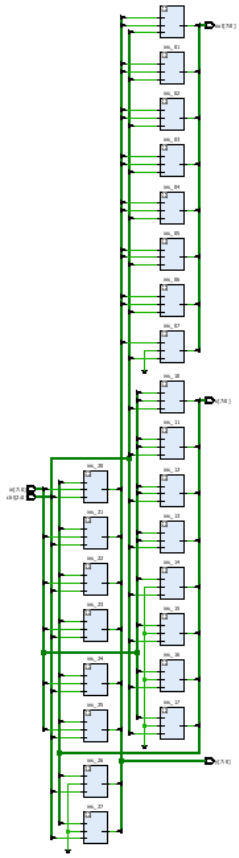
VERILOG CODE:

```
module BARALLEL_SHIFTER(input [7:0] in,
    input [2:0] ctrl,
    output [7:0] out,
    wire [7:0] x,y);
    //4-bit shift right
    mux2X1 ins_17 (.in0(in[7]),.in1(1'b0),.sel(ctrl[2]),.out(x[7]));
    mux2X1 ins_16 (.in0(in[6]),.in1(1'b0),.sel(ctrl[2]),.out(x[6]));
    mux2X1 ins_15 (.in0(in[5]),.in1(1'b0),.sel(ctrl[2]),.out(x[5]));
    mux2X1 ins_14 (.in0(in[4]),.in1(1'b0),.sel(ctrl[2]),.out(x[4]));
    mux2X1 ins_13 (.in0(in[3]),.in1(in[7]),.sel(ctrl[2]),.out(x[3]));
    mux2X1 ins_12 (.in0(in[2]),.in1(in[6]),.sel(ctrl[2]),.out(x[2]));
    mux2X1 ins_11 (.in0(in[1]),.in1(in[5]),.sel(ctrl[2]),.out(x[1]));
    mux2X1 ins_10 (.in0(in[0]),.in1(in[4]),.sel(ctrl[2]),.out(x[0]));
    //2-bit shift right
    mux2X1 ins_27 (.in0(x[7]),.in1(1'b0),.sel(ctrl[1]),.out(y[7]));
    mux2X1 ins_26 (.in0(x[6]),.in1(1'b0),.sel(ctrl[1]),.out(y[6]));
    mux2X1 ins_25 (.in0(x[5]),.in1(in[7]),.sel(ctrl[1]),.out(y[5]));
    mux2X1 ins_24 (.in0(x[4]),.in1(in[6]),.sel(ctrl[1]),.out(y[4]));
    mux2X1 ins_23 (.in0(x[3]),.in1(in[5]),.sel(ctrl[1]),.out(y[3]));
    mux2X1 ins_22 (.in0(x[2]),.in1(in[4]),.sel(ctrl[1]),.out(y[2]));
    mux2X1 ins_21 (.in0(x[1]),.in1(in[3]),.sel(ctrl[1]),.out(y[1]));
    mux2X1 ins_20 (.in0(x[0]),.in1(in[2]),.sel(ctrl[1]),.out(y[0]));
    //1-bit shift register
    mux2X1 ins_07 (.in0(y[7]),.in1(1'b0),.sel(ctrl[0]),.out(out[7]));
    mux2X1 ins_06 (.in0(y[6]),.in1(y[7]),.sel(ctrl[0]),.out(out[6]));
    mux2X1 ins_05 (.in0(y[5]),.in1(y[6]),.sel(ctrl[0]),.out(out[5]));
    mux2X1 ins_04 (.in0(y[4]),.in1(y[5]),.sel(ctrl[0]),.out(out[4]));
    mux2X1 ins_03 (.in0(y[3]),.in1(y[4]),.sel(ctrl[0]),.out(out[3]));
    mux2X1 ins_02 (.in0(y[2]),.in1(y[3]),.sel(ctrl[0]),.out(out[2]));
    mux2X1 ins_01 (.in0(y[1]),.in1(y[2]),.sel(ctrl[0]),.out(out[1]));
    mux2X1 ins_00 (.in0(y[0]),.in1(y[1]),.sel(ctrl[0]),.out(out[0]));
endmodule
module mux2X1(in0,in1,sel,out);
input in0,in1;
input sel;
output out;
assign out=(sel)?in1:in0;
endmodule
```

SIMULATION:



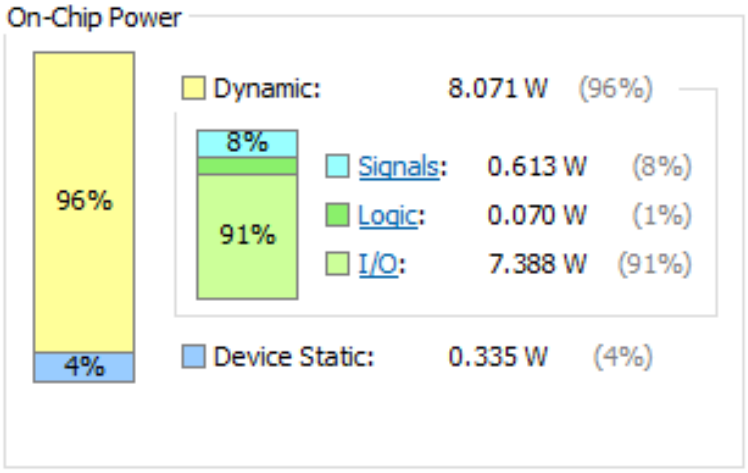
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**8.406 W**
Junction Temperature:	**36.8 ℃**
Thermal Margin:	48.2 ℃ (33.0 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-31: 1-BIT COMPARATOR USING 4:1 MUX

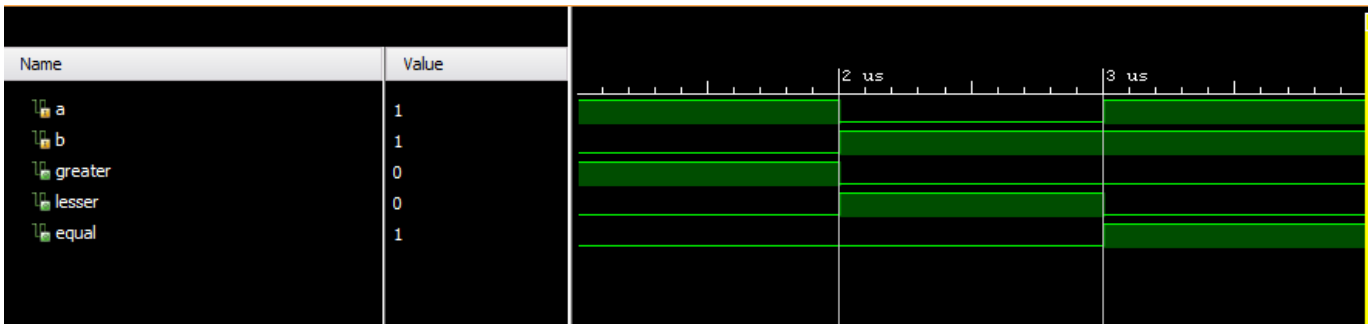
CODE FOR TESTBENCH:

```
module comparator_4bit_tb;
  parameter DATA_WIDTH = 4;
  reg [DATA_WIDTH-1:0] data_A;
  reg [DATA_WIDTH-1:0] data_B;
  reg [1:0] select;
  wire result;
  comparator_4bit uut (
    .data_A(data_A),
    .data_B(data_B),
    .select(select),
    .result(result)
  );
  initial begin
    data_A = 4'b0101;
    data_B = 4'b1010;
    select = 2'b00;
    #10;
    $display("Test case 1: data_A = %b, data_B = %b, select = %b, result = %b", data_A, data_B, select, result);
    data_A = 4'b1111;
    data_B = 4'b1111;
    select = 2'b01;
    #10;
    $display("Test case 2: data_A = %b, data_B = %b, select = %b, result = %b", data_A, data_B, select, result);
    $finish;
  end
endmodule
```

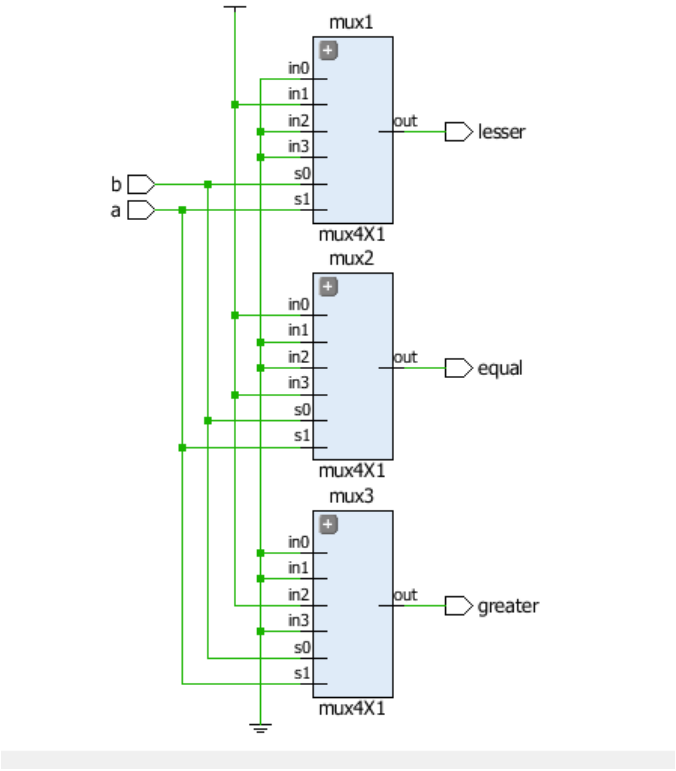
VERILOG CODE:

```
module mux4X1(
input in0,in1,in2,in3,s1,s0,
output out
);
assign out= s1 ? (s0 ? in3 : in2) : (s0 ? in1 : in0);
endmodule

module COMPARATOR_4_BIT(
input a,b,
output greater,lesser,equal
);
mux4X1 mux1(1'b0,1'b1,1'b0,1'b0,a,b,lesser);
mux4X1 mux2(1'b1,1'b0,1'b0,1'b1,a,b,equal);
mux4X1 mux3(1'b0,1'b0,1'b1,1'b0,a,b,greater);
endmodule
```

SIMULATION:



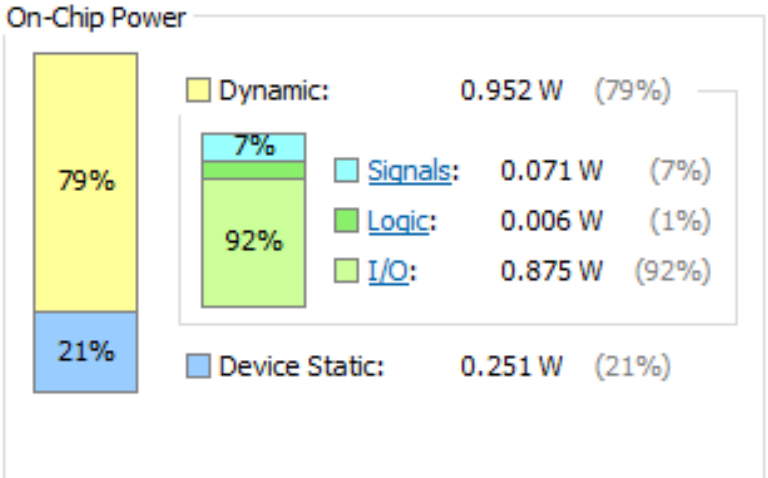
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.203 W**
Junction Temperature:	**26.7 °C**
Thermal Margin:	58.3 °C (40.2 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-32: LOGICAL, ALGEBRAIC AND ROTATE SHIFT OPERATIONS

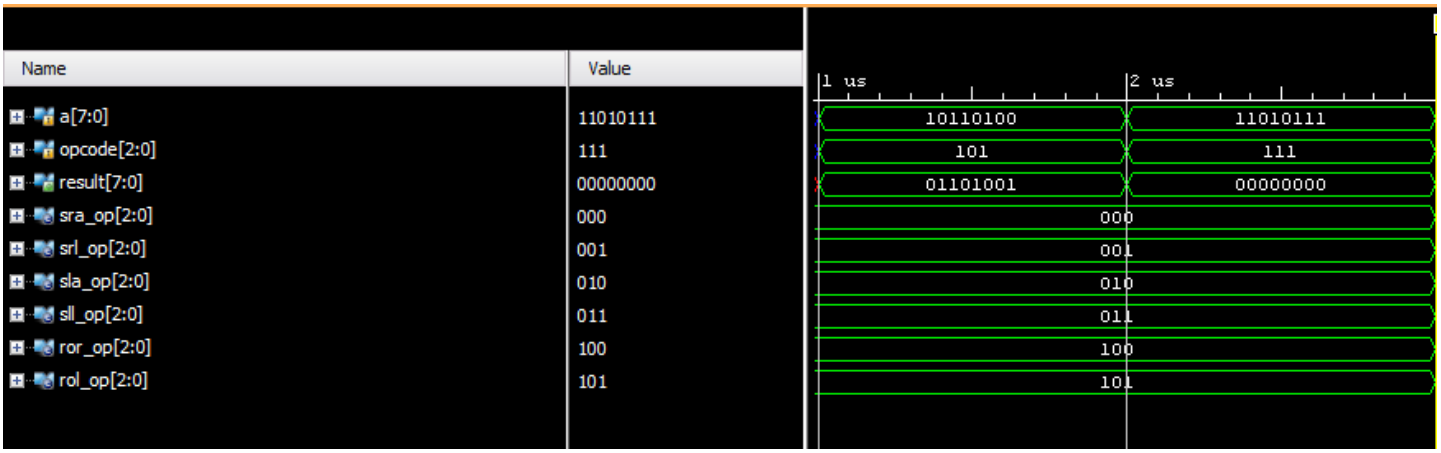
CODE FOR TESTBENCH:

```
module shift_operations_tb;
  reg [3:0] data_in;
  reg [1:0] shift_type;
  wire [3:0] data_out;
  shift_operations uut (
    .data_in(data_in),
    .shift_type(shift_type),
    .data_out(data_out)
  );
  initial begin
    data_in = 4'b1100;
    shift_type = 2'b00;
    #10;
    $display("Logical Right Shift: data_in = %b, data_out = %b", data_in, data_out);

    data_in = 4'b1101;
    shift_type = 2'b01;
    #10;
    $display("Arithmetic Right Shift: data_in = %b, data_out = %b", data_in, data_out);
    data_in = 4'b1100;
    shift_type = 2'b10;
    #10;
    $display("Rotate Left: data_in = %b, data_out = %b", data_in, data_out);
    $finish;
  end

endmodule
```

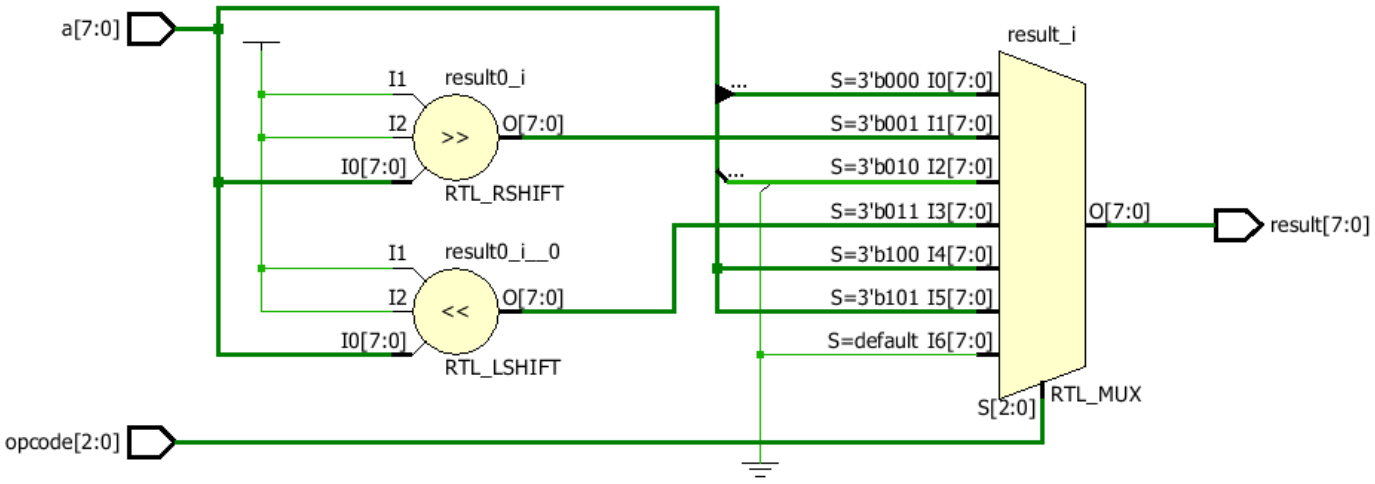
VERILOG CODE:

```
module SHIFT_ROTATE(
    input [7:0] a,
    input [2:0] opcode,
    output [7:0] result
    );


    paramtere sra_op = 3'b000,
    srl_op = 3'b001,
    sla_op = 3'b010,
    sll_op = 3'b011,
    ror_op = 3'b100,
    rol_op = 3'b101;

    always@(a or opcode)
    begin
    case(opcode)
    srl_op : result = {a[7], a[7], a[6], a[5], a[4], a[3], a[2], a[1]};
    srl_op : result = a>>1;
    sla_op : result = {a[6], a[5], a[4], a[3], a[2], a[1], a[0], 1'b0};
    sll_op : result = a<<1;
    ror_op : result = {a[0], a[7], a[6], a[5], a[4], a[3], a[2], a[1]};
    rol_op : result = {a[6], a[5], a[4], a[3], a[2], a[1], a[0], a[7]};
    default : result = 0;
    endcase
    end
endmodule
```

SIMULATION:



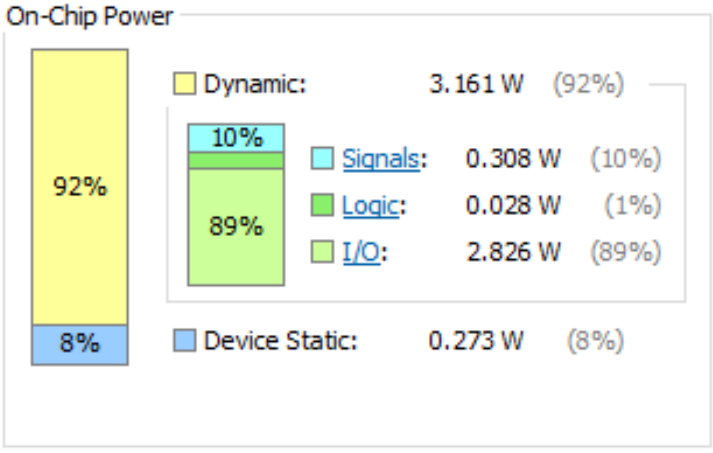
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**3.435 W**
Junction Temperature:	**29.8 °C**
Thermal Margin:	55.2 °C (37.9 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-33: ARITHMETIC LOGICAL OPERATIONS (ALU)

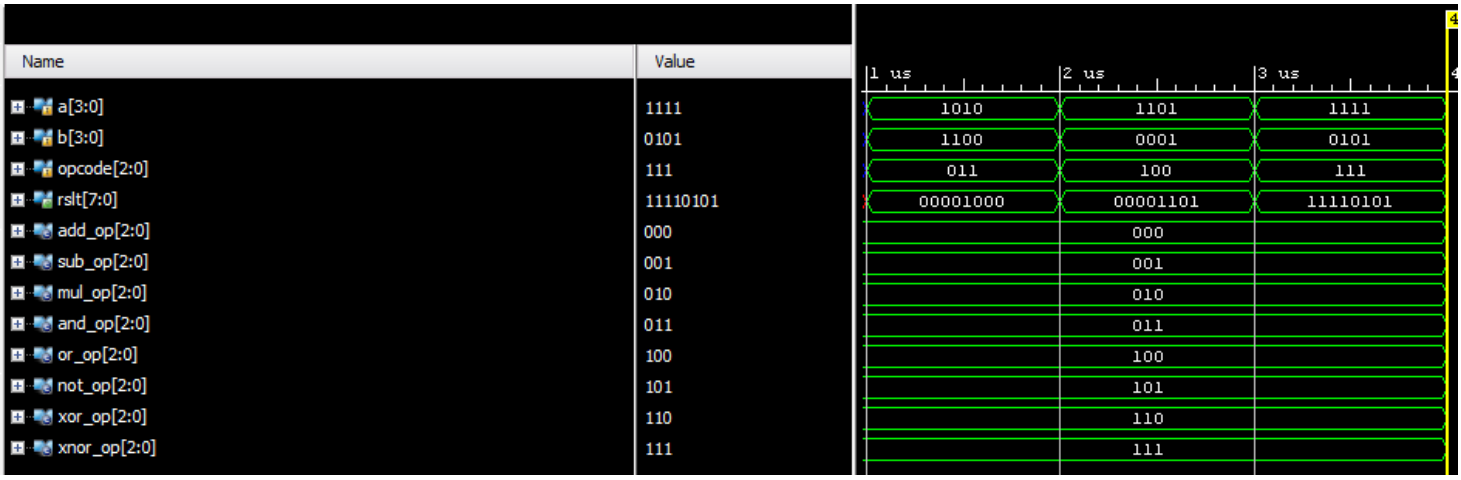
CODE FOR TESTBENCH:

```
module alu_tb;
  reg [3:0] operandA, operandB;
  reg [2:0] alu_ctrl;
  wire [3:0] result;
  alu my_alu (
    .A(operandA),
    .B(operandB),
    .ALUctrl(alu_ctrl),
    .Y(result)
  );
  reg clk;
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    operandA = 4'b0010;
    operandB = 4'b1101;
    $display("Starting ALU Testbench");
    alu_ctrl = 3'b000;
    #10;
    $display("ALU Operation: ADD");
    $display("Operand A: %b", operandA);
    $display("Operand B: %b", operandB);
    $display("Result: %b", result);
    alu_ctrl = 3'b001;
    #10;
    $display("ALU Operation: SUB");
    $display("Operand A: %b", operandA);
    $display("Operand B: %b", operandB);
    $display("Result: %b", result);
    $display("ALU Testbench finished");
    $finish;
  end
endmodule
```

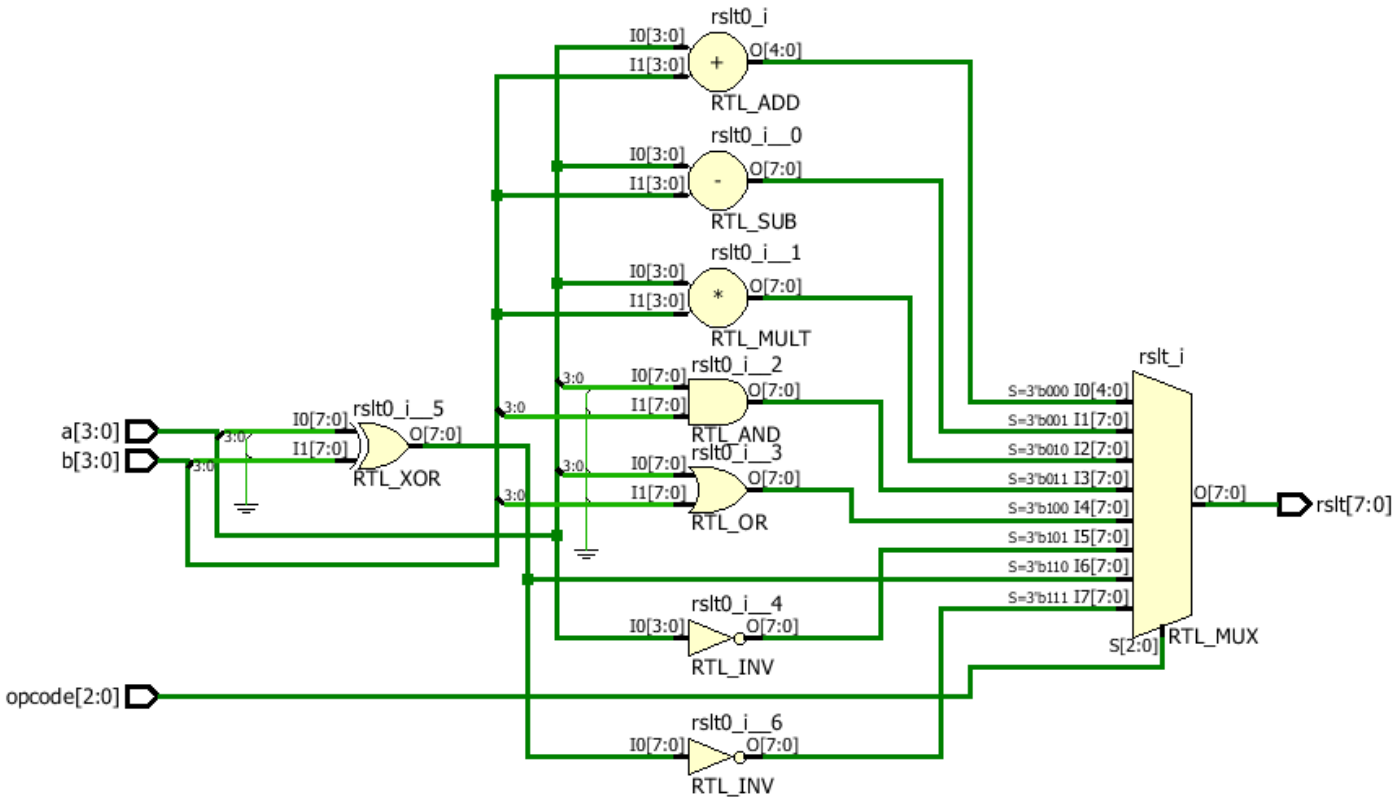
VERILOG CODE:

```
module ALU(
    input [3:0] a,
    input [3:0] b,
    input [2:0] opcode,
    output reg [7:0] rslt
    );
    parameter add_op = 3'b000,
    sub_op = 3'b001,
    mul_op = 3'b010,
    and_op = 3'b011,
    or_op = 3'b100,
    not_op = 3'b101,
    xor_op = 3'b110,
    xnor_op = 3'b111;

    always@(a or b or opcode)
    begin
    case (opcode)
    add_op : rslt = a + b;
    sub_op : rslt = a - b;
    mul_op : rslt = a * b;
    and_op : rslt = a & b;
    or_op : rslt = a | b;
    not_op : rslt = ~a;
    xor_op : rslt = a ^ b;
    xnor_op : rslt = ~(a ^ b);
    endcase
    end
endmodule
```

SIMULATION:



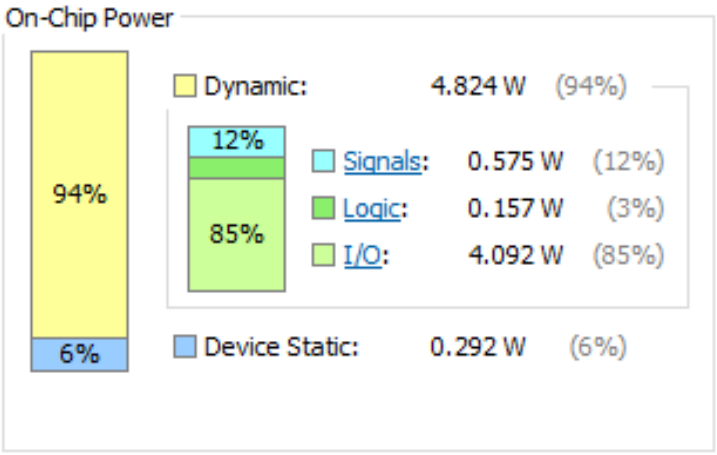
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**5.116 W**
Junction Temperature:	**32.2 ℃**
Thermal Margin:	52.8 ℃ (36.3 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-34: 4-BIT ASYNCHRONOUS DOWN COUNTER

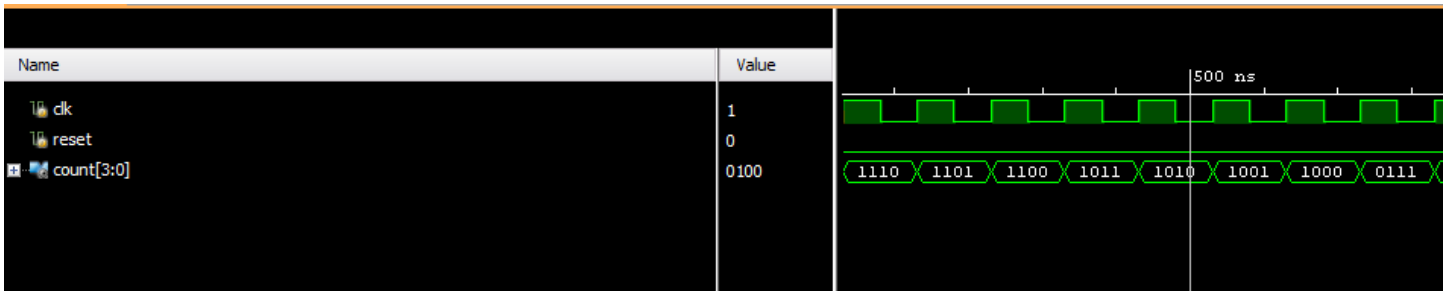
CODE FOR TESTBENCH:

```
module testbench;
 reg clk;
    reg reset;
    wire [3:0] count;

    async_down_counter_4bit counter (
        .clk(clk),
        .reset(reset),
        .count(count)
    );
    always begin
        #5 clk = ~clk;
    end
    initial begin
        reset = 1;
        #10 reset = 0;
    end
    initial begin
        $dumpfile("counter.vcd");
        $dumpvars(0, testbench);
        $display("Time\tCount");
        $monitor("%d\t%b", $time, count);
        #30 $finish;
    end

endmodule
```

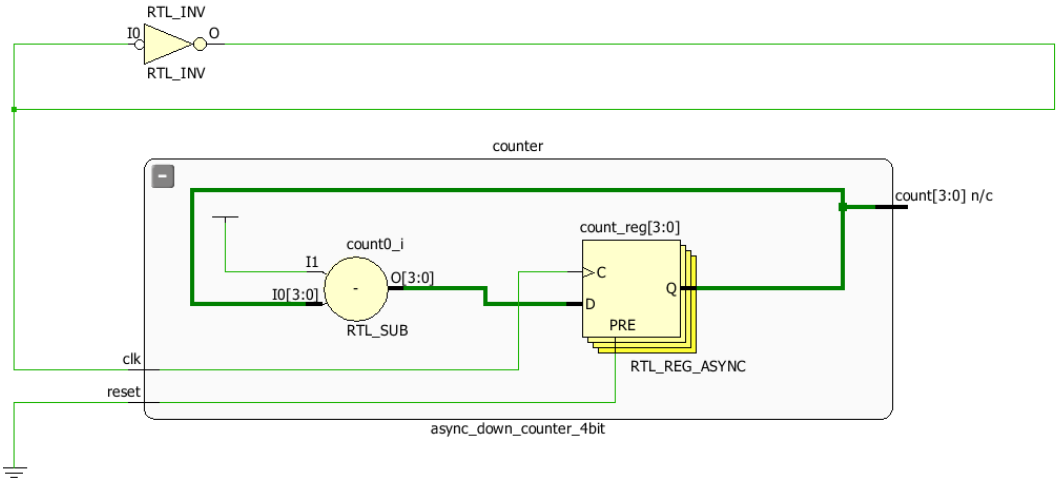
VERILOG CODE:

```
module async_down_counter_4bit (
    input wire clk,
    input wire reset,
    output reg [3:0] count
);

always @(posedge clk or posedge reset)
begin
    if (reset)
        count <= 4'b1111; // Reset the counter to 1111
    else
        count <= count - 1; // Decrement the counter by 1
end
endmodule
module testbench;
    reg clk;
    reg reset;
    wire [3:0] count;
    async_down_counter_4bit counter (
        .clk(clk),
        .reset(reset),
        .count(count)
    );
    always begin
        #5 clk = ~clk; // Toggle the clock every 5 time units
    end
    initial begin
        reset = 1;
        #10 reset = 0; // Deassert reset after 10 time units
    end
    initial begin
        $dumpfile("counter.vcd");
        $dumpvars(0, testbench);
        $display("Time\tCount");
        $monitor("%d\t%b", $time, count);
        #30 $finish;
    end
endmodule
```

SIMULATION:



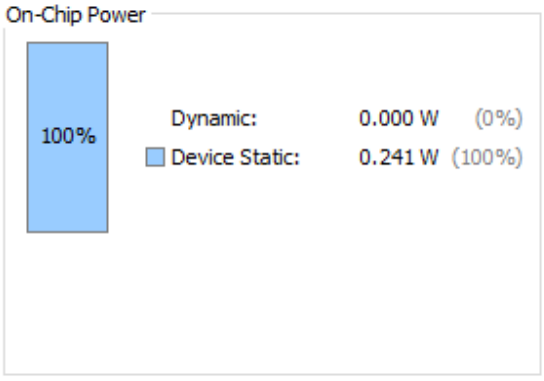
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-35: MOD-N UP DOWN COUNTER

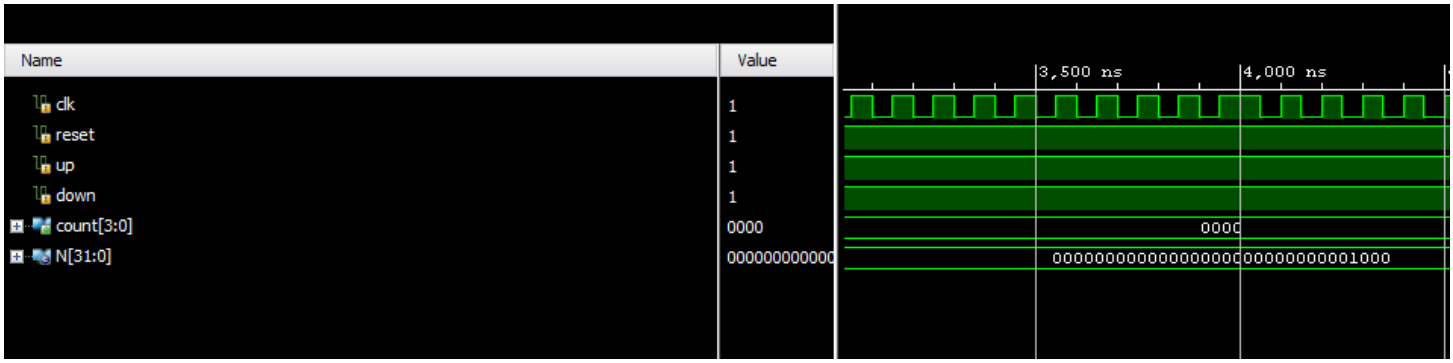
CODE FOR TESTBENCH:

```
module testbench;
    reg clk;
    reg reset;
    reg up;
    reg down;
    wire [2:0] count; /
    mod_n_updown_counter counter (
        .clk(clk),
        .reset(reset),
        .up(up),
        .down(down),
        .count(count)
    );
    always begin
        #5 clk = ~clk;
    end
    initial begin
        reset = 1;
        #10 reset = 0; // Deassert reset after 10 time units
    end
    initial begin
        up = 1;
        down = 0;
        #20 up = 0;
        #20 down = 1;
        #20 up = 1;
        #20 down = 0;
        #20 $finish;
    end
    initial begin
        $dumpfile("counter.vcd");
        $dumpvars(0, testbench);
        $display("Time\tCount");
        $monitor("%d\t%h", $time, count);
    end
endmodule
```

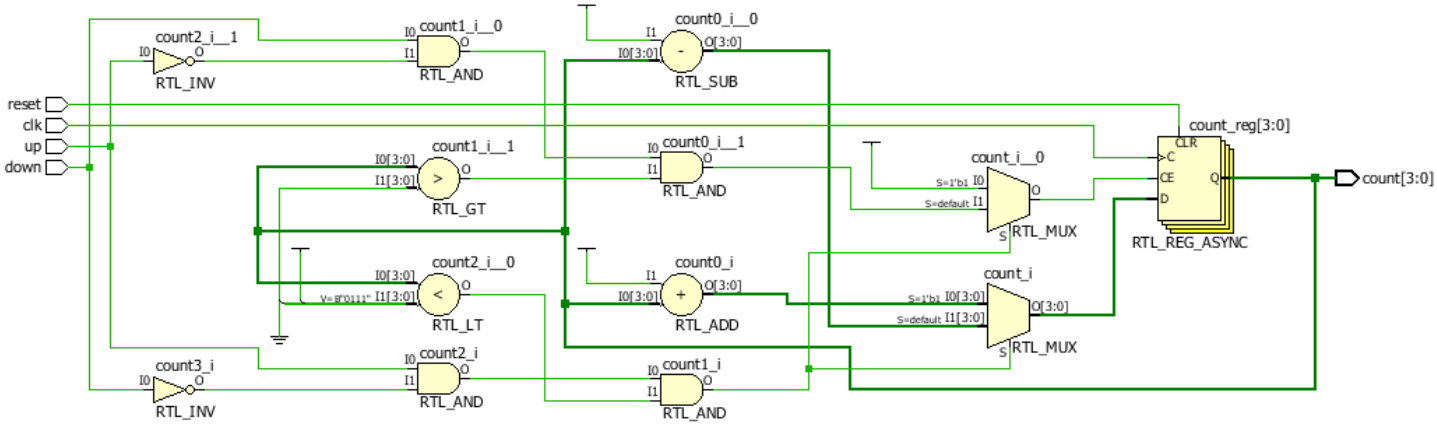
VERILOG CODE:

```
module mod_n_updown_counter (
    input wire clk,
    input wire reset,
    input wire up,
    input wire down,
    output reg [3:0] count // Assuming 4-bit counter
);

parameter N = 8; // Set N to the desired modulo value (e.g., 8)

always @(posedge clk or posedge reset)
begin
    if (reset)
        count <= 4'b0000; // Reset the counter to 0
    else if (up && !down && count < N - 1)
        count <= count + 1; // Count up
    else if (down && !up && count > 0)
        count <= count - 1; // Count down
end

endmodule
```

SIMULATION:



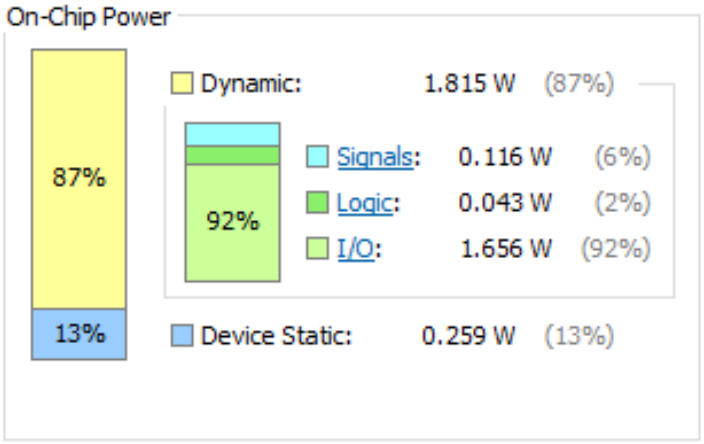
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.074 W**
Junction Temperature:	**27.9 ℃**
Thermal Margin:	57.1 ℃ (39.3 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-36: UNIVERSAL BINARY COUNTER

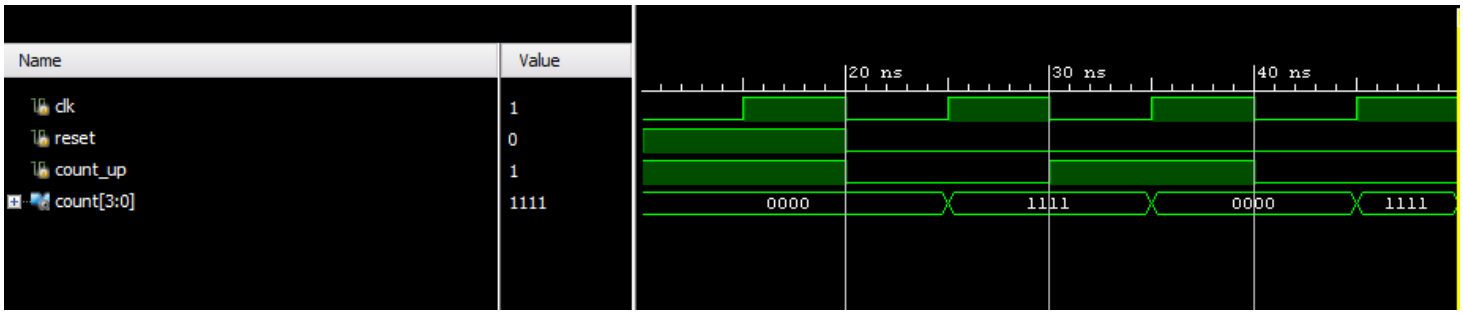
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg reset;
  reg count_up;
  wire [3:0] count;

  universal_binary_counter uut (
    .clk(clk),
    .reset(reset),
    .count_up(count_up),
    .count(count)
  );
  always begin
    #5 clk = ~clk;
  end

  initial begin
    clk = 0;
    reset = 0;
    count_up = 1;
    #10 reset = 1;
    #10 reset = 0;
    count_up = 0;
    #10;
    count_up = 1;
    #10;
    count_up = 0;
    #10;
    count_up = 1;
    $finish;
  end
  always @(posedge clk) begin
    $display("Count: %b", count);
  end
endmodule
```

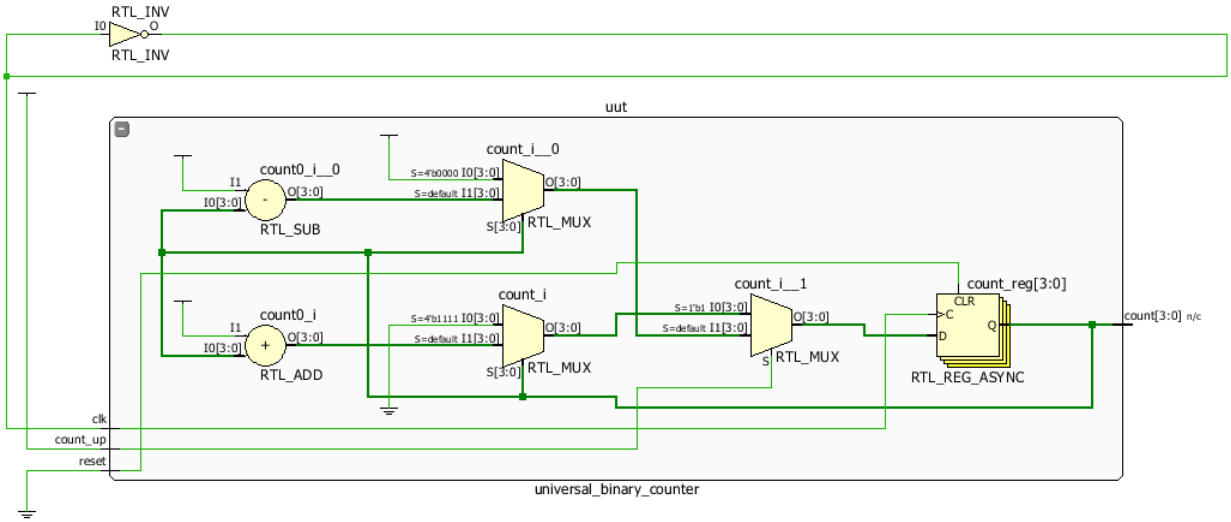
VERILOG CODE:

```
module universal_binary_counter (
  input wire clk,
  input wire reset,
  input wire count_up,
  output reg [3:0] count
);

always @(posedge clk or posedge reset) begin
  if (reset) begin
    count <= 4'b0000;
  end else begin
    if (count_up) begin
      if (count == 4'b1111) begin
        count <= 4'b0000;
      end else begin
        count <= count + 1;
      end
    end else begin
      if (count == 4'b0000) begin
        count <= 4'b1111;
      end else begin
        count <= count - 1;
      end
    end
  end
end

endmodule
```

SIMULATION:



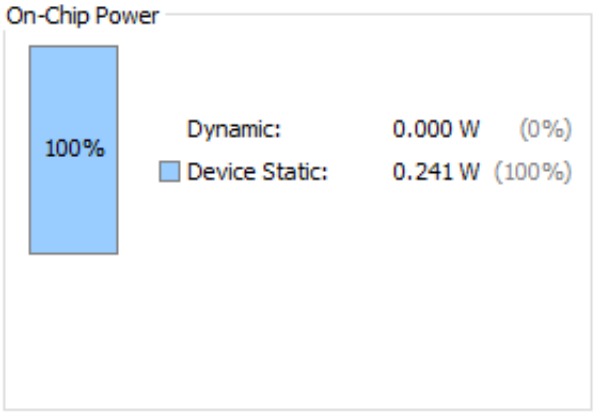
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-37: UNIVERSAL SHIFT REGISTER

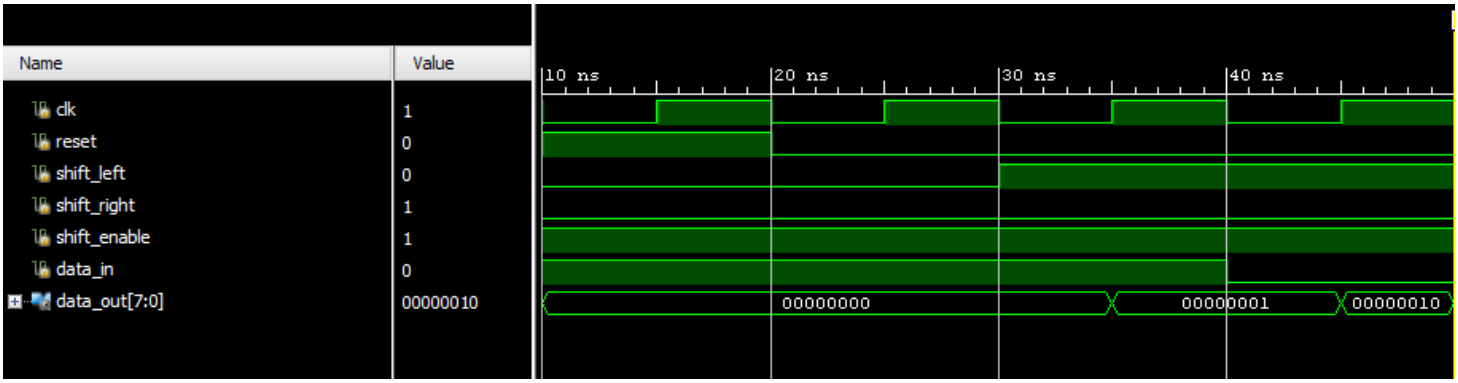
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg reset;
  reg shift_left;
  reg shift_right;
  reg shift_enable;
  reg data_in;
  wire [7:0] data_out;
  universal_shift_register uut (.clk(clk),.reset(reset),
    .shift_left(shift_left),
    .shift_right(shift_right),
    .shift_enable(shift_enable),
    .data_in(data_in),
    .data_out(data_out));
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    reset = 0;
    shift_left = 0;
    shift_right = 0;
    shift_enable = 1;
    data_in = 8'b11011011;
    #10 reset = 1;
    #10 reset = 0;
    #10 shift_left = 1;
    #10 shift_right = 0;
    data_in = 8'b00110010;
    #10 shift_left = 0;
    shift_right = 1;
    data_in = 8'b10101010;
    $finish;
  end
  always @(posedge clk) begin
    $display("Data Out: %b", data_out);
  end
endmodule
```

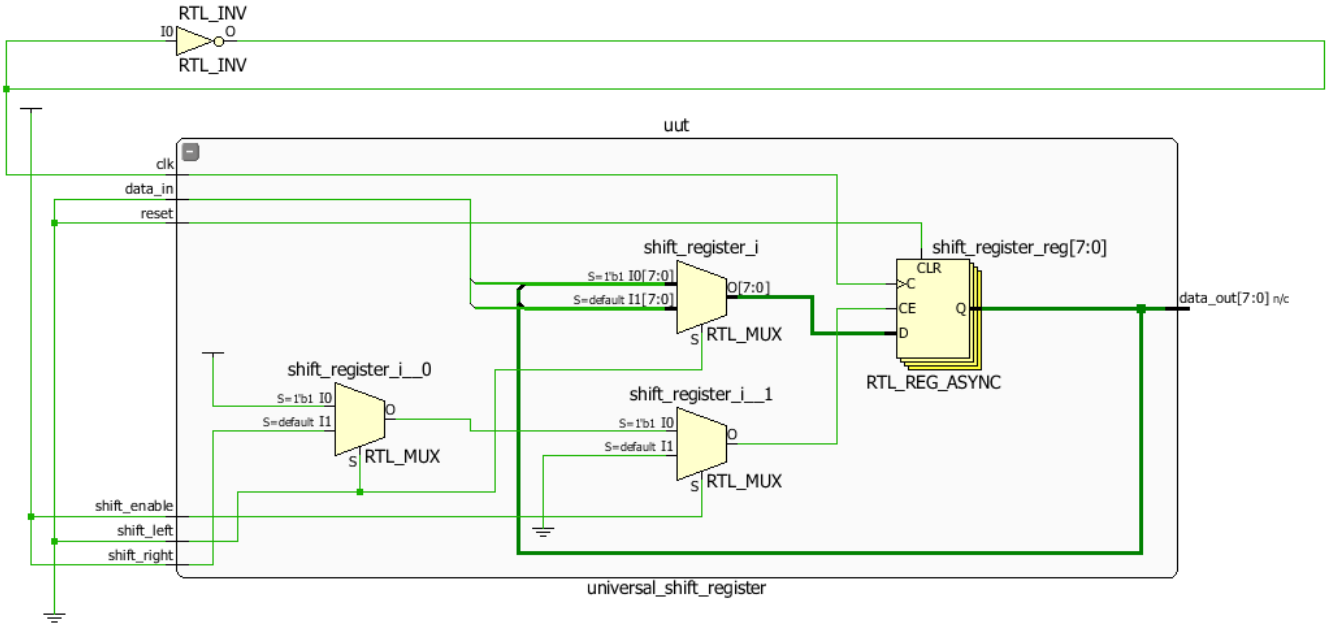
VERILOG CODE:

```
module universal_shift_register (
  input wire clk,
  input wire reset,
  input wire shift_left,
  input wire shift_right,
  input wire shift_enable,
  input wire data_in,
  output wire [7:0] data_out
);

reg [7:0] shift_register;

always @(posedge clk or posedge reset) begin
  if (reset) begin
    shift_register <= 8'b00000000;
  end else if (shift_enable) begin
    if (shift_left) begin
      shift_register <= {shift_register[6:0], data_in};
    end else if (shift_right) begin
      shift_register <= {data_in, shift_register[7:1]};
    end
  end
end
```

SIMULATION:



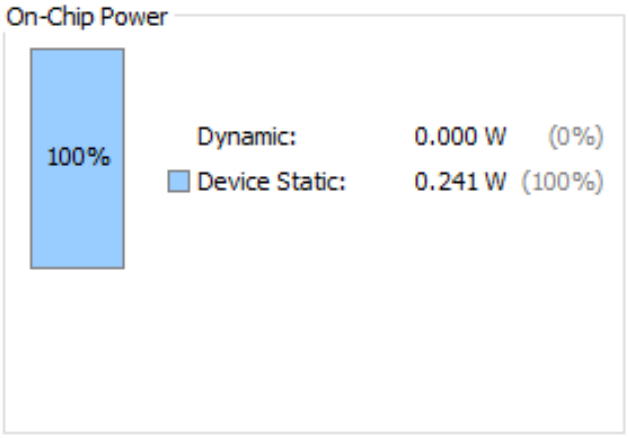
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-38: CN (CHANGE-NO CHANGE FLIPFLOP) USING 2:1 MUX

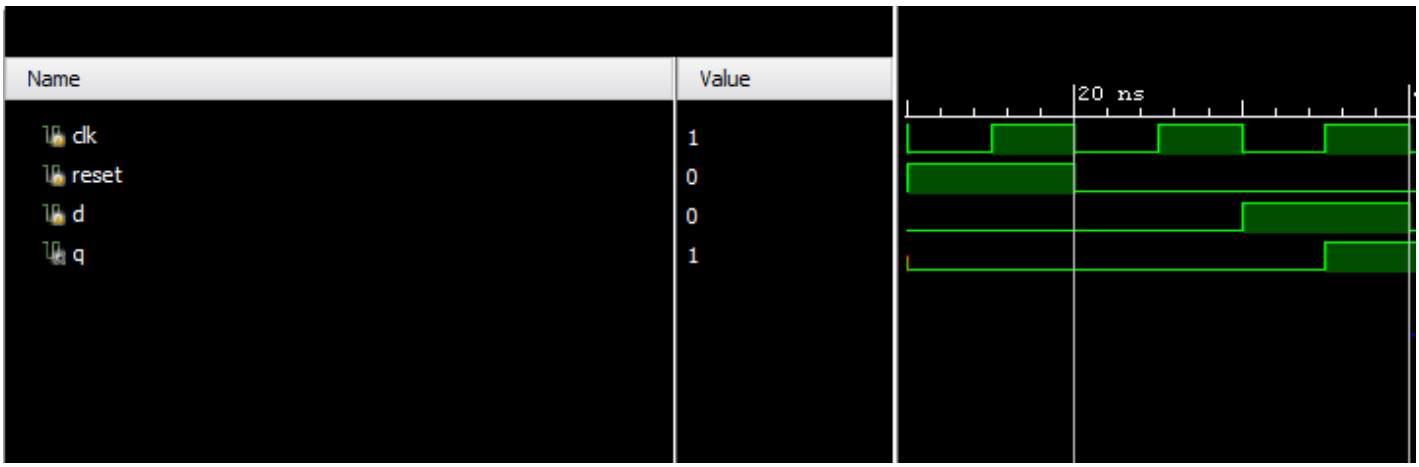
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg reset;
  reg d;
  wire q;
  CN_FlipFlop uut (
    .clk(clk),
    .reset(reset),
    .d(d),
    .q(q) );
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    reset = 0;
    d = 0;
    #10 reset = 1;
    #10 reset = 0;
    #10 d = 1;
    #10 d = 0;
    #10 d = 1;
    #10 d = 1;
    #10 d = 0;
    $finish;
  end
  always @(posedge clk) begin
    $display("Q = %b", q);
  end
endmodule
```

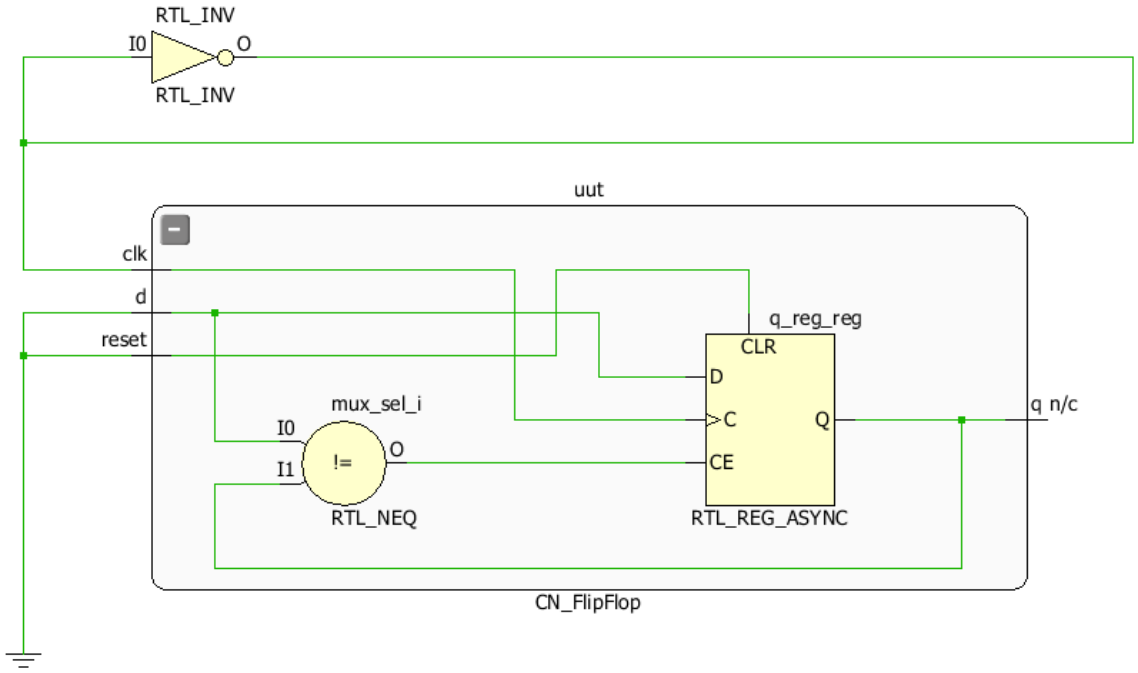
VERILOG CODE:

```
module CN_FlipFlop (
  input wire clk,
  input wire reset,
  input wire d,
  output wire q
);

wire mux_sel;
reg q_reg;

assign mux_sel = (d != q_reg);

always @(posedge clk, posedge reset) begin
  if (reset) begin
    q_reg <= 1'b0;
  end else begin
    if (mux_sel) begin
      q_reg <= d;
    end
  end
end

assign q = q_reg;

endmodule
```

SIMULATION:



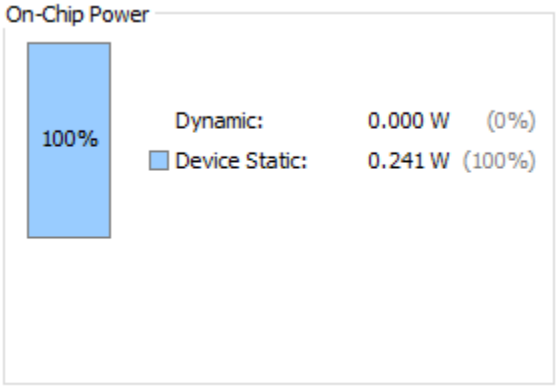
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-39: FREQUENCY DIVIDER BY ODD NUMBER

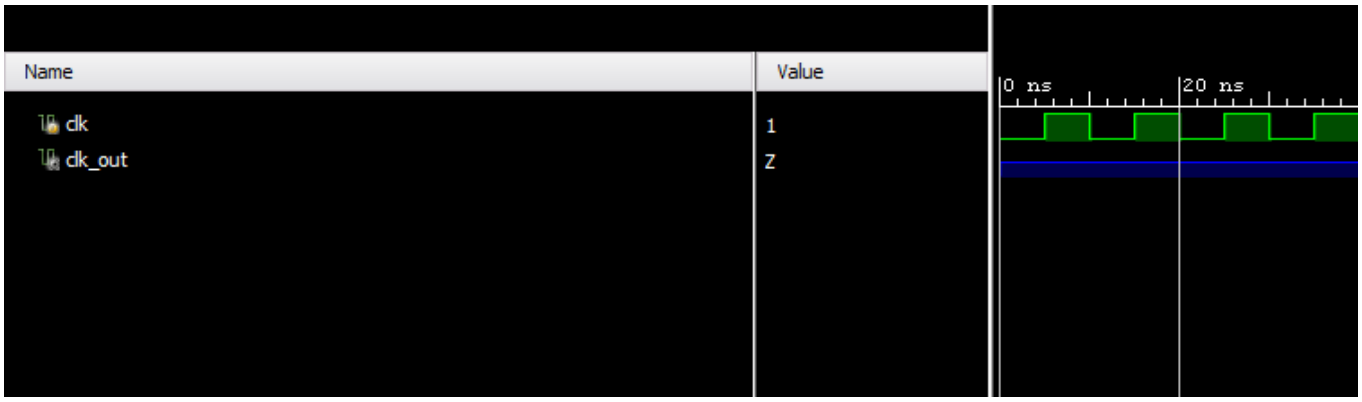
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  wire clk_out;

  frequency_divider_odd uut (
    .clk(clk),
    .clk_out(clk_out)
  );

  always begin
    #5 clk = ~clk;
  end

  initial begin
    clk = 0;

    #100;
    $finish;
  end

  always @(posedge clk_out) begin
    $display("Clock Out toggled at time %t", $realtime);
  end

endmodule
```

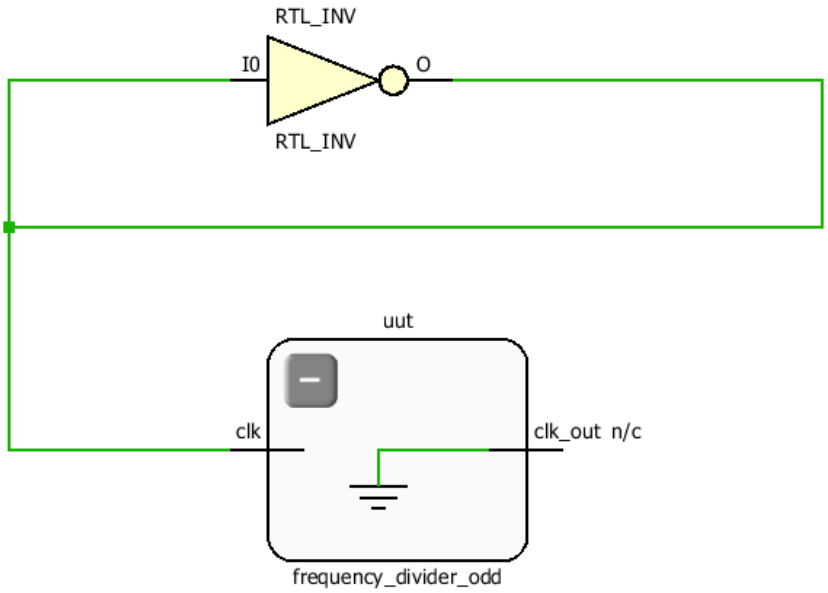
VERILOG CODE:

```
module frequency_divider_odd (
  input wire clk,
  output wire clk_out
);

reg [2:0] counter;

always @(posedge clk) begin
  if (counter == 3'b100) begin
    counter <= 3'b000;
//    clk_out <= ~clk_out;
  end else begin
    counter <= counter + 1;
  end
end

endmodule
```

SIMULATION:



RTL SCHEMATIC:

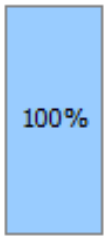


POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power



Dynamic:	0.000 W	(0%)
Device Static:	0.241 W	(100%)

CODE-40: GREATEST COMMON DIVISOR USING BEHAVIOURAL MODELLING

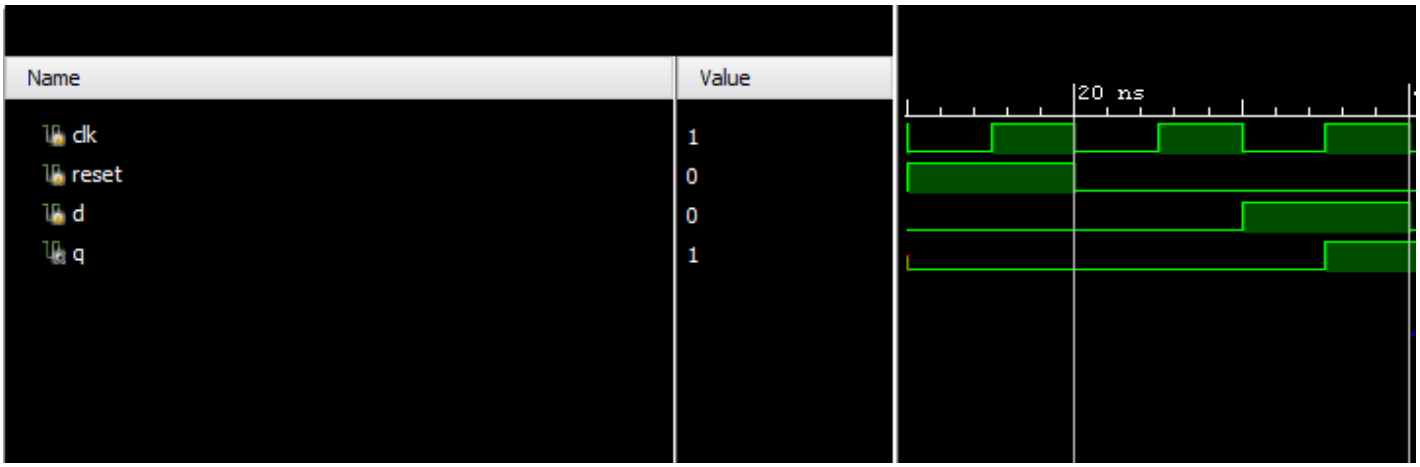
CODE FOR TESTBENCH:

```
module testbench;
  reg [15:0] a;
  reg [15:0] b;
  wire [15:0] result;

  gcd uut (
    .a(a),
    .b(b),
    .result(result)
  );

  initial begin
    a = 48;
    b = 18;
    #10;
    $display("GCD(%d, %d) = %d", a, b, result);
    $finish;
  end
endmodule
```

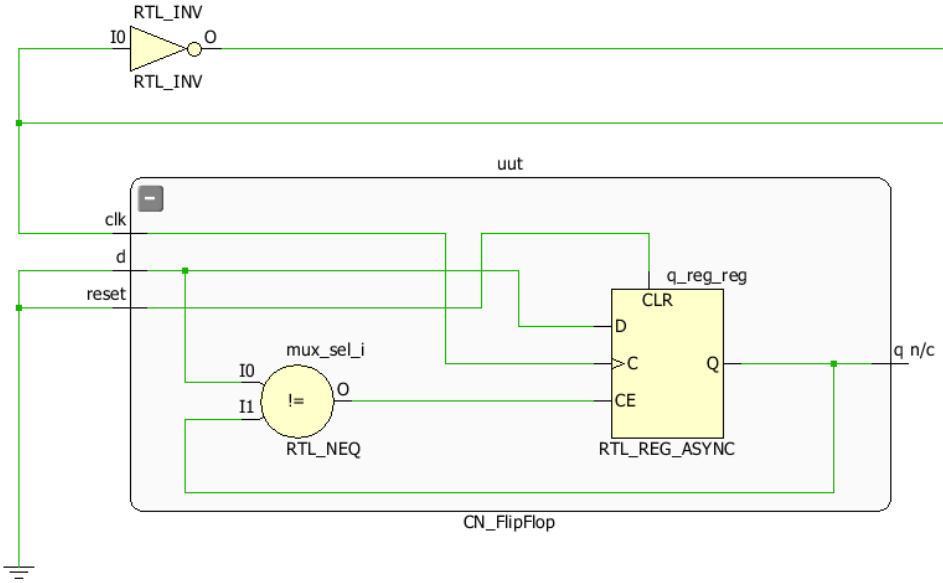
VERILOG CODE:

```
module gcd (
  input wire [15:0] a,
  input wire [15:0] b,
  output wire [15:0] result
);

always @* begin
  if (b == 0)
    result = a;
  else
    result = gcd(b, a % b);
end

endmodule
```

SIMULATION:



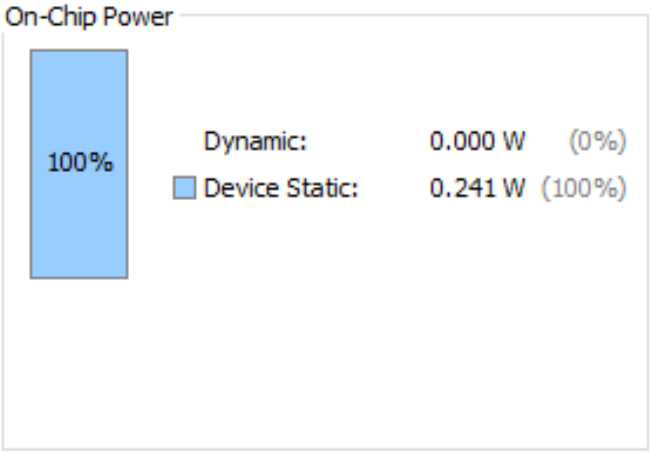
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-41: GREATEST COMMON DIVISOR VIA FSM

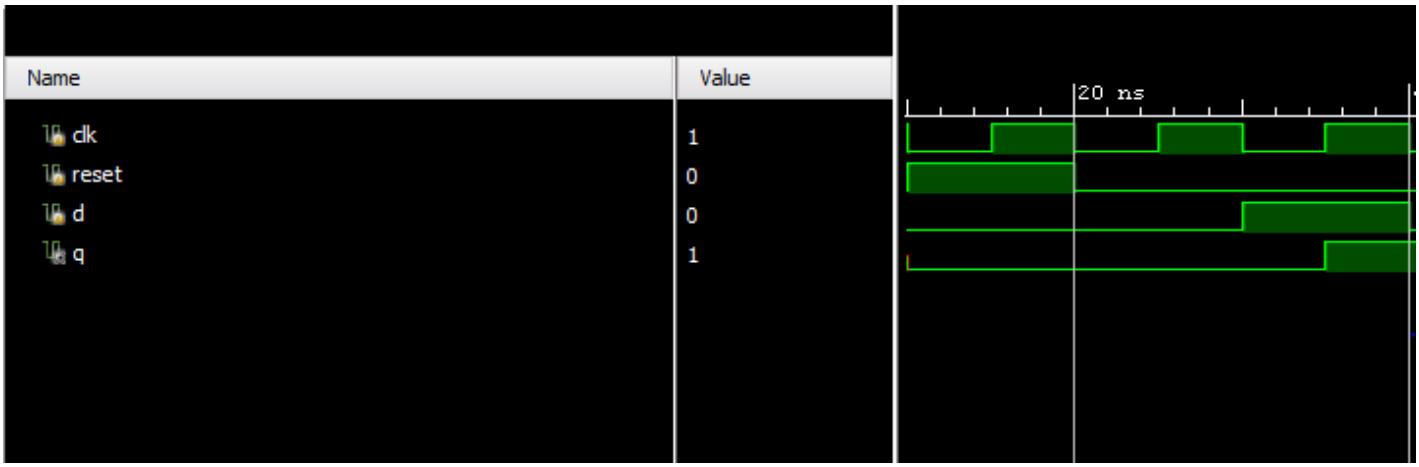
CODE FOR TESTBENCH:

```
module gcd_fsm_testbench;
  reg clk;
  reg reset;
  reg start;
  reg [31:0] a;
  reg [31:0] b;
  wire [31:0] gcd;
  gcd_fsm uut (
    .clk(clk),
    .reset(reset),
    .start(start),
    .a(a),
    .b(b),
    .gcd(gcd)
  );
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    reset = 0;
    start = 1;
    a = 48;
    b = 18;
    #10 reset = 1;
    #10 reset = 0;
    #10 start = 1;
    #10 start = 0;
    $finish  end
  always @(posedge clk) begin
    $display("GCD: %d", gcd);
  end
endmodule
```

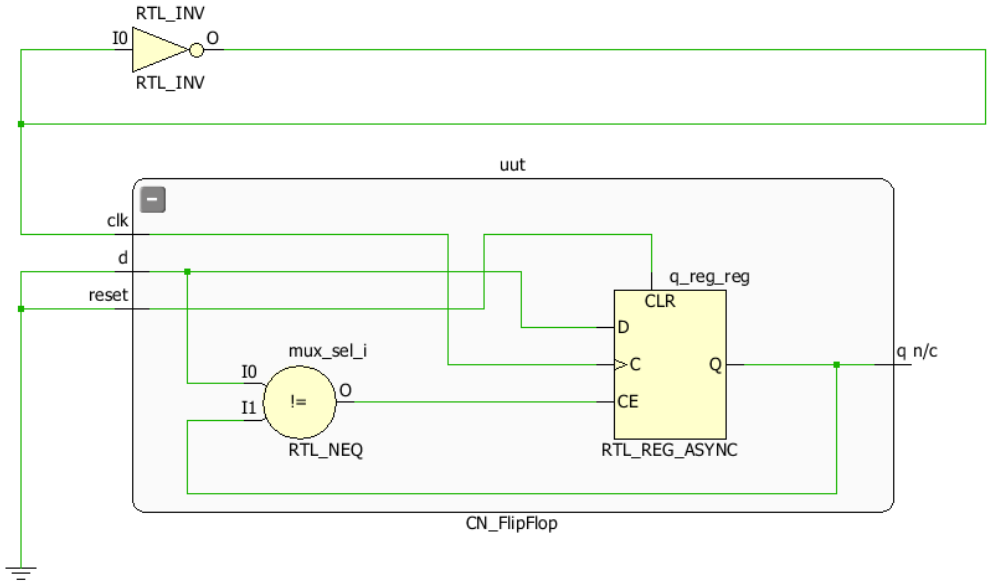
VERILOG CODE:

```
module gcd_fsm (
  input wire clk,
  input wire reset,
  input wire start,
  input wire [31:0] a,
  input wire [31:0] b,
  output wire [31:0] gcd
);

  typedef enum logic [3:0] {
    IDLE = 4'b0000,
    SUBTRACT = 4'b0001,
    COMPARE = 4'b0010,
    OUTPUT = 4'b0011
  } state_t;

  reg [3:0] state, next_state;
  reg [31:0] a_reg, b_reg, gcd_reg;

  always_ff @(posedge clk or posedge reset) begin
    if (reset)
      state <= IDLE;
    else
      state <= next_state;
  end

  always_ff @(posedge clk or posedge reset) begin
    if (reset) begin
      a_reg <= 32'h0;
      b_reg <= 32'h0;
      gcd_reg <= 32'h0;
    end else begin
      case (state)
        IDLE: begin
          a_reg <= a;
          b_reg <= b;
          gcd_reg <= 32'h0;
        end
        COMPARE: begin
          if (a_reg == b_reg)
            gcd_reg <= a_reg;
        end
        OUTPUT: begin
          gcd_reg <= a_reg;
        end
        default: begin
          a_reg <= a;
          b_reg <= b;
          gcd_reg <= 32'h0;
        end
      endcase
    end
  end

  always_ff @(posedge clk or posedge reset) begin
    if (reset)
      next_state <= IDLE;
    else
      next_state <= state;
  end

  always_comb begin
    case (state)
      IDLE: next_state = start ? SUBTRACT : IDLE;
      SUBTRACT: next_state = SUBTRACT;
      COMPARE: next_state = COMPARE;
      OUTPUT: next_state = OUTPUT;
      default: next_state = IDLE;
    endcase
  end
```

SIMULATION:



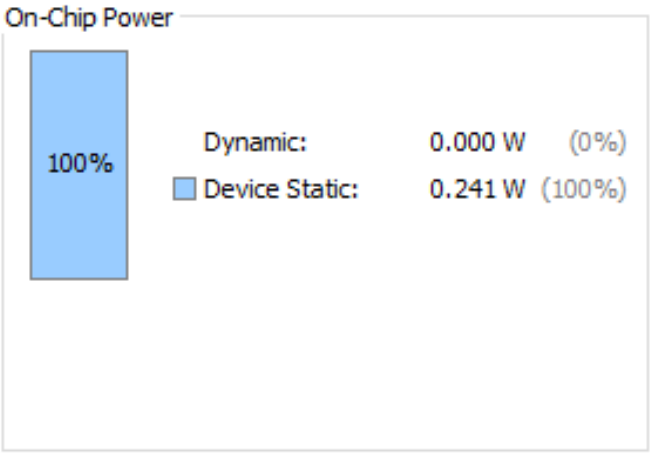
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-42: SINGLE PROT RAM

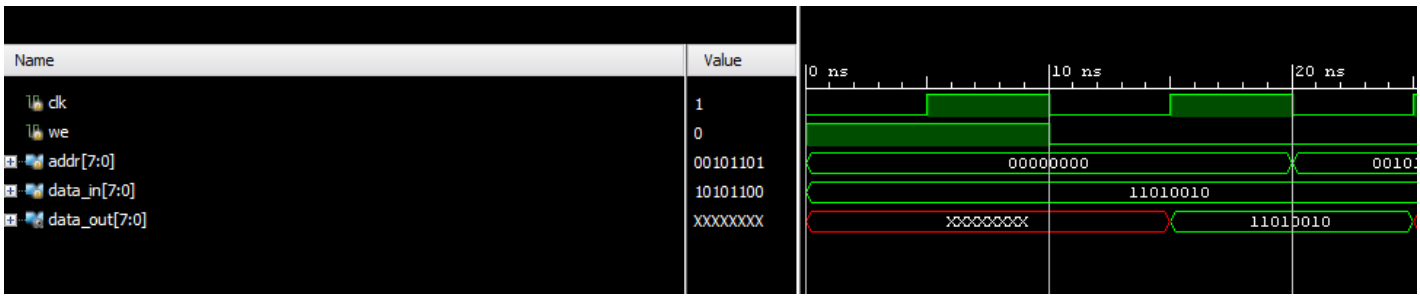
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg we;
  reg [7:0] addr;
  reg [7:0] data_in;
  wire [7:0] data_out;
  single_port_ram uut (
    .clk(clk),
    .we(we),
    .addr(addr),
    .data_in(data_in),
    .data_out(data_out)
  );
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    we = 1;
    addr = 8'b0000_0000;
    data_in = 8'b1101_0010;
    #10 we = 0;
    #10 addr = 8'b0010_1101;
    #10 data_in = 8'b1010_1100;
    $finish;
  end  always @(posedge clk) begin
    $display("Data Out: %h", data_out);
  end
endmodule
```

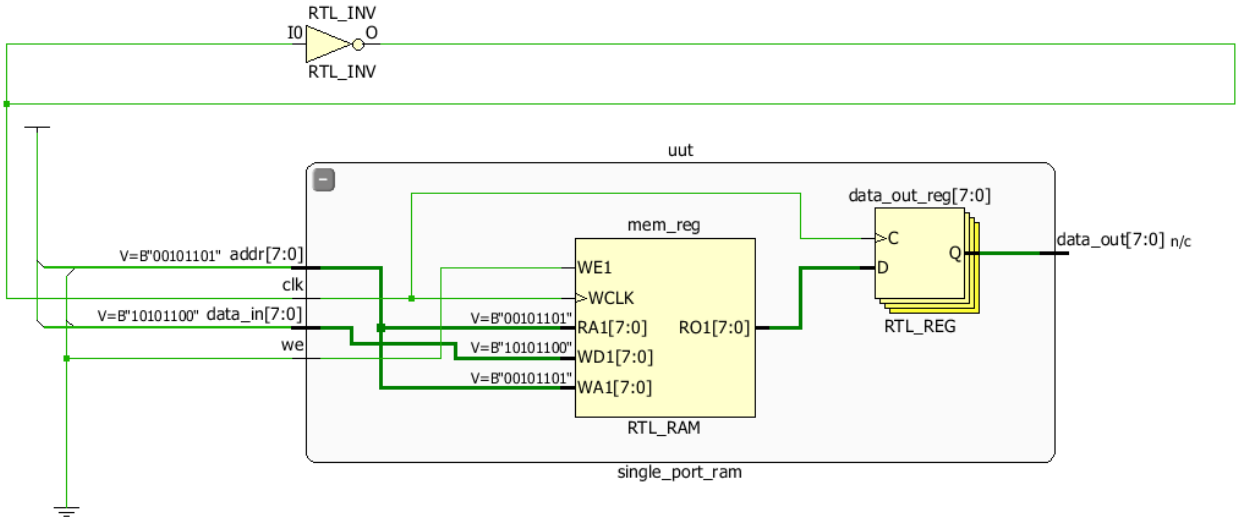
VERILOG CODE:

```
module single_port_ram (
  input wire clk,
  input wire we, // Write enable signal
  input wire [7:0] addr, // Address for read anc
  input wire [7:0] data_in, // Data input for wı
  output reg [7:0] data_out // Data output for ı
);

reg [7:0] mem [0:255]; // 256x8-bit memory

always @(posedge clk) begin
  if (we) begin
    mem[addr] <= data_in;
  end
  data_out <= mem[addr];
end

endmodule
```

SIMULATION:



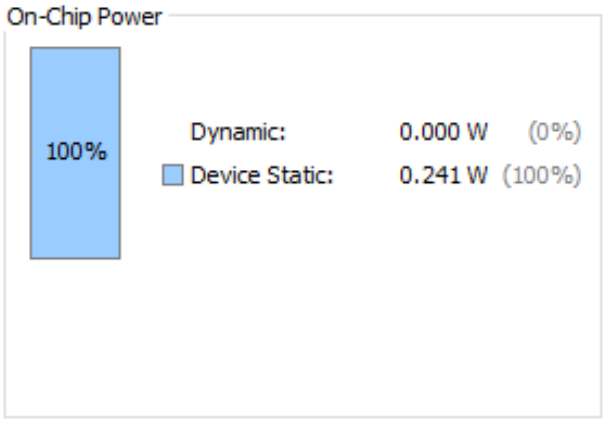
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-43: DUAL PROT RAM

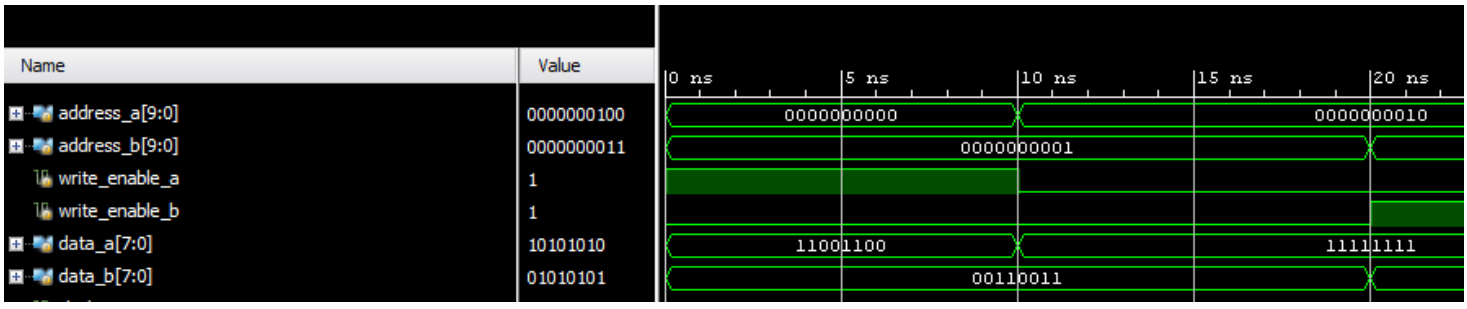
CODE FOR TESTBENCH:

```
module testbench;
  reg [9:0] address_a;
  reg [9:0] address_b;
  reg write_enable_a;
  reg write_enable_b;
  reg [7:0] data_a;
  reg [7:0] data_b;
  reg clock;
  wire [7:0] q_a;
  wire [7:0] q_b;
  dual_port_ram uut (
    .address_a(address_a),
    .address_b(address_b),
    .write_enable_a(write_enable_a),
    .write_enable_b(write_enable_b),
    .data_a(data_a),
    .data_b(data_b),
    .clock(clock),
    .q_a(q_a),
    .q_b(q_b)
  );
  always begin
    #5 clock = ~clock;
  end
  initial begin
    address_a = 0;
    address_b = 1;
    write_enable_a = 1;
    data_a = 8'b11001100;
    write_enable_b = 0;
    data_b = 8'b00110011;
    #10 address_a = 2;
    write_enable_a = 0;
    data_a = 8'b11111111;
    #10 address_b = 3;
    write_enable_b = 1;
    data_b = 8'b01010101;
    #10 address_a = 4;
```

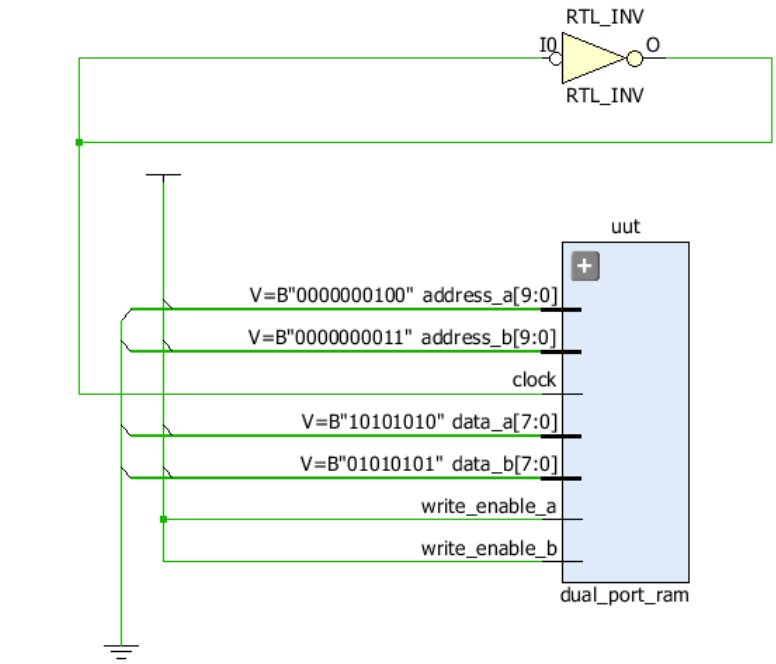
VERILOG CODE:

```
module dual_port_ram (
  input wire [9:0] address_a,
  input wire [9:0] address_b,
  input wire write_enable_a,
  input wire write_enable_b,
  input wire [7:0] data_a,
  input wire [7:0] data_b,
  input wire clock,
  output reg [7:0] q_a,
  output reg [7:0] q_b
);

reg [7:0] mem [0:1023];

always @(posedge clock) begin
  if (write_enable_a) begin
    mem[address_a] <= data_a;
  end

  if (write_enable_b) begin
    mem[address_b] <= data_b;
  end

  q_a <= mem[address_a];
  q_b <= mem[address_b];
end

endmodule
```

SIMULATION:



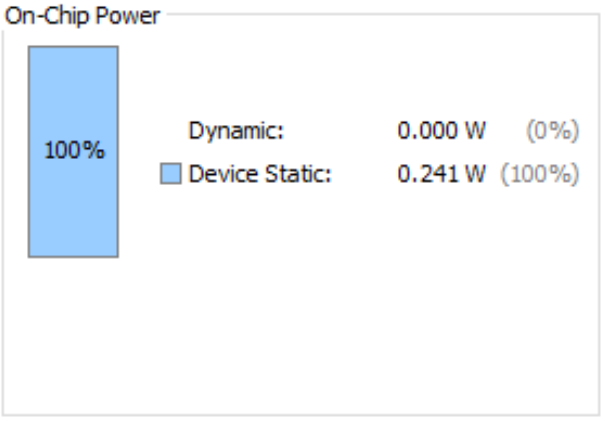
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-44: CLOCK BUFFER

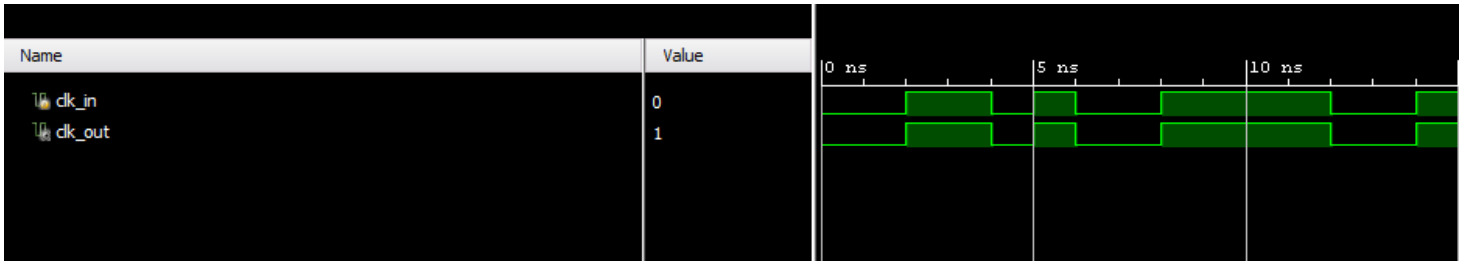
CODE FOR TESTBENCH:

```
module testbench;
  reg clk_in;
  wire clk_out;

  clock_buffer uut (
    .clk_in(clk_in),
    .clk_out(clk_out)
  );

  initial begin
    clk_in = 0;
    #5 clk_in = 1;
    #5 clk_in = 0;
    #5 clk_in = 1;
    #5 clk_in = 0;
    $finish;
  end

  always begin
    #2 clk_in = ~clk_in;
  end
endmodule
```

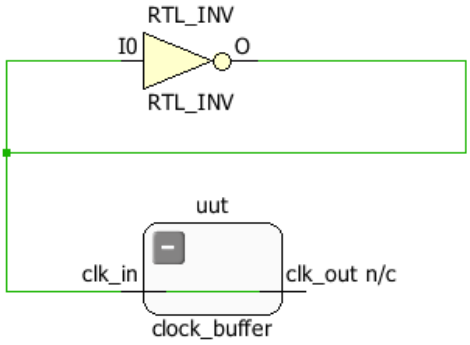
VERILOG CODE:

```
module clock_buffer (
  input wire clk_in,
  output wire clk_out
);

assign clk_out = clk_in;

endmodule
```

SIMULATION:



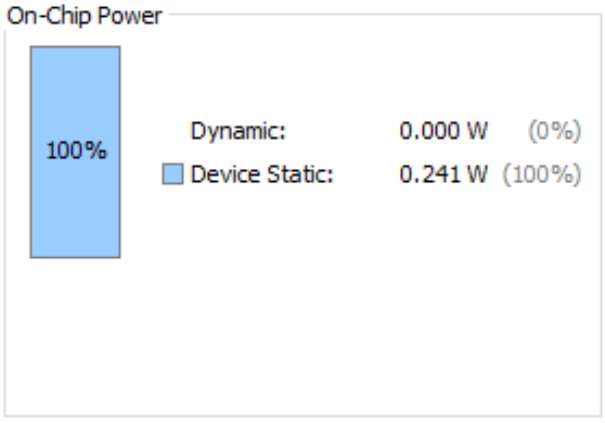
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-45: SYNCHRONOUS FIFO

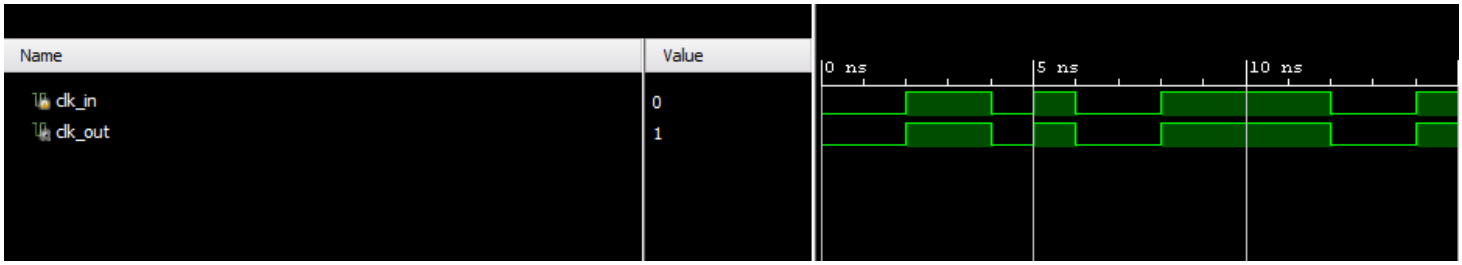
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg reset;
  reg write_enable;
  reg read_enable;
  reg [7:0] data_in;
  wire [7:0] data_out;
  wire full;
  wire empty;
  initial begin
    clk = 0;
    reset = 0;
    write_enable = 0;
    read_enable = 0;
    data_in = 8'b0;
    #10 reset = 1;
    #10 reset = 0;
    for (int i = 0; i < 8; i = i + 1) begin
      data_in = i;
      write_enable = 1;
      #10;
    end
    for (int i = 0; i < 8; i = i + 1) begin
      read_enable = 1;
      #10;
      read_enable = 0;
    end
    $finish;
  end
  always begin
    #5 clk = ~clk;
  end
endmodule
```

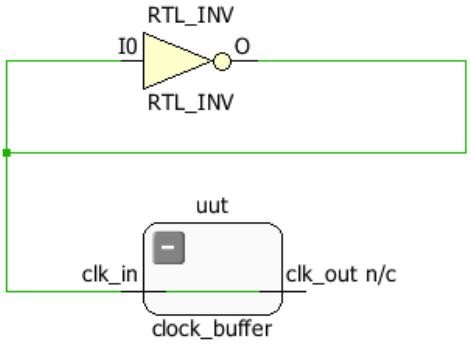
VERILOG CODE:

```
module synchronous_fifo (
  input wire clk,
  input wire reset,
  input wire write_enable,
  input wire read_enable,
  input wire [7:0] data_in,
  output wire [7:0] data_out,
  output wire full,
  output wire empty
);
  parameter DEPTH = 16;
  reg [7:0] memory [0:DEPTH-1];
  reg [3:0] write_ptr = 4'b0000;
  reg [3:0] read_ptr = 4'b0000;
  wire [3:0] next_write_ptr;
  wire [3:0] next_read_ptr;

  assign next_write_ptr = (write_enable) ? (write_ptr == DEPTH - 1 ? 4'b0000 : write_ptr + 1) : write_ptr;
  assign next_read_ptr = (read_enable) ? (read_ptr == DEPTH - 1 ? 4'b0000 : read_ptr + 1) : read_ptr;

  always @(posedge clk or posedge reset) begin
    if (reset) begin
      write_ptr <= 4'b0000;
      read_ptr <= 4'b0000;
    end else begin
      write_ptr <= next_write_ptr;
      read_ptr <= next_read_ptr;
      if (write_enable)
        memory[write_ptr] <= data_in;
    end
  end

  assign data_out = (empty) ? 8'b0 : memory[read_ptr];
  assign full = (next_write_ptr == next_read_ptr) && (write_enable);
  assign empty = (next_write_ptr == next_read_ptr) && (read_enable);

endmodule
```

SIMULATION:



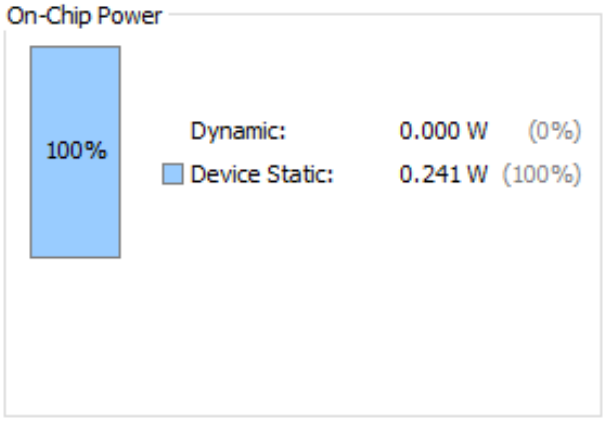
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-46: PRIORITY ENCODER

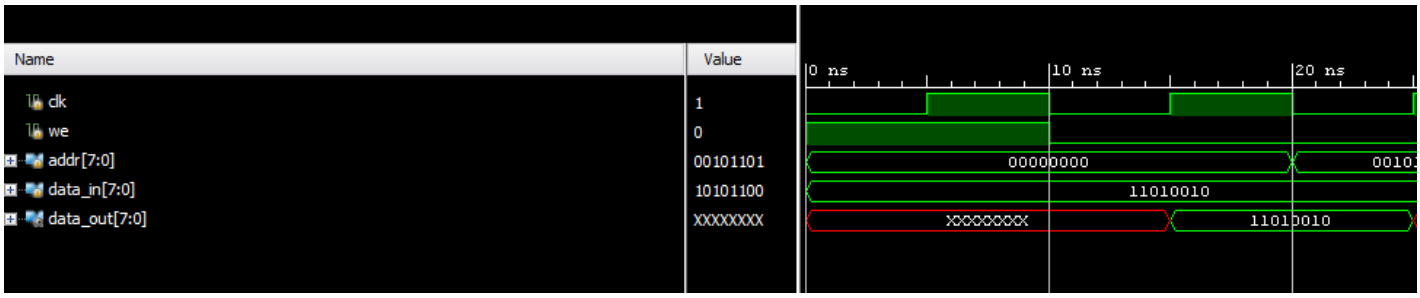
CODE FOR TESTBENCH:

```
module testbench;
  reg [3:0] inputs;
  wire [1:0] out;

  priority_encoder uut (
    .inputs(inputs),
    .out(out)
  );

  initial begin
    inputs = 4'b0000;
    #10 inputs = 4'b0001;
    #10 inputs = 4'b0010;
    #10 inputs = 4'b0100;
    #10 inputs = 4'b1000;

    $finish;
  end

  always begin
    $display("Inputs: %b, Out: %b", inputs, out);
  end

endmodule
```

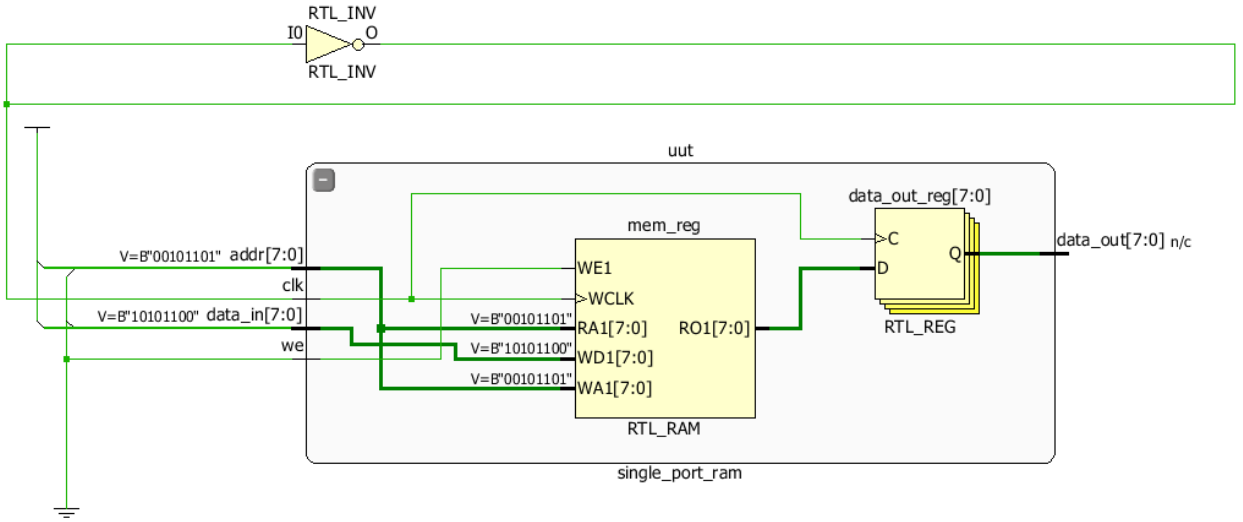
VERILOG CODE:

```
module priority_encoder (
  input wire [3:0] inputs,
  output reg [1:0] out
);

assign out[0] = ~|inputs;
assign out[1] = |inputs;

endmodule
```

SIMULATION:



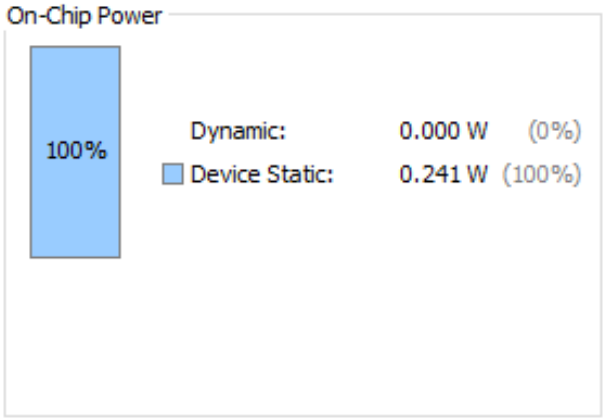
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-47: SEVEN SEGMENT DISPLAY USING ROM

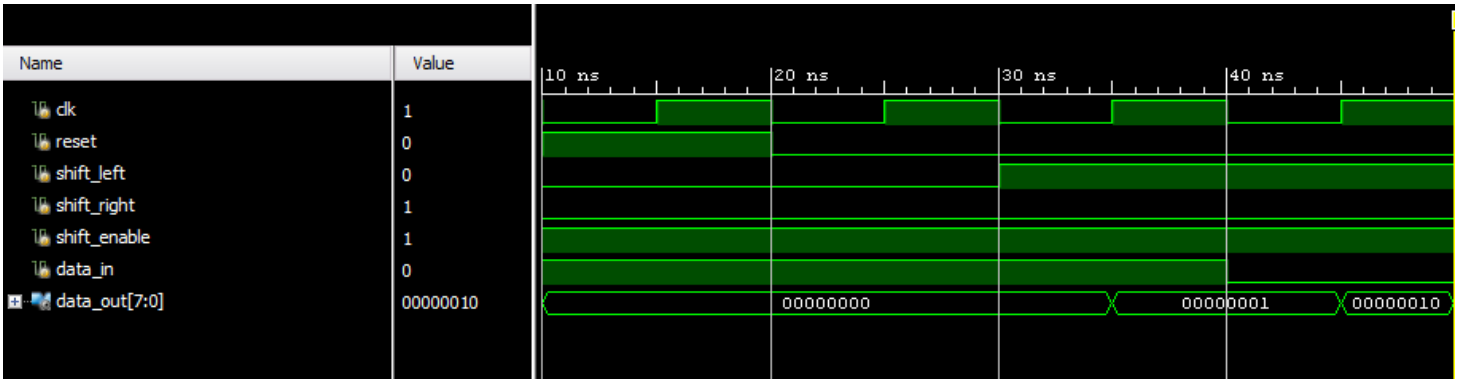
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg reset;
  reg shift_left;
  reg shift_right;
  reg shift_enable;
  reg data_in;
  wire [7:0] data_out;
  universal_shift_register uut (.clk(clk),.reset(reset),
    .shift_left(shift_left),
    .shift_right(shift_right),
    .shift_enable(shift_enable),
    .data_in(data_in),
    .data_out(data_out));
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    reset = 0;
    shift_left = 0;
    shift_right = 0;
    shift_enable = 1;
    data_in = 8'b11011011;
    #10 reset = 1;
    #10 reset = 0;
    #10 shift_left = 1;
    #10 shift_right = 0;
    data_in = 8'b00110010;
    #10 shift_left = 0;
    shift_right = 1;
    data_in = 8'b10101010;
    $finish;
  end
  always @(posedge clk) begin
    $display("Data Out: %b", data_out);
  end
endmodule
```

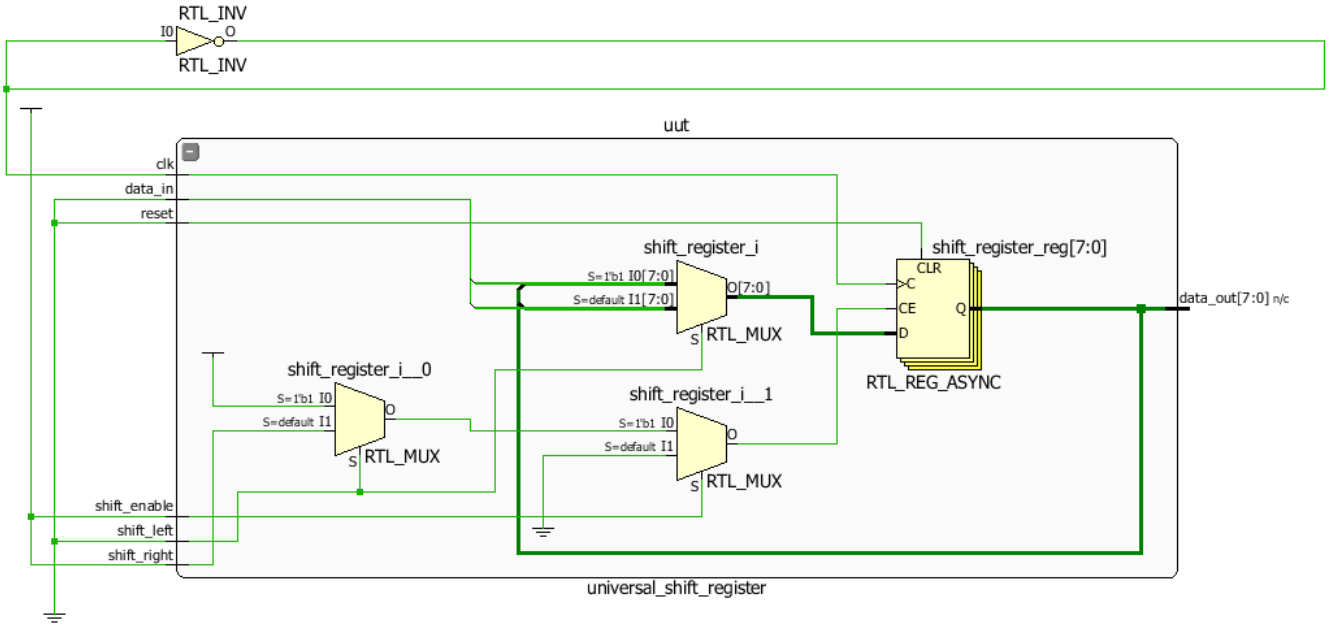
VERILOG CODE:

```
module universal_shift_register (
  input wire clk,
  input wire reset,
  input wire shift_left,
  input wire shift_right,
  input wire shift_enable,
  input wire data_in,
  output wire [7:0] data_out
);

reg [7:0] shift_register;

always @(posedge clk or posedge reset) begin
  if (reset) begin
    shift_register <= 8'b00000000;
  end else if (shift_enable) begin
    if (shift_left) begin
      shift_register <= {shift_register[6:0], data_in};
    end else if (shift_right) begin
      shift_register <= {data_in, shift_register[7:1]};
    end
  end
end
```

SIMULATION:



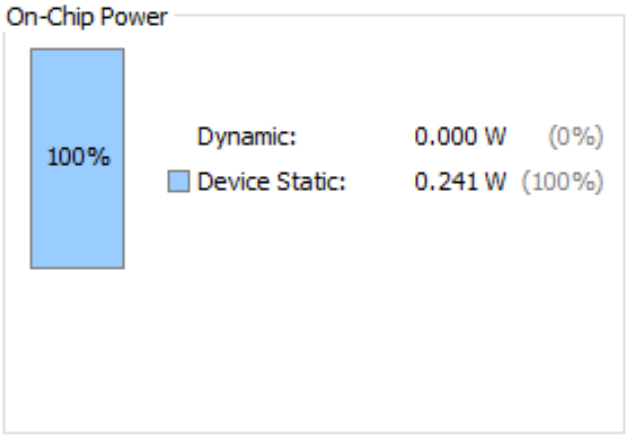
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-48: SERIAL ADDER

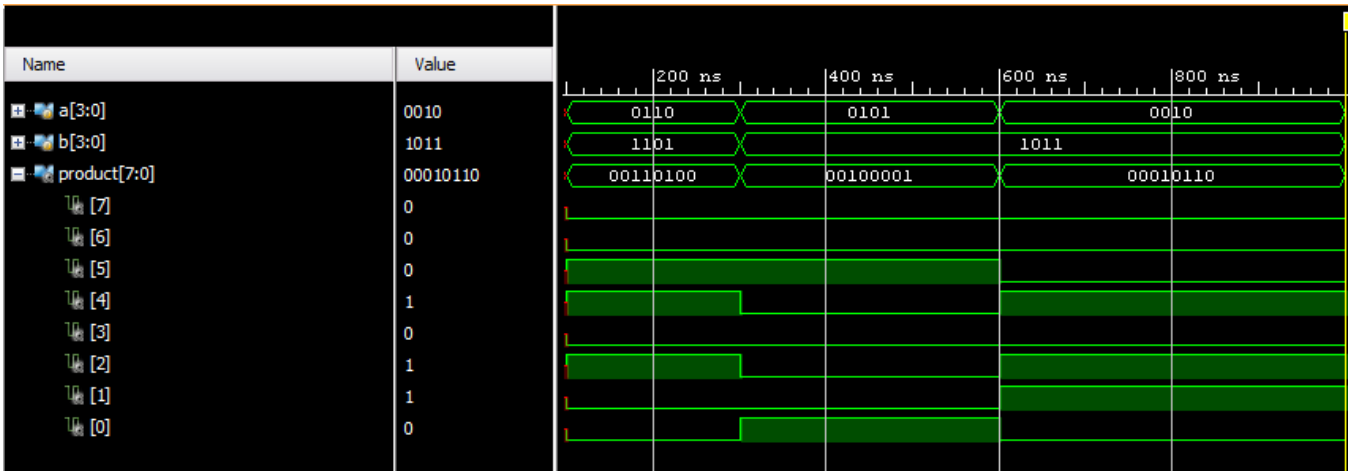
CODE FOR TESTBENCH:

```
module testbench;
reg [3:0]a,b;
wire [7:0] product;

    MULTIPLYER dut(a,b,product);
    initial
    begin
    $monitor("a=%b b=%b product=%b",a,b,product);

    #100 a[0]=0; a[1]=1; a[2]=1; a[3]=0;
         b[0]=1; b[1]=0; b[2]=1; b[3]=1;
    #200 a[0]=1; a[1]=0; a[2]=1; a[3]=0;
         b[0]=1; b[1]=1; b[2]=0; b[3]=1;
    #300 a[0]=0; a[1]=1; a[2]=0; a[3]=0;
         b[0]=1; b[1]=1; b[2]=0; b[3]=1;
         end
         endmodule
```

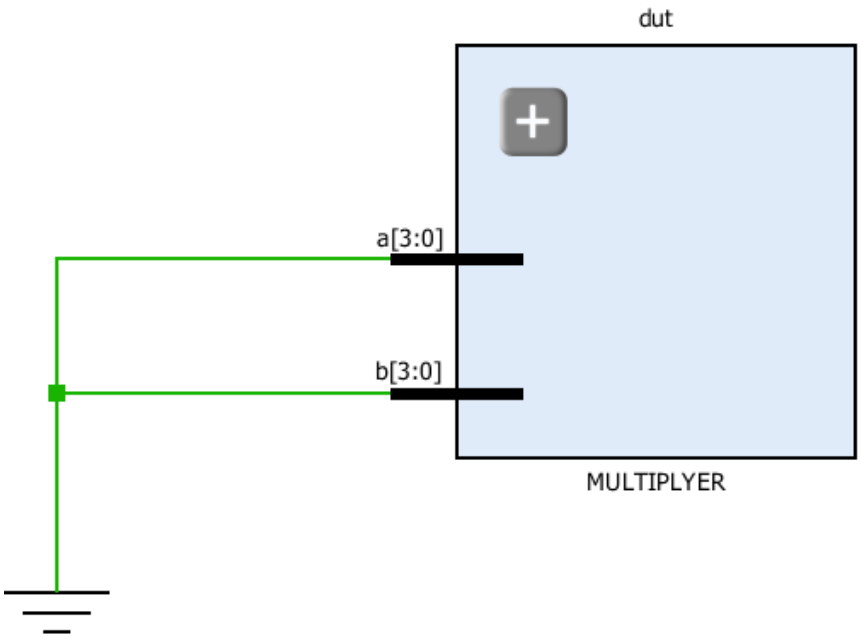
VERILOG CODE:

```
module MULTIPLYER(
    input [3:0] a,
    input [3:0] b,
    output [7:0] product
    );
    wire [3:0] m0;
    wire [4:0] m1;
    wire [5:0] m2;
    wire [6:0] m3;
    wire [7:0] s1,s2,s3;
    assign m0={4{a[0]}}&b[3:0];
    assign m1={4{a[1]}}&b[3:0];
    assign m2={4{a[2]}}&b[3:0];
    assign m3={4{a[3]}}&b[3:0];

    assign s1=m0+(m1<<1);
    assign s2=s1+(m2<<1);
    assign s3=s2+(m3<<1);
    assign product= s3;
endmodule
```

SIMULATION:



RTL SCHEMATIC:

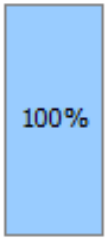


POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 ℃**
Thermal Margin:	59.7 ℃ (41.1 W)
Effective ϑJA:	1.4 ℃/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power



Dynamic:	0.000 W	(0%)
Device Static:	0.241 W	(100%)

CODE-49: FIXED PRIORITY ARBITAR

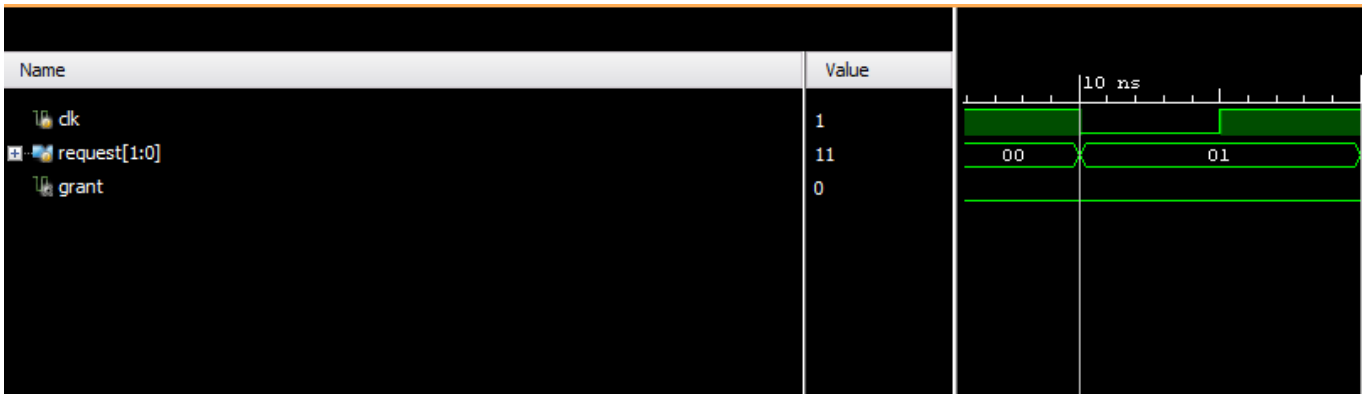
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg [1:0] request;
  wire grant;
  fixed_priority_arbiter uut (
    .clk(clk),
    .request(request),
    .grant(grant)
  );
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    request = 2'b00;

    #10 request = 2'b01;
    #10 request = 2'b10;
    #10 request = 2'b11;
    $finish;
  end
  always @(posedge clk) begin
    $display("Grant = %b", grant);
  end
endmodule
```

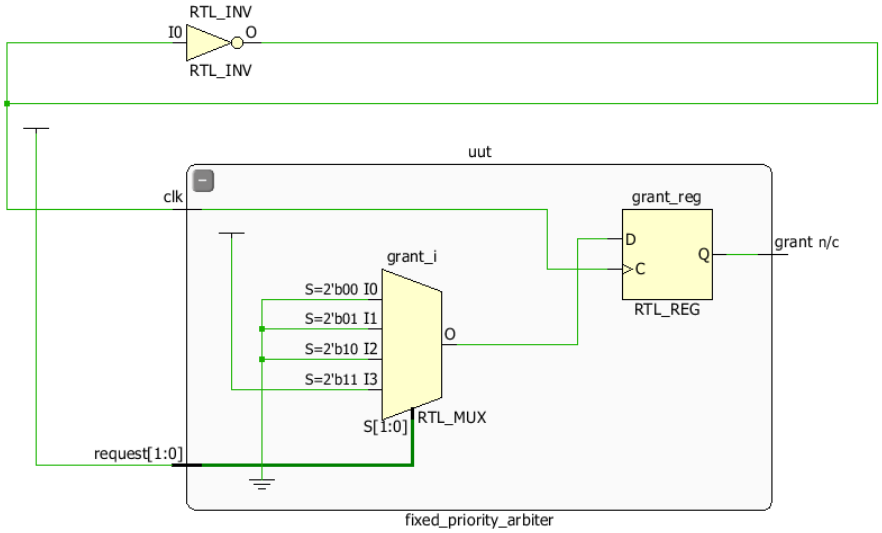
VERILOG CODE:

```
module fixed_priority_arbiter (
  input wire clk,
  input wire [1:0] request, // Input request lines
  output reg grant          // Output grant line
);

always @(posedge clk) begin
  case (request)
    2'b00: grant <= 1'b0;
    2'b01: grant <= 1'b0;
    2'b10: grant <= 1'b0;
    2'b11: grant <= 1'b1;
    default: grant <= 1'b0;
  endcase
end

endmodule
```

SIMULATION:



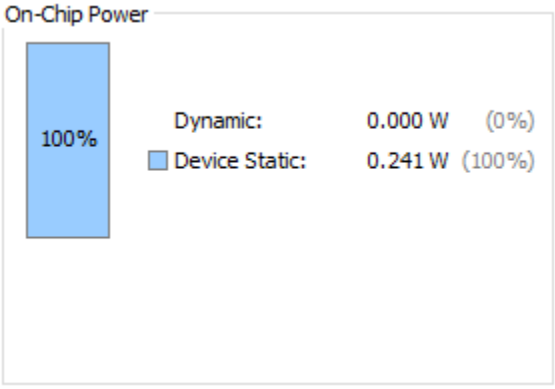
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



CODE-50: ROUND ROBIN ARBITAR

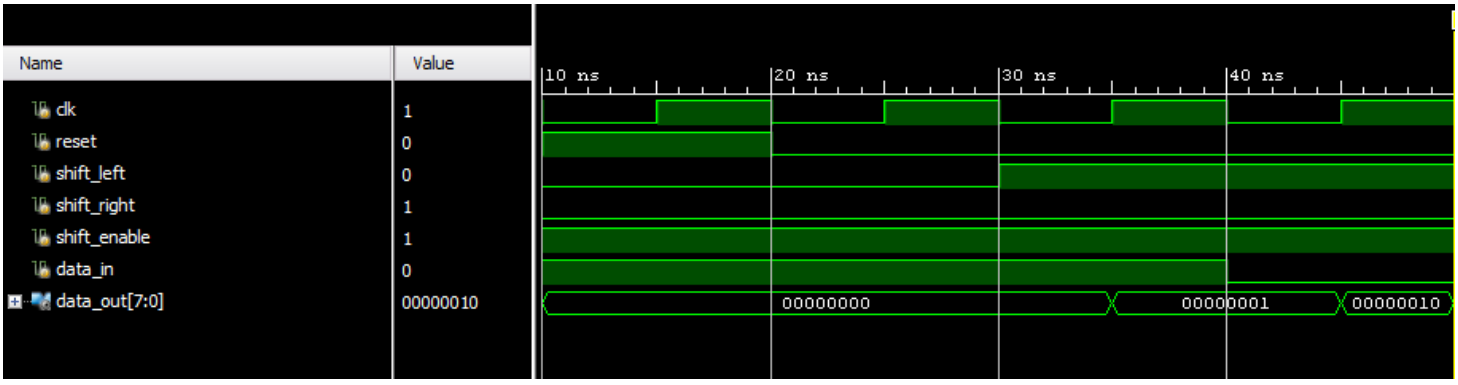
CODE FOR TESTBENCH:

```
module testbench;
  reg clk;
  reg reset;
  reg shift_left;
  reg shift_right;
  reg shift_enable;
  reg data_in;
  wire [7:0] data_out;
  universal_shift_register uut (.clk(clk),.reset(reset),
    .shift_left(shift_left),
    .shift_right(shift_right),
    .shift_enable(shift_enable),
    .data_in(data_in),
    .data_out(data_out));
  always begin
    #5 clk = ~clk;
  end
  initial begin
    clk = 0;
    reset = 0;
    shift_left = 0;
    shift_right = 0;
    shift_enable = 1;
    data_in = 8'b11011011;
    #10 reset = 1;
    #10 reset = 0;
    #10 shift_left = 1;
    #10 shift_right = 0;
    data_in = 8'b00110010;
    #10 shift_left = 0;
    shift_right = 1;
    data_in = 8'b10101010;
    $finish;
  end
  always @(posedge clk) begin
    $display("Data Out: %b", data_out);
  end
endmodule
```

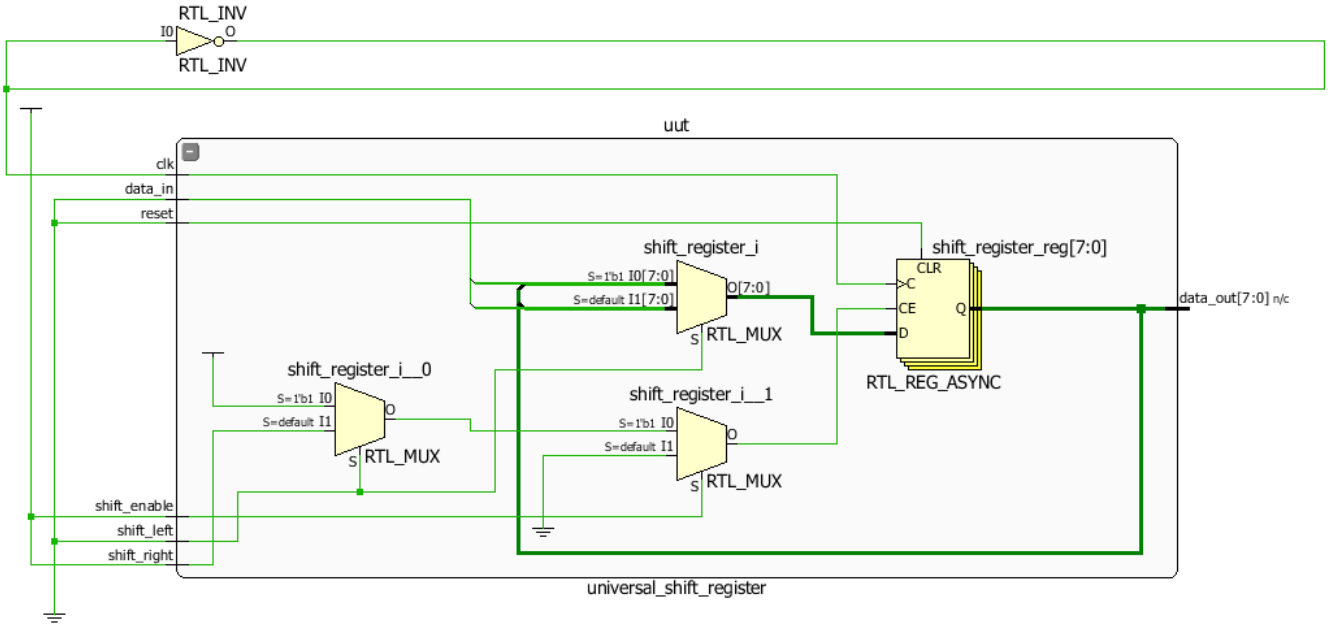
VERILOG CODE:

```
module universal_shift_register (
  input wire clk,
  input wire reset,
  input wire shift_left,
  input wire shift_right,
  input wire shift_enable,
  input wire data_in,
  output wire [7:0] data_out
);

reg [7:0] shift_register;

always @(posedge clk or posedge reset) begin
  if (reset) begin
    shift_register <= 8'b00000000;
  end else if (shift_enable) begin
    if (shift_left) begin
      shift_register <= {shift_register[6:0], data_in};
    end else if (shift_right) begin
      shift_register <= {data_in, shift_register[7:1]};
    end
  end
end
```

SIMULATION:



RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.241 W**
Junction Temperature:	**25.3 °C**
Thermal Margin:	59.7 °C (41.1 W)
Effective ϑJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low