



**BIRLA VISHVAKARMA MAHAVIDYALAY**  
**(AN AUTONOMOUS INSTITUTION)**  
**ELECTRONICS ENGINEERING DEPARTMENT**  
**A.Y. 2023-2024**

**DIGITAL SYSTEM DESIGN: -25 VERILOG**  
**CODES**

**NAME: SHREYA VERMA**

**ID NO.: 21EL001**

**SEMESTER: 5<sup>TH</sup>**

**BATCH: A – BATCH**

**BRANCH: ELECTRONICS ENGINEERING**

<b>SR. NO.</b>	<b>LIST</b>
<b>1.</b>	<b>CLOCK DIVIDER</b>
<b>2.</b>	<b>JOHNSON COUNTER</b>
<b>3.</b>	<b>RING COUNTER</b>
<b>4.</b>	<b>5 INPUT MAJORITY CIRCUIT</b>
<b>5.</b>	<b>PARITY GENERATOR</b>
<b>6.</b>	<b>BINARY TO ONE HOT ENCODER</b>
<b>7.</b>	<b>4-BIT BCD SYNCHRONOUS COUNTER</b>
<b>8.</b>	<b>4-BIT CARRY LOOKAHEAD ADDER</b>
<b>9.</b>	<b>N-BIT COMPARATOR</b>
<b>10.</b>	<b>SERIAL IN SERIAL OUT SHIFT REGISTER</b>
<b>11.</b>	<b>SERIAL IN PARALLEL OUT SHIFT REGISTER</b>
<b>12.</b>	<b>PARALLEL IN PARALLEL OUT REGISTER</b>
<b>13.</b>	<b>PARALLEL IN SERIAL OUT REGISTER</b>
<b>14.</b>	<b>BIDIRECTION SHIFT REGISTER</b>
<b>15.</b>	<b>PRBS SEQUENCE GENERATOR</b>
<b>16.</b>	<b>8-BIT SUBTRACTOR</b>
<b>17.</b>	<b>8-BIT ADDER/SUBTRACTOR</b>
<b>18.</b>	<b>4-BIT MULTIPLIER</b>
<b>19.</b>	<b>FIXED POINT DIVISION</b>
<b>20.</b>	<b>MASTER SLAVE JK FLIP FLOP</b>
<b>21.</b>	<b>POSITIVE EDGE DETECTOR</b>

<b>22.</b>	<b>BCD ADDER</b>
<b>23.</b>	<b>4-BIT CARRY SELECT ADDER</b>
<b>24.</b>	<b>MOORE FSM 1010 SEQUENCE DETECTOR</b>
<b>25.</b>	<b>N:1 MUX</b>

# CODE-1: CLOCK DIVIDER

## CODE FOR TESTBENCH:

```
module testbench;
reg Clk,Rst;
wire [3:0] Count;
wire D2,D4,D8,D16;

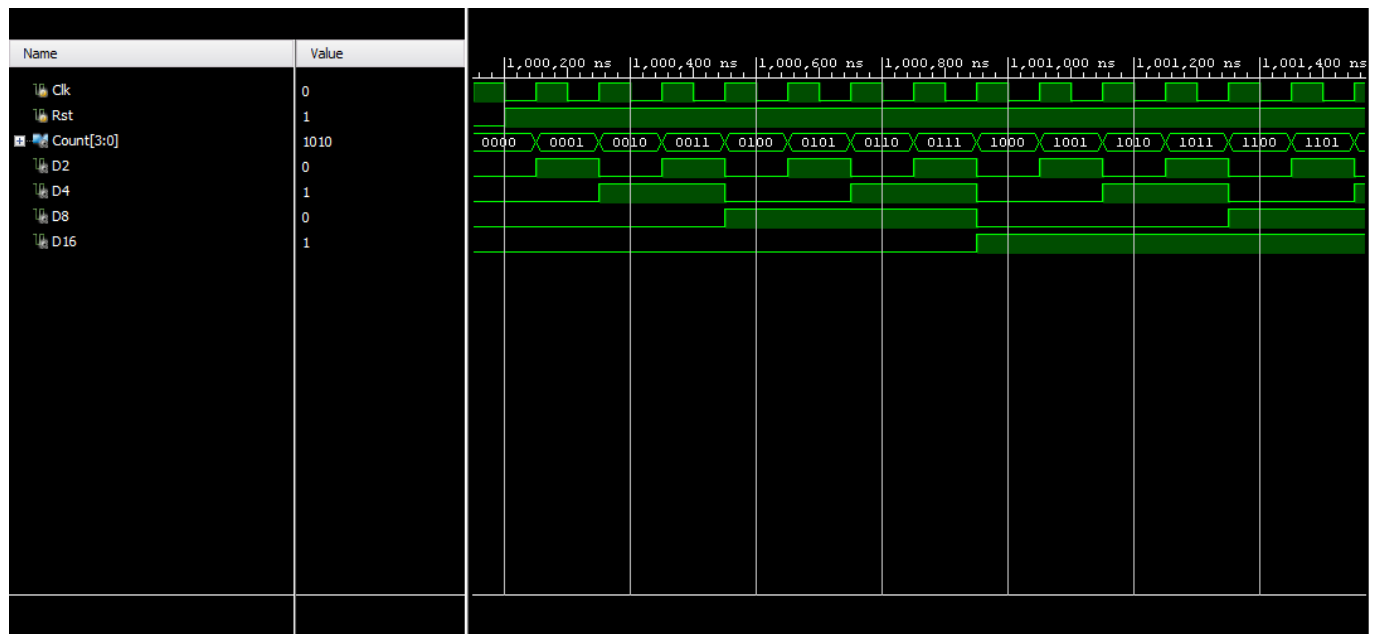
Clock_Divider dut(Clk,Rst,Count,D2,D4,D8,D16);
initial
begin
$monitor("Clk=%b Rst=%b Count=%b D2=%b D4=%b D8=%b D16=%b",Clk,Rst,Count,D2,D4,D8,D16);
end
always
begin
#50 Clk = ~Clk;
end
initial
begin
#100 Rst = 1;
#100 Rst = 0;

$finish;
end
endmodule
```

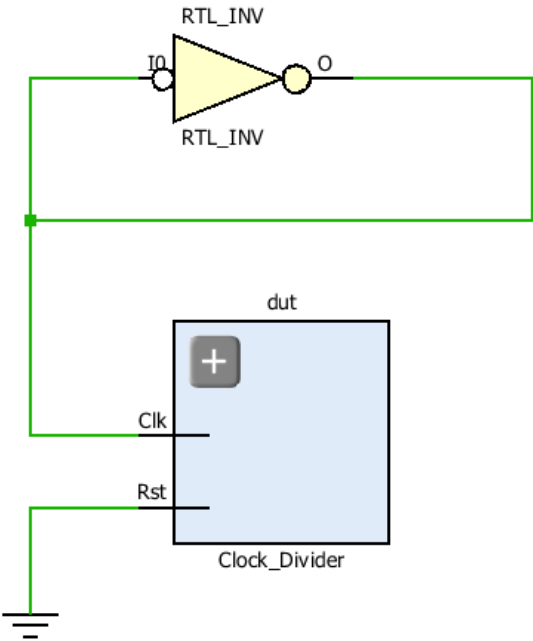
## VERILOG CODE:

```
module Clock_Divider(  
    input Clk,  
    input Rst,  
    output reg [3:0] Count,  
    output reg D2,D4,D8,D16  
);  
always@(posedge Clk)  
begin  
    if (Rst==0)  
        Count=4'b0000;  
    else  
        Count=Count+1;  
        D2=Count[0];  
        D4=Count[1];  
        D8=Count[2];  
        D16=Count[3];  
    end  
endmodule
```

## SIMULATION:



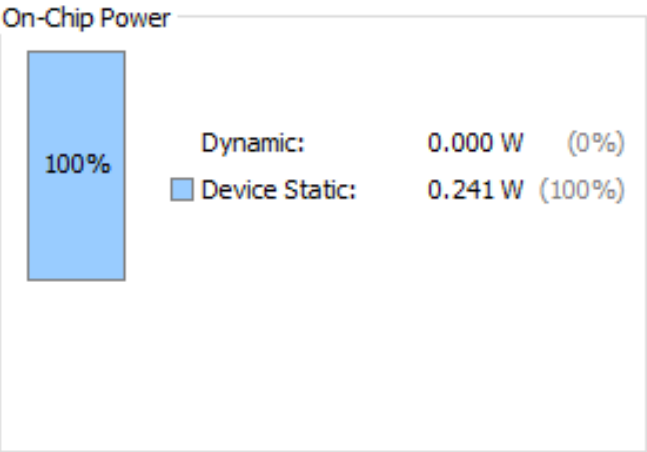
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.241 W
Junction Temperature:	25.3 °C
Thermal Margin:	59.7 °C (41.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	<a href="#">Low</a>



# CODE-2: JOHNSON COUNTER

## CODE FOR TESTBENCH:

```
module testbench;
reg Clk,Rst;
reg [3:0] Width;
wire [3:0] Count;

JOHNSON_COUNTER dut(Clk,Rst,Width,Count);
initial
begin
$monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
end
always
begin
#50 Clk = ~Clk;
end
initial
begin
#100 Rst = 1;
#100 Rst = 0;

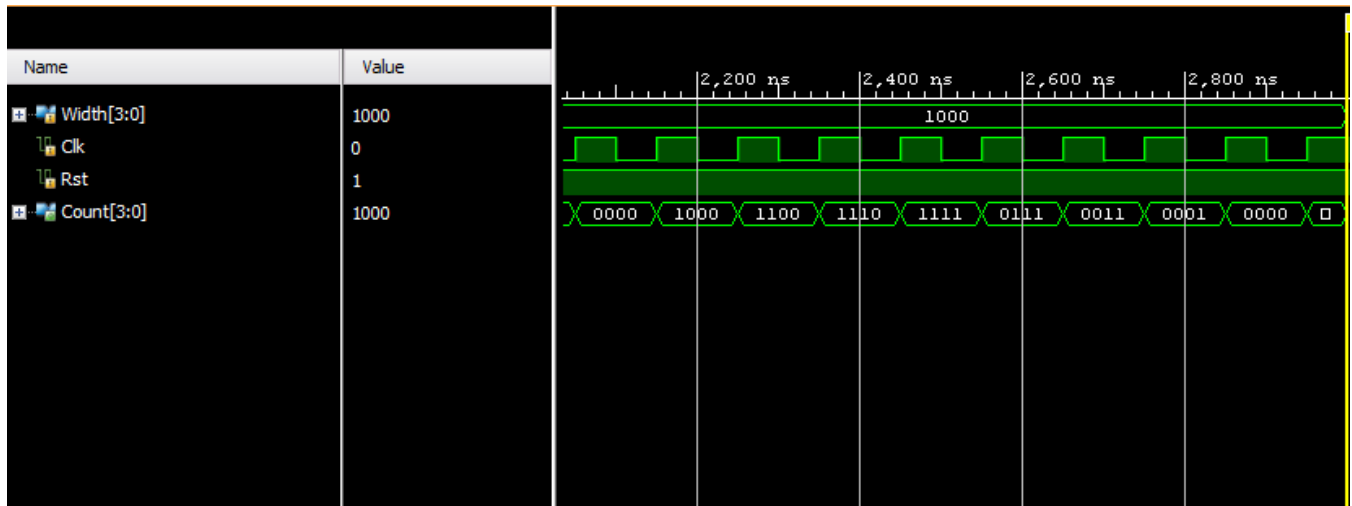
$finish;
end
endmodule
```

## VERILOG CODE:

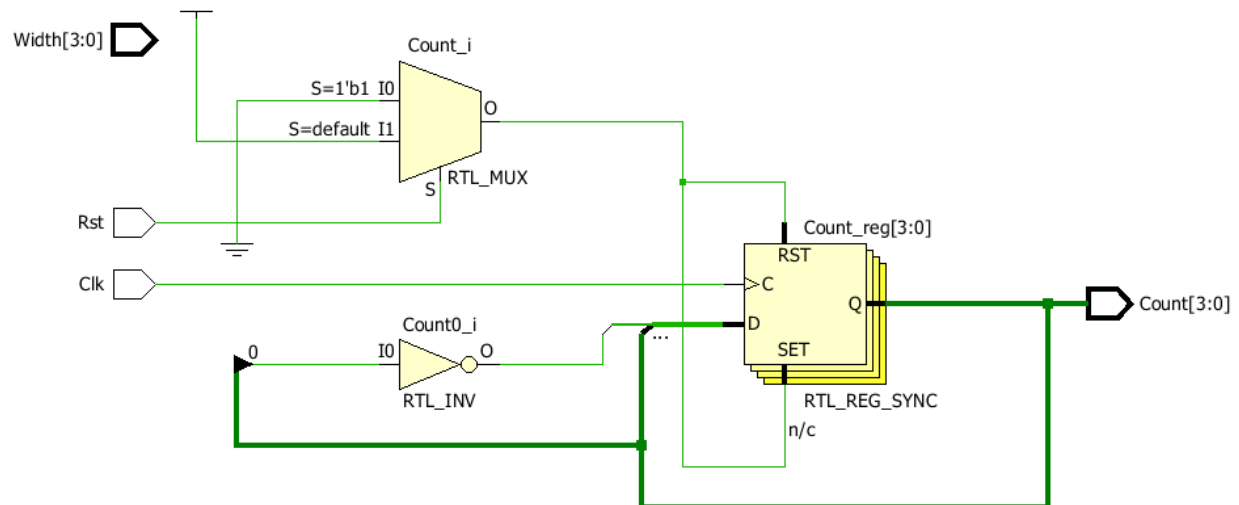
```
module JOHNSON_COUNTER(
input [3:0] Width,
input Clk,
input Rst,
output reg [3:0] Count
);

always@(posedge Clk)
begin
if(Rst)
Count={~Count[0],Count[3:1]};
else
Count=4'b0001;
end
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

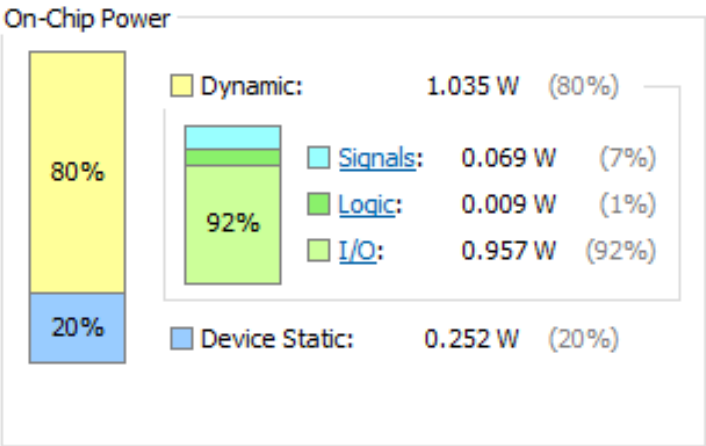




# POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	1.287 W
Junction Temperature:	26.8 °C
Thermal Margin:	58.2 °C (40.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



# CODE-3: RING COUNTER

## CODE FOR TESTBENCH:

```
module testbench;
reg [3:0] Width;
reg Clk,Rst;
wire [3:0] Count;

RING_COUNTER dut(Clk,Rst,Width,Count);

initial
begin
$monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
end

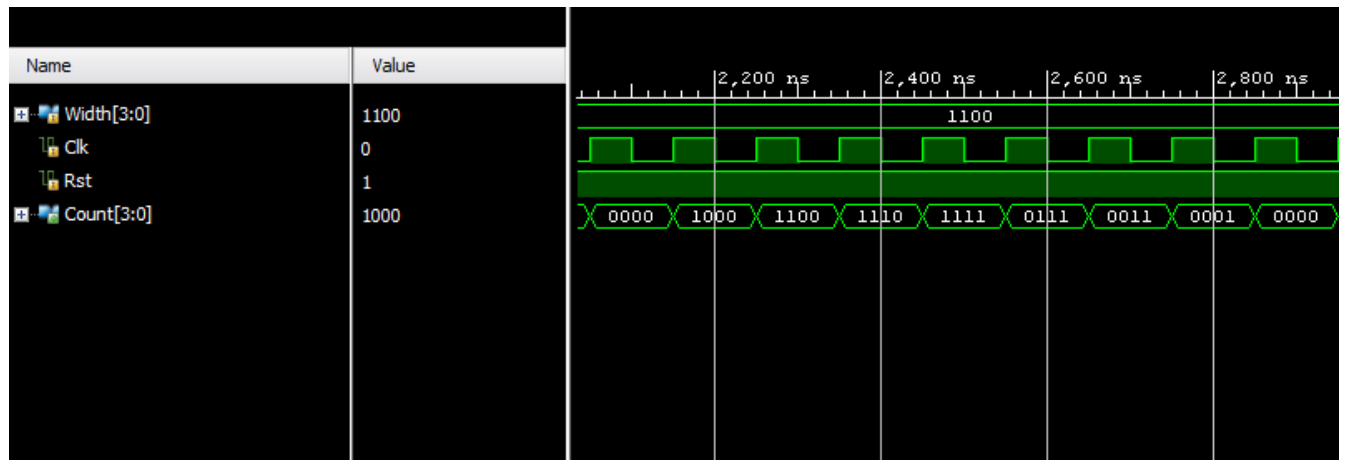
always
begin
#50 Clk=~Clk;
end
initial
begin
#100 Rst=1;
#100 Rst=0;
$finish;
end
endmodule
```

## VERILOG CODE:

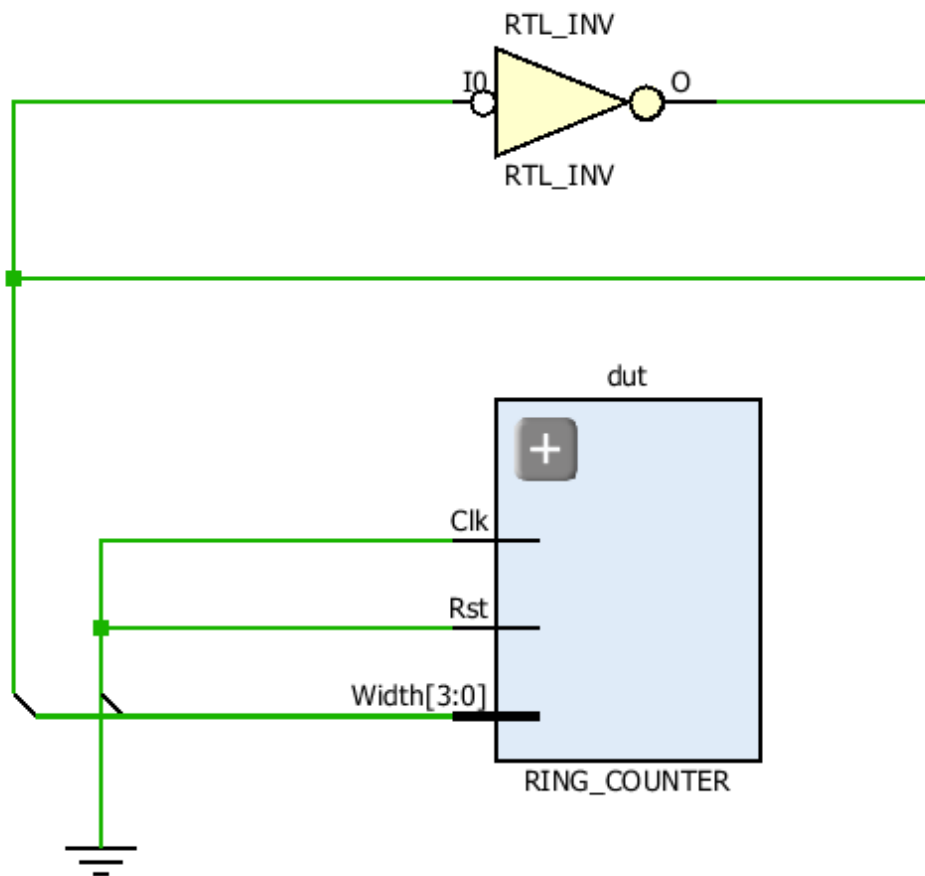
```
module RING_COUNTER(
input [3:0] Width,
input Clk,
input Rst,
output reg [3:0] Count
);

always@(posedge Clk)
begin
if(Rst)
Count={~Count[0],Count[3:1]};
else
Count=4'b0001;
end
endmodule
```

## SIMULATION:



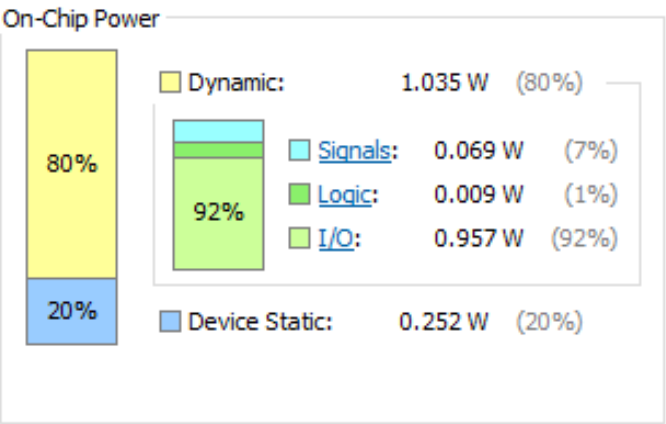
## RTL SCHEMATIC:



# POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>1.287 W</b>
<b>Junction Temperature:</b>	<b>26.8 °C</b>
Thermal Margin:	58.2 °C (40.1 W)
Effective $\theta_{JA}$ :	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	<a href="#">Low</a>



# CODE-4: 5 INPUT MAJORITY CIRCUIT

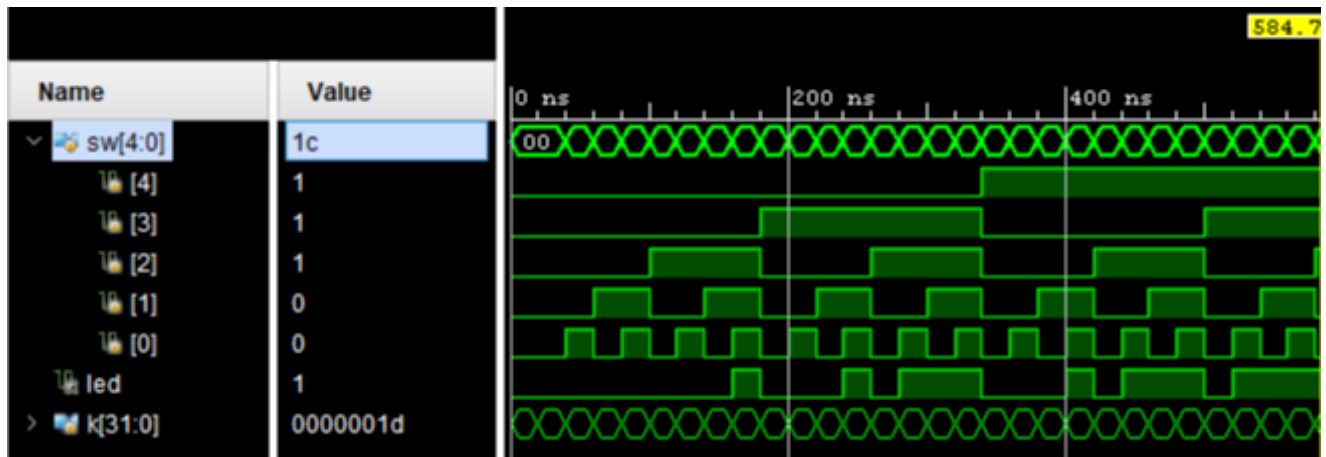
## CODE FOR TESTBENCH:

```
module testbench;
reg [4:0] x;
wire z;
INPUT_MAJORITY_CIRCUIT dut(x[0],x[1],x[2],x[3],x[4],z);
initial
begin
$monitor("x[0]=%b x[1]=%b x[2]=%b x[3]=%b x[4]=%b z=%b",x[0],x[1],x[2],x[3],x[4],z);
#2 x[0]=0; x[1]=0; x[2]=0; x[3]=0; x[4]=0;
#3 x[0]=0; x[1]=0; x[2]=0; x[3]=0; x[4]=1;
#4 x[0]=0; x[1]=0; x[2]=0; x[3]=1; x[4]=0;
#5 x[0]=0; x[1]=0; x[2]=0; x[3]=1; x[4]=1;
#6 x[0]=0; x[1]=0; x[2]=1; x[3]=0; x[4]=0;
#7 x[0]=0; x[1]=0; x[2]=1; x[3]=0; x[4]=1;
#8 x[0]=0; x[1]=0; x[2]=1; x[3]=1; x[4]=0;
#9 x[0]=0; x[1]=1; x[2]=1; x[3]=1; x[4]=1;
#10 x[0]=0; x[1]=1; x[2]=0; x[3]=0; x[4]=0;
#11 x[0]=0; x[1]=1; x[2]=0; x[3]=0; x[4]=1;
#12 x[0]=0; x[1]=1; x[2]=0; x[3]=1; x[4]=0;
#13 x[0]=0; x[1]=1; x[2]=0; x[3]=1; x[4]=1;
#14 x[0]=0; x[1]=1; x[2]=1; x[3]=0; x[4]=0;
#15 x[0]=0; x[1]=1; x[2]=1; x[3]=0; x[4]=1;
#16 x[0]=0; x[1]=1; x[2]=1; x[3]=1; x[4]=0;
#17 x[0]=0; x[1]=1; x[2]=1; x[3]=1; x[4]=1;
#18 x[0]=1; x[1]=0; x[2]=0; x[3]=0; x[4]=0;
#19 x[0]=1; x[1]=0; x[2]=0; x[3]=0; x[4]=1;
end
endmodule
```

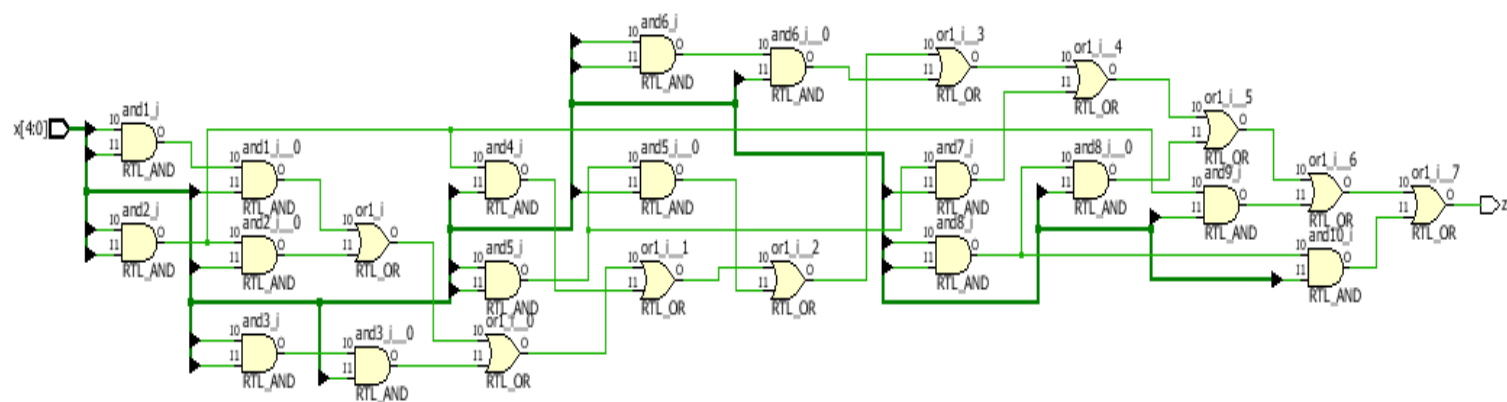
## VERILOG CODE:

```
module INPUT_MAJORITY_CIRCUIT(  
    input [4:0] x,  
    output z  
);  
    wire [9:0] w;  
    and and1(w[0],x[2],x[3],x[4]);  
    and and2(w[1],x[1],x[3],x[4]);  
    and and3(w[2],x[1],x[2],x[4]);  
    and and4(w[3],x[1],x[3],x[2]);  
    and and5(w[4],x[0],x[3],x[4]);  
    and and6(w[5],x[0],x[2],x[4]);  
    and and7(w[6],x[0],x[3],x[2]);  
    and and8(w[7],x[1],x[0],x[4]);  
    and and9(w[8],x[1],x[3],x[0]);  
    and and10(w[9],x[1],x[0],x[2]);  
    or or1(z,w[0],w[1],w[2],w[3],w[4],w[5],w[6],w[7],w[8],w[9]);  
endmodule
```

## SIMULATION:



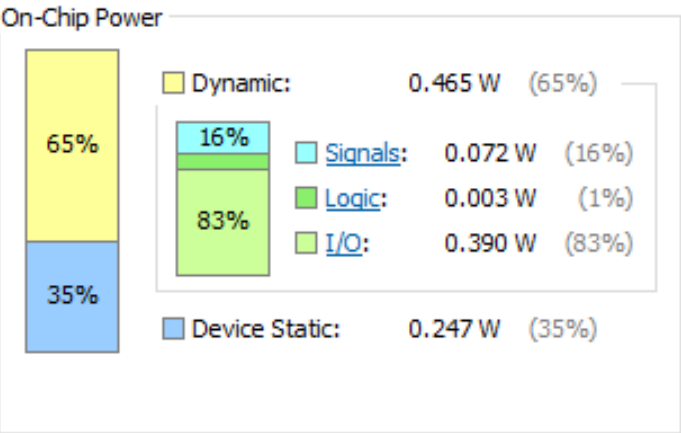
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.712 W
Junction Temperature:	26.0 °C
Thermal Margin:	59.0 °C (40.6 W)
Effective $\theta_{JA}$ :	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



# CODE-5: PARITY GENERATOR

## CODE FOR TESTBENCH:

```
module testbench;
reg x,y,z;
wire result;

    PARITY_GENERATOR dut(x,y,z,result);

    initial
    begin
        $monitor("x=%b y=%b z=%b result=%b",x,y,z,result);

        #100 x=0; y=0; z=0;
        #200 x=0; y=0; z=1;
        #300 x=0; y=1; z=0;
        #400 x=0; y=1; z=1;
        #500 x=1; y=0; z=0;
        #600 x=1; y=0; z=1;
        #700 x=1; y=1; z=0;
        #800 x=1; y=1; z=1;

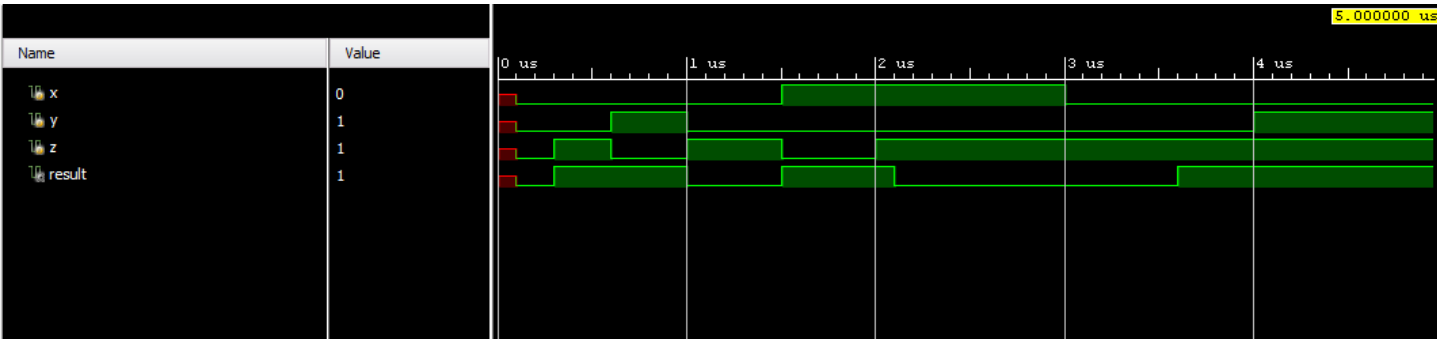
    end
endmodule
```

## VERILOG CODE:

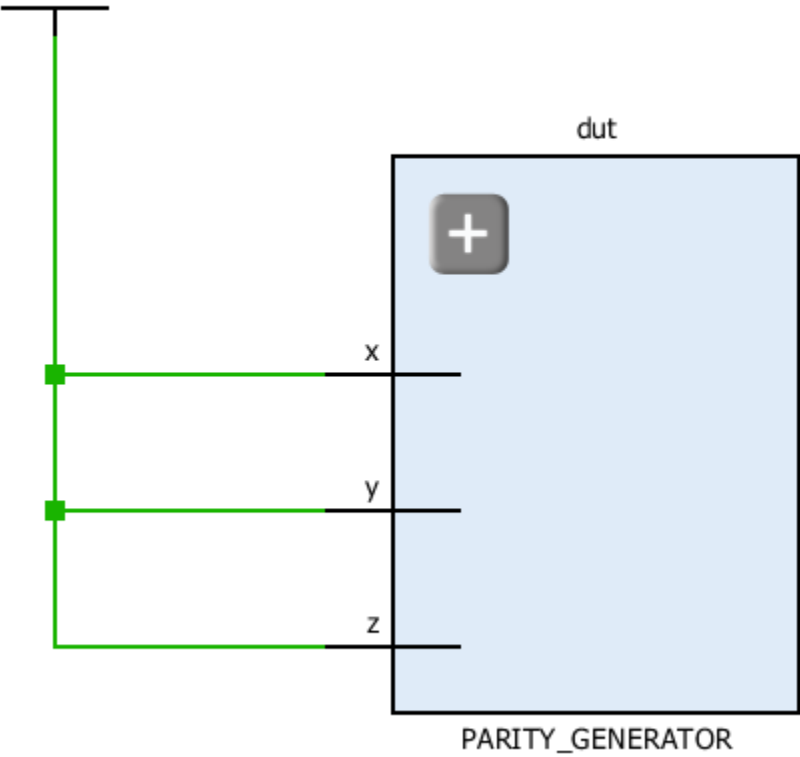
```
module PARITY_GENERATOR(
    input x,
    input y,
    input z,
    output result
);
    assign result= x^y^z;
endmodule
```



SIMULATION:



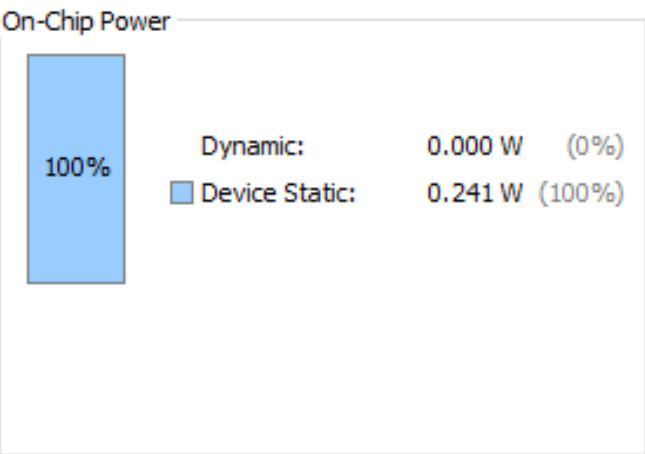
RTL SCHEMATIC:



# POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>0.241 W</b>
<b>Junction Temperature:</b>	<b>25.3 °C</b>
Thermal Margin:	59.7 °C (41.1 W)
Effective $\theta_{JA}$ :	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	<a href="#">Low</a>



# CODE-6: BINARY TO ONE HOT ENCODER

## CODE FOR TESTBENCH:

```
module testbench;
reg [1:0] bin_i;
wire [1:0] one_hot_o;

BINARY_TO_ONE_HOT_ENCODER dut(bin_i,one_hot_o);

initial
begin
$monitor("bin_i=%b one_hot_o=%b",bin_i,one_hot_o);

#100 bin_i[0]=0; bin_i[1]=0;
#200 bin_i[0]=0; bin_i[1]=1;
#300 bin_i[0]=1; bin_i[1]=0;
#400 bin_i[0]=1; bin_i[1]=1;

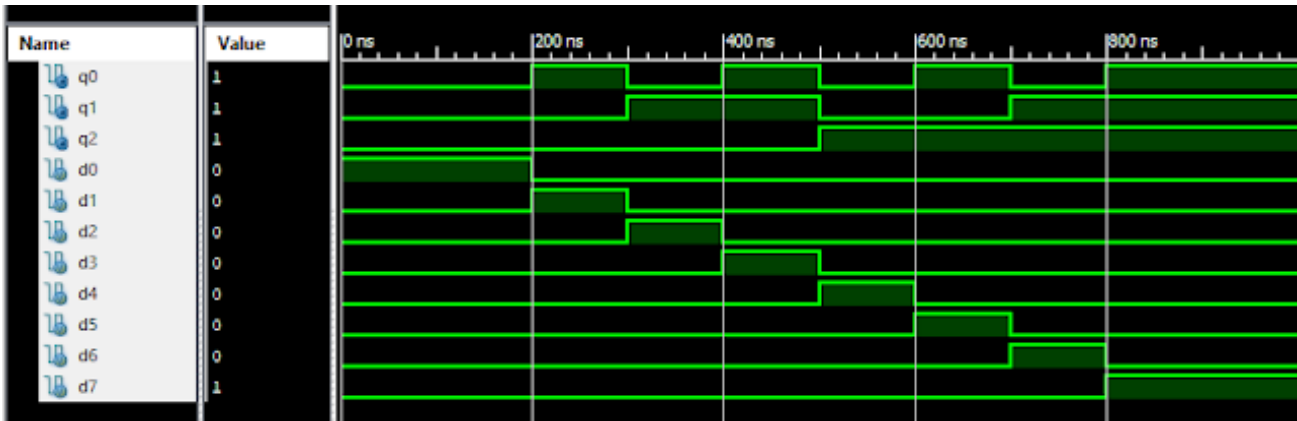
end
endmodule
```

## VERILOG CODE:

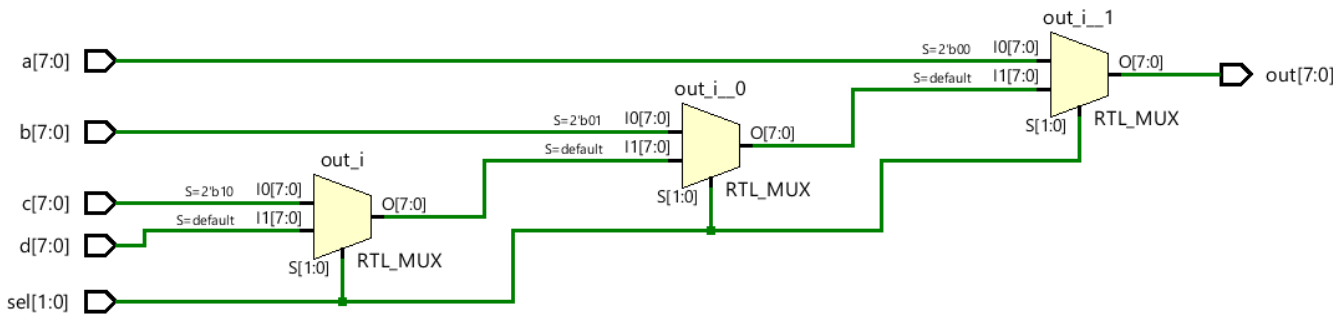
```
module BINARY_TO_ONE_HOT_ENCODER(
    input [2:0] bin_i,
    output [7:0] one_hot_o
);
    parameter bin_w=4;
    parameter one_hot_w=16;
    input [1:0] bin_i;
    output reg [1:0] one_hot_o;

    assign one_hot_o = (1<<bin_i);
endmodule
```

SIMULATION:



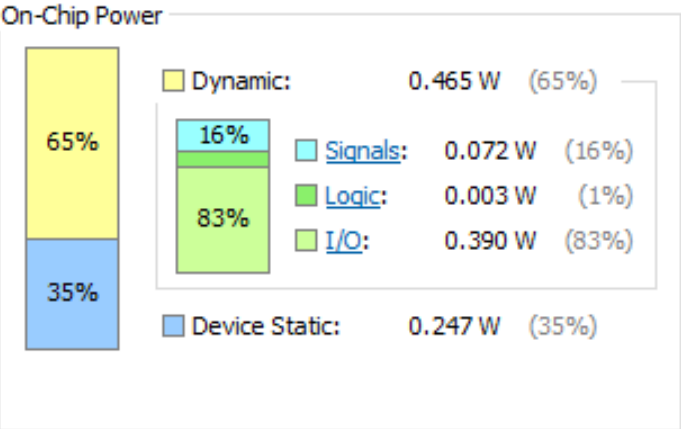
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 0.712 W  
**Junction Temperature:** 26.0 °C  
Thermal Margin: 59.0 °C (40.6 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)



# CODE-7: 4 BIT BCD SYNCHRONOUS COUNTER

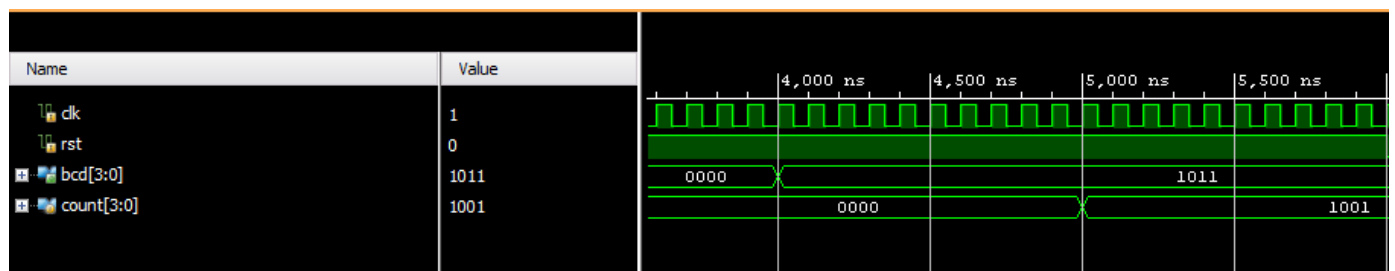
## CODE FOR TESTBENCH:

```
module bcd_counter(  
    input wire clk,          // Clock input  
    input wire rst,          // Reset input  
    output wire [3:0] bcd // 4-bit BCD output  
);  
  
reg [3:0] count;           // 4-bit counter  
  
always @(posedge clk or posedge rst) begin  
    if (rst) begin  
        count <= 4'b0000; // Reset the counter to 0  
    end else begin  
        // Increment the counter  
        if (count == 4'b1001) begin  
            count <= 4'b0000; // Reset to 0 when it reaches 9 (BCD)  
        end else begin  
            count <= count + 1;  
        end  
    end  
end  
  
assign bcd = count; // Output BCD  
  
endmodule
```

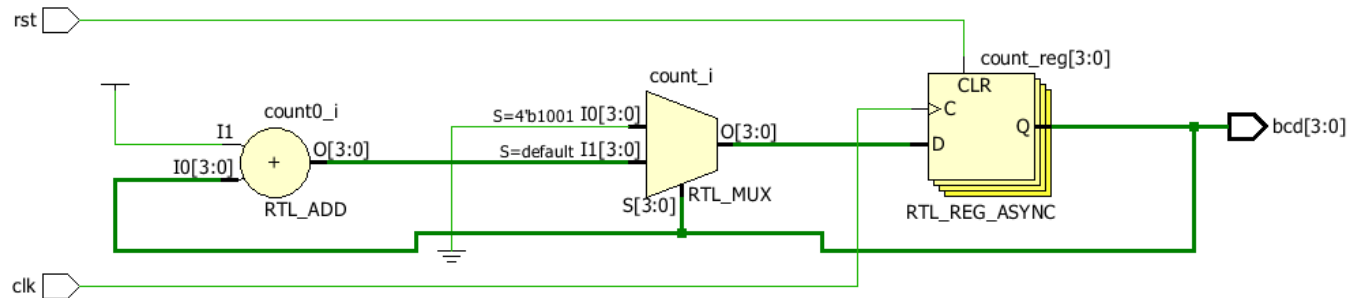
## VERILOG CODE:

```
module BCD_COUNTER(  
    input Clk,  
    input Clear,  
    output [3:0] Count  
);  
    reg [3:0] t;  
    always@(posedge Clk)  
    begin  
        if(Clear)  
            t <= 4'b0000;  
            Count <= 4'b0000;  
        end  
        else  
            begin  
                t <= t+1;  
                if(t==4'b1001)  
                    begin  
                        t <= 4'b0000;  
                    end  
                Count <= t;  
            end  
        end  
    end  
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

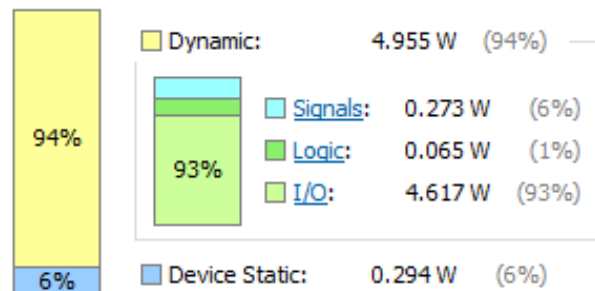


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 5.248 W  
**Junction Temperature:** 32.3 °C  
Thermal Margin: 52.7 °C (36.1 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power



# CODE-8: 4 - BIT CARRY LOOK AHEAD ADDER

## CODE FOR TESTBENCH:

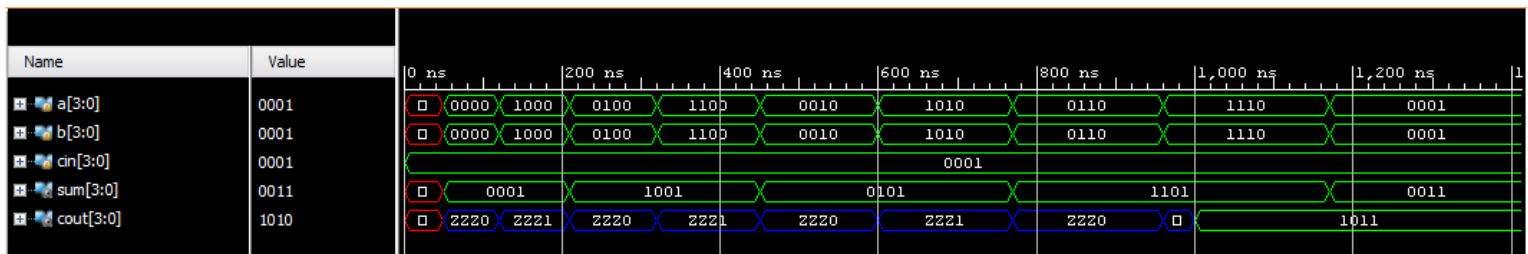
```
module testbench;
reg [3:0] a, b, cin;
wire [3:0] sum, cout;
CARRY_LOOK_AHEAD_ADDER dut(a,b,cin,sum,cout);
initial
begin
$monitor("a=%b b=%b cin=%b sum=%b cout=%b",a,b,cin,sum,cout);
    cin=1;
#50 a[0]=0; a[1]=0; a[2]=0; a[3]=0;
    b[0]=0; b[1]=0; b[2]=0; b[3]=0;
#70 a[0]=0; a[1]=0; a[2]=0; a[3]=1;
    b[0]=0; b[1]=0; b[2]=0; b[3]=1;
#90 a[0]=0; a[1]=0; a[2]=1; a[3]=0;
    b[0]=0; b[1]=0; b[2]=1; b[3]=0;
#110 a[0]=0; a[1]=0; a[2]=1; a[3]=1;
    b[0]=0; b[1]=0; b[2]=1; b[3]=1;
#130 a[0]=0; a[1]=1; a[2]=0; a[3]=0;
    b[0]=0; b[1]=1; b[2]=0; b[3]=0;
#150 a[0]=0; a[1]=1; a[2]=0; a[3]=1;
    b[0]=0; b[1]=1; b[2]=0; b[3]=1;
#170 a[0]=0; a[1]=1; a[2]=1; a[3]=0;
    b[0]=0; b[1]=1; b[2]=1; b[3]=0;
#190 a[0]=0; a[1]=1; a[2]=1; a[3]=1;
    b[0]=0; b[1]=1; b[2]=1; b[3]=1;
#210 a[0]=1; a[1]=0; a[2]=0; a[3]=0;
    b[0]=1; b[1]=0; b[2]=0; b[3]=0;
end
endmodule
```



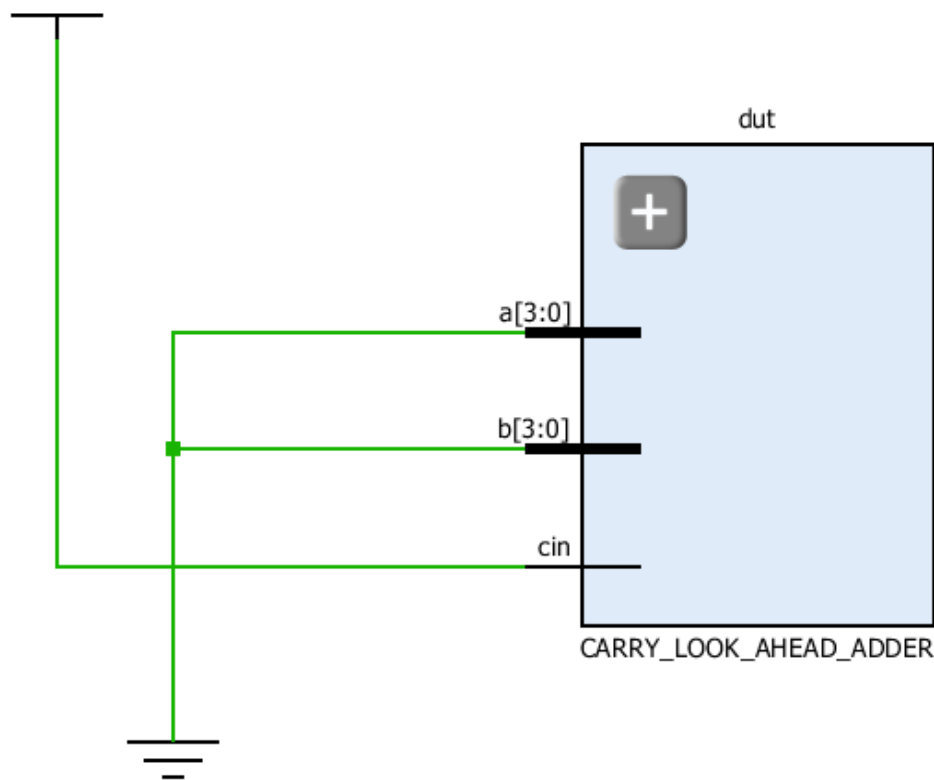
## VERILOG CODE:

```
module CARRY_LOOK_AHEAD_ADDER(  
    input [3:0] a,  
    input [3:0] b,  
    input cin,  
    output [3:0] sum,  
    output cout  
);  
    and (g0,a[0],b[0]),  
    (g1,a[1],b[1]),  
    (g2,a[2],b[2]),  
    (g3,a[3],b[3]);  
    xor (p0,a[0],b[0]),  
    (p1,a[1],b[1]),  
    (p2,a[2],b[2]),  
    (p3,a[3],b[3]);  
    xor (sum[0],p0,cin),  
    (sum[1],p1,c0),  
    (sum[2],p2,c1),  
    (sum[3],p3,c2);  
    assign c0= g0 | (p0 & cin),  
    c1= g1 | (p1 & g0) | (p1 & p0 & cin),  
    c2= g2 | (p2 & g1) | (p2 & p1 & g0) | (p2 & p1 & p0 & cin),  
    c3= g3 | (p3 & g2) | (p3 & p2 & g1) | (p3 & p2 & p1 & g0) | (p3 & p2 & p1 & p0 & cin);  
    assign cout=c3;  
  
endmodule
```

## SIMULATION:



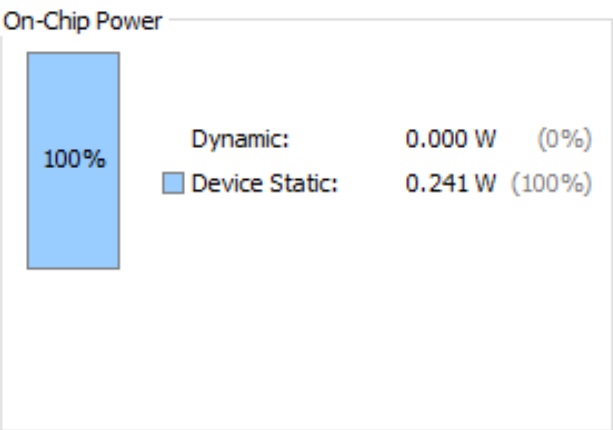
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>0.241 W</b>
<b>Junction Temperature:</b>	<b>25.3 °C</b>
Thermal Margin:	59.7 °C (41.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	<a href="#">Low</a>



# CODE-9: N - BIT COMPARATOR

## CODE FOR TESTBENCH:

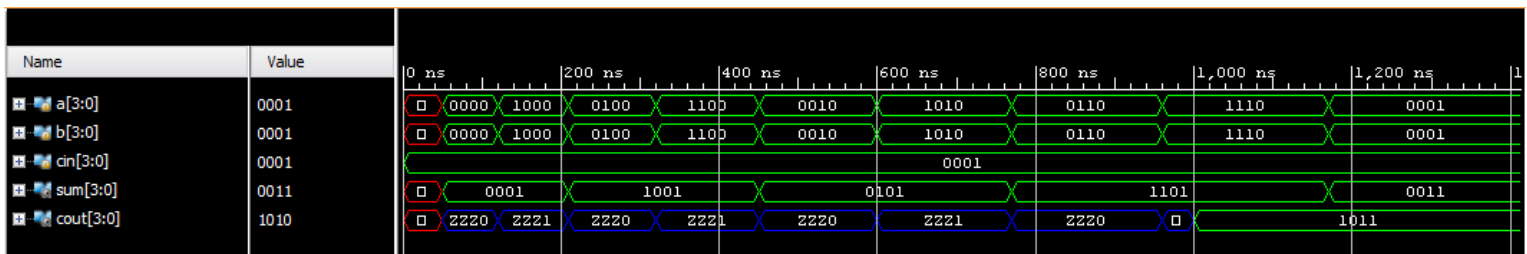
```
module testbench;
reg [1:0] a,b;
wire L,E,G;
N_BIT_COMPARATOR dut(a,b,L,E,G);
initial
begin
$monitor("a=%b b=%b L=%b E=%b G=%b",a,b,L,E,G);
#100 a[0]=0; a[1]=0;
      b[0]=0; b[1]=0;
#200 a[0]=0; a[1]=1;
      b[0]=0; b[1]=1;
#300 a[0]=1; a[1]=0;
      b[0]=1; b[1]=0;
#400 a[0]=1; a[1]=1;
      b[0]=1; b[1]=1;
#500 a[0]=0; a[1]=0;
      b[0]=0; b[1]=0;
#600 a[0]=0; a[1]=1;
      b[0]=0; b[1]=1;
end
endmodule
```

---

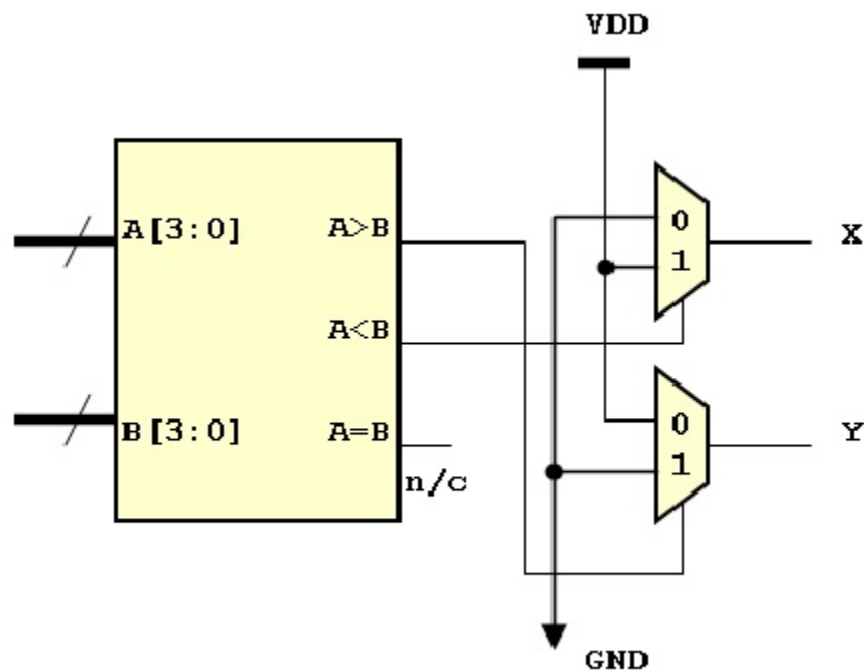
## VERILOG CODE:

```
module N_BIT_COMPARATOR(  
    input [1:0] a,  
    input [1:0] b,  
    output L,  
    output G,  
    output E  
);  
parameter n=32;  
input [1:0] a,b;  
output L,G,E;  
reg L=0, G=0, E=0;  
always@(a,b)  
begin  
    if(a>b)  
    begin  
        L=0; E=0; G=1;  
    end  
    else if (a<b)  
    begin  
        L=1; E=0; G=0;  
    end  
    else  
    begin  
        L=0; E=1; G=0;  
    end  
end  
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

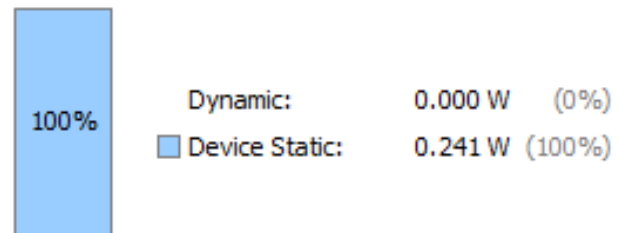


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 0.241 W  
**Junction Temperature:** 25.3 °C  
Thermal Margin: 59.7 °C (41.1 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power



# CODE-10: SERIAL IN SERIAL OUT SHIFT REGISTER

## CODE FOR TESTBENCH:

```
module testbench;
reg [3:0] Width;
reg Clk,Rst;
wire [3:0] Count;

RING_COUNTER dut(Clk,Rst,Width,Count);

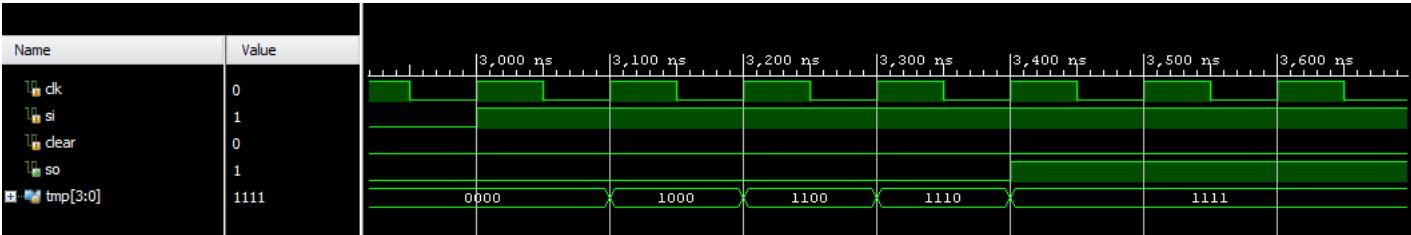
initial
begin
$monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
end

always
begin
#50 Clk=~Clk;
end
initial
begin
#100 Rst=1;
#100 Rst=0;
$finish;
end
endmodule
```

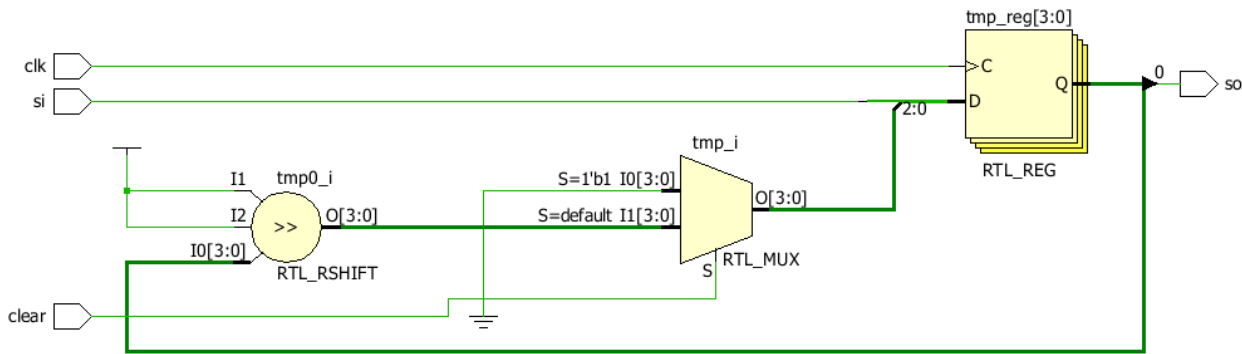
## VERILOG CODE:

```
module SISO_REG(
input clk,
input si,
input clear,
output so
);
reg [3:0] tmp;
always@(posedge clk)
begin
if(clear)
tmp <=4'b0000;
else
tmp <= tmp >>1;
tmp[3] <= si;
end
assign so = tmp;
endmodule
```

# SIMULATION:



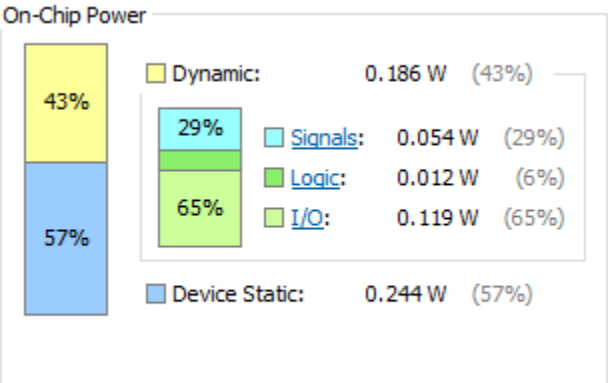
# RTL SCHEMATIC:



# POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.43 W
Junction Temperature:	25.6 °C
Thermal Margin:	59.4 °C (40.9 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



# CODE-1 1: SERIAL IN PARALLEL OUT SHIFT REGISTER

## CODE FOR TESTBENCH:

```
module testbench;
  reg clk,clear;
  reg [3:0] din;
  wire [3:0] dout;

  SIPO_REG dut(clk,clear,din,dout);
  initial
  begin
    $monitor("clk=%b clear=%b din=%b dout=%b",clk,clear,din,dout);

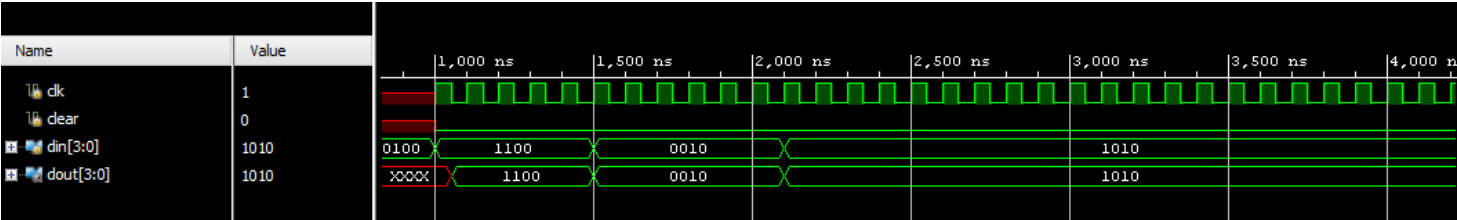
    #100 din[0]=0; din[1]=0; din[2]=0; din[3]=0;
    #200 din[0]=0; din[1]=0; din[2]=0; din[3]=1;
    #300 din[0]=0; din[1]=0; din[2]=1; din[3]=0;
    #400 din[0]=0; din[1]=0; din[2]=1; din[3]=1;
    #500 din[0]=0; din[1]=1; din[2]=0; din[3]=0;
    #600 din[0]=0; din[1]=1; din[2]=0; din[3]=1;
  end
endmodule
```

## VERILOG CODE:

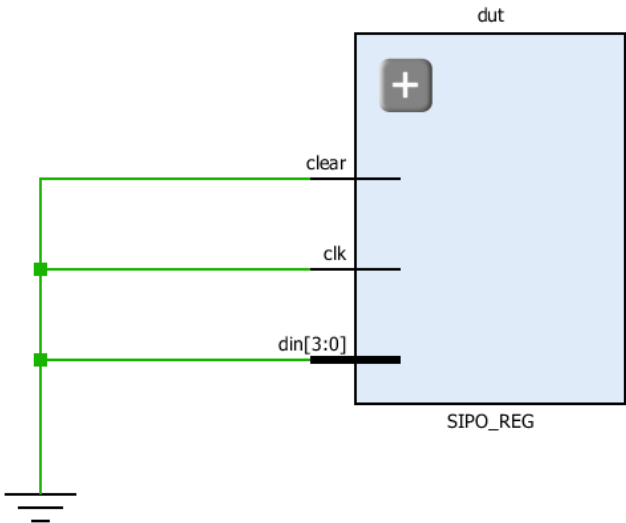
```
module SIPO_REG(
  input clk,
  input clear,
  input [3:0] din,
  output reg [3:0] dout
);
  always@(posedge clk)
  begin
    if(clear)
      dout <= 4'b0000;
    else
      dout <= din;
    end
endmodule
```



SIMULATION:



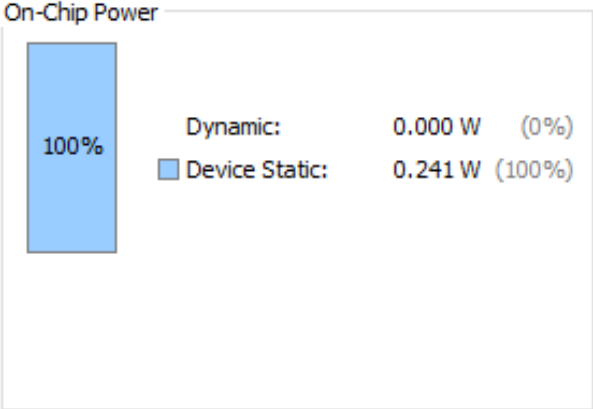
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.241 W
Junction Temperature:	25.3 °C
Thermal Margin:	59.7 °C (41.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



# CODE-12: PARALLEL IN PARALLEL OUT SHIFT REGISTER

## CODE FOR TESTBENCH:

```
module testbench;
    reg clk,clear;
    reg [3:0] din;
    wire [3:0] dout;

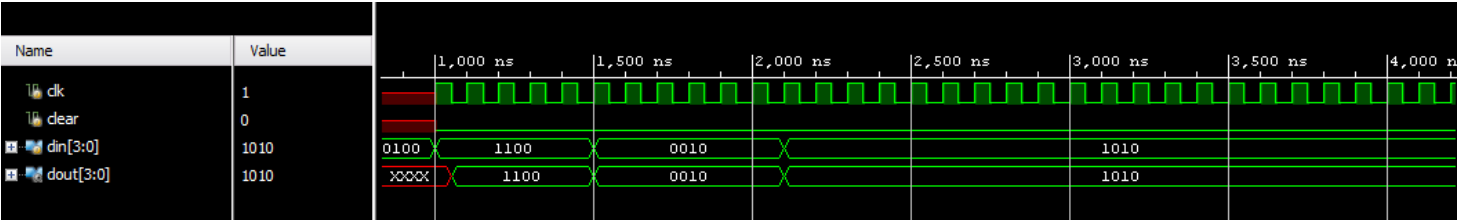
    PIPO_REG dut(clk,clear,din,dout);
    initial
    begin
        $monitor("clk=%b clear=%b din=%b dout=%b",clk,clear,din,dout);

        #100 din[0]=0; din[1]=0; din[2]=0; din[3]=0;
        #200 din[0]=0; din[1]=0; din[2]=0; din[3]=1;
        #300 din[0]=0; din[1]=0; din[2]=1; din[3]=0;
        #400 din[0]=0; din[1]=0; din[2]=1; din[3]=1;
        #500 din[0]=0; din[1]=1; din[2]=0; din[3]=0;
        #600 din[0]=0; din[1]=1; din[2]=0; din[3]=1;
    end
endmodule
```

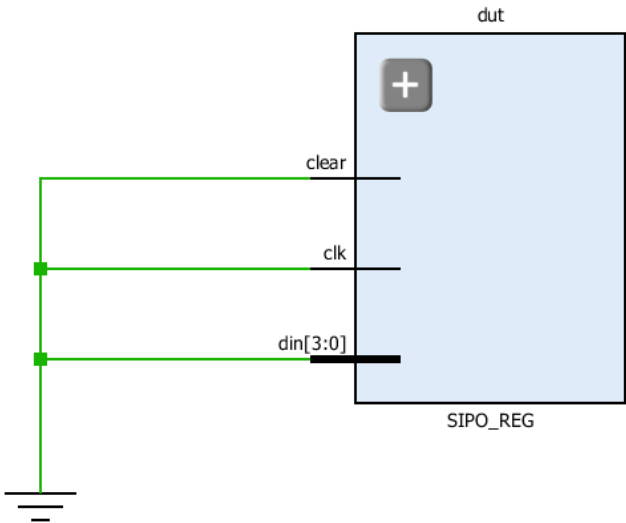
## VERILOG CODE:

```
module PIPO_REG(
    input clk,
    input clear,
    input [3:0] din,
    output reg [3:0] dout
);
    always@(posedge clk)
    begin
        if(clear)
            dout <= 4'b0000;
        else
            dout <= din;
        end
    endmodule
```

SIMULATION:



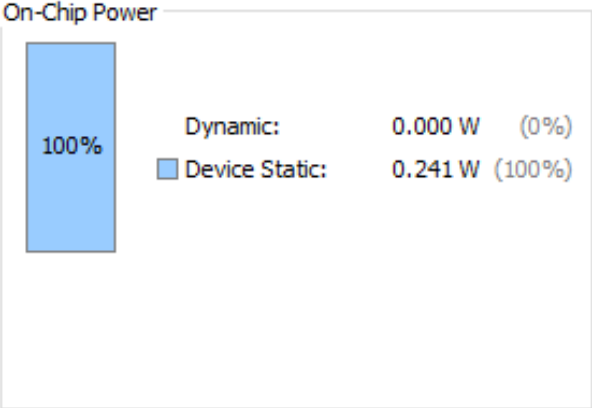
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.241 W
Junction Temperature:	25.3 °C
Thermal Margin:	59.7 °C (41.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



# CODE-13: PARALLEL IN SERIAL OUT SHIFT REGISTER

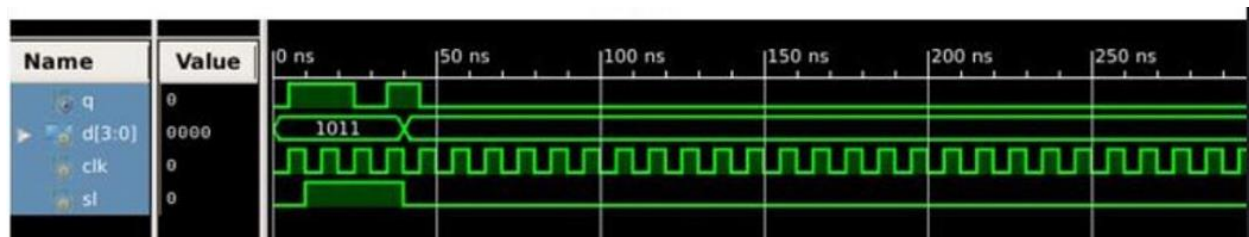
## CODE FOR TESTBENCH:

```
module s1(  
    input a,b,s1,  
    output q  
);  
assign q = (~s1&b) | (s1&a);  
endmodule  
  
module dff(  
    input d,clk,  
    output q  
);  
reg q=0;  
always@(posedge clk)  
begin  
    q <= d;  
end  
endmodule  
  
module PISO_REG(  
    input [3:0] d,  
    input clk,  
    input s1,  
    output q  
);  
wire q1,q2,q3,d1,d2,d3;  
dff a(d[3],clk,q1);  
s1 a1(q1,d[2],s1,d1);  
dff b(d1,clk,q2);  
s1 b1(q2,d[1],s1,d2);  
dff c(d2,clk,q3);  
s1 c1(q3,d[0],s1,d3);  
dff dd(d3,clk,q);  
endmodule
```

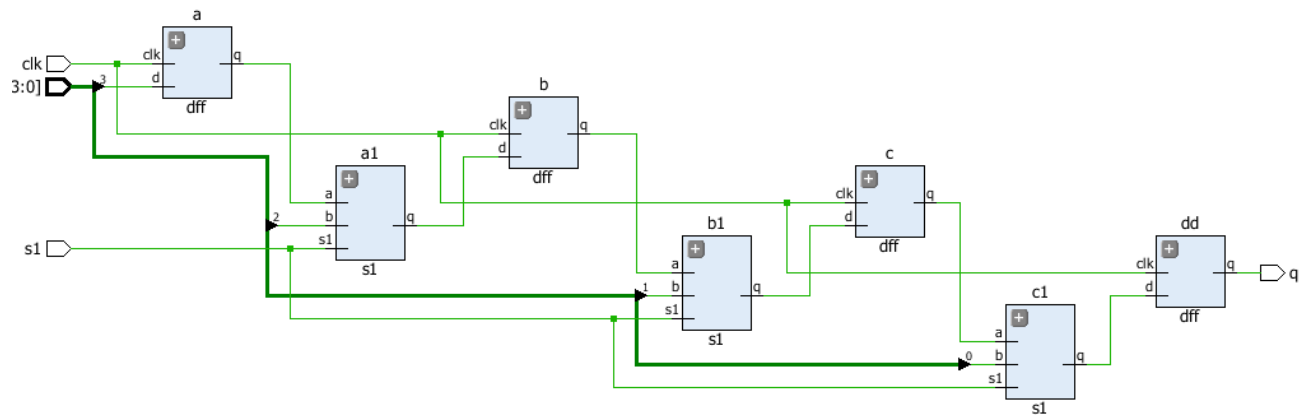
## VERILOG CODE:

```
module s1(  
    input a,b,s1,  
    output q  
);  
assign q = (~s1&b) | (s1&a);  
endmodule  
  
module dff(  
    input d,clk,  
    output q  
);  
    reg q=0;  
    always@(posedge clk)  
    begin  
        q <= d;  
    end  
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

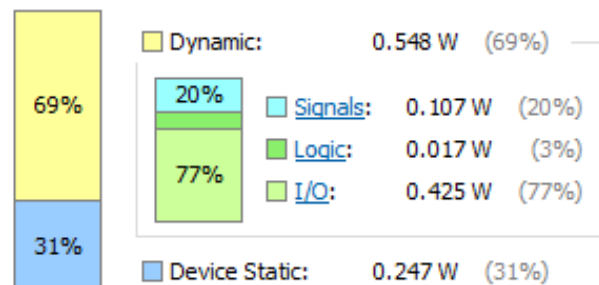


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 0.796 W  
**Junction Temperature:** 26.1 °C  
Thermal Margin: 58.9 °C (40.6 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power



# CODE-14: BIDIRECTIONAL SHIFT REGISTER

## CODE FOR TESTBENCH:

```
module testbench;
  reg [3:0] Width;
  reg Clk,Rst;
  wire [3:0] Count;

  RING_COUNTER dut(Clk,Rst,Width,Count);

  initial
  begin
    $monitor("Clk=%b Rst=%b Width=%b Count=%b",Clk,Rst,Width,Count);
  end

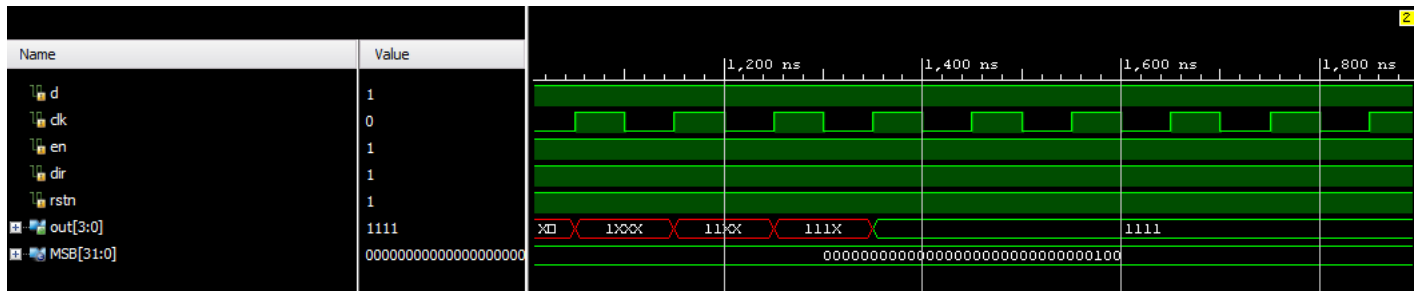
  always
  begin
    #50 Clk=~Clk;
  end

  initial
  begin
    #100 Rst=1;
    #100 Rst=0;
    $finish;
  end
endmodule
```

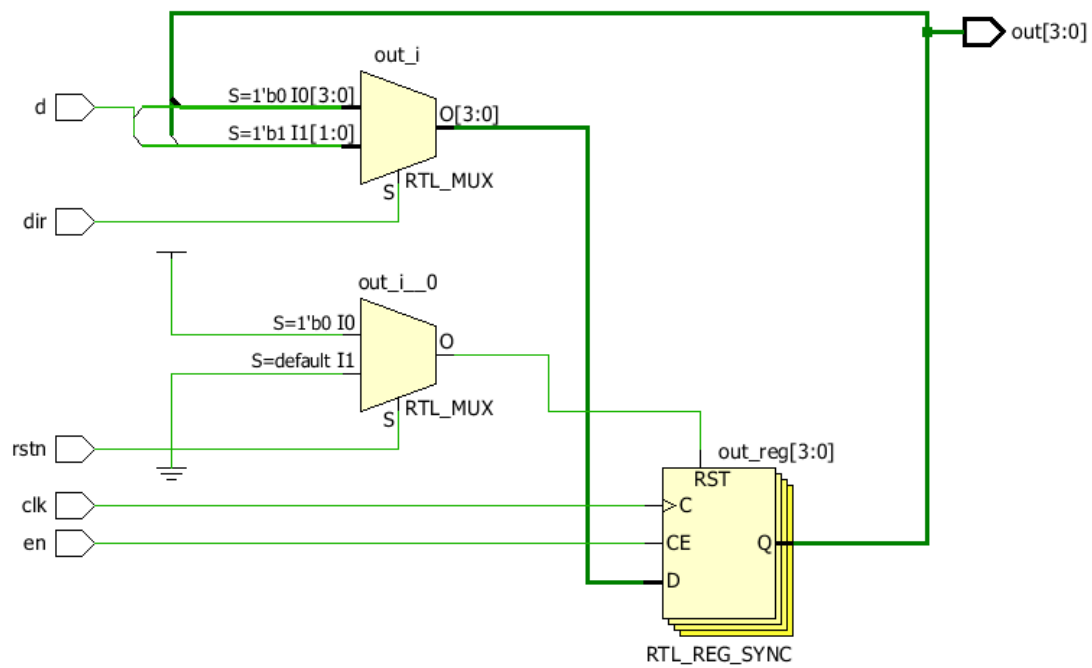
## VERILOG CODE:

```
module BIDIRECTIONAL_SHIFT_REG
#(parameter MSB=4)
(
  input d,
  input clk,
  input en,
  input dir,
  input rstn,
  output reg [MSB-1:0] out
);
  always@(posedge clk)
  if(!rstn)
    out <= 0;
  else
  begin
    if(en)
      case (dir)
        0: out <= {out[MSB-2:0],d};
        1: out <= {d,out[MSB-1:1]};
      endcase
    else
      out <= out;
    end
  end
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

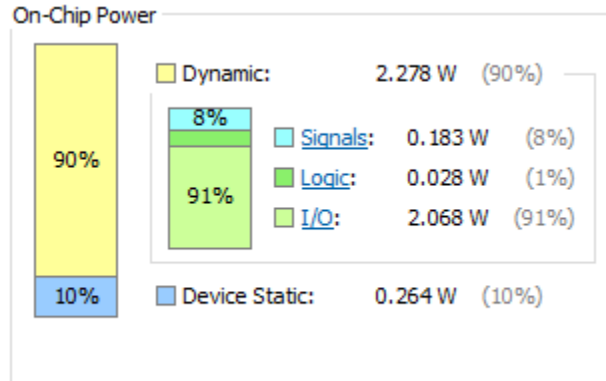




## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 2.542 W  
**Junction Temperature:** 28.6 °C  
Thermal Margin: 56.4 °C (38.8 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)



# CODE-15: PRBS SEQUENCE GENERATOR

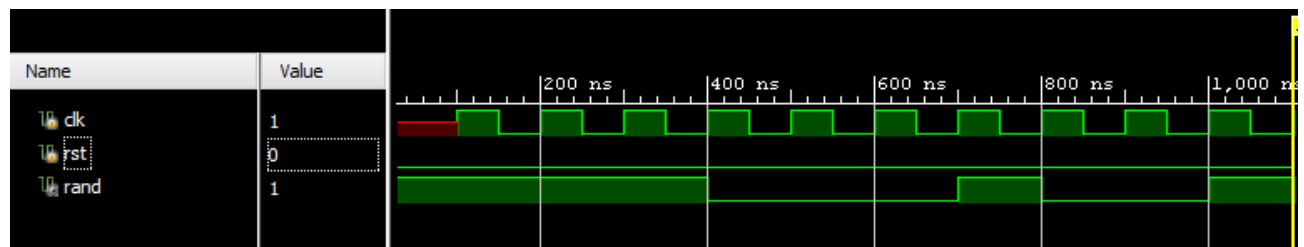
## CODE FOR TESTBENCH:

```
module tb_PRBS_SEQUENCE_GENERATOR;
    reg clk;
    reg rst;
    wire rand;
    PRBS_SEQUENCE_GENERATOR uut (
        .clk(clk),
        .rst(rst),
        .rand(rand)
    );
    always begin
        #5 clk = ~clk;
    end
    initial begin
        rst = 1;
        #10 rst = 0;
    end
    initial begin
        $display("Time\tPRBS Output");
        $monitor("%d\t%b", $time, rand);
        #100;
        $finish;
    end
endmodule
```

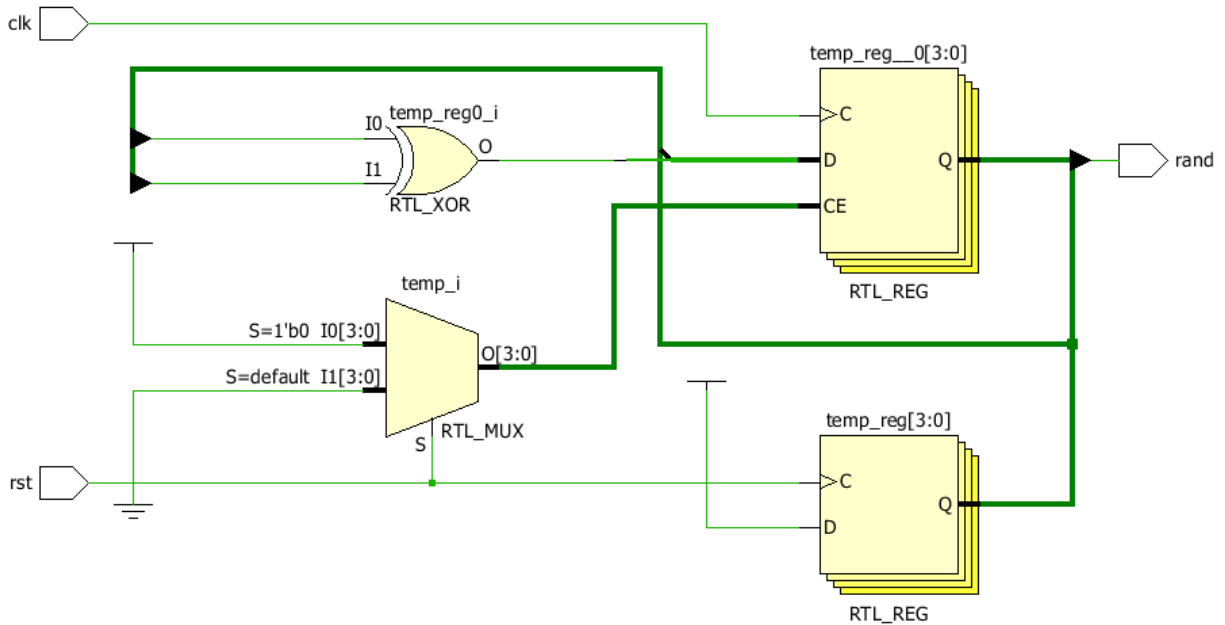
## VERILOG CODE:

```
module PRBS_SEQUENCE_GENERATOR(  
input clk,rst,  
output rand  
);  
  
reg [3:0] temp;  
always@(posedge rst)  
begin  
temp <= 4'hf;  
end  
always@(posedge clk)  
begin  
if (~rst)  
begin  
temp <= {temp[0]^temp[1],temp[3],temp[2],temp[1]};  
end  
end  
assign rand = temp[0];  
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

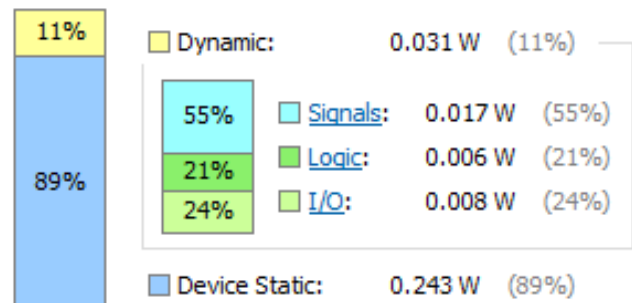


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 0.274 W  
**Junction Temperature:** 25.4 °C  
Thermal Margin: 59.6 °C (41.1 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power



# CODE-16: 8 – BIT SUBTRACTOR

## CODE FOR TESTBENCH:

```
module testbench;
reg [7:0] a,b;
wire [7:0] result;
SUBTRACTOR_8_BIT dut(a,b,result);

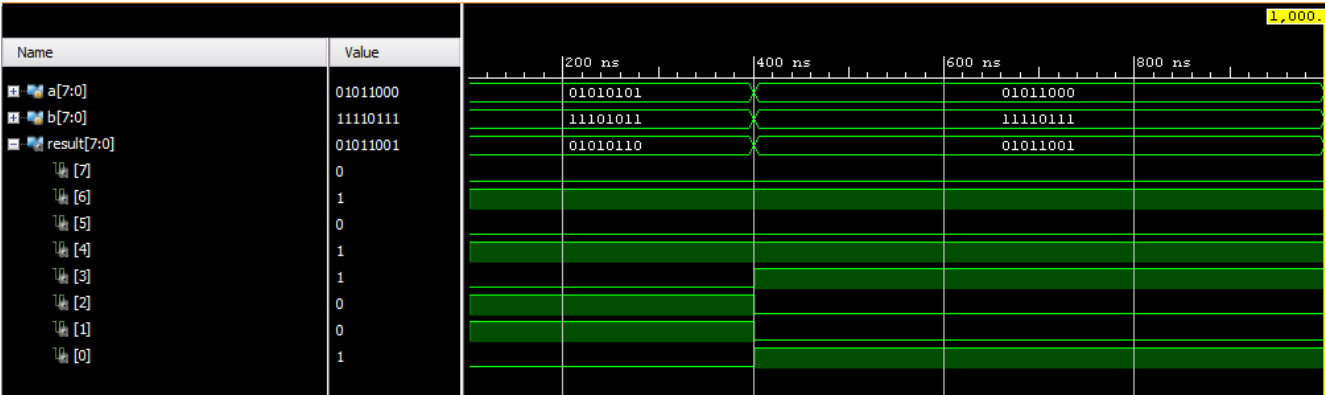
initial
begin
$monitor("a=%b b=%b result=%b",a,b,result);
#100 a[0]=1; a[1]=0; a[2]=1; a[3]=0; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
    b[0]=1; b[1]=1; b[2]=0; b[3]=1; b[4]=0; b[5]=1; b[6]=1; b[7]=1;
#300 a[0]=0; a[1]=0; a[2]=0; a[3]=1; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
    b[0]=1; b[1]=1; b[2]=1; b[3]=0; b[4]=1; b[5]=1; b[6]=1; b[7]=1;
end
endmodule
```

## VERILOG CODE:

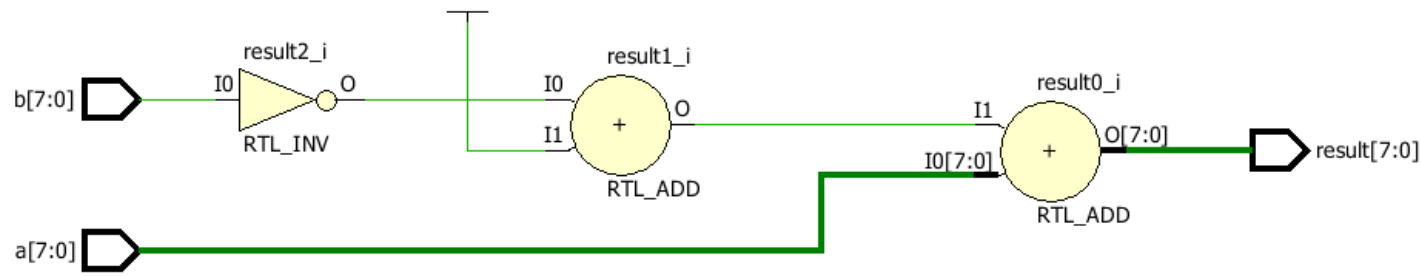
```
module SUBTRACTOR_8_BIT(
    input [7:0] a,
    input [7:0] b,
    output reg [7:0] result
);

    reg neg_b;
    always@(a or b)
    begin
        neg_b = ~ b + 1;
        result = a + neg_b;
    end
endmodule
```

SIMULATION:



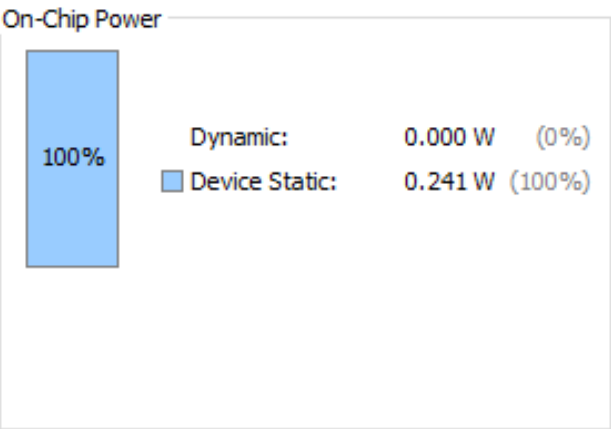
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.241 W
Junction Temperature:	25.3 °C
Thermal Margin:	59.7 °C (41.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



# CODE-17: 8 – BIT ADDER SUBTRACTOR

## CODE FOR TESTBENCH:

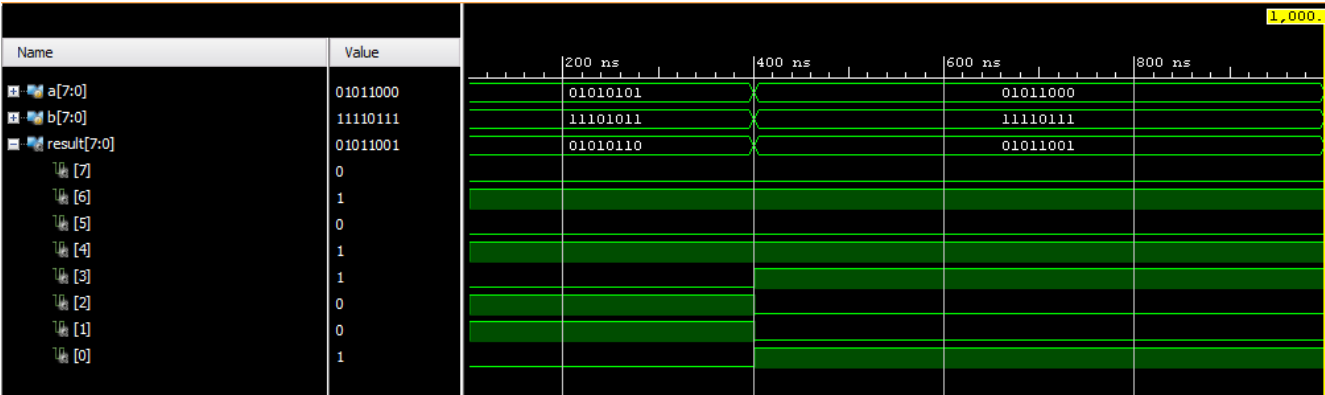
```
module testbench;
reg [7:0] a,b;
wire [7:0] result;
SUBTRACTOR_8_BIT dut(a,b,result);

initial
begin
$monitor("a=%b b=%b result=%b",a,b,result);
#100 a[0]=1; a[1]=0; a[2]=1; a[3]=0; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
    b[0]=1; b[1]=1; b[2]=0; b[3]=1; b[4]=0; b[5]=1; b[6]=1; b[7]=1;
#300 a[0]=0; a[1]=0; a[2]=0; a[3]=1; a[4]=1; a[5]=0; a[6]=1; a[7]=0;
    b[0]=1; b[1]=1; b[2]=1; b[3]=0; b[4]=1; b[5]=1; b[6]=1; b[7]=1;
    end
endmodule
```

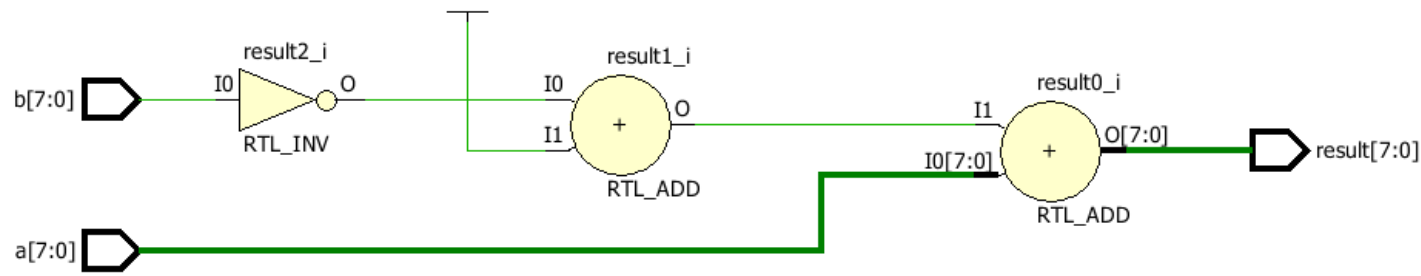
## VERILOG CODE:

```
module ADDER_SUBTRACTOR_8_BIT(
    input [7:0] a,
    input [7:0] b,
    input mode,
    output reg [7:0] result,
    output reg ovfl
);
wire [7:0] a,b;
wire mode;
reg [7:0] neg_b;
always@(a or b or mode)
begin
    if(mode==0)
    begin
        result = a+b;
        ovfl = (a[7] & b[7] & ~result[7]) | (~a[7] & ~b[7] & result[7]);
    end
    else
    begin
        neg_b = ~b+1;
        result = a + neg_b;
        ovfl = (a[7] & neg_b[7] & ~result[7]) | (~a[7] & ~neg_b[7] & result[7]);
    end
end
endmodule
```

SIMULATION:



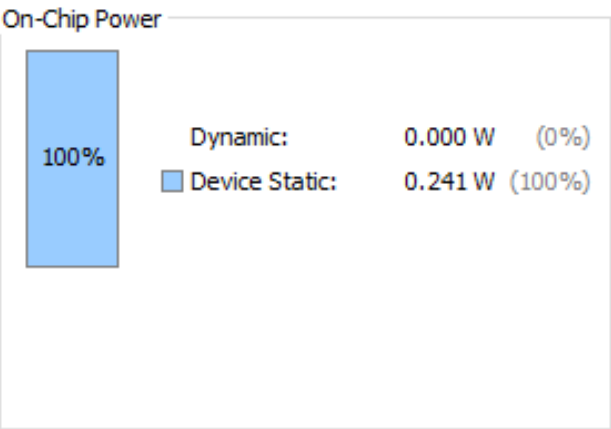
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.241 W
Junction Temperature:	25.3 °C
Thermal Margin:	59.7 °C (41.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low





# CODE-18: 4 – BIT MULTIPLYER

## CODE FOR TESTBENCH:

```
module testbench;
reg [3:0]a,b;
wire [7:0] product;

    MULTIPLYER dut(a,b,product);
    initial
    begin
        $monitor("a=%b b=%b product=%b",a,b,product);

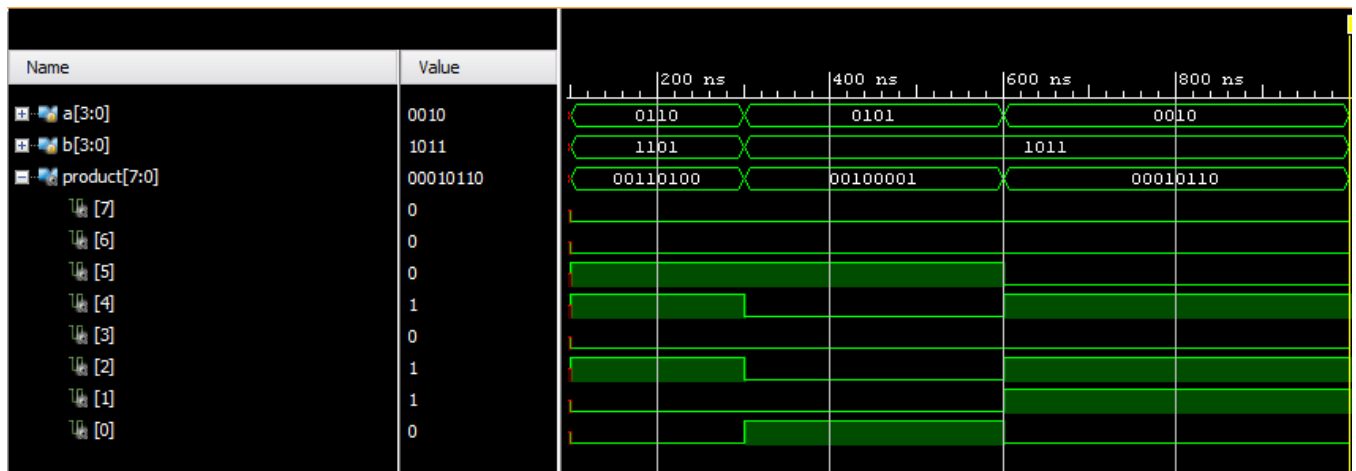
        #100 a[0]=0; a[1]=1; a[2]=1; a[3]=0;
            b[0]=1; b[1]=0; b[2]=1; b[3]=1;
        #200 a[0]=1; a[1]=0; a[2]=1; a[3]=0;
            b[0]=1; b[1]=1; b[2]=0; b[3]=1;
        #300 a[0]=0; a[1]=1; a[2]=0; a[3]=0;
            b[0]=1; b[1]=1; b[2]=0; b[3]=1;
    end
endmodule
```

## VERILOG CODE:

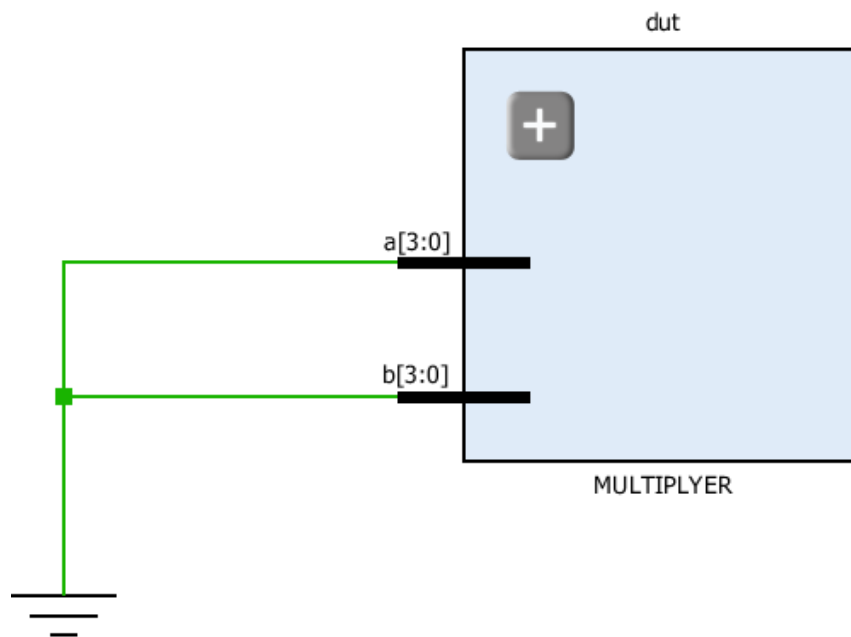
```
module MULTIPLYER(
    input [3:0] a,
    input [3:0] b,
    output [7:0] product
);
    wire [3:0] m0;
    wire [4:0] m1;
    wire [5:0] m2;
    wire [6:0] m3;
    wire [7:0] s1,s2,s3;
    assign m0={4{a[0]}}&b[3:0];
    assign m1={4{a[1]}}&b[3:0];
    assign m2={4{a[2]}}&b[3:0];
    assign m3={4{a[3]}}&b[3:0];

    assign s1=m0+(m1<<1);
    assign s2=s1+(m2<<1);
    assign s3=s2+(m3<<1);
    assign product= s3;
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:



## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** **0.241 W**

**Junction Temperature:** **25.3 °C**

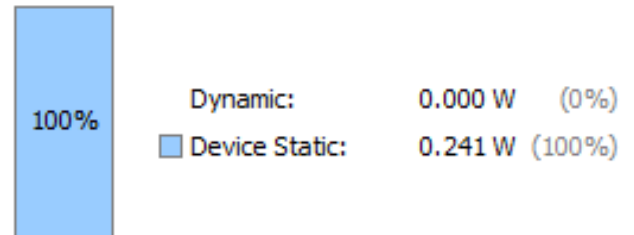
Thermal Margin: 59.7 °C (41.1 W)

Effective  $\theta_{JA}$ : 1.4 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: [Low](#)

### On-Chip Power



# CODE-19: FIXED POINT DIVISION

## CODE FOR TESTBENCH:

```
module testbench;
reg [7:0]a;
reg [3:0]b;
reg start;
wire [7:0] result;

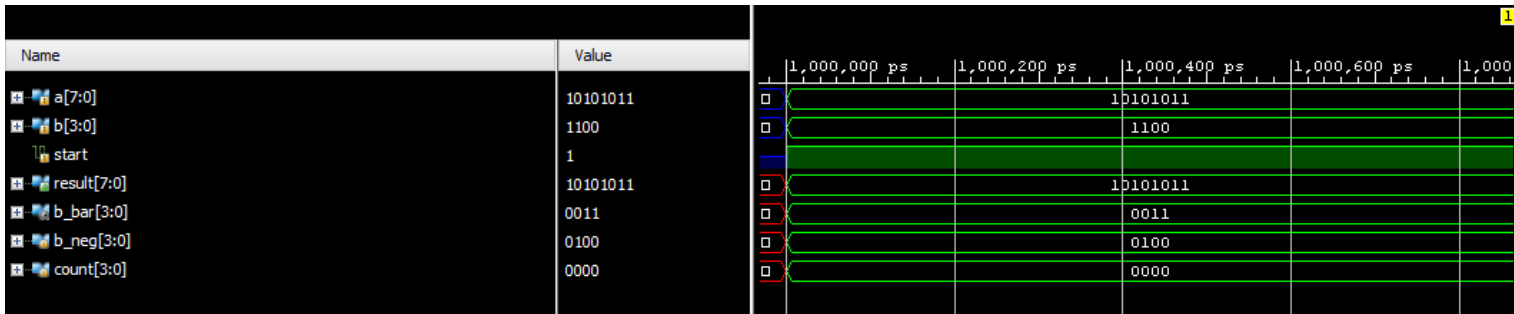
    FIXED_POINT_DIVISION dut(a,b,start,result);
    initial
    begin
        $monitor("a=%b b=%b start=%b result=%b",a,b,start,result);

        #100 a[0]=0; a[1]=1; a[2]=1; a[3]=0; a[4]=1; a[5]=0; a[6]=1; a[7]=1;
            b[0]=1; b[1]=0; b[2]=1; b[3]=1;
        #200 a[0]=1; a[1]=0; a[2]=1; a[3]=0; a[4]=0; a[5]=1; a[6]=0; a[7]=0;
            b[0]=1; b[1]=1; b[2]=0; b[3]=1;
        #300 a[0]=0; a[1]=1; a[2]=0; a[3]=0; a[4]=1; a[5]=1; a[6]=1; a[7]=1;
            b[0]=1; b[1]=1; b[2]=0; b[3]=1;
    end
endmodule
```

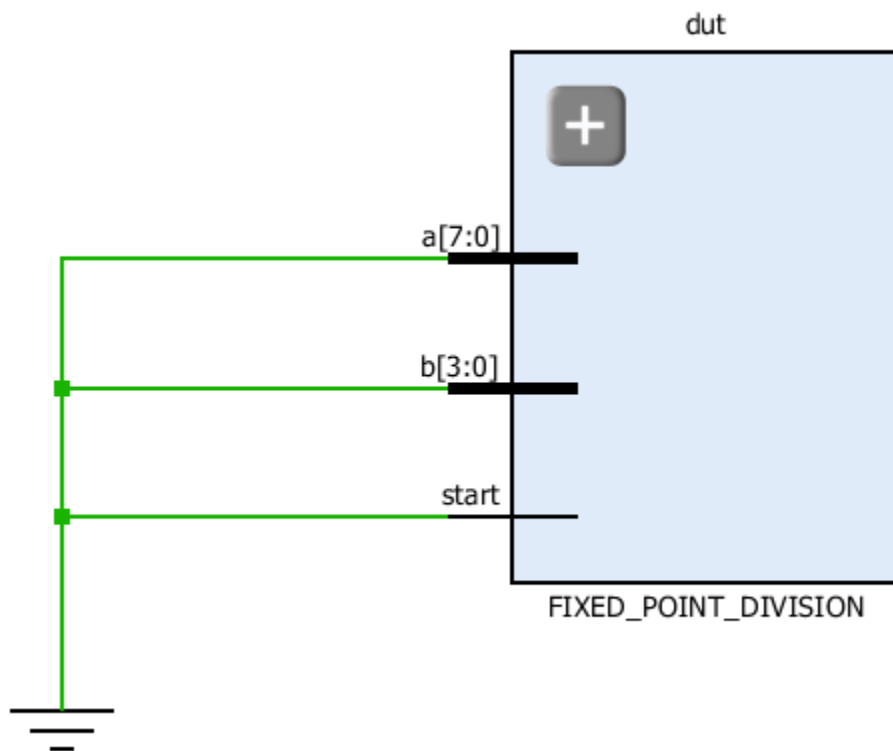
## VERILOG CODE:

```
module FIXED_POINT_DIVISION(  
    input [7:0] a,  
    input [3:0] b,  
    input start,  
    output reg [7:0] result  
);  
    wire[3:0] b_bar;  
    reg [3:0] b_neg;  
  
    reg [3:0] count;  
    assign b_bar=~b;  
    always@(b_bar)  
        b_neg=b_bar+1;  
    always@(posedge start)  
    begin  
        result=a;  
        count=4'b0000;  
        if((a!=0) && (b!=0))  
            while (count)  
            begin  
                result=result<<1;  
                result={(result[7:4] + b), result[3:1],1'b0};  
                count=count-1;  
            end  
            else  
            begin  
                result={(result[7:1],1'b1)};  
                count=count-1;  
            end  
            end  
    end  
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

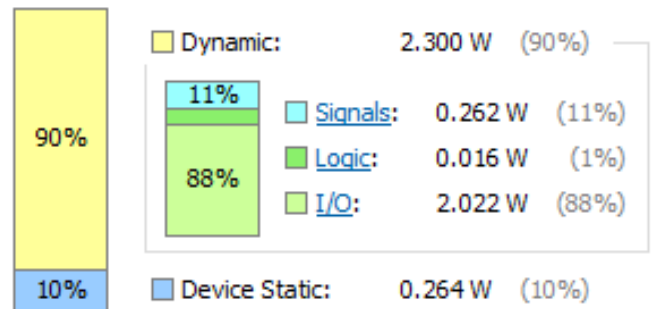


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** **2.564 W**  
**Junction Temperature:** **28.6 °C**  
Thermal Margin: 56.4 °C (38.8 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power



# CODE-20: MASTER SLAVE JK FLIP FLOP

## CODE FOR TESTBENCH:

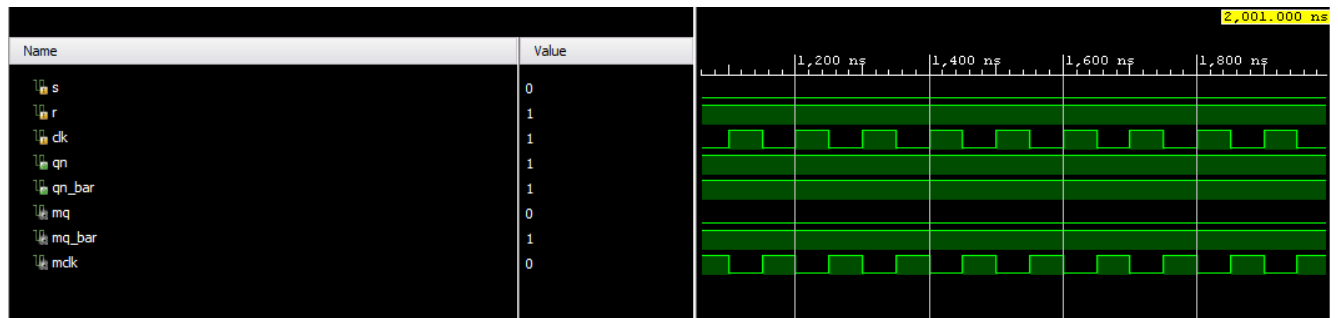
```
module master_slave(  
    input s,r,clk,  
    output qn,qn_bar  
);  
    wire mq;  
    wire mq_bar;  
    wire mclk;  
    assign mclk=~clk;  
    JK_FF master(s,r,clk,mq,mq_bar);  
    JK_FF slave(mq,mq_bar,mclk,qn,qn_bar);  
endmodule
```

## VERILOG CODE:

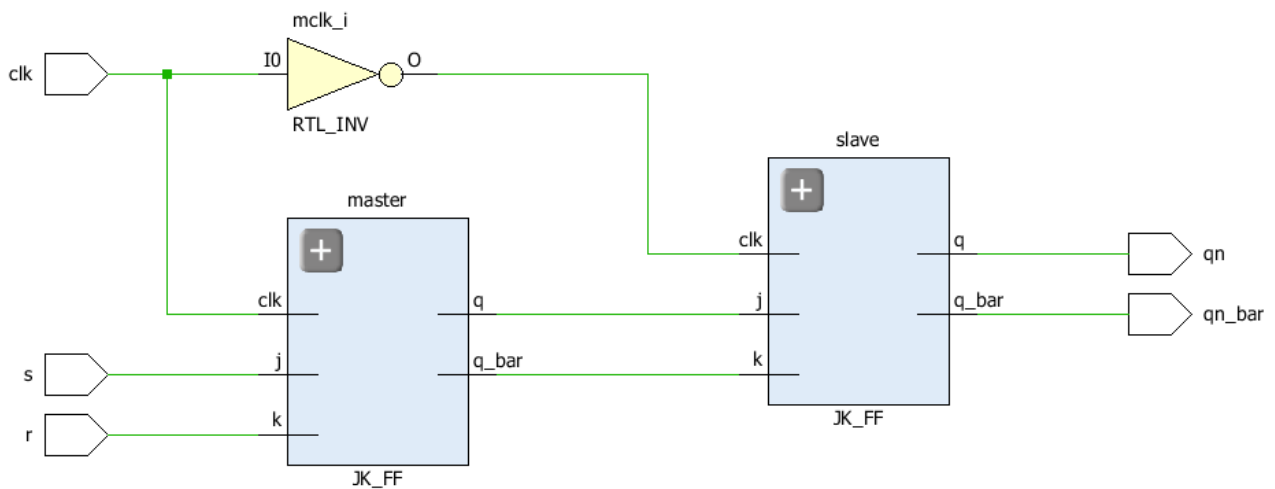
```
module JK_FF(  
    input j,  
    input k,  
    input clk,  
    output reg q,  
    output q_bar  
);  
    assign q_bar=~q;  
    always@(posedge clk)  
    begin  
        case({j,k})  
            2'b00: q<=q;  
            2'b01: q<=0;  
            2'b10: q<=1;  
            2'b11: q<=~q;  
        endcase  
    end  
endmodule  
  
module master_slave(  
    input s,r,clk,  
    output qn,qn_bar  
);  
    wire mq;  
    wire mq_bar;  
    wire mclk;  
    assign mclk=~clk;  
    JK_FF master(s,r,clk,mq,mq_bar);  
    JK_FF slave(mq,mq_bar,mclk,qn,qn_bar);  
endmodule
```



## SIMULATION:



## RTL SCHEMATIC:

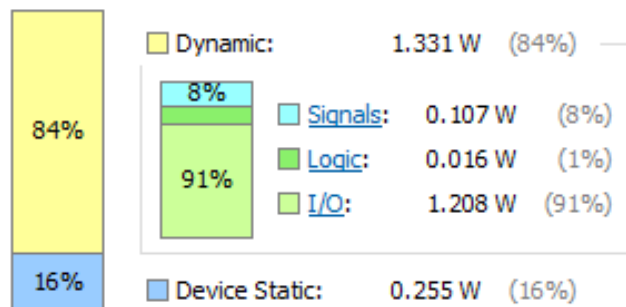


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 1.586 W  
**Junction Temperature:** 27.2 °C  
Thermal Margin: 57.8 °C (39.8 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power



# CODE-21: POSITIVE EDGE DETECTOR

## CODE FOR TESTBENCH:

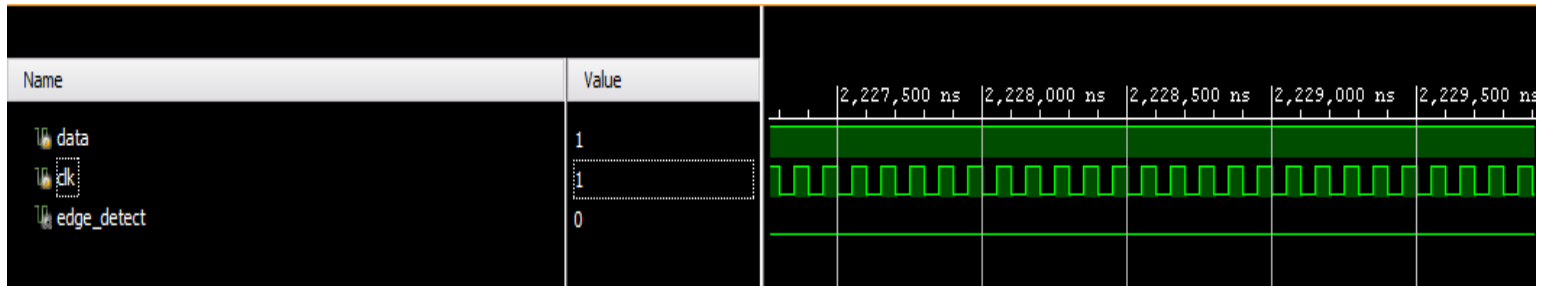
```
module testbench;
  reg data,clk;
  wire edge_detect;
  EDGE_DETECTOR dut(data,clk,edge_detect);
  initial
  begin
    $monitor("data=%b clk=%b edge_detect=%b",data,clk,edge_detect);
  end
  always
  begin
    #50   clk = ~clk;

    end
endmodule
```

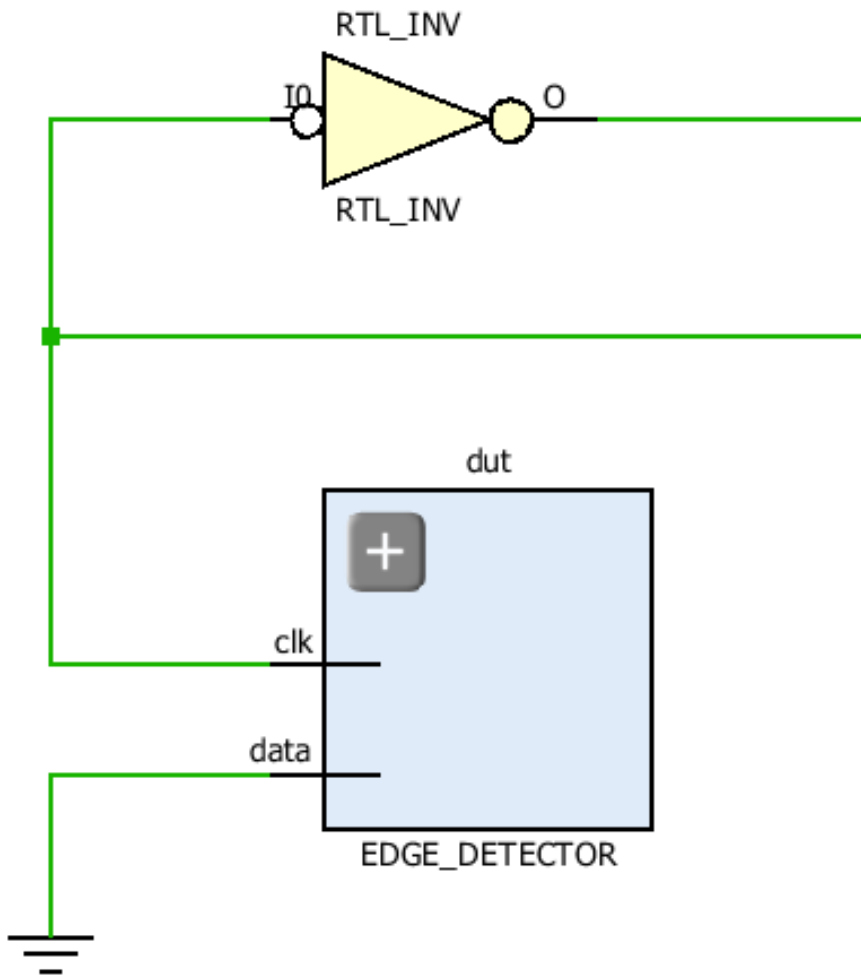
## VERILOG CODE:

```
module EDGE_DETECTOR(
  input data,
  input clk,
  output edge_detect
);
  reg data_d;
  always@(posedge clk)
  begin
    data_d <= data;
  end
  assign edge_detect= data & ~data_d;
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:

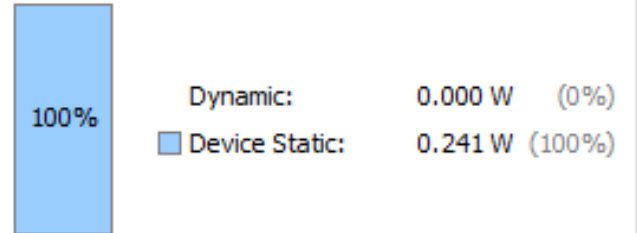


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** **0.241 W**  
**Junction Temperature:** **25.3 °C**  
Thermal Margin: 59.7 °C (41.1 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power



# CODE-22: BCD ADDER

## CODE FOR TESTBENCH:

```
module BCD_Adder_Testbench;
reg [3:0] A, B;
wire [3:0] Sum;
wire CarryOut;
BCD_Adder uut(
    .A(A),
    .B(B),
    .Sum(Sum),
    .CarryOut(CarryOut)
);
initial begin
    $display("Testing BCD Adder");

    A = 4'b0101;
    B = 4'b0011;
    #10 $display("A = %b, B = %b, Sum = %b, CarryOut = %b", A, B, Sum, CarryOut);

    A = 4'b1001;
    B = 4'b1001;
    #10 $display("A = %b, B = %b, Sum = %b, CarryOut = %b", A, B, Sum, CarryOut);

    A = 4'b0000;
    B = 4'b0000;
    #10 $display("A = %b, B = %b, Sum = %b, CarryOut = %b", A, B, Sum, CarryOut);

    $finish;
end
endmodule
```

---

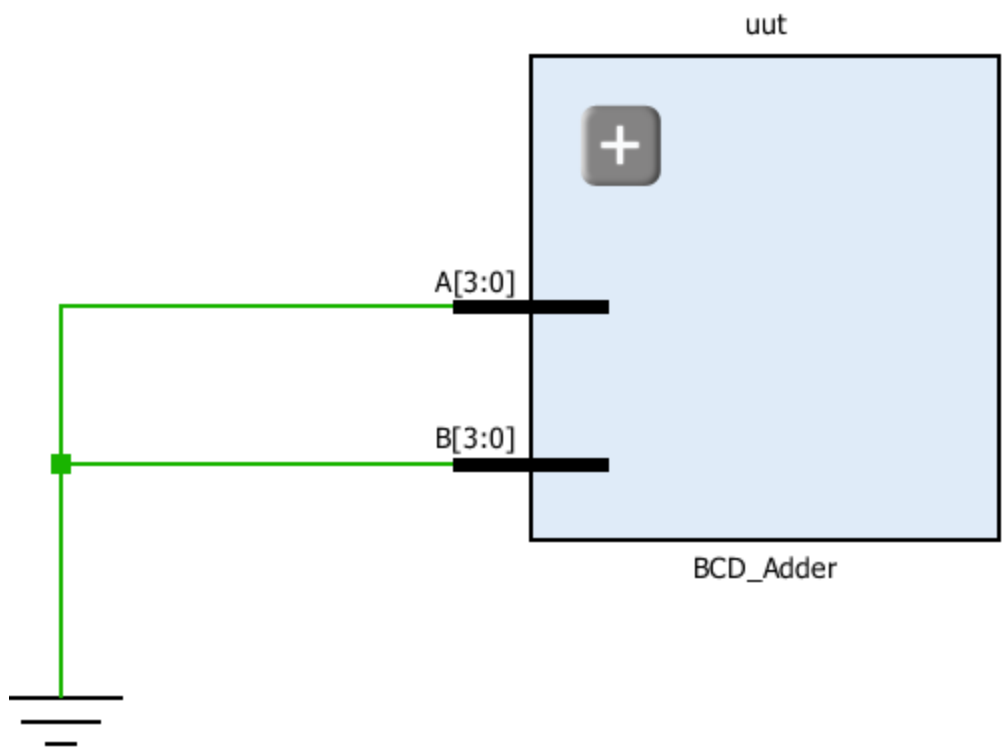
## VERILOG CODE:

```
module BCD_Adder(  
    input [3:0] A,  
    input [3:0] B,  
    output reg [3:0] Sum,  
    output reg CarryOut  
);  
  
always @(*) begin  
    Sum = A + B;  
    if (Sum >= 10) begin  
        Sum = Sum - 10;  
        CarryOut = 1;  
    end else begin  
        CarryOut = 0;  
    end  
end  
  
endmodule
```

## SIMULATION:

Name		Value						
			0 ns	10 ns	20 ns	30 ns	40 ns	50 ns
A[3:0]		1010	0101	1001	0000		1010	
B[3:0]		1111	0011	1001	0000		0011	
Sum[3:0]		0011	1000	0010	0000		0011	
CarryOut		1						

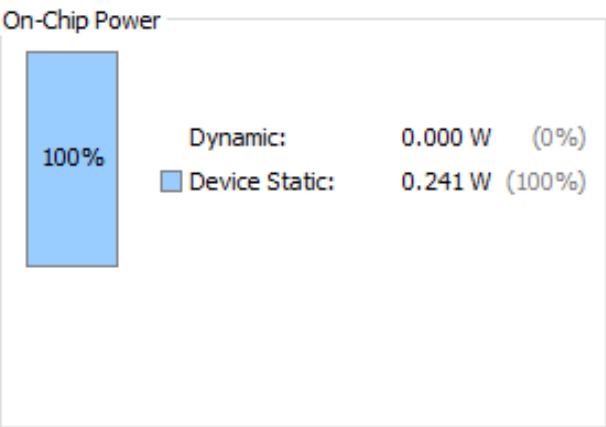
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>0.241 W</b>
<b>Junction Temperature:</b>	<b>25.3 °C</b>
Thermal Margin:	59.7 °C (41.1 W)
Effective $\theta_{JA}$ :	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	<a href="#">Low</a>



# CODE-23: 4-BIT CARRY SELECT ADDER

## CODE FOR TESTBENCH:

```
module testbench;
    reg [3:0] x,y;
    reg carry;
    wire [3:0] s;

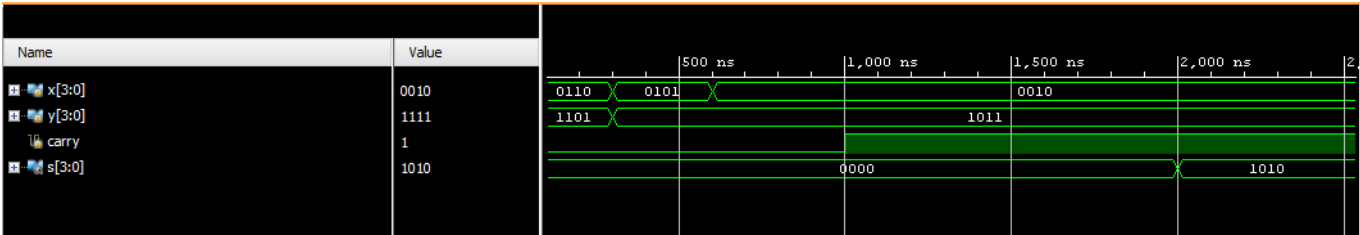
    CARRY_SELECT dut(x,y,carry,s);
    initial
    begin
        $monitor("x=%b y=%b carry=%b s=%b",x,y,carry,s);
        carry = 1;
        carry = ~carry;
        #100 x[0]=0; x[1]=1; x[2]=1; x[3]=0;
            y[0]=1; y[1]=0; y[2]=1; y[3]=1;
        #200 x[0]=1; x[1]=0; x[2]=1; x[3]=0;
            y[0]=1; y[1]=1; y[2]=0; y[3]=1;
        #300 x[0]=0; x[1]=1; x[2]=0; x[3]=0;
            y[0]=1; y[1]=1; y[2]=0; y[3]=1;
        end
    endmodule
```



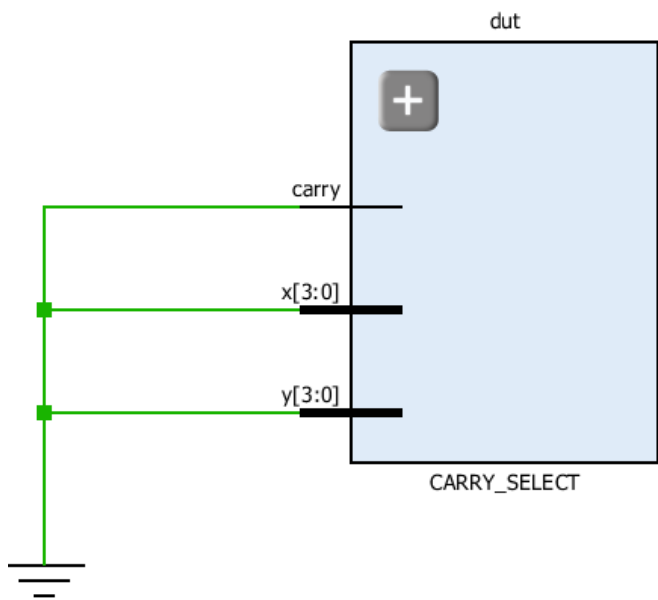
## VERILOG CODE:

```
module FULL_ADDER(  
    input a,  
    input b,  
    input cin,  
    output reg S,cout  
);  
    always@(a or b or cin)  
    begin  
        S = a^b^cin;  
        cout = a&b | b&cin | cin&a;  
    end  
endmodule  
  
module mux(  
    input a,b,  
    input S,  
    output reg y  
);  
    always@(a,b,S)  
    begin  
        y = S&a | S&b;  
    end  
endmodule  
  
module CARRY_SELECT(  
    input [3:0] x,  
    input [3:0] y,  
    input carry,  
    output [3:0] s,  
    output cout  
);  
    wire w1,w2,w3,w4,w5,w6,w7,w8,w9,w10,w11,w12,w13,w14,w15,w16;  
    FULL_ADDER fa0(x[0],y[0],1'b0,w1,w2);  
    FULL_ADDER fa1(x[1],y[1],w2,w3,w4);  
    FULL_ADDER fa2(x[2],y[2],w4,w5,w6);  
  
    FULL_ADDER fa3(x[3],y[3],w6,w7,w8);  
    FULL_ADDER fa4(x[0],y[0],1'b1,w9,w10);  
    FULL_ADDER fa5(x[1],y[1],w10,w11,w12);  
    FULL_ADDER fa6(x[2],y[2],w12,w13,w14);  
    FULL_ADDER fa7(x[3],y[3],w14,w15,w16);  
    mux mu0(w1,w9,carry,s[0]);  
    mux mu1(w3,w11,carry,s[1]);  
    mux mu2(w5,w13,carry,s[2]);  
    mux mu3(w7,w15,carry,s[3]);  
    mux mu4(w8,w16,carry,cout);  
endmodule
```

SIMULATION:



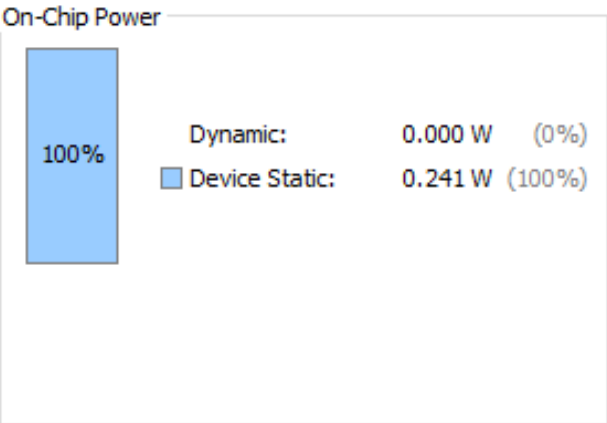
RTL SCHEMATIC:



POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.241 W
Junction Temperature:	25.3 °C
Thermal Margin:	59.7 °C (41.1 W)
Effective θJA:	1.4 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



# CODE-24: MOORE FSM 1010 SEQUENCE DETECTOR

## CODE FOR TESTBENCH:

```
module testbench;
reg din,clk,rst;
wire y;
    MOORE_FSM dut(din,clk,rst,y);
    initial
    begin
        $monitor("din=%b clk=%b rst=%b y=%b",din,clk,rst,y);
    end
    always
    begin
        #50    clk = ~clk;
    end

endmodule
```

## VERILOG CODE:

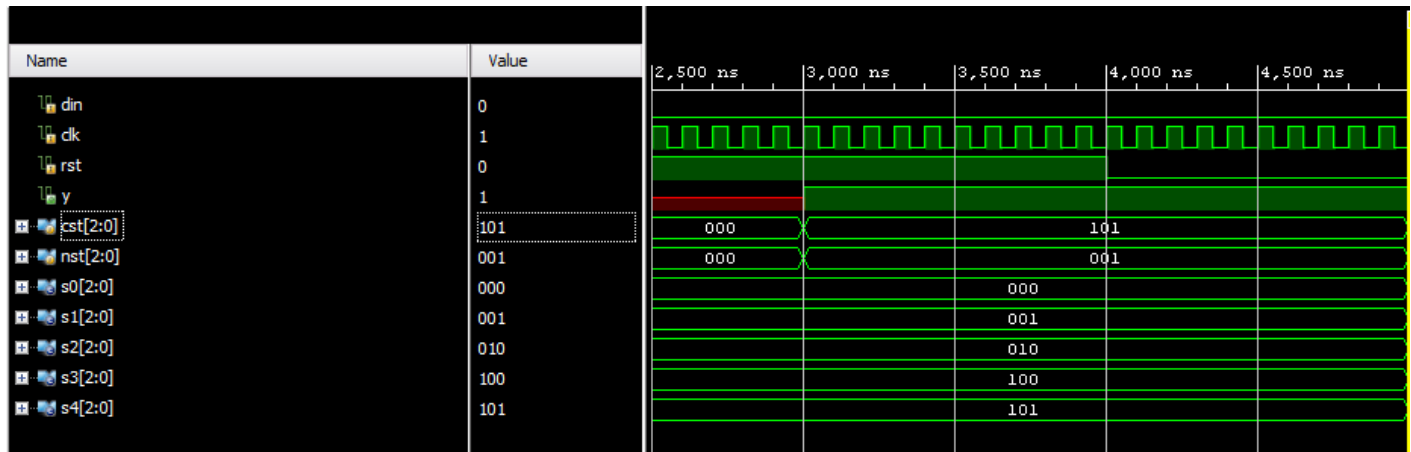
```
module MOORE_FSM(  
    input din,  
    input clk,  
    input rst,  
    output reg y  
);  
    reg [2:0] cst,nst;  
    localparam s0=3'b000,  
               s1=3'b001,  
               s2=3'b010,  
               s3=3'b100,  
               s4=3'b101;  
    always@(cst or din)  
    begin  
        case(cst)  
            s0 : if(din==1'b1)  
                begin  
                    nst = s1;  
                    y=1'b0;  
                end  
            else nst = cst;  
            s1 : if(din==1'b0)  
                begin  
                    nst = s2;  
                    y=1'b0;  
                end  
            else  
                begin  
                    nst = cst;  
                    y=1'b0;  
                end  
            s2 : if(din==1'b1)  
                begin  
                    nst = s3;  
                    y=1'b0;  
                end  
            else  
                begin  
                    nst = cst;  
                    y=1'b0;  
                end  
        endcase  
        cst = nst;  
    end
```

```

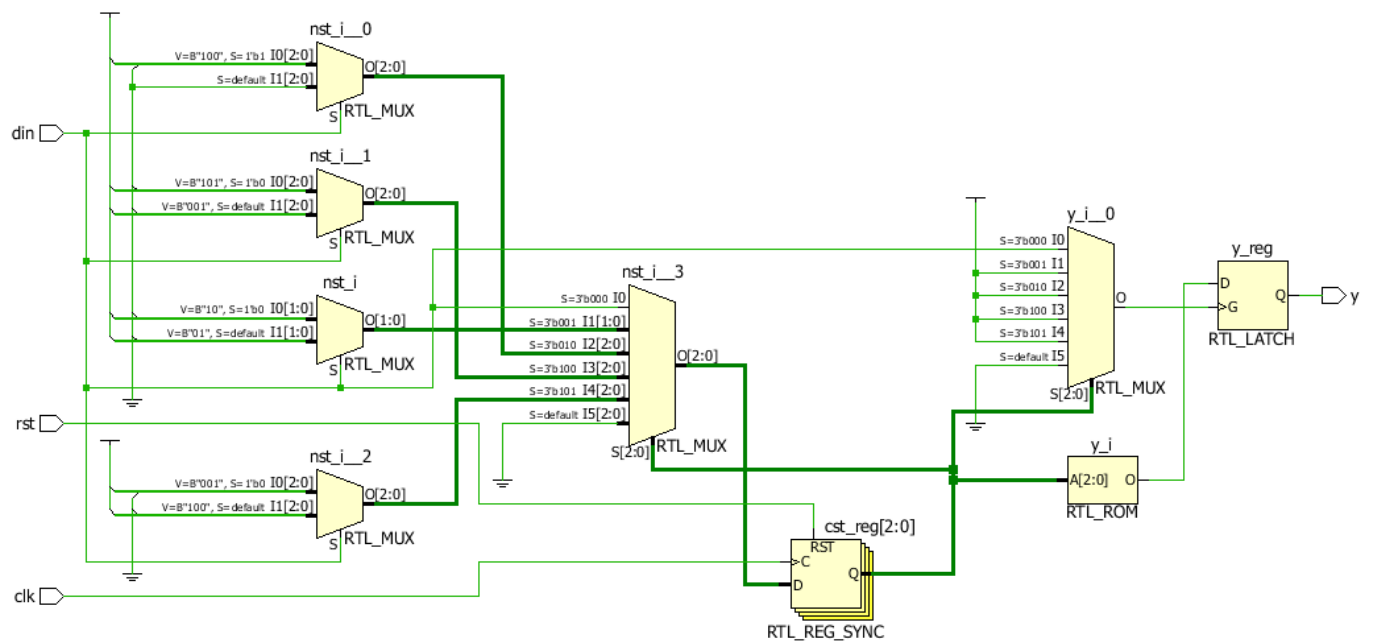
        begin
            nst = s0;
            y=1'b0;
        end
s3 : if(din==1'b0)
            begin
                nst = s4;
                y=1'b0;
            end
        else
            begin
                nst = s1;
                y=1'b0;
            end
s4 : if(din==1'b0)
            begin
                nst = s1;
                y=1'b1;
            end
        else
            begin
                nst = s3;
                y=1'b1;
            end
default: nst=s0;
endcase
end
always@(posedge clk)
begin
    if(rst)
        cst<=s0;
    else
        cst<=nst;
    end
endmodule

```

## SIMULATION:



## RTL SCHEMATIC:

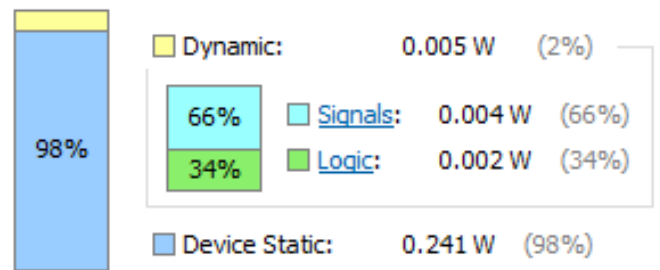


## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:**                   **0.246 W**  
**Junction Temperature:**               **25.3 °C**  
Thermal Margin:                        59.7 °C (41.1 W)  
Effective  $\theta_{JA}$ :                         1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level:                      [Low](#)

### On-Chip Power



# CODE-25: N:1 MUX

## CODE FOR TESTBENCH:

```
module testbench;

    N_MUX uut (
        .data_inputs({16'b00000001, 16'b00000010, 16'b00000100, 16'b00001000,
                      16'b00010000, 16'b00100000, 16'b01000000, 16'b10000000,
                      16'b00000001, 16'b00000010, 16'b00000100, 16'b00001000,
                      16'b00010000, 16'b00100000, 16'b01000000, 16'b10000000}),
        .sel(sel),
        .Y(Y)
    );
    reg [15:0] in;
    reg [3:0] sel;
    wire y;
    reg clk = 0;
    always #5 clk = ~clk;
    initial begin
        sel = 4'b0000;
        #10;

        sel = 4'b0101;
        #10;

        sel = 4'b1111;
        #10;
        $finish;
    end

    always @(posedge clk)
    begin
        $monitor("sel = %b in = %b y=%b", sel, in, y);
    end

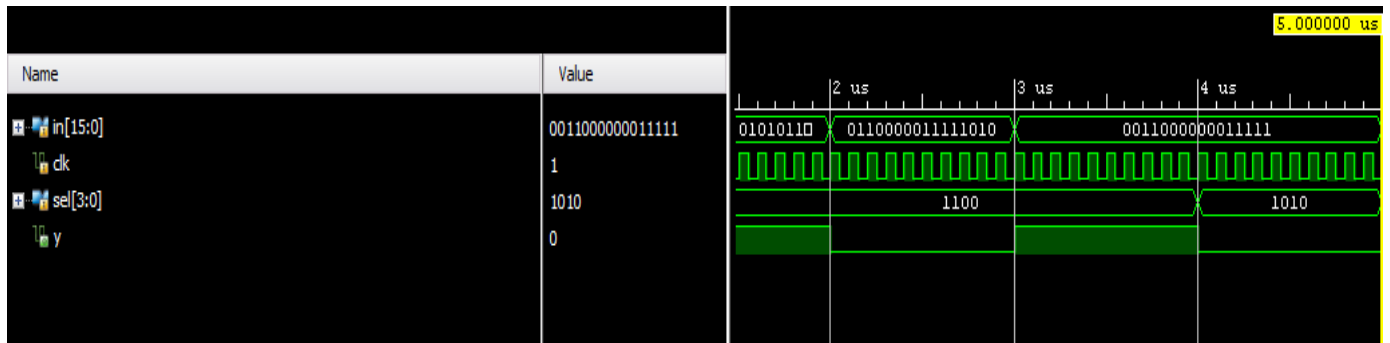
endmodule
```



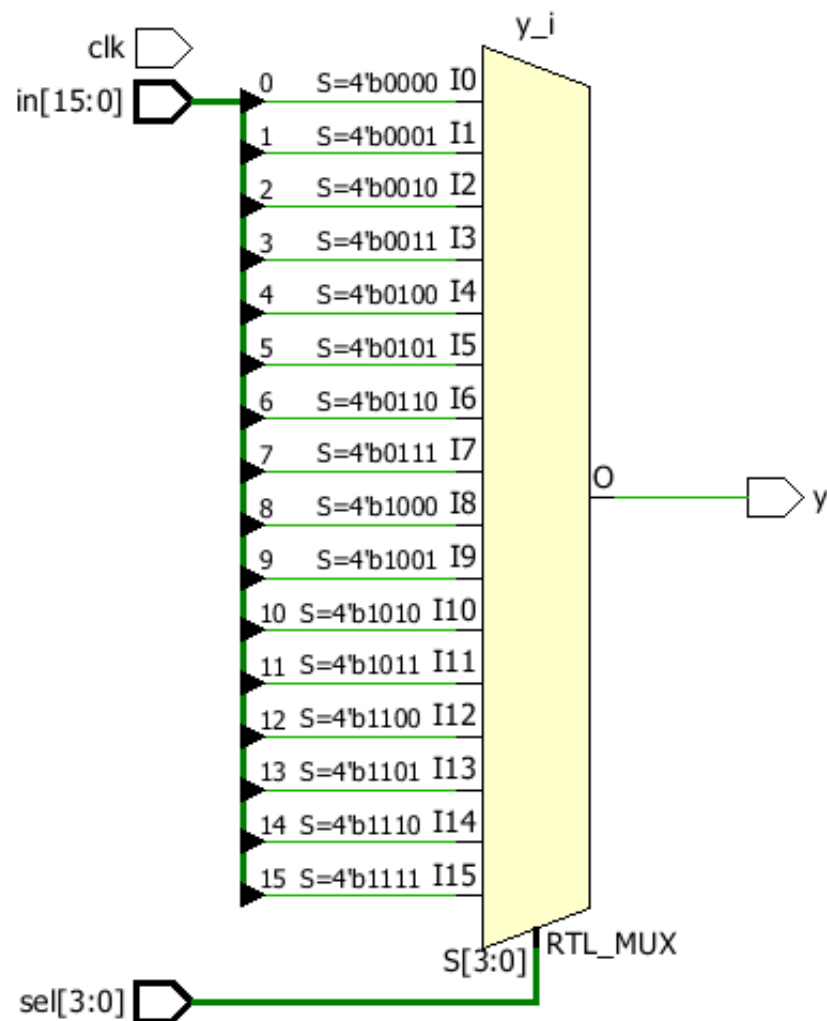
## VERILOG CODE:

```
module N_MUX(  
    input [15:0] in,  
    input clk,  
    input [3:0] sel,  
    output reg y  
);  
  
always@(in or sel)  
begin  
    case(sel)  
        4'b0000 : y = in[0];  
        4'b0001 : y = in[1];  
        4'b0010 : y = in[2];  
        4'b0011 : y = in[3];  
        4'b0100 : y = in[4];  
        4'b0101 : y = in[5];  
        4'b0110 : y = in[6];  
        4'b0111 : y = in[7];  
        4'b1000 : y = in[8];  
        4'b1001 : y = in[9];  
        4'b1010 : y = in[10];  
        4'b1011 : y = in[11];  
        4'b1100 : y = in[12];  
        4'b1101 : y = in[13];  
        4'b1110 : y = in[14];  
        4'b1111 : y = in[15];  
        default : y = 4'b0000;  
    endcase  
end  
endmodule
```

## SIMULATION:



## RTL SCHEMATIC:



## POWER REPORT:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** **1.202 W**  
**Junction Temperature:** **26.7 °C**  
Thermal Margin: 58.3 °C (40.2 W)  
Effective  $\theta_{JA}$ : 1.4 °C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: [Low](#)

### On-Chip Power

