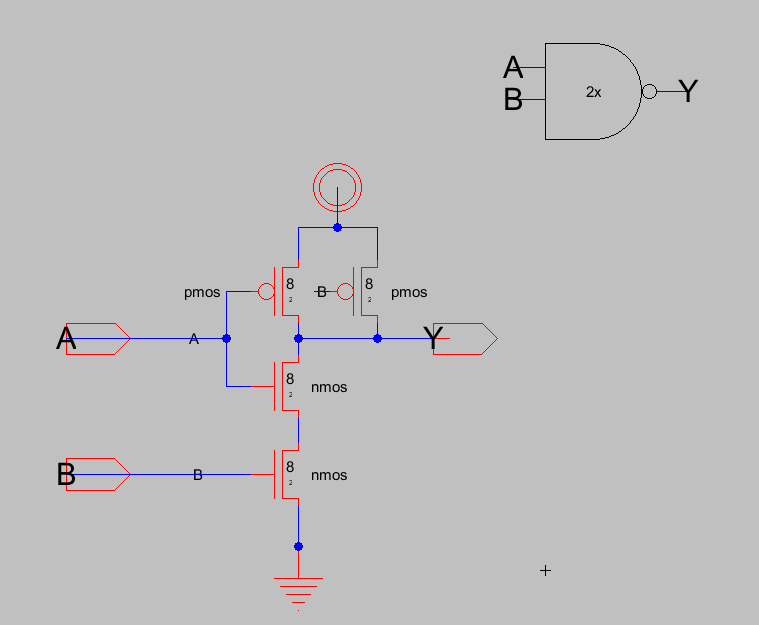
**T5 – NAND with 1x Drive Strength**

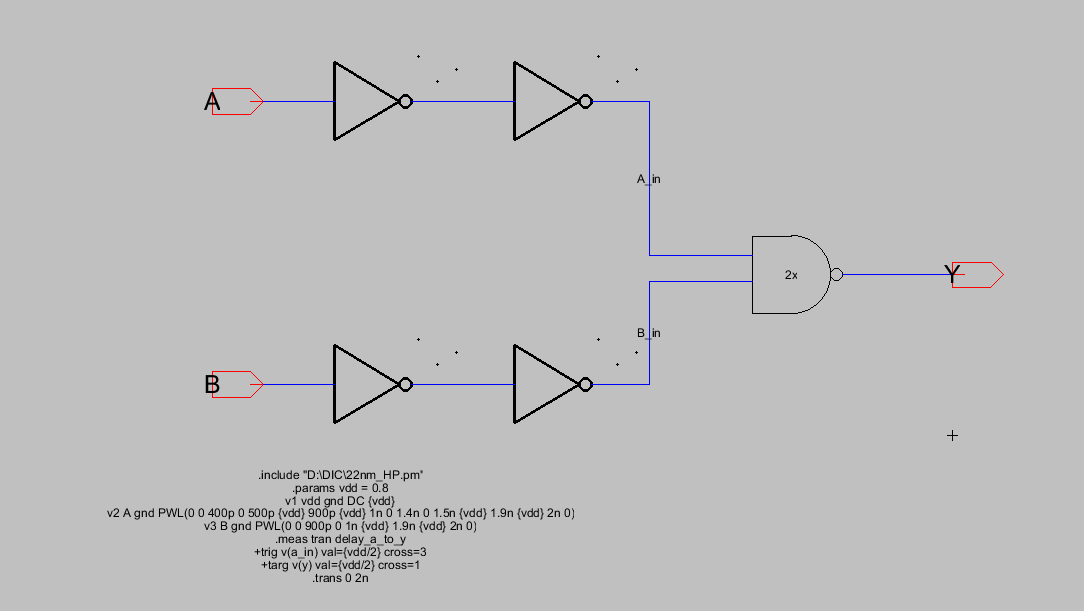
Schematic

Layout of the 2x NAND along with its icon:

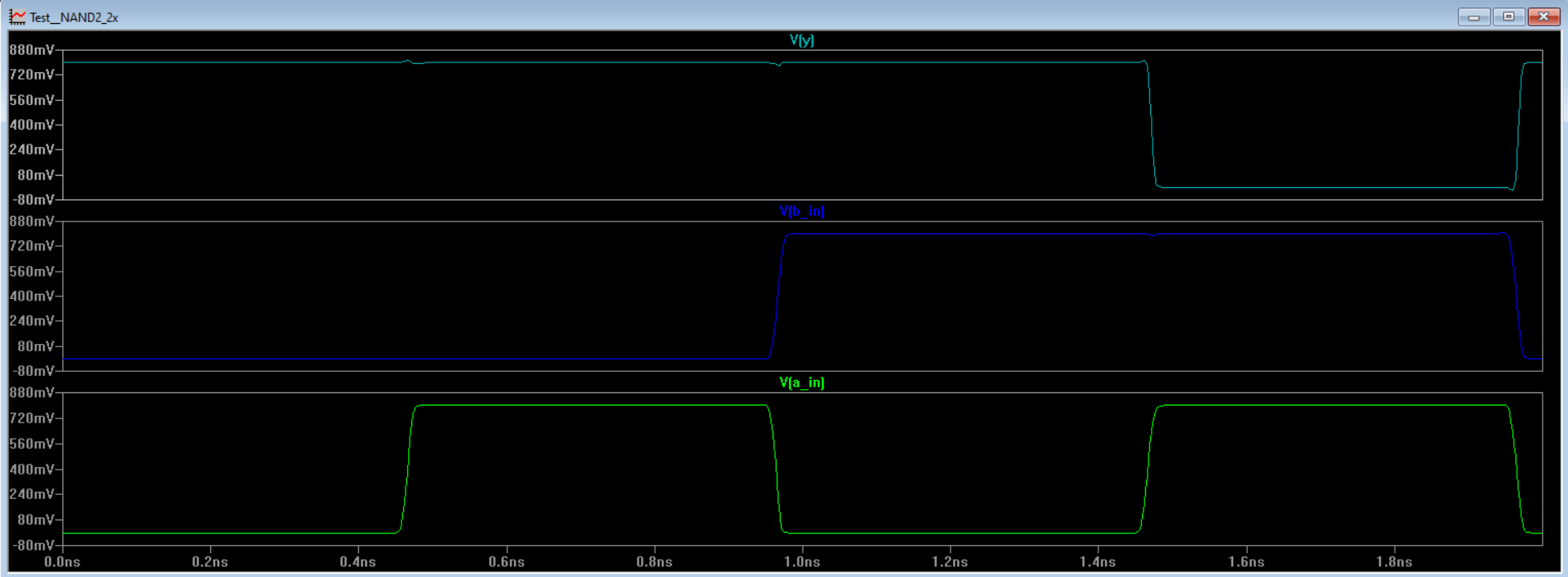


Simulation of Schematic

Simulation of the NAND gate with inputs fed in through buffer:



Simulated Waveforms – Output, NAND\_inp\_A, NAND\_inp\_B (in order)



Captured delay:

