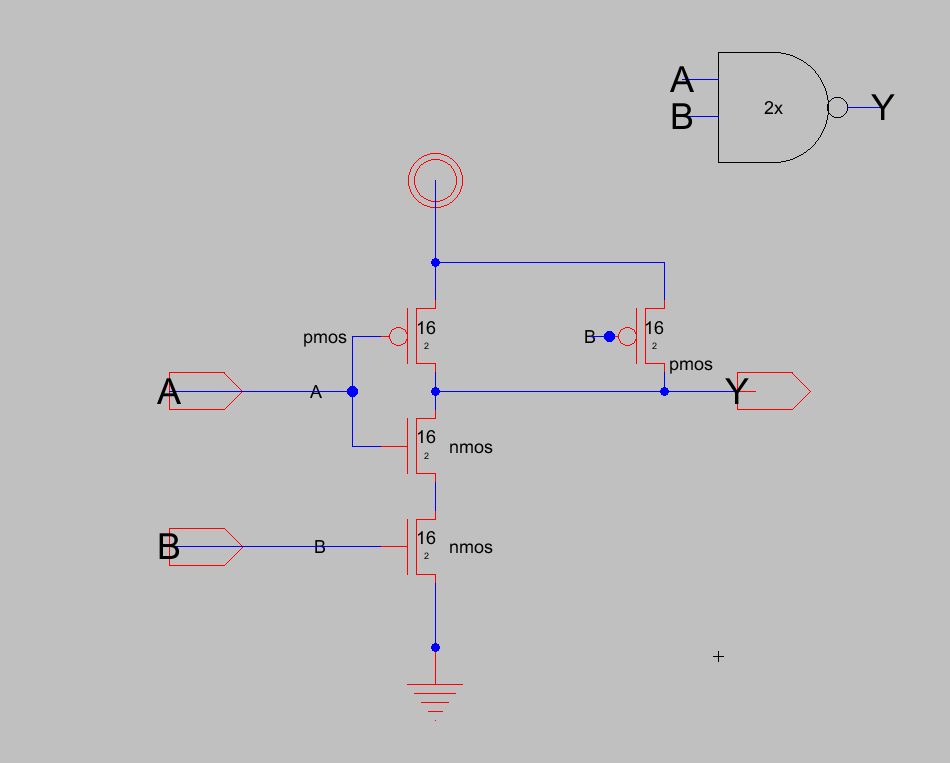
**T5 – NAND with 2x Drive Strength**

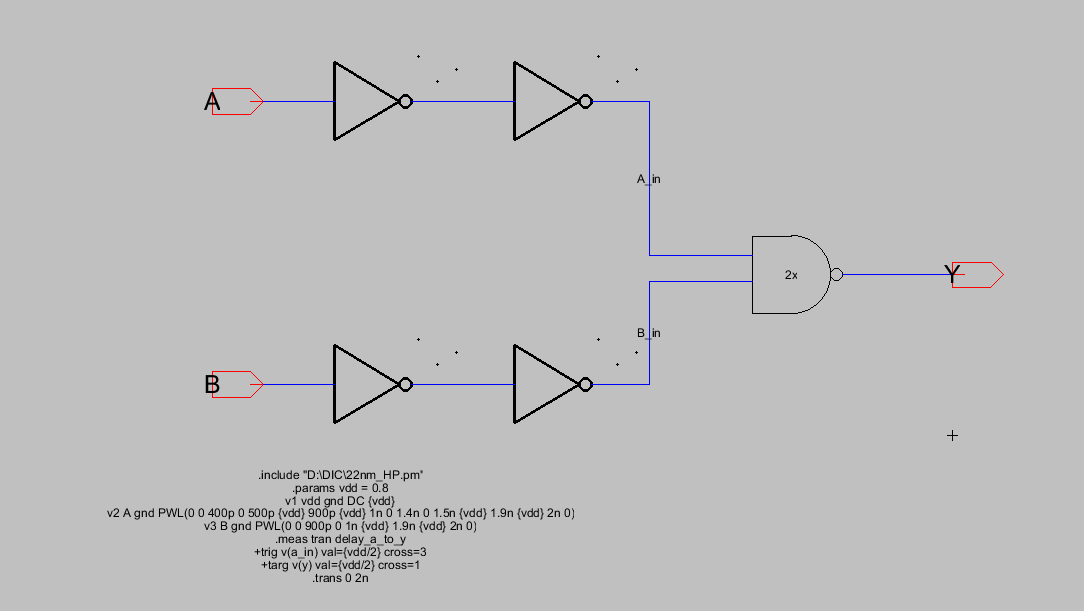
Schematic

Layout of the 2x NAND along with its icon:

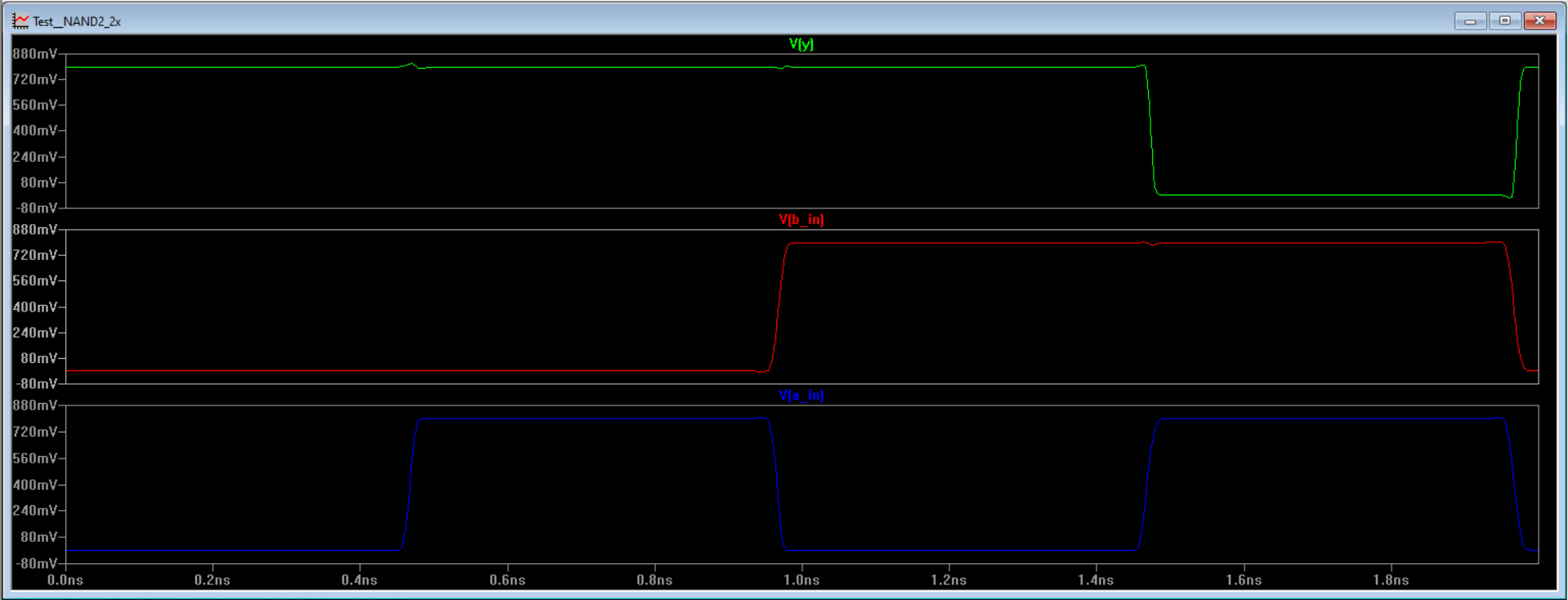


Simulation of Schematic

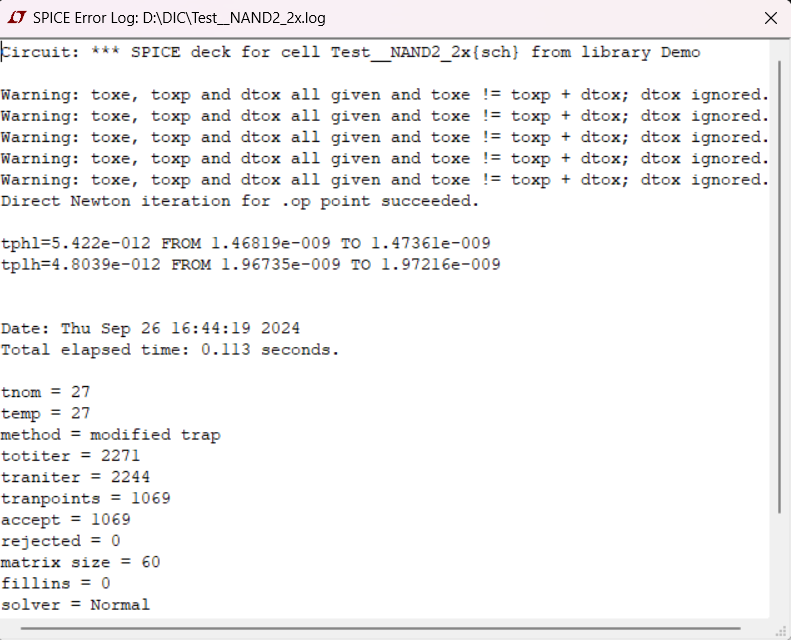
Simulation of the NAND gate with inputs fed in through buffer:



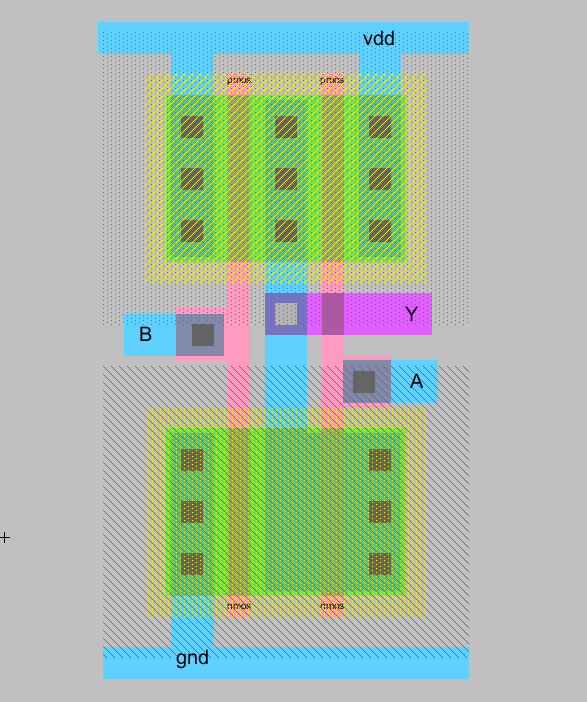
Simulated Waveforms – Output, NAND\_inp\_A, NAND\_inp\_B (in order)



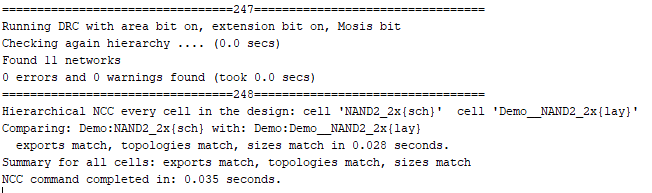
Captured delay:



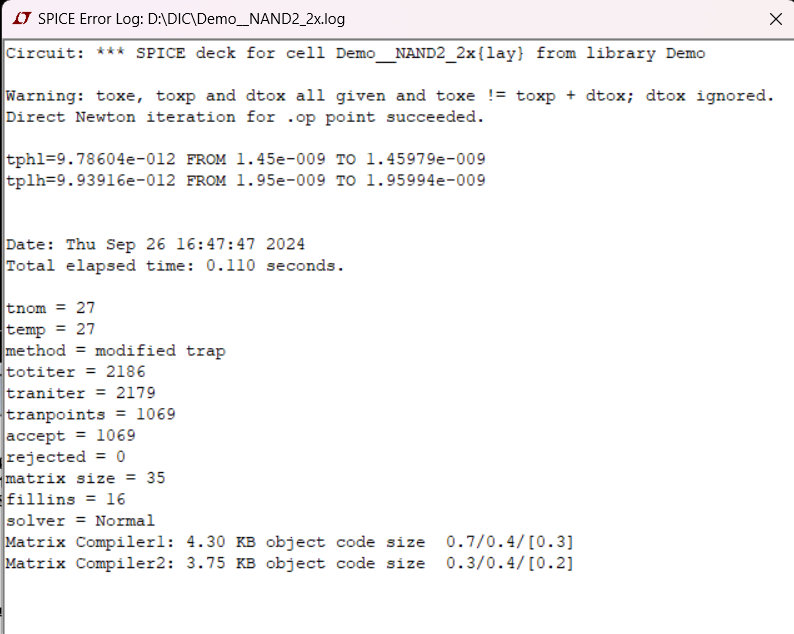
Layout of NAND2 – 2x drive strength



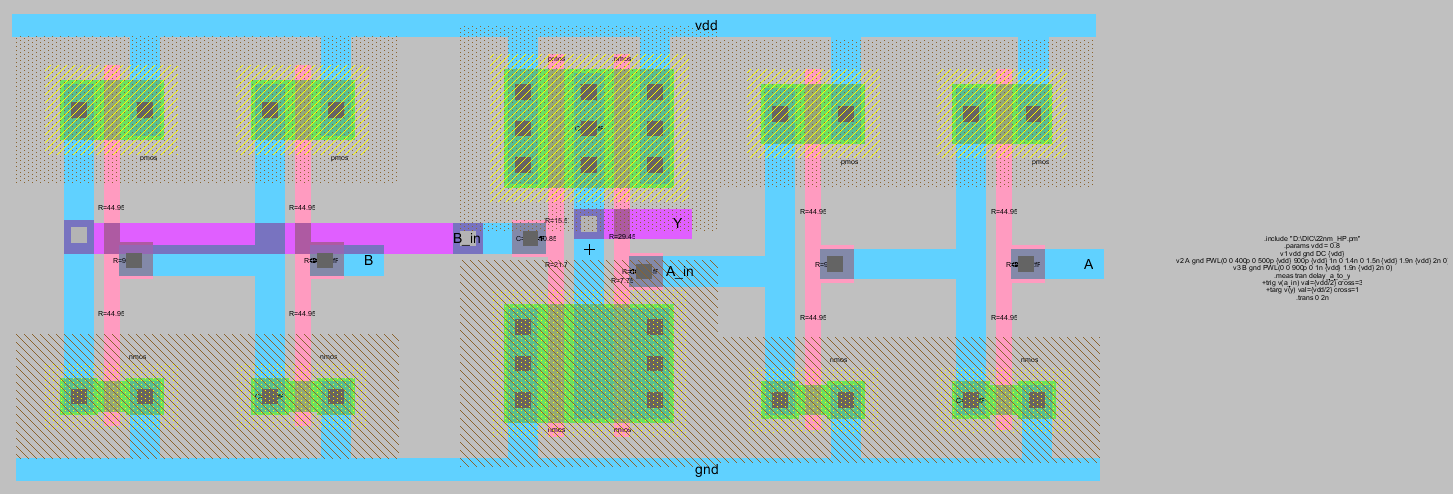
DRC / LVS



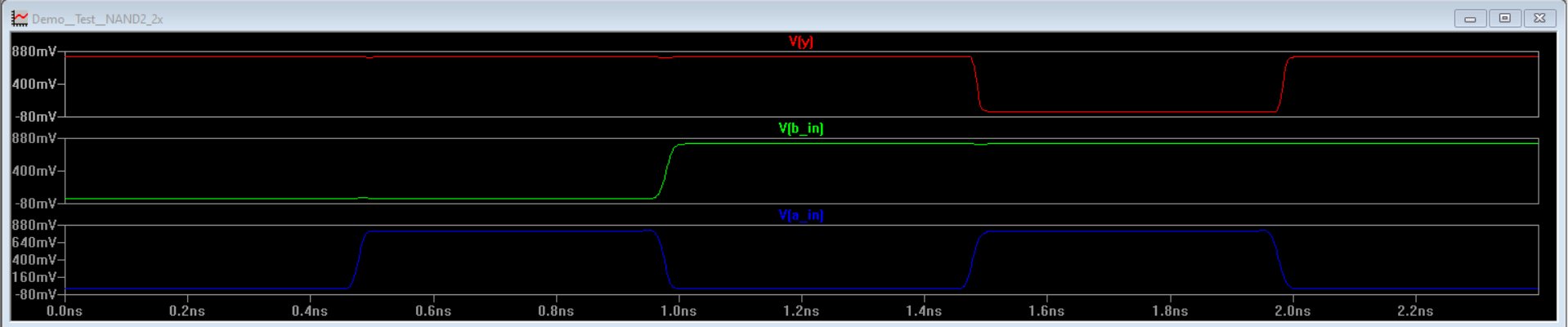
Capturing Delay of RC extracted Layout without passing inputs through buffers:



Layout with input Buffers



Simulation for the same



Capturing Delay for the same

