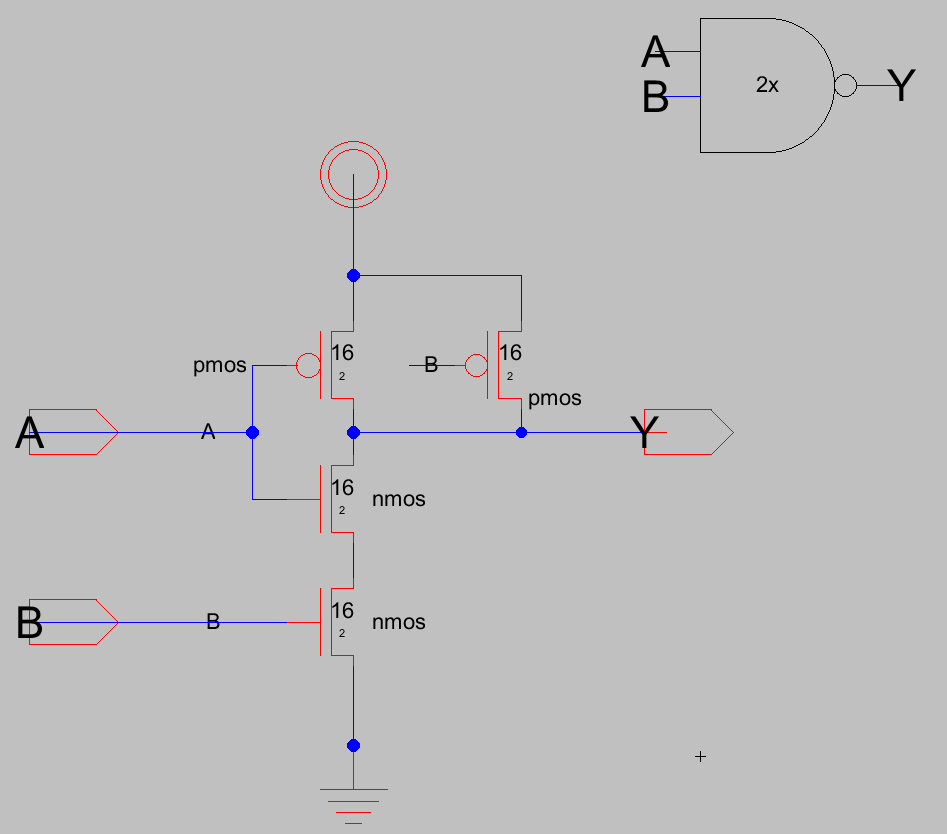
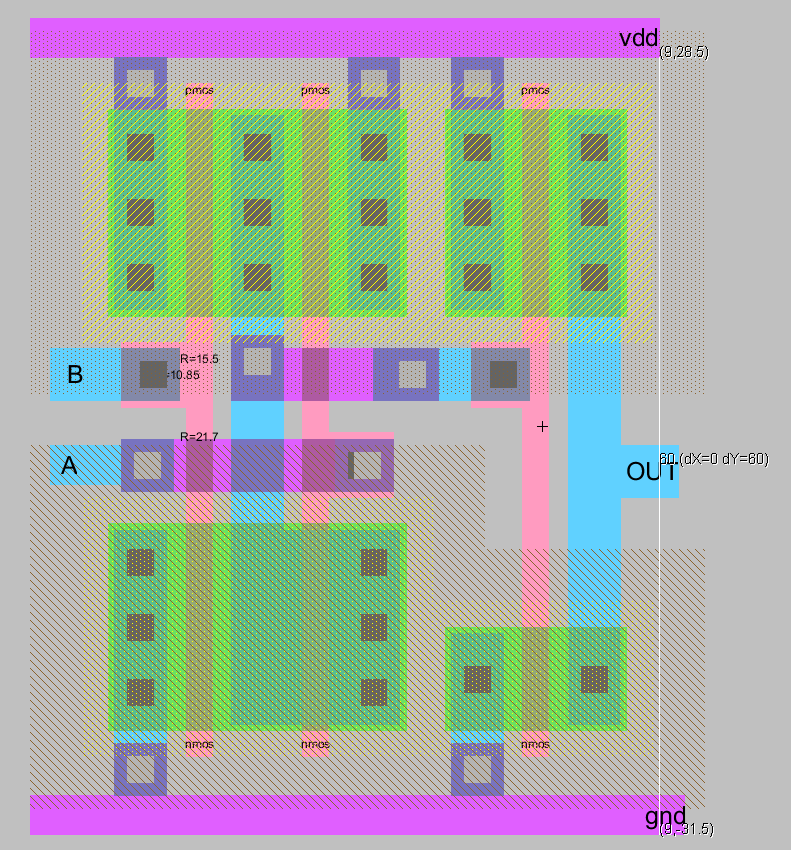
**Batch Tutorial – (6a) – AND2\_2x**

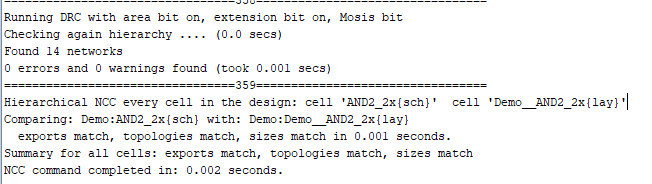
Schematic003A



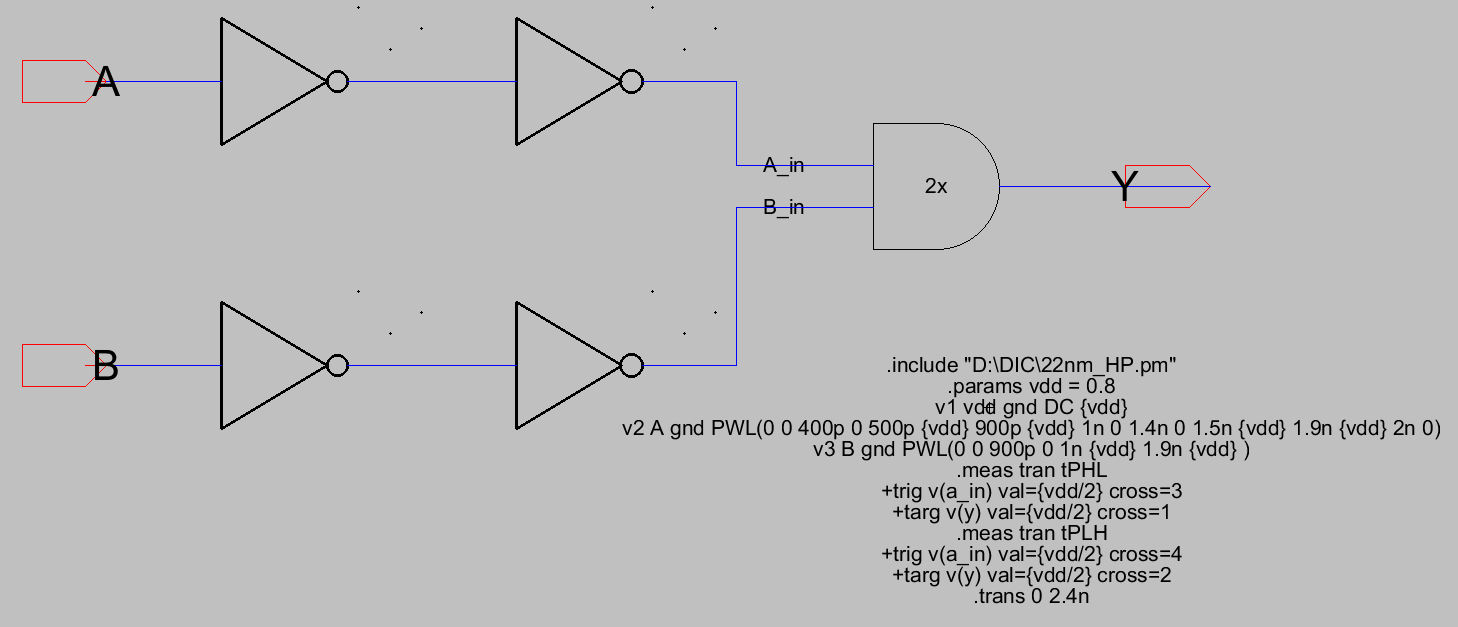
Layout:



DRS & LVS Reports

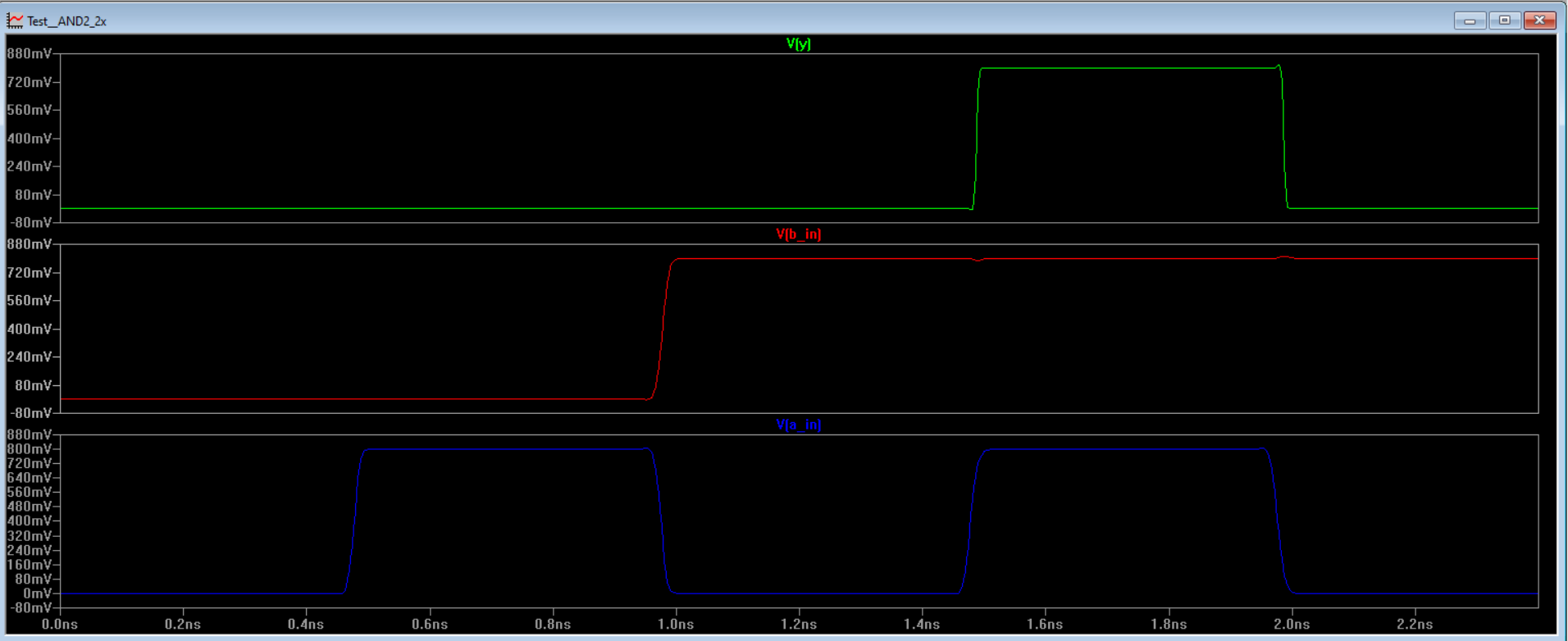


Testbench:

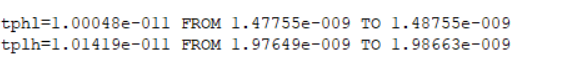


SIMULATION BEFORE RC EXTRACTION:

Simulated Waveforms:

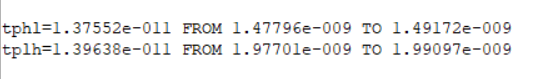


tPLH and tPHL:

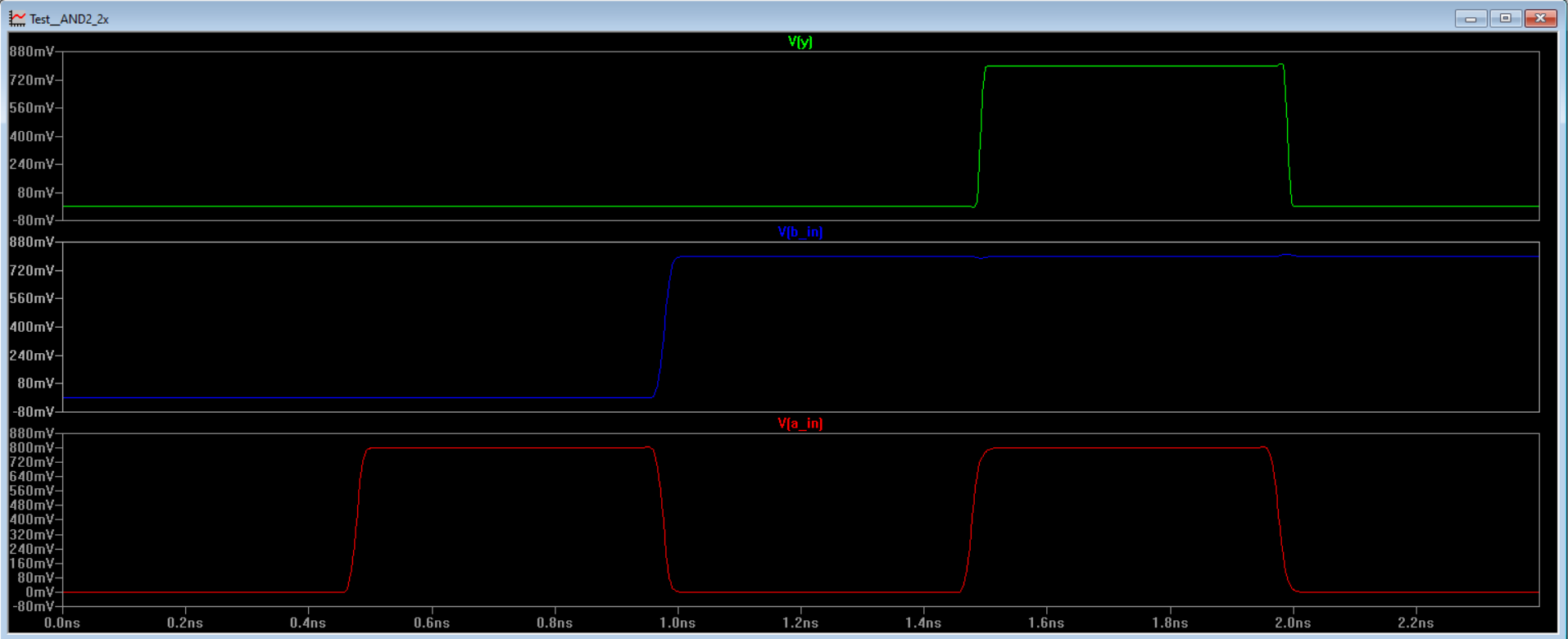


POST RC EXTRACTION:

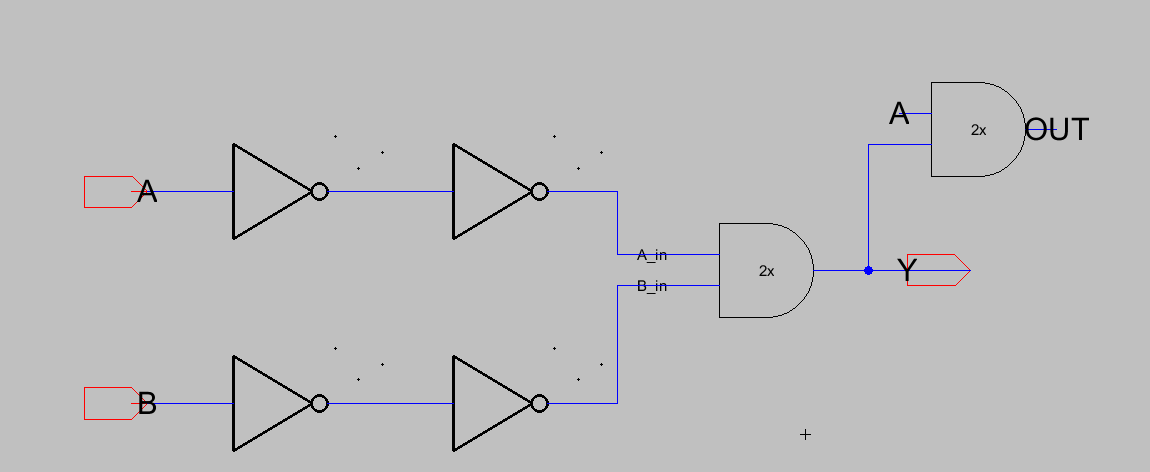
tPLH and tPHL:

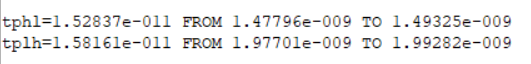


Simulated Waveforms:



Delay Measurement when driving a load:

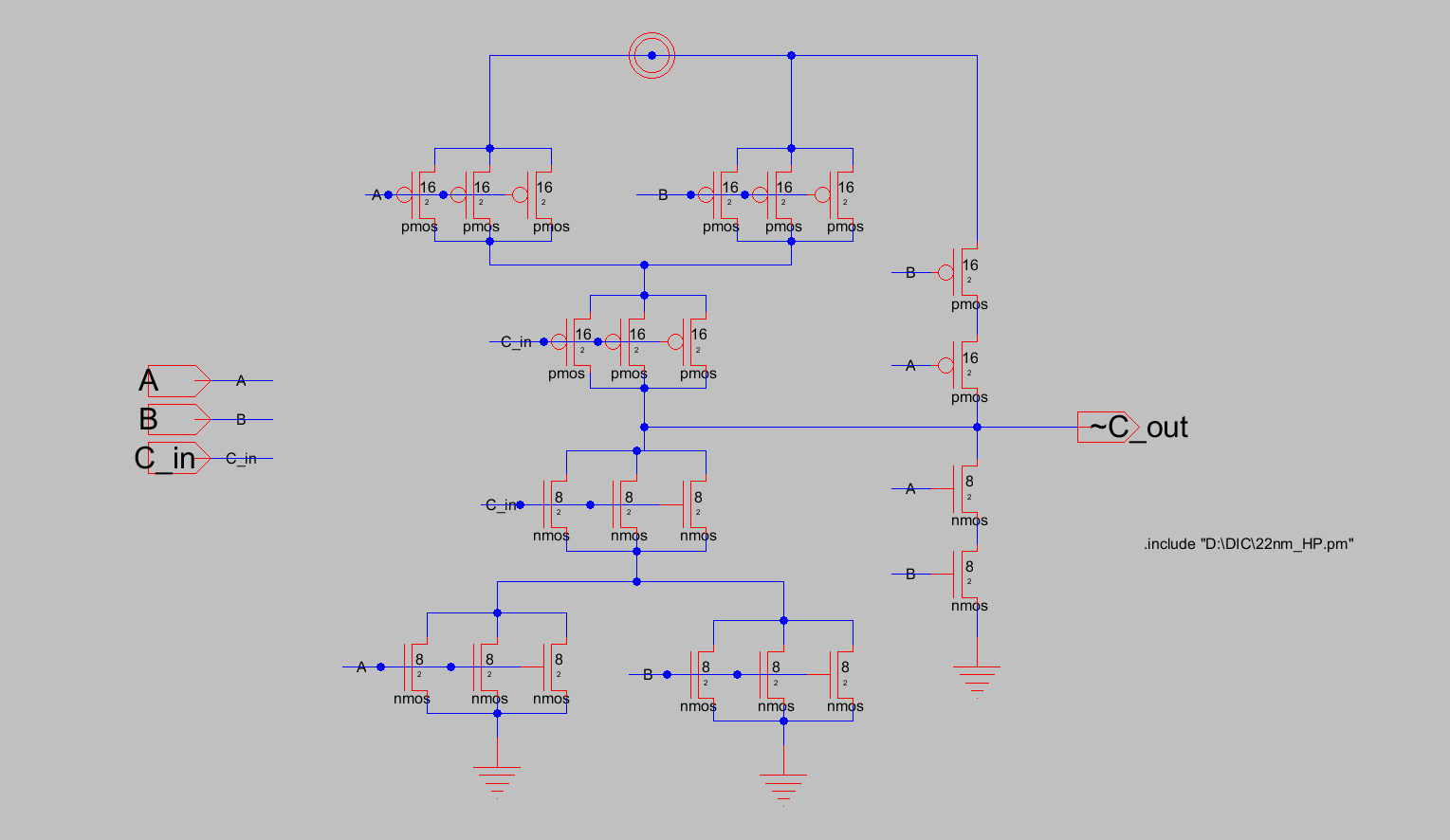




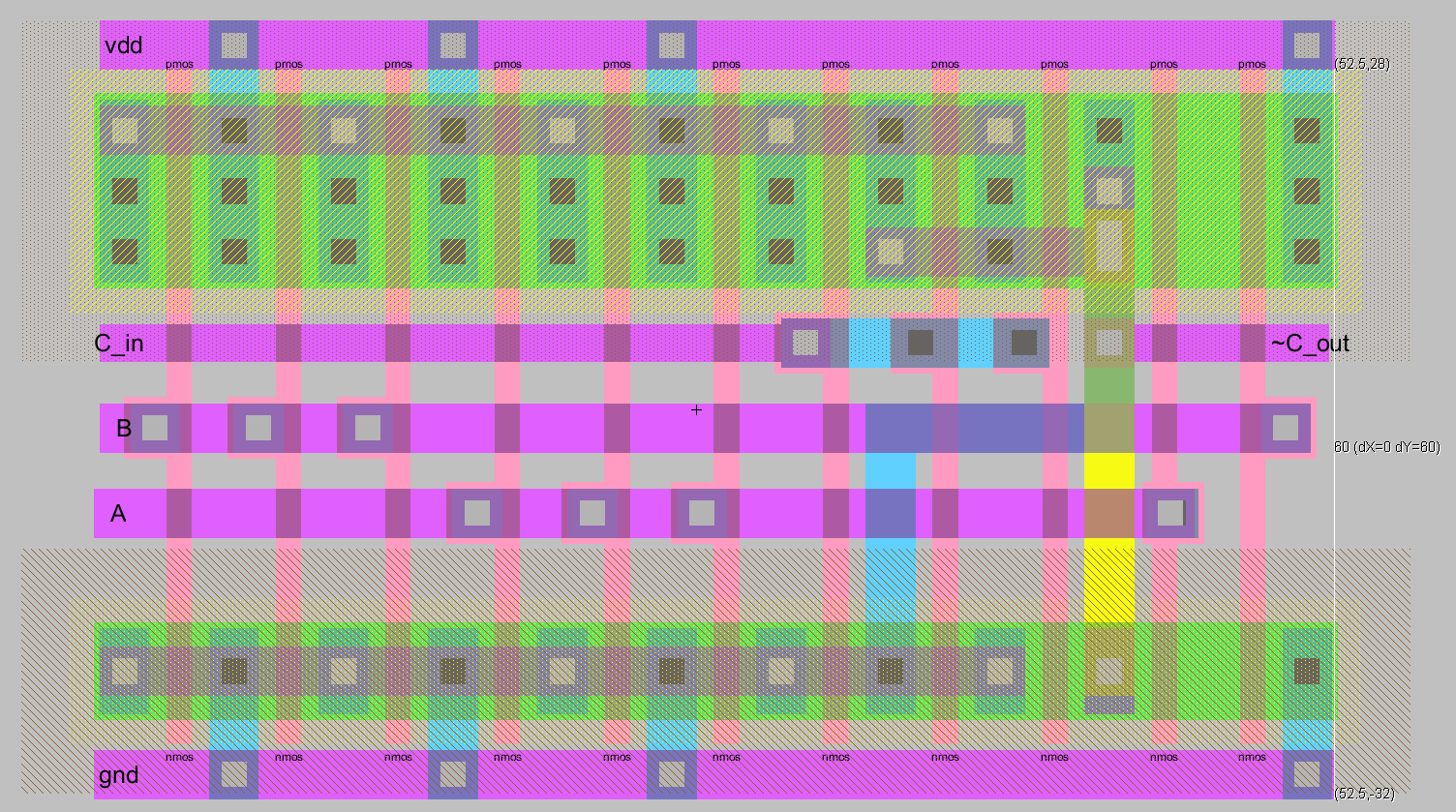
**Batch Tutorial – (6b)**

**Full Adder Carry Generation (3x)**

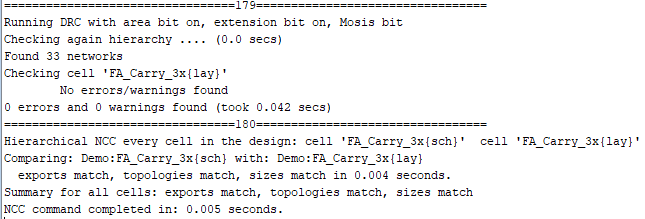
Schematic:

****

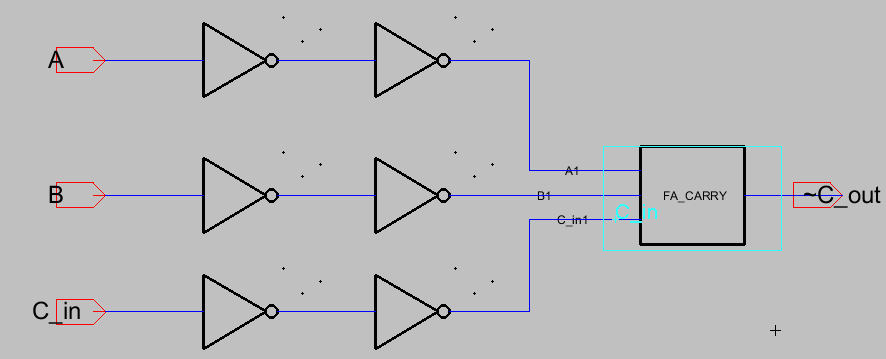
Layout:



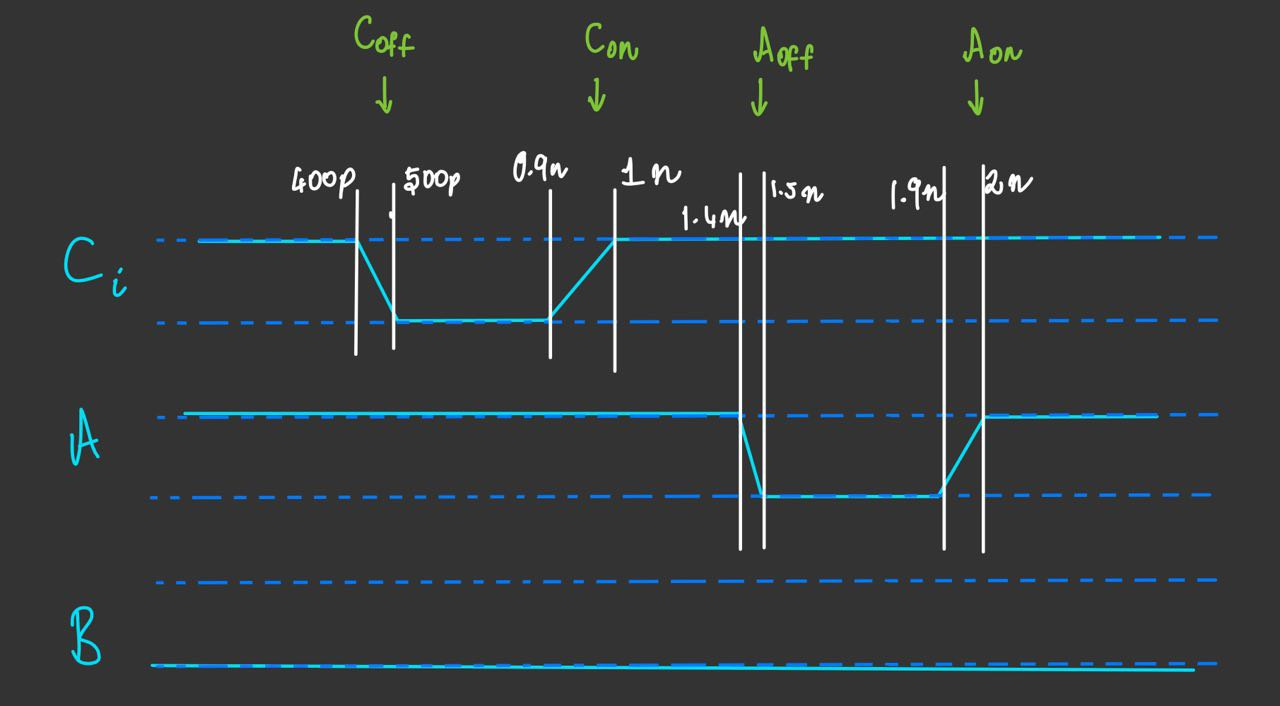
DRS & LVS Reports



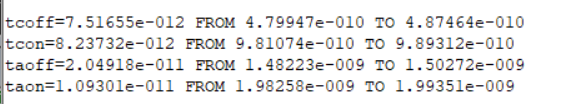
Testbench with RC extracted FA:



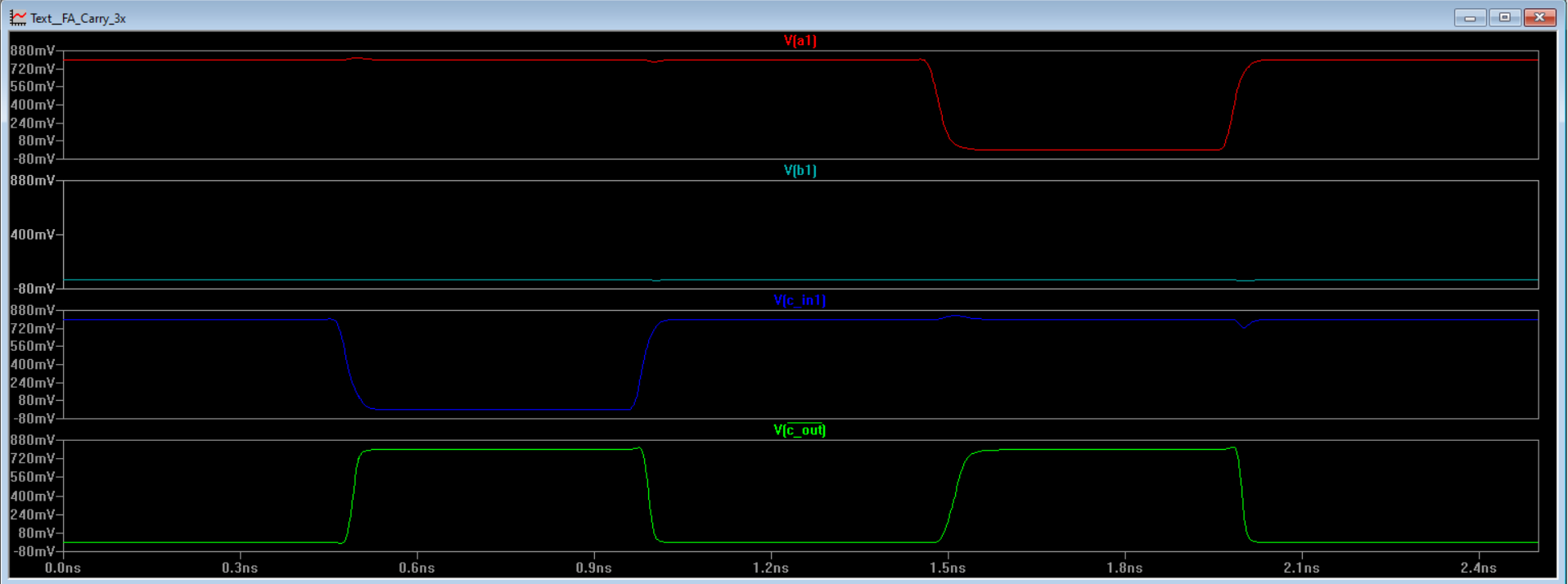
Simulation Inputs:



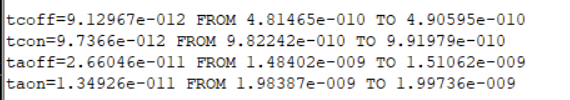
Delay Measurements without RC extraction:



Simulation Waveforms:



Delay Measurements with RC extraction:



Extra Delay % after RC extraction:

Delay due to transition in Cin: (contributing to Critical Path)

TCoff = 16.95%

TCon = 18.20%

Delay due to transition in A:

TAoff = 29.83%

TAon = 23.44%

Delay Measurements – Driving a load

