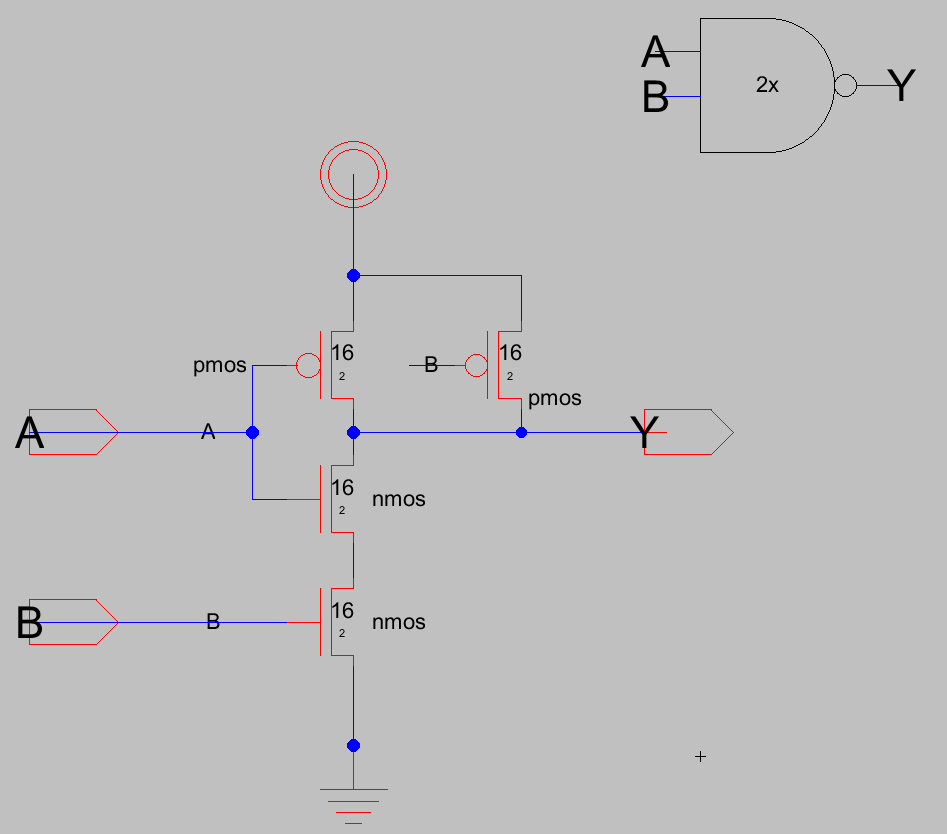
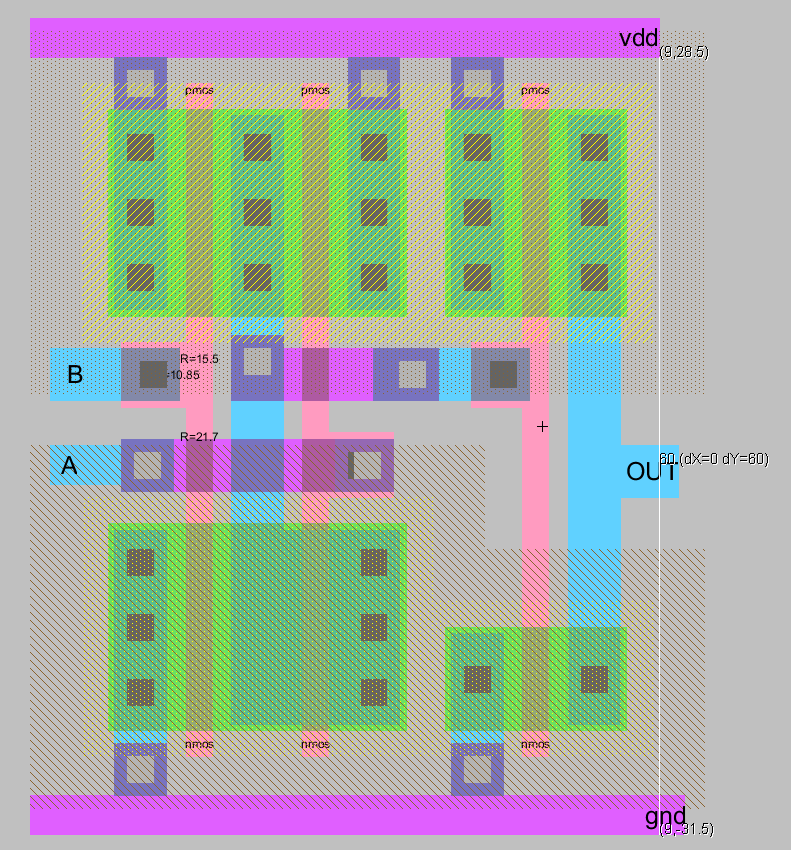
**Batch Tutorial – (6a) – AND2\_2x**

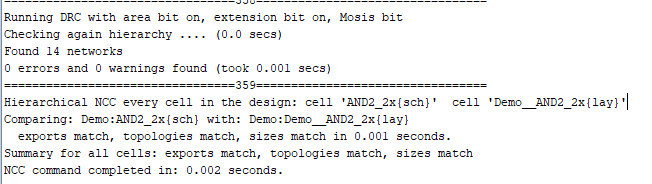
Schematic:



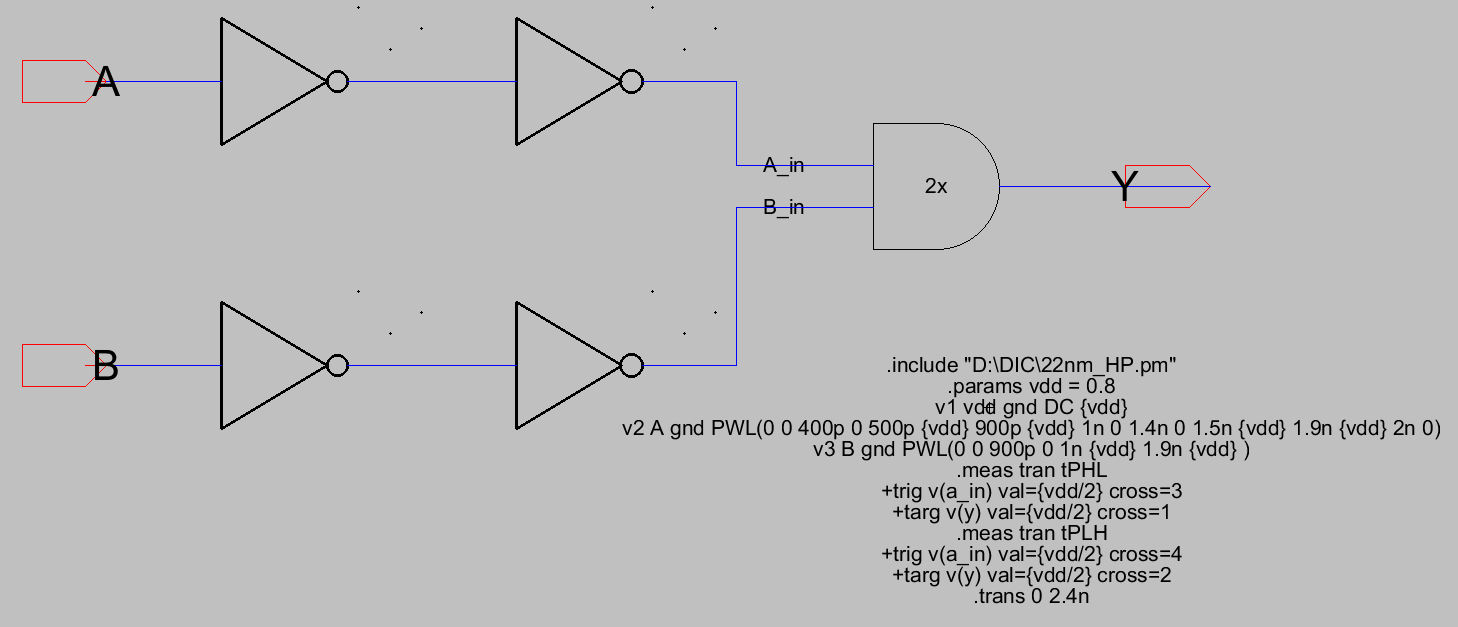
Layout:



DRS & LVS Reports

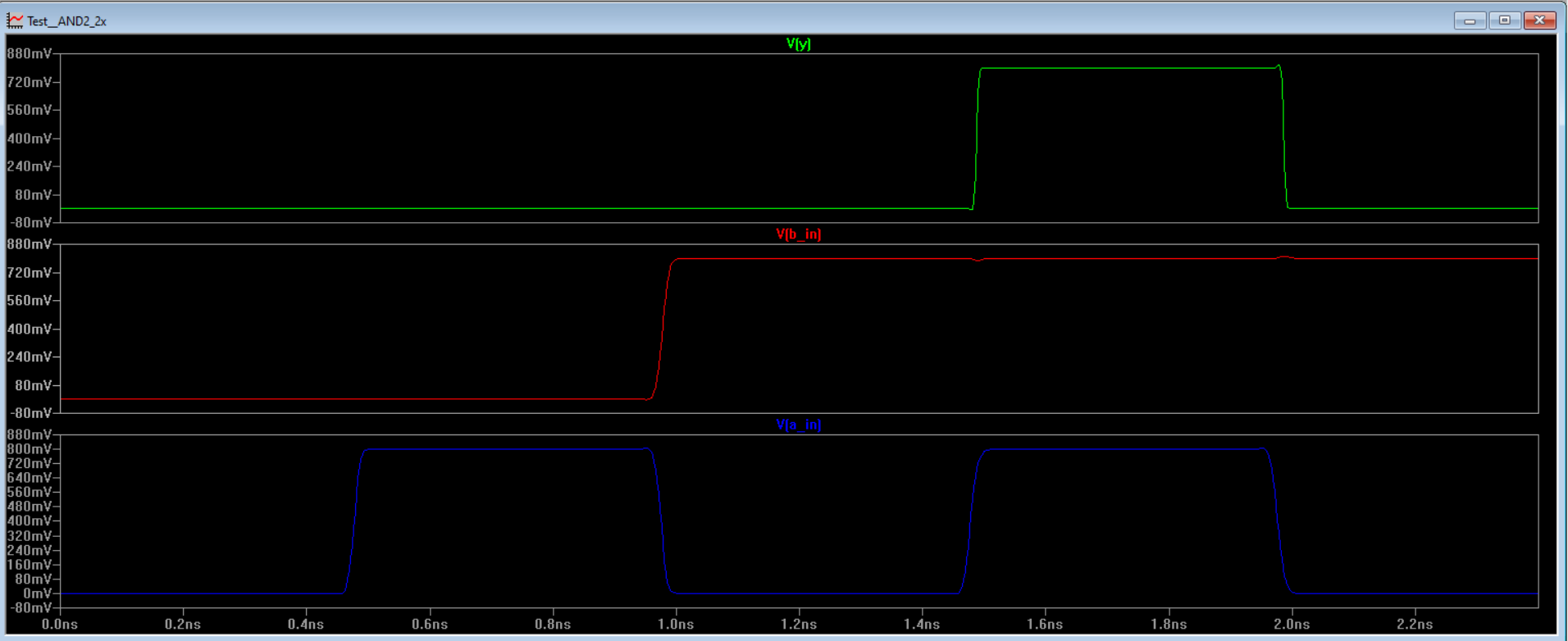


Testbench:

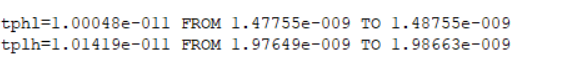


SIMULATION BEFORE RC EXTRACTION:

Simulated Waveforms:

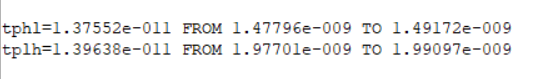


tPLH and tPHL:



POST RC EXTRACTION:

tPLH and tPHL:



Simulated Waveforms:

