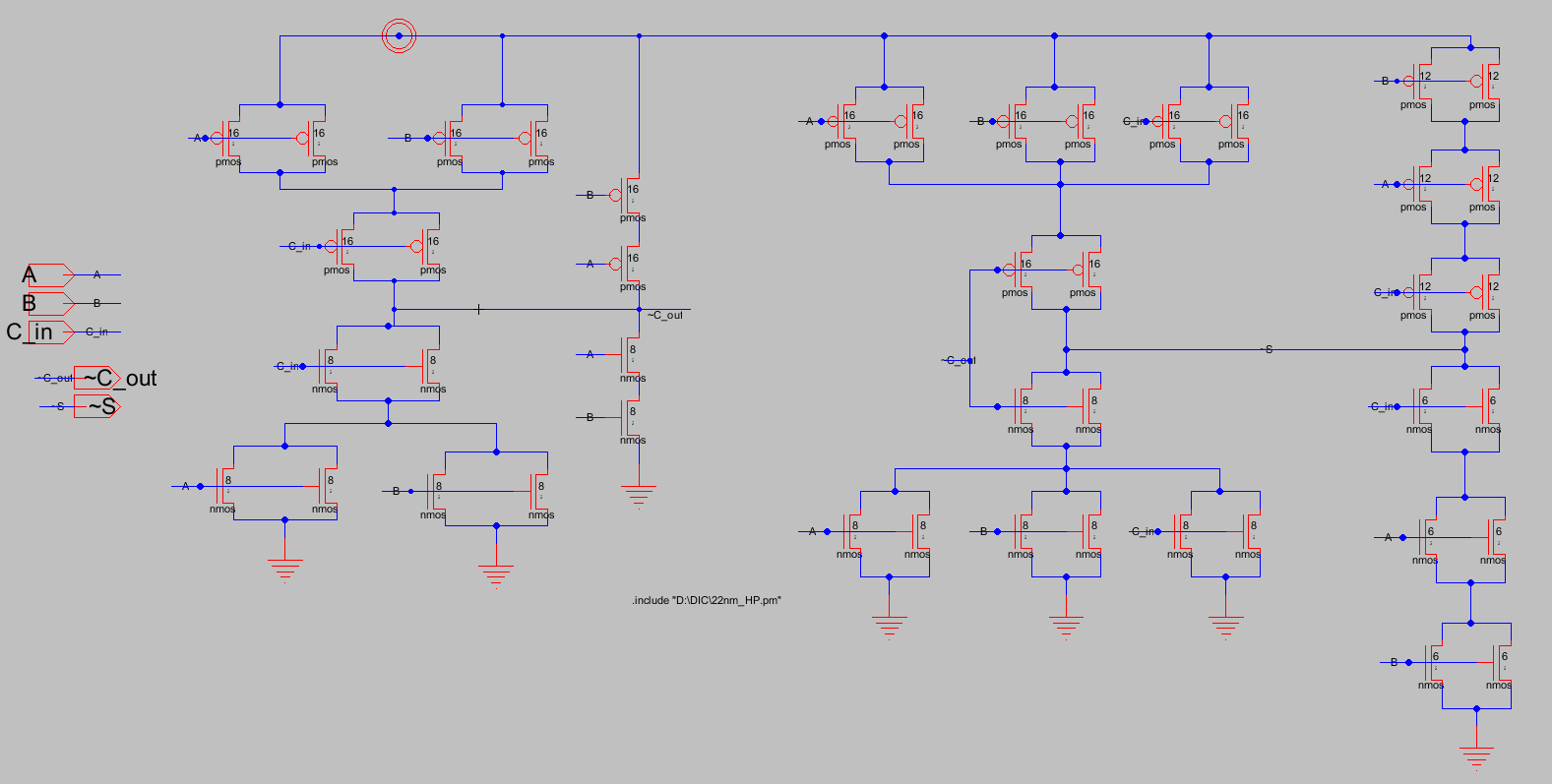
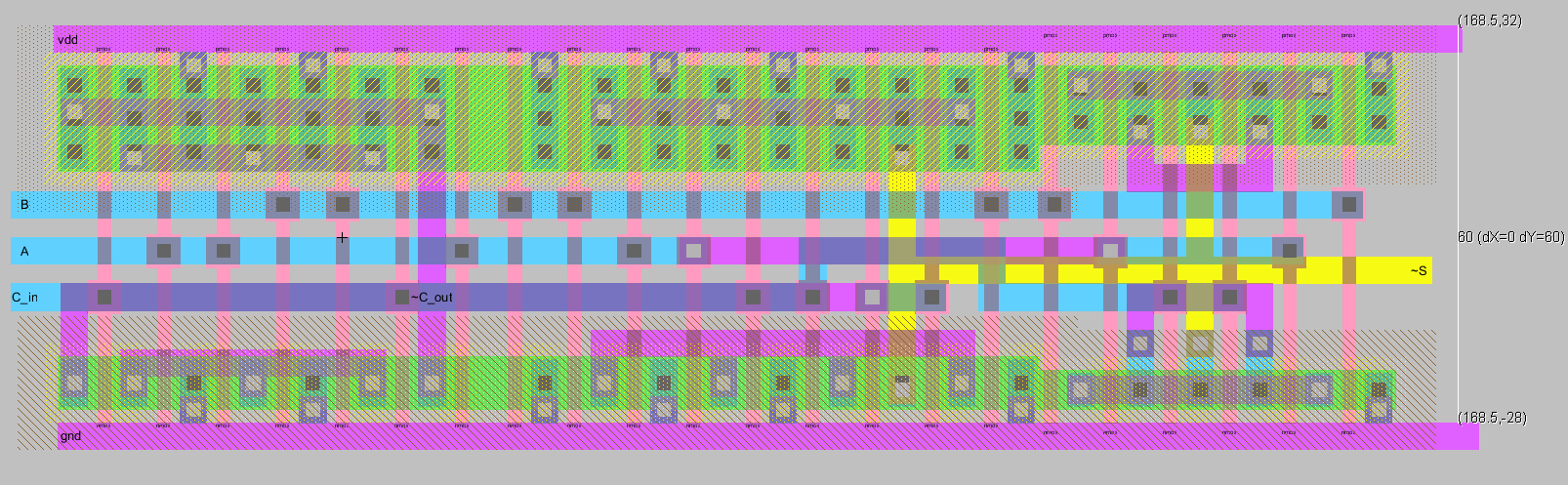
**Batch Tutorial – (7a)**

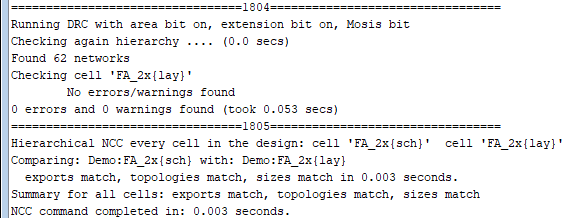
**Full Adder Sum Generation (2x)**

Schematic:

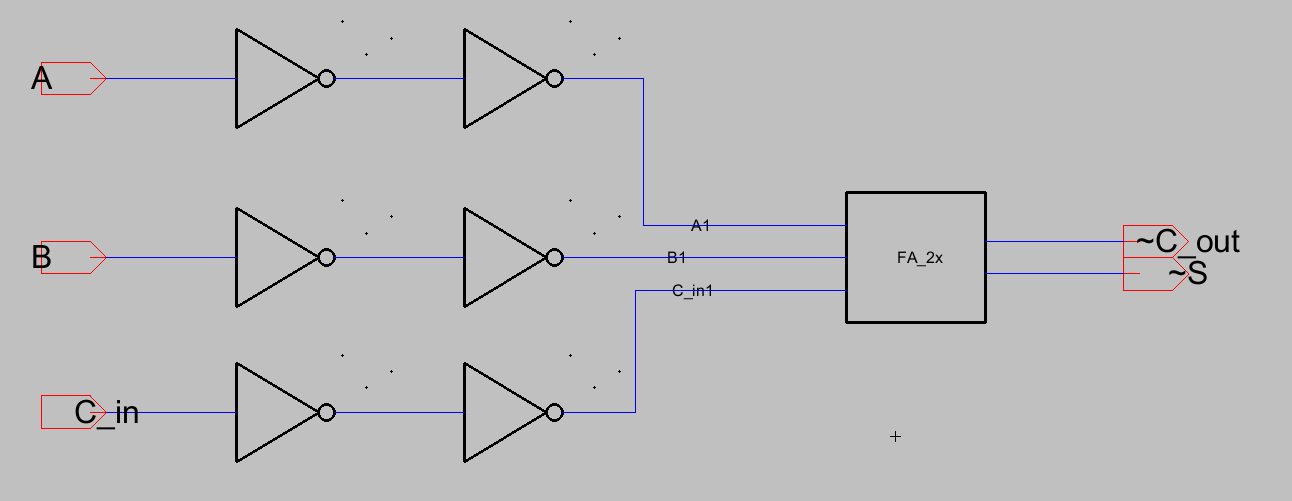


Layout:

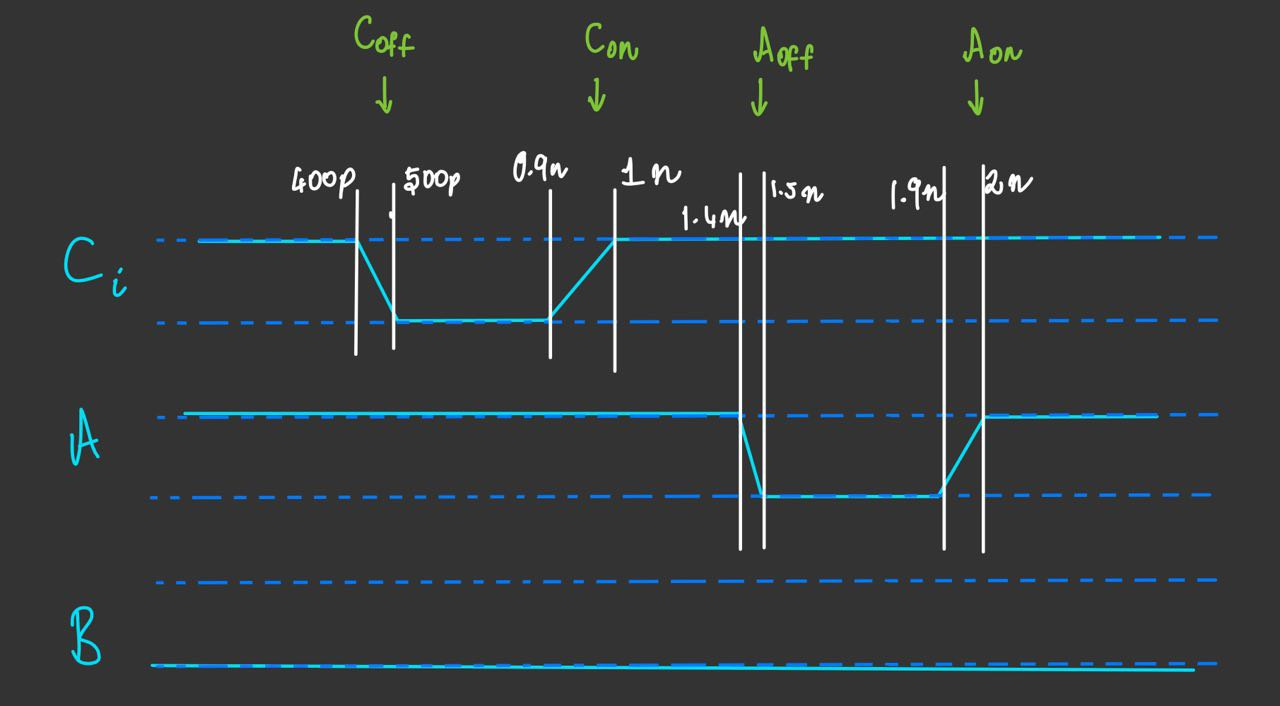


DRC/LVS Reports:

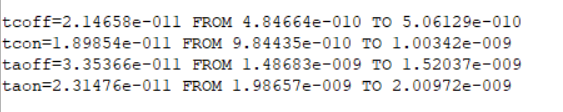
Testbench with RC extracted FA:



Simulation Inputs:



Delay Measurements with RC extraction:



Simulated Waveforms:

