DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION

(Effective from the Academic Year 2021 - 2022)

SEMESTER - III

Course Code	**21CS32**	**CIA Marks**	**50**
Number of Contact Hours/Week (L:T:P:S)	**3:0:2:0**	**SEE Marks**	**50**
Total Hours of Pedagogy	**40 L + 20 P**	**Exam Hours**	**3 Hours**

CREDITS – 4

Prerequisites:

- Basic logic design principles and various functions of digital computer.

Course Objectives:

This course will enable students to:

- Illustrate combinational digital circuits.
- Demonstrate the use of flipflops to design registers and counters.
- Explain the basic sub systems of a computer, their organization, structure and operation.
- Describe memory hierarchy and concept of cache memory.
- Describe arithmetic and logical operations with integer operands.
- Demonstrate different ways of communicating with I/O devices and standard I/O interfaces.
- Illustrate organization of a simple processor and other computing systems using instruction level parallelism.

COURSE CONTENTS

MODULE - 1

Module Contents	Lecture Hours
Combinational Logic Design: Karnaugh Map**,** Minimization of complete and incomplete Boolean expressions using K-Map, Multiplexers, Three state buffers, Decoders and Encoders, Programmable Logic devices.	**8 Hours**

MODULE - 2

Sequential Logic Design: Flip-Flops and its Applications**:** Master Slave Flip-Flops, Edge-Triggered Flip-Flops, Registers, Counters, Design of Synchronous Counters.	**8 Hours**

MODULE - 3

Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. **Memory System:** Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations.	**8 Hours**

MODULE – 4	
Arithmetic: Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers. **Input/Output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits.	**8 Hours**
MODULE - 5	
Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Hard-wired Control, Micro programmed Control. **Machine Instructions and Addressing Modes:** Memory Location and Addresses, Instructions and Instruction Sequencing, Addressing Modes.	**8 Hours**

COURSE OUTCOMES

Upon completion of this course, the students will be able to:

CO No.	Course Outcome Description	Bloom's Taxonomy Level
CO1	Simplify digital circuits using Karnaugh Map.	CL3
CO2	Evaluate the logic design principles through flip flops, counters and registers to develop circuits.	CL3
CO3	Identify and design of memory organization and achieve interconnection.	CL3
CO4	Understand Arithmetic and logical operations and I/O modules.	CL2
CO5	Analyze the functions of basic processing unit with machine instructions and programs.	CL2

LABORATORY CONTENTS

Exp. No.	Experiment Description	CO No.	Bloom's Taxonomy Level
1.	Design and implement Half adder, Half subtractor, Full adder and Full Subtractor using basic gates.	CO1	CL3
2.	Given a 4-variable logic expression, simplify it using appropriate technique and realize the simplified logic expression using 8:1 multiplexer IC.	CO1	CL3
3.	Design and implement code converter I) Binary to Gray (II) Gray to Binary Code.	CO1	CL3
4.	Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working.	CO2	CL3
5.	Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display.	CO2	CL3
6.	Synthesis of Combinational Multipliers to multiply two 4-bit binary numbers.	CO3	CL3
7.	Design and simulate Booth's Multiplier to multiply two signed integers.	CO4	CL3
8.	Design and realization of 16-bit ALU (Arithmetic Logic Unit).	CO4	CL3
9.	Design and simulate 4x4 RAM.	CO5	CL3

Assessment Strategy:

- Assessment will be both CIA and SEE.
- The practical sessions of the IPCC shall be for CIE only.
- The theory component of the IPCC shall be for both CIA and SEE respectively.
- The questions from the practical sessions may also be included for Theory SEE.

SEE Question Paper Pattern:

- The question paper will have **TEN** full questions.
- Each full question consisting of 20 marks.
- There will be 2 full questions from all the FIVE modules.
- Each full question will have a maximum of four sub-questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning,2019
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill, 2002

Reference Books:

1. Digital Principles and Design, Donald D. Givone, 1st Edition, 2002, Tata McGraw-Hill Publishers.
2. Computer Organization And Architecture Designing For Performance, William Stallings 11th Edition, 2019, Pearson.
3. Logic and Computer Design Fundamentals, M. Morris Mano Charles Kime, 4th Edition 2014, Pearson.
4. David A. Bell, Electronic Devices and Circuits, 5th Edition, Oxford University Press, 2008bbbbb
5. Digital Design and Computer Architecture, David M Harris, Sarah L Harris, 2nd Edition, 2013, Elsevier Morgan Kaufmann Publishers.

Reference Web Links and Video Lectures (e - Resources):

1. https://nptel.ac.in/courses/108/105/108105132/
2. https://nptel.ac.in/courses/106/103/106103068/
3. https://nptel.ac.in/content/storage2/courses/106103068/pdf/coa.pdf
4. https://nptel.ac.in/courses/106/105/106105163/
5. https://nptel.ac.in/courses/106/106/106106092/
6. https://nptel.ac.in/courses/106/106/106106166/
7. http://www.nptelvideos.in/2012/11/computer-organization.html
8. http://vlabs.iitkgp.ac.in/coa/index.html
9. http://vlabs.iitkgp.ac.in/dec