EXPERIMENT NO:9

TITLE: Realization of RS, JK and D flip flop using universal logic gates.

OBJECTIVE: To implement RS, JK and D flip flop using NAND gates.

EQUIPMENTS:

Sl No.	Name	Manufacturer	Model No.	Specification

THEORY:

Flip Flops are memory elements capable of storing one bit of information. A flip flop circuit can maintain a binary state indefinitely until directed by an input signal to switch states. A flip flop has two states. A flip flop has two states i.e. set state when Q=1 and reset when Q=1.There are different types of flip flops like RS,JK, D and T flip flops.

Preset (Pr) and Clear (Cr) inputs are called asynchronous inputs.

When Pr=1 and Cr=1 circuit will operate as normal flip flops.
When Pr=1 and Cr=0 the flop flop will reset.
When Pr=0 and Cr=1 the flip flop will set.

The condition Pr=Cr=0 must not be used since, this leads to uncertain state.

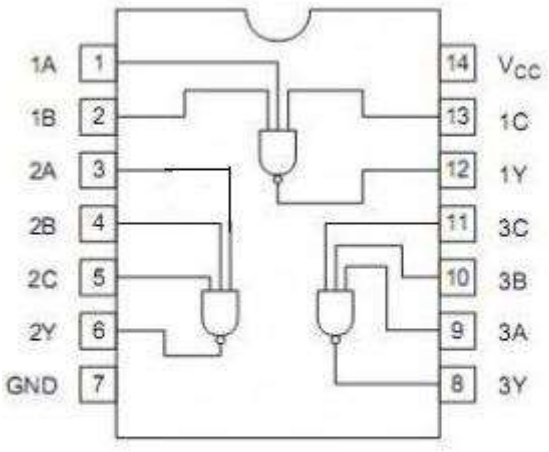
- RS FLIP FLOP: Clocked RS flip flop consists of four NAND gates. When the clock input is low the output remains unchanged. When the clock input is high, output changes according to values of the present.

- JK FLIP FLOP: JK flip flop is a refinement of an RS flip flop. The undefined states in a SR flip flop are defined in a JK flip flop.

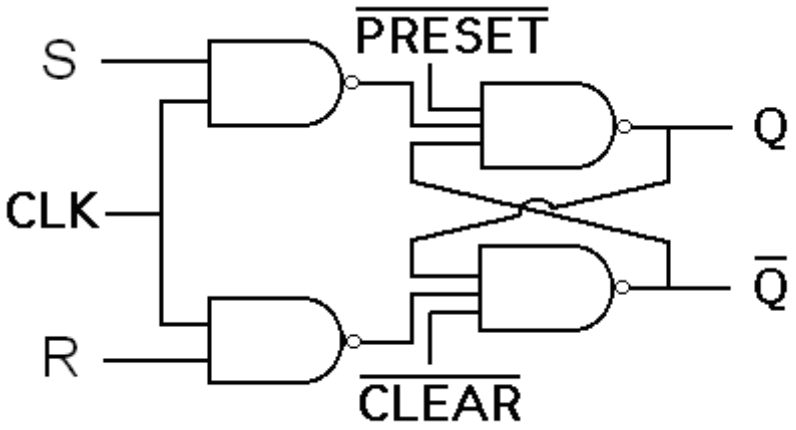
- D FLIP FLOP:D flip flop receives its designation from its ability to transfer data into a flip flop. It is basically. An SR flip flop with an inverter at the R input.

CIRCUIT DIAGRAM

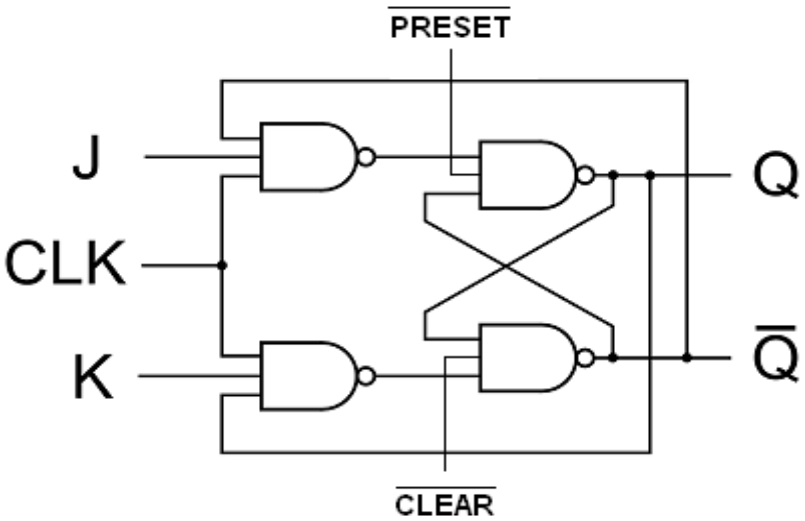
7410 3-input NAND gate



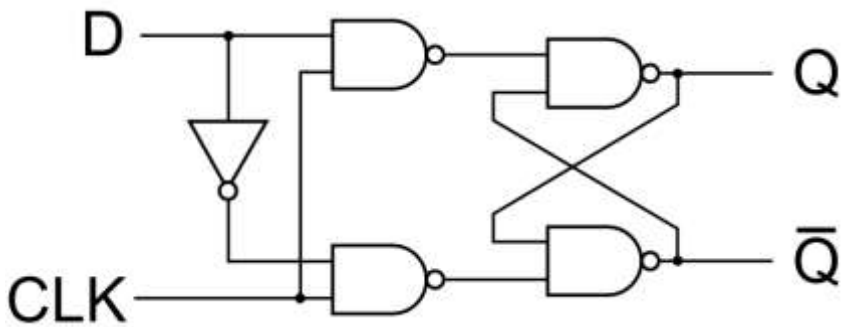
74LS10 Pin Configuration



SR FLIP FLOP



JK FLIP FLOP



D FLIP FLOP

Truth Table:

a)RS flip flop

Clock CK	Preset Pr	Clear Cr	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
1	1	1	0	0	0 (previous condition)		1
1	1	1	0	0	1	1 (previous condition)	0
1	1	1	0	1	0	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	0	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	0	undefined	undefined
1	1	1	1	1	1	undefined	undefined

b) JK flip flop

Clock CK	Preset Pr	Clear Cr	J	K	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
1	1	1	0	0	0	0 (previous condition)	1
1	1	1	0	0	1	1 (previous condition)	0
1	1	1	0	1	0	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	0	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	0	1 (Toggle State)	0
1	1	1	1	1	1	0 (Toggle State)	1

c)*D flip flop*

Clock CLK	Preset Pr	Clear Cr	D	Qn	Q_{n+1}	$\overline{Q_{n+1}}$
1	**1**	**1**	**0**	**0**	**0**	**1**
1	**1**	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**	**1**	**0**

Observation Table:

a)RS flip flop

Clock CK	Preset Pr	Clear Cr	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
H	H	H	L	L	L	L	H
H	H	H	L	L	H	H	L
H	H	H	L	H	L	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	L	H	L
H	H	H	H	L	H	H	L
H	H	H	H	H	L	H (undefined)	H (undefined)
H	H	H	H	H	H	H (undefined)	H (undefined)

b) JK flip flop

Observation Table:

Clock CK	Preset Pr	Clear Cr	J	K	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
H	H	H	L	L	L	L (previous condition)	H
H	H	H	L	L	H	H (previous condition)	L
H	H	H	L	H	L	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	L	H	L
H	H	H	H	L	H	H	L
H	H	H	H	H	L	H (Toggle State)	L
H	H	H	H	H	H	L (Toggle State)	H

c)*D flip flop*

Observational Table:

Clock CLK	Preset Pr	Clear Cr	D	Qn	Q_{n+1}	$\overline{Q_{n+1}}$
H	**H**	**H**	**L**	**L**	**L**	**H**
H	**H**	**H**	**L**	**H**	**L**	**H**
H	**H**	**H**	**H**	**L**	**H**	**L**
H	**H**	**H**	**H**	**H**	**H**	**L**

DISCUSSIONS:

The experimental results were exactly in agreement with the theoretically proposed truth tables and hence the SR, JK and D flip flop were successfully constructed using NAND gates.