

MPI

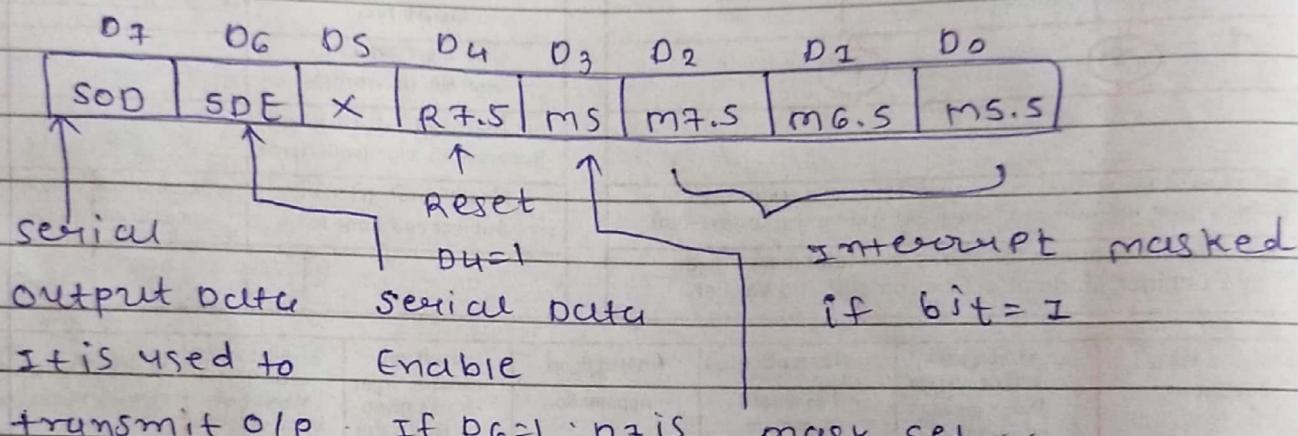
Roll No - 209

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[Q-1]

[a] SIM - Set Interrupt mask



Example:-

MVI A, 08H

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	1	0	0	0

[b] PUSH: Push the register pair onto the stack

PUSH RP

Registers

A			
B	06	40	C
D			E
H			L

Memory

SP →	23	0008
SP →	06	0007
SP →	40	0006
		0005
		0004
		0003
		0002
		0001

PUSH B

SP ← SP - 1

SP ← B

SP ← SP - 1 SP ← C

→ The SP register is decremented and the contents of the high order register (B,D,H) are copied into that location.

→ The SP register is decremented again and the contents of the low-order register (C,E,L) are copied to that location.

POP: POP OFF STACK TO THE REGISTER PAIR
REGISTER

A			
B	06	40	C
D			E
H			L

Memory

POP B

C ← SP

SP ← SP + 1

B ← SP

SP ← SP + 1

$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$

memory

$SP \rightarrow$	03	0008
$SP \rightarrow$	06	0007
$SP \rightarrow$	40	0006
		0005
		0004
		0003
		0002
		0001

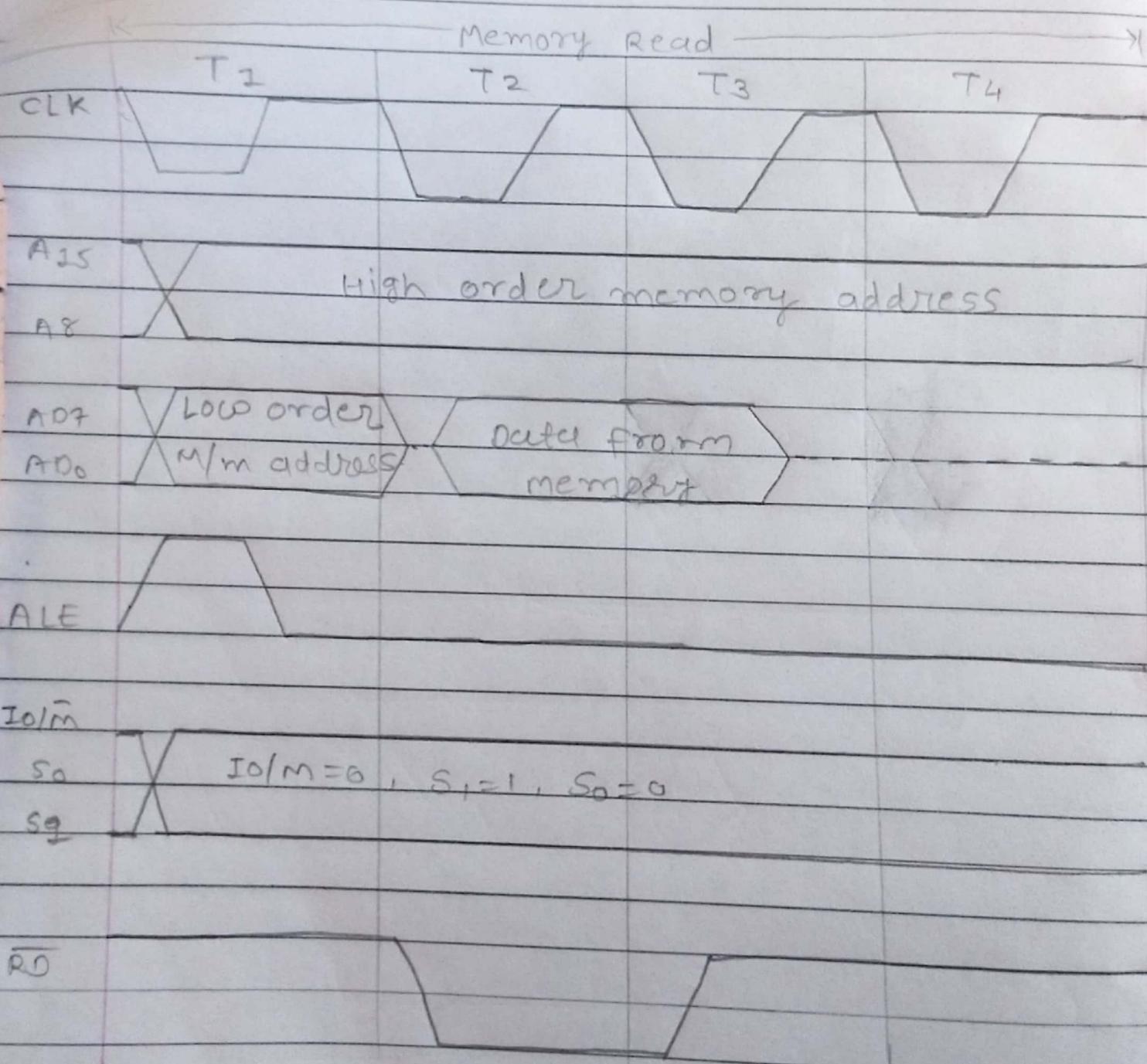
→ The stack pointer is incremented by 1 and the contents of that memory location are copied to the high-order register (B1D1H) of the operand.

→ The stack pointer register is again incremented by 1

C]

[Q-2]

memory read



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$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$

[6] Pin diagram of 8085

X ₁	1	46	V _{cc}
X ₂	2	39	HOLD
RESET OUT	3	38	HLDA
SOD	4	37	CLK(OUT)
SID	5	36	<u>RESET IN</u>
TRAP	6	35	READY
RST 7.5	7	34	I _O /M
RST 6.5	8	33	S _I
RSTS.5	9	32	<u>RD</u>
INTR	10	31	<u>WR</u>
<u>INTA</u>	11	30	ALE
AD ₀	12	29	S _O
AD ₁	13	28	A ₁₅
AD ₂	14	27	A ₁₄
AD ₃	15	26	A ₁₃
AD ₄	16	25	A ₁₂
AD ₅	17	24	A ₁₁
AD ₆	18	23	A ₁₀
AD ₇	19	22	A ₉
V _{SS}	20	21	A ₈

→ 16 signal lines are used as address bus.

A₁₅-A₈ and A₀₇-A₀

→ A₀₇-A₀ are used for dual purpose.

→ A₁₅-A₈ are unidirectional and used to carry High-order address of 16-bit address.

→ A₀₇-A₀ are bidirectional low order address.

Two control signals

1. RD - Active low

2. WR - Active High

Three status signals

1. S₁

2. S₀

3. ~~RESET~~ IO/R

To indicate beginning of operation

ALE \leftarrow 1 Address bus

ALE \leftarrow 0 Data bus

→ S₁ and S₀ are status signals to identify various operations.

→ V_{CC} is power supply pin

→ V_{SS} is ground reference

$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$

→ X1 and X2 is frequency internally pin

→ CLK (OUT) signal is used as system clock for other I/O devices for synchronization with microprocessor.

→ INTR (Input) is used for general purpose interrupt.

→ INTA (Output) - Interrupt Acknowledge.

→ RST 7.5, RST 6.5 and RST 5.5 all are best level interrupts.

→ TRAP is non maskable interrupt and it is highest priority.

→ HOLD pin is hold the address of register.

→ HLDA Hold acknowledge. Hold the request.

→ Ready (Input)

this signal is used to delay the microprocessor read or write cycles until low-responding peripheral is ready to send or accept data.

→ Reset IN - When the signal on this pin goes low the program counter is set to zero, the buses are tri-stated & microprocessor is reset.

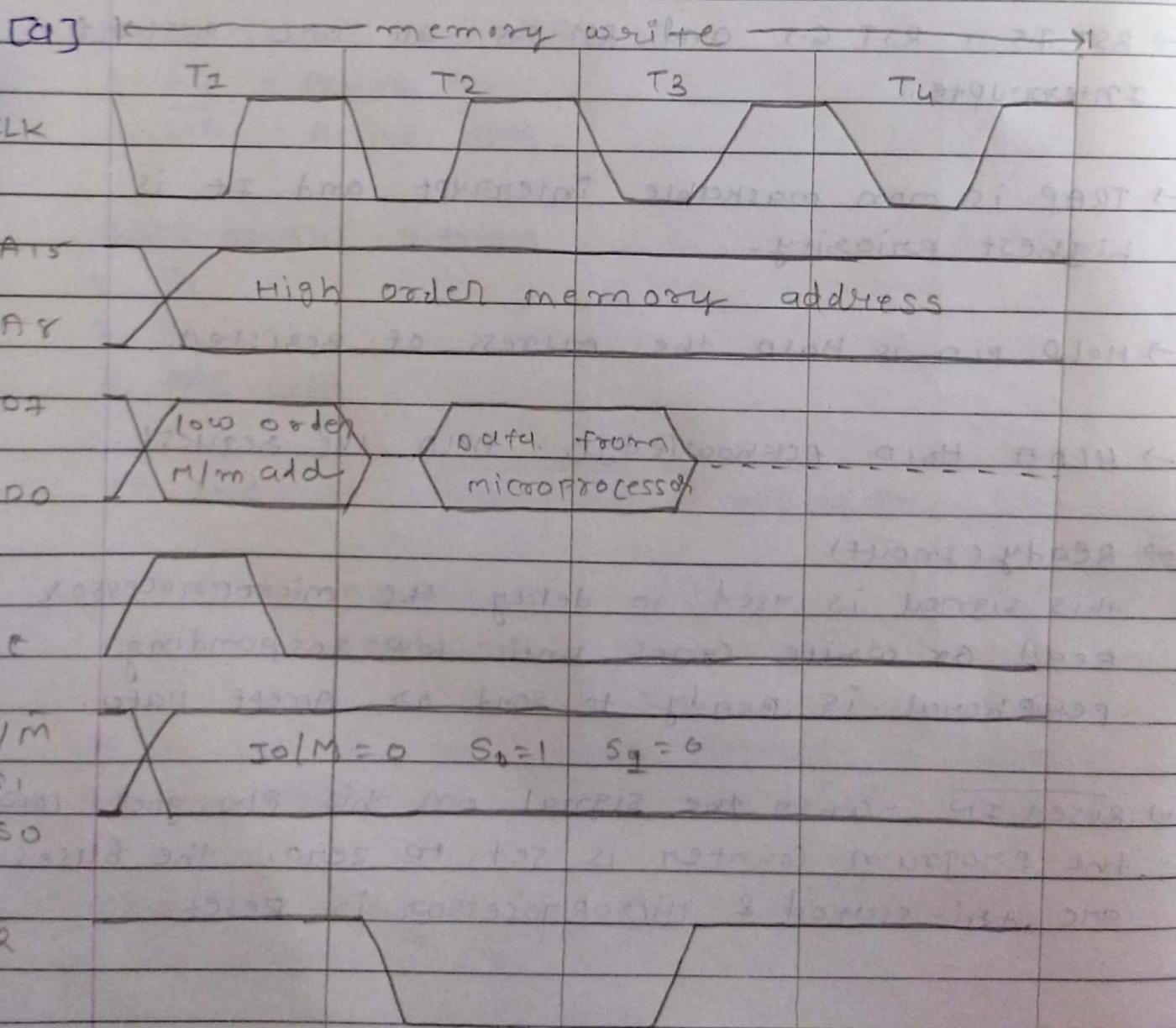
209 = 34H = 00100101011101

→ Reset out - this signal indicates that microprocessor is being reset. The signal is also used to reset other device.

→ SIO - serial input data

SOO - serial output data

Memory write OR



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$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$

[b] Block diagram

- Accumulator used to store 8-bit data to perform arithmetic & logical operations.
- result of operation is stored in accumulator
- Temp Register is used to hold data during ALU operation.
- Instruction Register when instruction is fetched from memory, it is loaded in the Instruction Register.
- Instruction decoder decodes the information present in the instruction register.
- ALU performs computing functions
- Accumulator, temporary Register and flag Registers are part of ALU.
- Each Register can hold 8-bit data.
- These Register pairs can work in pair to hold 16-bit data and their pairing combination is like B-C, D-E & H-L.
- It is 16-bit Register works like stack, which is always incremented / decremented by 2 during push and pop operations.

- multiplexer pulls out the right group of bits, depending on the instruction
- The content stored in the SP and PC is loaded into the Address Buffer and Data/Address Buffer
- x_1 and x_2 are frequency control signals
- CLK OUT perform synchronization with peripheral device.
- Ready Input signal to synchronize microprocessor with peripheral device
- \overline{RD} or \overline{WR} , Read/Write either to / from memory or peripherals.
- ALE Address Latch Enable control signal.
- SOISI shows read/write status memory or I/O.
- HOLD and HLDA control signal.
- Reset microprocessor and other devices.
- TRAP, RST7.5, RST6.5, RST6.5, INTR are interrupt.
- S1D and S0D Serial port communication

[Q-3]

[A] mov A, FF27H

2) LDAX

LXI H, FF27H

LDAX 2

3) LDA

LDA FF27H

[B] → mov

→ The mov instruction is used to move data between registers, memory location and I/O pin

mov B, R

→ LXI

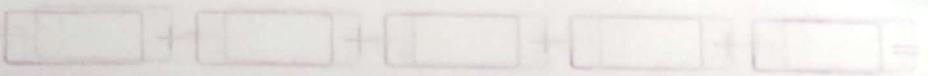
→ The LXI instruction is used to load 16-bit immediate data into a pin

→ LXI HL, 1234H

→ MVI

→ The MVI instruction is used to move 8-bit immediate value into a reg or memory loc.
MVI M, #H.

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[C] load #8H into register C using MVI
MVI C, A8H

→ mask the Higher-order bits (D7-D4) of Register C using ANI
ANI 0FH

→ sent the lower order bits (D3-D0) of register C to an output port using OUT
OUT 01H (assuming) the output port is 01H

[OR]

[Q] 1) MOV

MV M, 58H

2) STAX

MVI A, 58H

LXI H, 1200H

STAX M

3) STA

MVI A, 58H

STA 2000H

$$\boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} + \boxed{\quad} = \boxed{\quad}$$

CB

1) CISC (Complex Instruction set computer)

→ this type of instruction set is designed to perform a wide range of complex instruction that can be executed using a single instruction.

→ CISC instruction sets usually have large instruction sets

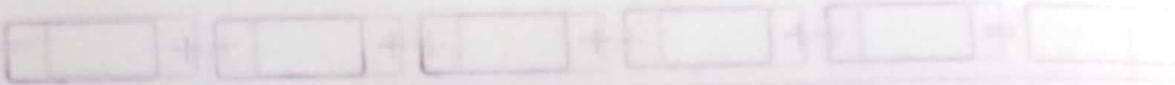
2) RISC (Reduced instruction set computer)

→ this type of instruction set is designed to execute simple instruction at a high speed and minimize the time spent fetching and decoding instruction B.

3) very long instruction sets

→ this type of instruction sets is designed to execute multiple instruction in parallel by combining them into a single structure.

→ use complex scheduling algorithm.



[c]

1) XRA A

register contents: A=0 B=0

flag status: S=0, Z=1, C2=0

2) MVI B, 4AH

register contents: A=0 B=4AH

flag status: S=0, Z=0, C2=0

3) SUI 4FH

register contents: A=B5H B=UAH

flag status: S=1, Z=0, C2=1

4) ANA B

register contents: A=0 B=4AH

flag ~~status~~ status: S=0, Z=1, C2=0

5) HLT

stops the execution of program

register content A=0 B=UAH

flag register S=0, Z=0, C2=0