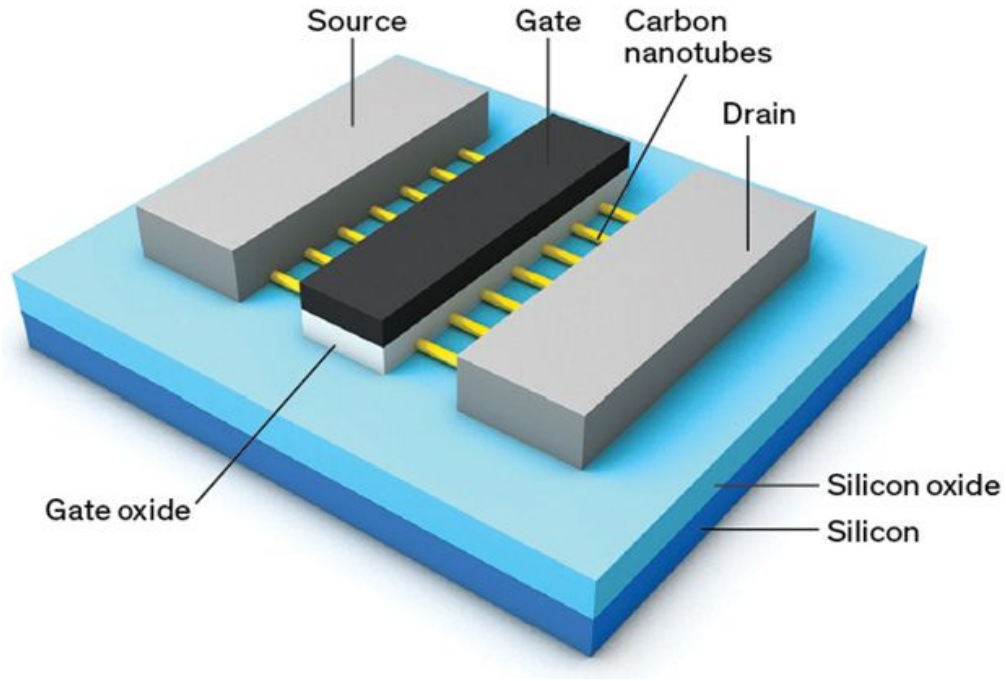
EE-311 (VLSI SYSTEMS & TECHNOLOGY)

CNTFET

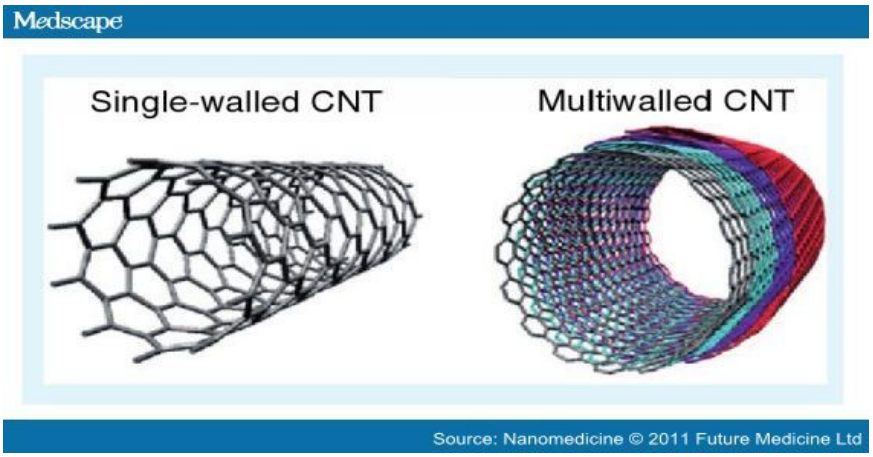
(CARBON NANOTUBE FIELD EFFECT TRANSISTOR)



Introduction-

A **carbon nanotube field-effect transistor (CNTFET)** refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure.

Carbon Nanotube - Carbon nanotubes (CNTs) are cylindrical molecules that consist of rolled-up sheets of single-layer carbon atoms (graphene). They can be **single-walled (SWCNT)** with a diameter of less than 1 nanometer (nm) or **multi-walled (MWCNT)**, consisting of several concentrically interlinked nanotubes, with diameters reaching more than 100 nm. Their length can reach several micrometers or even millimeters.



CNTs are chemically bonded with **sp2 bonds**, an extremely strong form of molecular interaction. ultra-high strength, low-weight materials that possess highly conductive electrical and thermal properties. This makes them highly attractive for numerous applications.

- Their mechanical tensile strength can be 400 times that of steel;
- They are very light-weight – their density is one sixth of that of steel;
- Their thermal conductivity is better than that of diamond;
- They have a very high aspect ratio greater than 1000, i.e. in relation to their length they are extremely thin;
- A tip-surface area near the theoretical limit (the smaller the tip-surface area, the more concentrated the electric field, and the greater the field enhancement factor);
- Highly chemically stable and resist virtually any chemical impact unless they are simultaneously exposed to high temperatures and oxygen - a property that makes them extremely resistant to corrosion;

All these properties make carbon nanotubes ideal candidates for electronic devices, chemical/electrochemical and biosensors, transistors, electron field emitters, lithium-ion batteries, white light sources, hydrogen storage cells, cathode ray tubes (CRTs), electrostatic discharge (ESD) and electrical-shielding applications.

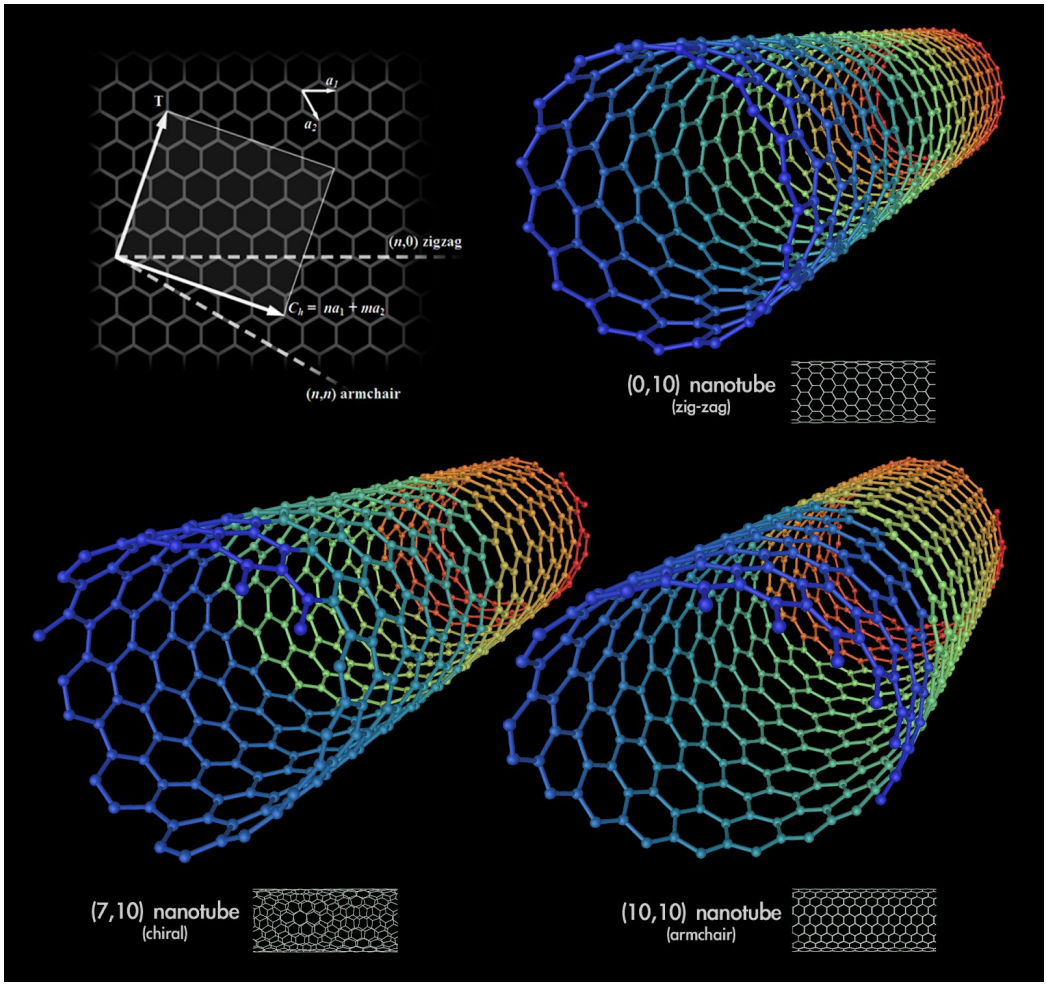
Three types of CNTs can be identified based on way of folding the graphene sheet:

1. Armchair (n1 = n2)
2. Zig-Zag (n1 = 0 or n2 = 0)
3. Chiral (otherwise).

$$C_h = na_1 + ma_2$$

Zig-Zag-One defines a "zigzag" path on a graphene-like lattice as a path that turns 60 degrees, alternating left and right, after stepping through each bond.

Armchair -One define an "armchair" path as one that makes two left turns of 60 degrees followed by two right turns every four steps



Need of New Technology?

- As the size becomes smaller, scaling the silicon MOSFET becomes harder.
- Requirement of high performance channel material.
- High mobility requirement.
- High leakage Currents. (in MOSFETS)
- Extreme Short Channel Effects.
- High Field Effect.
- High charge mobility in Carbon Nanotubes(CNTs).
- CNTFETs can be scaled to much smaller sizes.

EXPLANATION -

- Power supply and Threshold Voltage-
  - The MOSFET channel down-scaling tends to involve proportional reduction in supply voltage to keep electric field and active power within limits. However, the threshold voltage cannot be scaled down much. This is because the passive power (due to transistor off-state leakage) constitutes a significant portion of the total power dissipation in high performance CMOS products. The major power consumed in this state is due to leakage current through the device. Therefore, VT scaling has slowed down to avoid dramatic increase in IOFF. To achieve large drive current, the gate overdrive (VDD – VT) needs to be significant and therefore VDD scaling also has to slow down, which results in increase active power density.

- High electric fields-
  - As mentioned above, the supply voltage cannot be reduced in proportion to channel length, hence the scaling will increase the electric field strength across the gate oxide. Carrier mobilities are degraded due to higher vertical electric fields in MOSFET channel which in worst cases can cause breakdown

of the barrier and hence higher leakage currents which can cause damage to the device.

- Gate oxide tunneling-
  - Since the electron thermal voltage, kT/q, is a constant at room temperature, the ratio between operating voltage and the thermal voltage shrinks with scaling down of MOSFET. This leads to higher leakage currents stemming from the thermal diffusion of electrons. With reduction in channel lengths, an appropriate reduction in oxide thickness is also needed. The thin oxide films subject to quantum mechanical tunneling, giving rise to gate leakage current that increases exponentially as the oxide thickness is scaled down. Further scaling can be realized by replacing the oxide gate dielectric with a high-permittivity (high-k) gate dielectric.

- Parasitic resistances and capacitances-
  - As transistor dimensions are reduced, parasitic resistances and capacitances both scale unfavorably with reduced pitch. Therefore, influence of parasitic elements on concurrent increases significantly. These parasitic elements will diminish the performance gain by transistor scaling.

- Hot-carrier-
  - When carriers possess high energies having effective temperature greater than the lattice temperature, they are said to be hot. These carriers are not in thermal equilibrium with the lattice because they cannot transfer their energy to the lattice atoms fast enough. They are generated in inverted channel region when MOSFET is operating in linear or saturation mode. The main problems which arise due to hot carriers are parasitic gate currents, drain current degradation, decrease in transconductance, shift of threshold voltage with time. Using graded drain profile reduces generation of hot carriers.

- Source to drain tunneling-
  - If the MOSFETs channel length between source and drain becomes small enough for electrons to tunnel through the barrier without the gate bias, it

can no longer be operated as a switch. Device scaling should be carried out with appropriate limits on dimensions for proper behavior .

- Randomness of dopant distribution-
  - The effect of randomness of dopant distribution on the MOSFET characteristics becomes more extreme in small devices, because precise position of the individual dopant atoms cannot be managed. So, as the device dimensions are reduced it becomes difficult to place the dopant atoms at exact and required positions.

- Heat dissipation-
  - MOSFETs release their energy in the form of heat in the resistive parts. If this heat is not dissipated properly, hot spots are created on the circuit which causes the material to overheat resulting in malfunction of the device.

- Interconnect delays-
  - Reduction of the wire width increases the resistance and hence increases the delay. This reduces the speed and hence device may not function much faster due to large interconnect delays. The purpose of scaling is not only to increase the device density on chip but also to increase its speed.
- Short-channel effect-
  - As the channel length becomes comparable to the source-substrate or drain-substrate depletion depth, the total amount of depletion charge in the substrate decreases. This results in **reduction of threshold voltage.**

As the device scaling is approaching its physical size limitations, the technology cycle is getting slow down due to increasing power consumption, process variation, and fabrication cost. To continue the historical growth for the next decade, various studies have been conducted to overcome ever increasing challenges. Nowadays there are device scaling tradeoffs between performance and power consumption, therefore technological innovations which can achieve high performance through very low power are required. These efforts have made conventional MOSFETs evolve in various ways with new materials, new structures, and so on.

Theoretical Analysis & Working Principle-

In the past few decades, miniaturization of transistors has always obeyed the **moore's law**: the number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years. Nanoscale field effect transistors in the **sub-10 nm regime**, suffer from short channel effects such as direct tunneling from source to drain, increase in gate-leakage current and punch-through effect. These effects have posed severe problems for miniaturized transistors and directed the recent research toward better alternative semiconductors than silicon.

Semiconducting **carbon nanotubes (CNTs)** because of their properties like large mean free path, excellent carrier mobility and improved electrostatics at nanoscales as the result of their non-planar structure, have been known as the best ideal replacement for silicon.

Theoretically, CNTFETs could reach a higher frequency domain (terahertz regime) than conventional semiconductor technologies.

By using a single-wall CNT as the channel between two electrodes which work as the source and drain contacts of a FET, a **coaxial CNTFET** can be fabricated. Coaxial devices are of special interest because their geometry allows for better electrostatics because the gate contact wraps all around the channel (CNT) and has a very good control on carrier transport.

Type of **Metal-CNT** contacts plays a crucial role in the output characteristics of the transistor. Heavily doped semiconductors because of the ability to form Ohmic contacts can be used as ideal electrodes but they suffer from high parasitic resistance.Existence of potential barrier at the metal-CNT interface, changes the device to a CNTFET resembling to Schottky barrier MOSFETs. However, heavily doped CNT contacts can be used to get to a behavior similar to conventional MOSFETs.

CNTFETs can be fabricated with Ohmic or Schottky contacts.The type of the contact determines the dominant mechanism of current transport and device output characteristics.

CNTFETs are mainly divided into **Schottky barrier CNTFETs (SB-CNTFETs)** with metallic electrodes which form Schottky contacts and MOSFET-like CNTFETs with doped CNT electrodes which form Ohmic contacts.In SB-CNTFETs, tunneling of electrons and holes from the potential barriers at the source and drain junctions constitutes the current. The barrier width is modulated by the application of gate voltage, and thus, the transconductance of the device is dependent on the gate voltage

The other type of the CNTFETs takes advantage of the n-doped CNT as the contact. Potassium doped source and drain regions have been demonstrated and the behavior like MOSFETs have been experimentally verified. In this type of transistors a potential barrier is formed at the middle of the channel and modulation of the barrier height by the gate voltage controls the current.

Working principle-

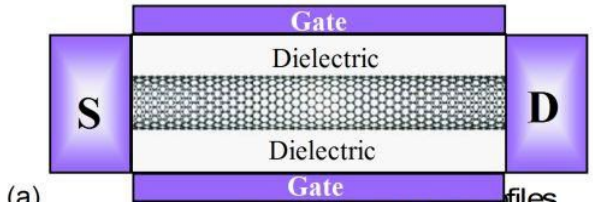
Basic principle operation of CNFET is the same as MOSFET where electrons are supplied by source terminal and drain terminal will collect these electrons .

In other words, current is actually flowing from drain to source terminal .

Gate terminal controls current intensity in the transistor channel and the transistor is in off state if no gate voltage is applied.

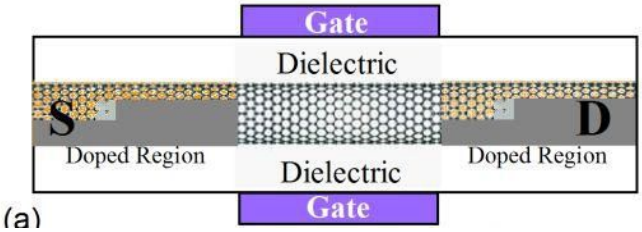
SB CNTFET-

- SB-CNFET works on the principle of direct tunneling through the schottky barrier at the source channel junction .
- The barrier width is controlled by the gate voltage and hence the transconductance of the device depends on the gate voltage.
- At low gate bias, large barrier limits the current in the channel . As gate bias is increased, it reduces the barrier width, which increases quantum mechanical tunneling through the barrier , and therefore increases current flow in transistor channel.
- In SBCNET, the transistor action occurs by modulating the transmission coefficient of the device.



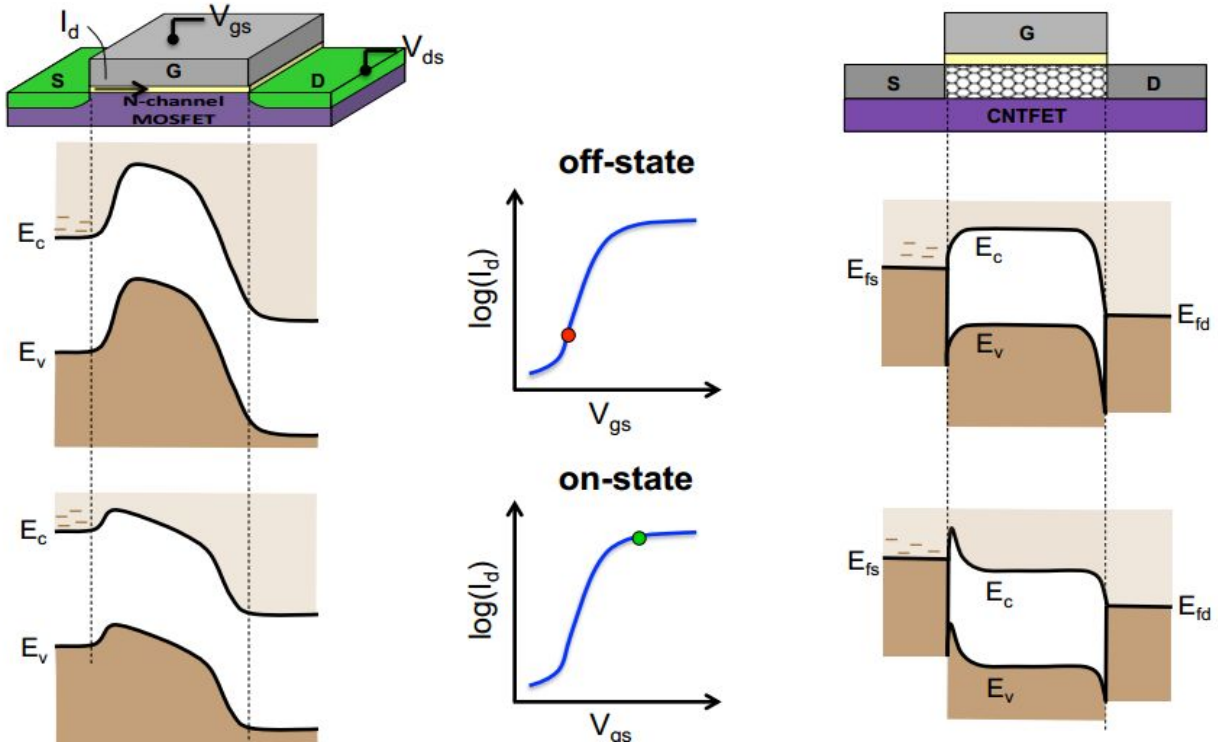
MOSFET like CNTFET-

- The structure of this device is slightly different than SB-CNFET since it used heavily doped terminals instead of metal.
- This device is formed in order to overcome problems in SB-CNFET by operating like normal MOSFET.
- This device operates on the principle of modulation the barrier height by gate voltage application. The drain current is controlled by number of charge that is induced in the channel by gate terminal.

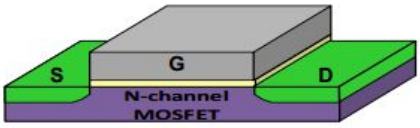


How CNTFET works?

•Operation of CNTFET compared with Si-MOSFET



Standard MOSFET



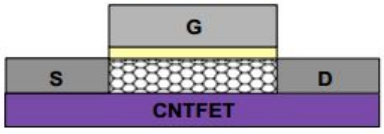
$$I_d = \mu_{eff} \frac{W}{L} C_{ox}\left(V_g - V_t\right) V_{ds}$$

- μ_{eff}: carrier mobility
- $\frac{W}{L}$: spatial dependence
- $C_{ox}\left(V_g - V_t\right)$: charge in channel
- V_{ds}: bias dependence

→ no DOS consideration

→ no consideration of contacts

CNTFET



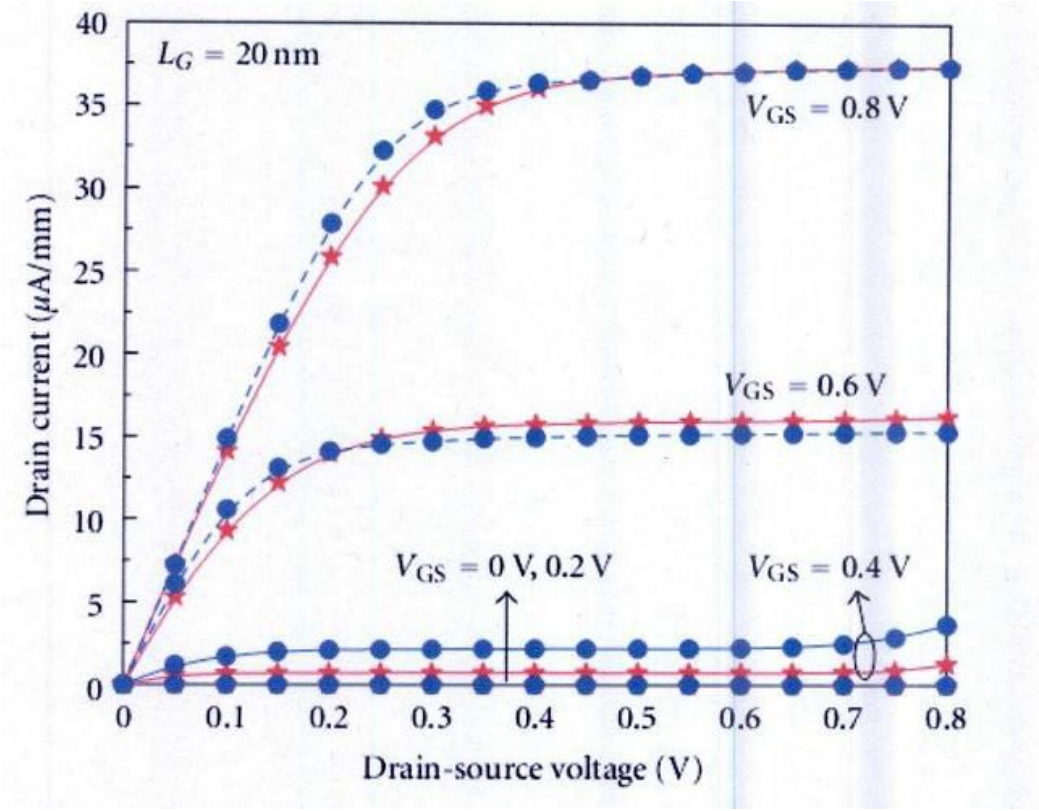
$$I_d = q \int_{E_{fs}}^{E_{fd}} f(E,T) \cdot v(E) \cdot T(E) \cdot D(E) \cdot dE$$

- $\int_{E_{fs}}^{E_{fd}} f(E,T)$: bias dependence (carrier injection determined by states between source/drain Fermi levels)
- $v(E)$: carrier (Fermi) velocity
- $T(E)$: transmission at contacts
- $D(E) \cdot dE$: charge in channel

→ no spatial dependence

→ no mobility dependence

Id/Vds curve-



	MOSFET	CNTFET
Gc	5uF/cm2	2.4uF/cm2
Id	500uA/um	1500 uA/um
Mobility	7x10^6 cm/s	3.5x10^6 cm/s
Thermal velocity	-	2 times of mosfet

Important Aspects of CNTFETs-

3.1. Ambipolarity

One of the important aspects of nanotube transistors is the ambipolarity or unipolarity of their current-voltage characteristics. SB-CNTFETs exhibit strong ambipolar behavior. For high enough gate voltages the tunneling probability of electrons through the source schottky barrier in the conduction band is high and for the low and negative gate voltages, a Schottky barrier is formed at the drain in valence band and tunneling of holes increases the current. However for MOSFET-like CNTFETs only positive gate voltages because of lowering the barrier in the channel increase the current.Ambipolar behavior of the SB-CNTFETs constraints the use of these transistors in conventional CMOS logic families.

3.2. High Permittivity Gate Dielectrics

The relatively low dielectric constant of SiO_2 (at 3.9) limits its use in transistors as gate lengths scale down to tens of nanometers. As the device dimensions approach the 10 nm regime, strong electrostatic coupling of source/drain electrodes arises fundamental challenges especially about the gate control over the channel. Enhancing the gate efficiency requires thinner gate oxides. However, due to excessive direct tunneling leakage currents through the ultra-thin dielectric, the gate dielectric layer is already approaching its limit (~ 1nm) and the only feasible way is to use high-κ gate dielectrics which afford high gate capacitance without relying on ultra-small film thickness.

3.3. On/Off Current

Comparison shows that MOSFET-like CNTFETs due to absence of Schottky barriers have a lower off leakage current. On the other hand, in the on state, there is no barrier at the source-channel junction and hence, the device demonstrates significantly higher on current. The minimum current of the SB-CNTFETs occurs when the contribution of the electron and hole tunneling currents to the total current becomes equal, that is when $V_G = V_D/2$ where the energy band diagram is symmetric. For each power supply voltage (V_D), the off-current is defined as the minimal leakage point $V_G(off) = V_D/2$ and the on-current is defined at $V_G(on) = V_G(off) + V_D$. There exists a trade-off: reducing the off-current by lowering the power supply voltage degrades the on-current.

3.4. Transconductance

transconductance (g_m) of the SB-CNTFETs is severely limited by the Schottky barriers in the on state.transconductance of the MOSFET-like CNTFET is higher than the SB-CNTFET. The high-κ gate insulator improves the CNTFET performance by reducing the self-consistent potential produced by the charge on the tube.For the SB-CNTFETs the transconductance tends to saturate when the gate insulator dielectric constant is large. The reason is that the self-consistent potential produced by the charge on the tube is already small and further improving the gate dielectric constant does not help to significantly reduce the Schottky barrier thickness and the transistor performance

3.5. Gate Capacitance

For a one dimensional nanotube FET, the total capacitance between the gate and the channel (gate capacitance) depends both on the geometry and the density of states (DOS). If the electrostatic potential on the channel (V_S) is uniform, then the voltage drop over the gate oxide is also uniform and the gate voltage V_G is the summation of the channel potential and the voltage drop over the gate oxide. This can be modeled as the potential division between two capacitances which means the gate capacitance (total capacitance) can be modeled as a series of electrostatic (geometry dependent) capacitance and the quantum (DOS dependent) capacitance

3.6. Fringing Capacitance

The fringing fields between the gate metal and source and drain contacts result in capacitances which are called fringing or parasitic capacitances. Fringing field becomes more important when the channel length of a CNTFET is reduced.

3.7. Cutoff Frequency

The cutoff frequency of the intrinsic CNTFET is called the intrinsic and the cutoff frequency of the CNTFET with inclusion of the parasitic capacitances is called the extrinsic cutoff

frequency. When the parasitic capacitances are small extrinsic cutoff frequency approaches the intrinsic cutoff frequency.

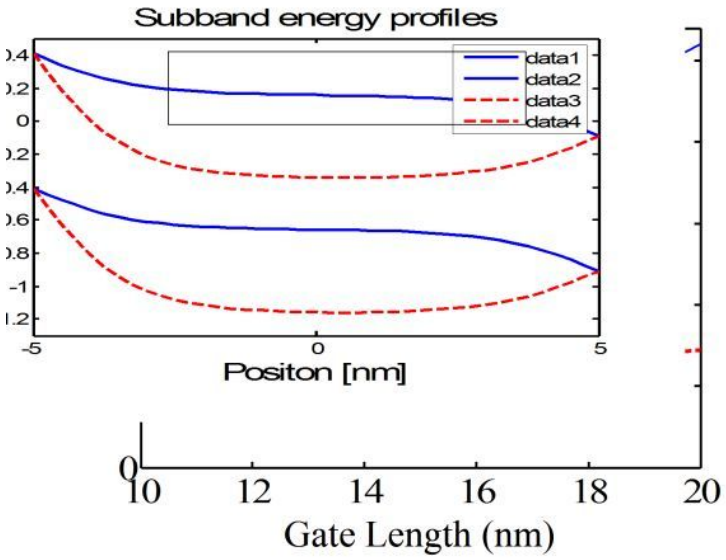
$$\frac{1}{2\pi f_T} = (R_S + R_D)C_{gd} + \frac{1}{g_m}(C_g + C_{gs} + C_{gd}) + \frac{g_d}{g_m}(R_S + R_D)(C_g + C_{gs} + C_{gd})$$

3.8. Intrinsic Delay

The main limitation to a faster intrinsic delay time is the gate capacitance resulting from fringing fields through the high-κ dielectric directly from the gate to source and gate to drainThe intrinsic delay is one of the most important performance metrics for digital electronic applications and characterizes how fast a transistor switches. The **switching delay** can be calculated from:

$$\tau = (Q_{on} - Q_{off})/I_{On}$$

Qon is the total charge of the channel at on state (VG = VD(on));
Qoff is the total charge of the channel at off state (VG=0, VD = VD(on));
IOn is the on current.



Fabrication of CNTFETs-

INTRODUCTION-

Common problems in the fabrication of carbon nanotube field-effect transistors (CNTFETs) include the positioning of tubes across electrodes and poor device electrical performance due to the presence of metallic nanotubes intermixed with semiconducting ones.

Types of CNTFETs-

There are four major types of CNTFETs based on their evolution:

1. Back-gated CNTFETs
2. Top-gated CNTFETs
3. Wrap-around gate CNTFETs
4. Suspended CNTFETs

The fabrication and evolution of each of these CNTFETs are discussed in detail in this report. The Top-gated CNTFETs are studied in more detail because there is a good trade-off between the device performance and the complexity of design and fabrication, in the case of these particular CNTFETs.

A. Back-gated CNTFETs

The earliest techniques for fabricating carbon nanotube (CNT) field-effect transistors involved

- Pre-patterning parallel strips of metal across a silicon dioxide substrate, and
- Depositing the CNTs on top in a random pattern (as shown in Figure-1a).
- The semiconducting CNTs that happened to fall across two metal strips meet all the requirements necessary for a rudimentary field-effect transistor.

- One metal strip is the "source" contact while the other is the "drain" contact.
- The silicon oxide substrate can be used as the gate oxide and adding a metal contact on the back makes the semiconducting CNT gateable (Figure-1b).

This technique suffered from several drawbacks:

1. The first was the metal contact, which actually had very little contact with the CNT, since the nanotube just lay on top of it and the contact area was therefore very small.
2. Due to the semiconducting nature of the CNT, a Schottky barrier forms at the metal-semiconductor interface, increasing the contact resistance.
3. The second drawback was due to the back-gate device geometry. Its thickness made it difficult to switch the devices on and off using low voltages, and the fabrication process led to poor contact between the gate dielectric and CNT.

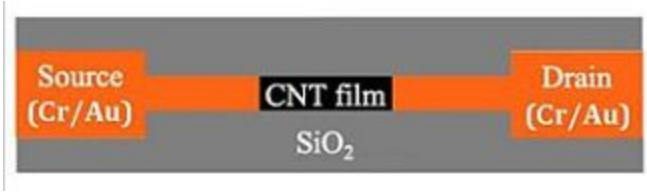


Figure-1a

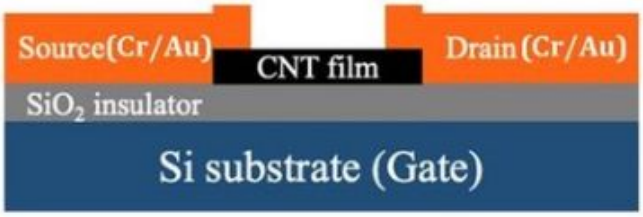


Figure-1b

B. Top-gated CNTFETs

Eventually, researchers migrated from the back-gate approach to a more advanced top-gate fabrication process (step-by-step Process in Figure-2):

- In the first step, single-walled carbon nanotubes are solution deposited onto a silicon oxide substrate.
- Individual nanotubes are then located via an atomic force microscope or scanning electron microscope. After an individual tube is isolated, source and drain contacts are defined and patterned using high-resolution electron-beam lithography.
- A high temperature anneal step reduces the contact resistance by improving adhesion between the contacts and CNT.
- A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporation or atomic layer deposition.
- Finally, the top gate contact is deposited on the gate dielectric, completing the process.

Advantages of Top-gated CNTFETs:

- Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case.
- Due to the thinness of the gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage.

Due to these advantages, the top-gated CNTFETs are generally preferred over the back-gated CNTFETs.

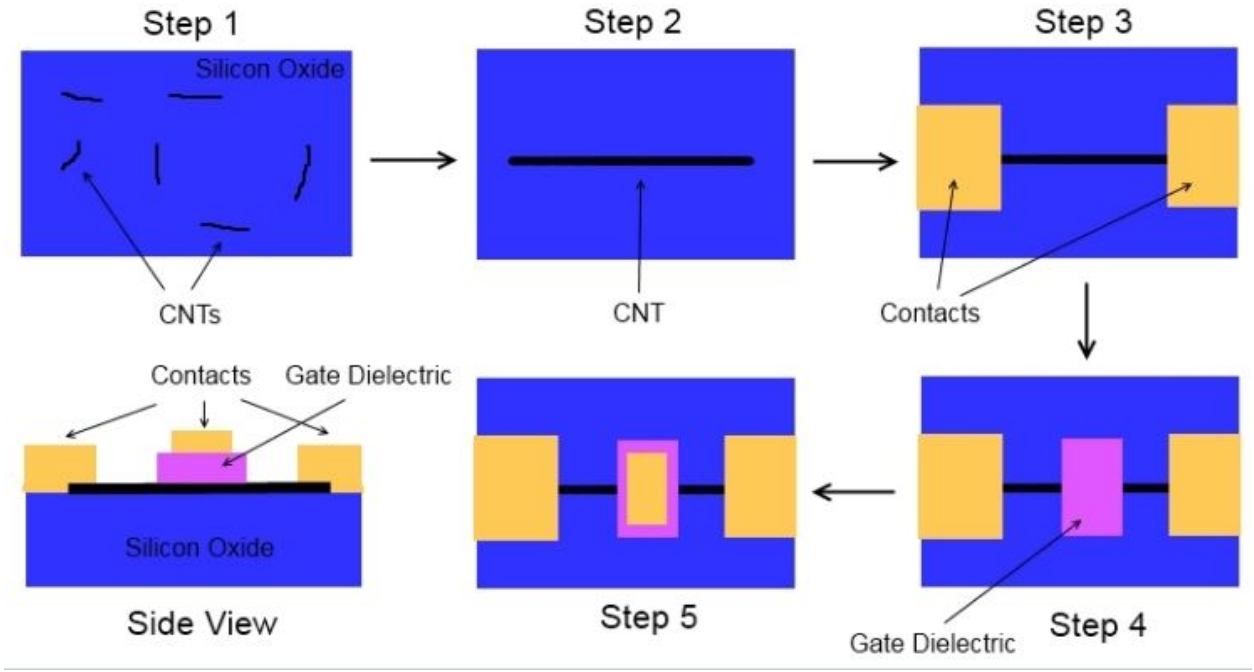


Figure-2: Fabrication Steps of Top-gated CNTFET

C. Wrap-around gate CNTFETs

Wrap-around gate CNTFETs, also known as gate-all-around CNTFETs were developed in 2008 and are a further improvement upon the top-gate device geometry.

In this device, instead of gating just the part of the CNT that is closer to the metal gate contact, the entire circumference of the nanotube is gated (Figure-3). This should ideally improve the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.

- Device fabrication begins by first wrapping CNTs in a gate dielectric and gate contact via atomic layer deposition.
- These wrapped nanotubes are then solution-deposited on an insulating substrate, where the wrappings are partially etched off, exposing the ends of the nanotube.
- The source, drain, and gate contacts are then deposited onto the CNT ends and the metallic outer gate wrapping.

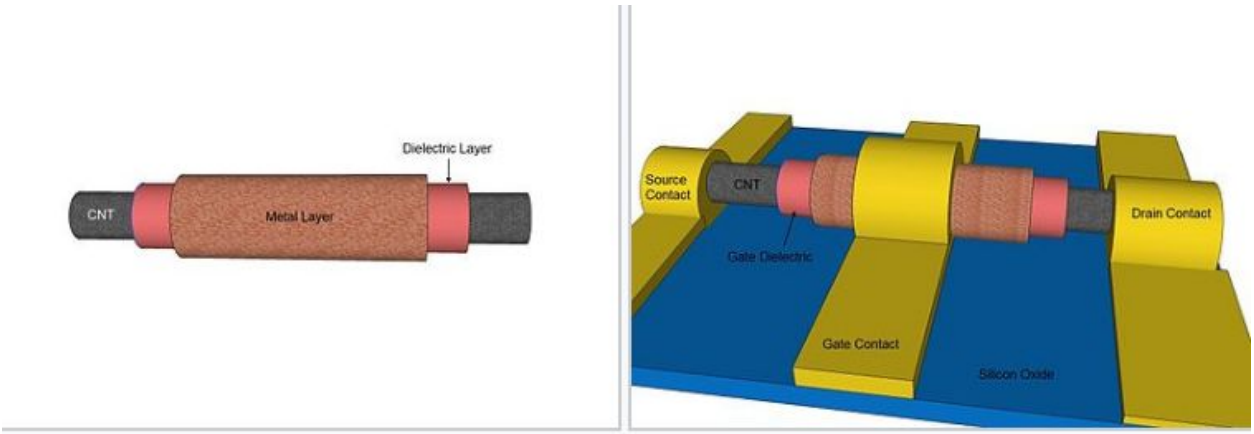


Figure-3

D. Suspended CNTFETs

Yet another CNTFET device geometry involves suspending the nanotube over a trench to reduce contact with the substrate and gate oxide (Figure-4). This technique has the advantage of reduced scattering at the CNT-substrate interface, improving device performance.

There are many methods used to fabricate suspended CNTFETs, ranging from growing them over trenches using catalyst particles, transferring them onto a substrate and then under-etching the dielectric beneath and transfer-printing onto a trenched substrate.

- The main problem suffered by suspended CNTFETs is that they have very limited material options for use as a gate dielectric (generally air or vacuum)
- And applying a gate bias has the effect of pulling the nanotube closer to the gate, which places an upper limit on how much the nanotube can be gated.
- This technique will also only work for shorter nanotubes, as longer tubes will flex in the middle and droop towards the gate, possibly touching the metal contact and shorting the device.

In general, suspended CNTFETs are not practical for commercial applications, but they can be useful for studying the intrinsic properties of clean nanotubes.

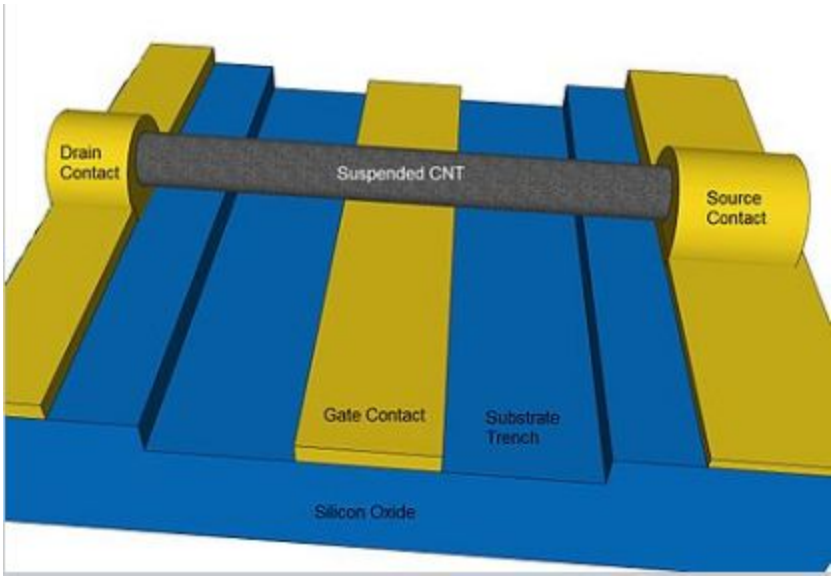


Figure-4

Relevant activities over recent years

Here are some recent activities related to the CNTFETs and some brief specifications:

1. (1998) First-ever FET based on CNTs

- Discovered by **Sander J. Tans, Alwin R. M. Verschueren & Cees Dekker**.
- Two metal Electrodes were used in the fabrication of this CNTFET.
- Single Wall CNTs (SWCNTs) were used.
- This CNTFET could be operated at room temperature, which was a big achievement of that time.
- I-V data in accordance with the available semiconductors models of that time.

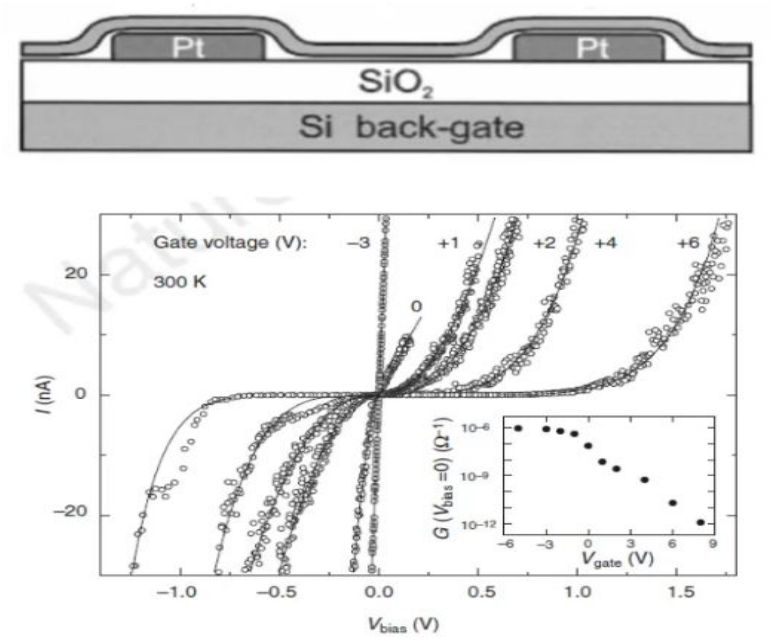


Figure-5: First CNTFET and its IV characteristics

2. (2001) Single walled CNTs based FETs logic circuits

- Gain was observed to be greater than (>) 10dB.
- On-Off ratio of these devices was found to be 105.
- Different logic operations were successfully implemented.

3. (2006) Five stage Ring Oscillator on a single CNT

- 12 CNTFETs were used to make the ring oscillator.
- Resonance was observed at frequencies of 13MHz and 52MHz at voltages of 0.5 V and 0.92 V respectively.
- The per stage delay of 1.9 ns was there in the oscillator.

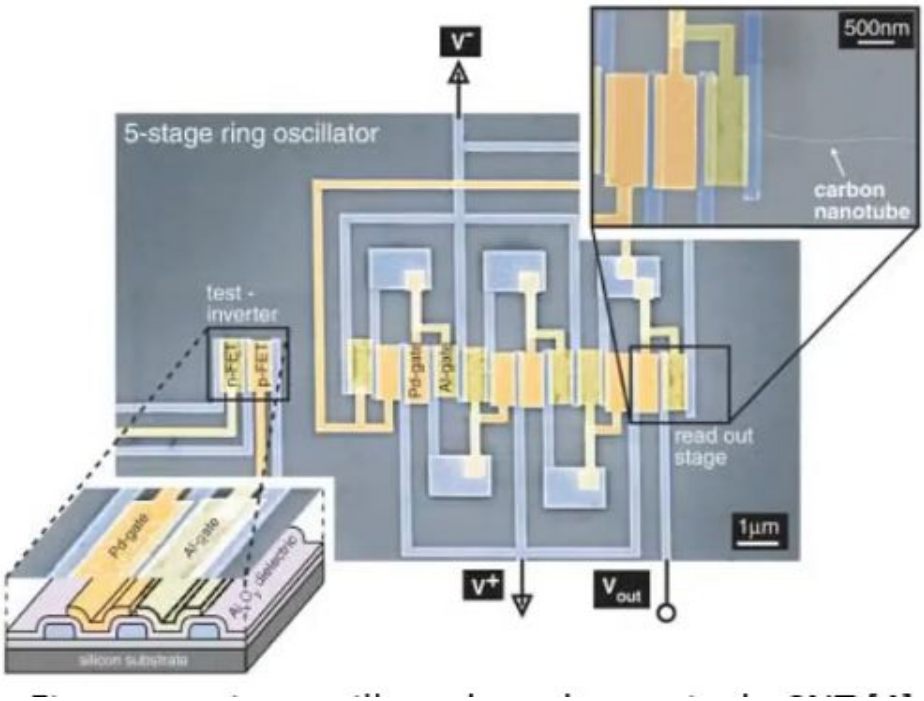


Figure-6: Ring Oscillator using CNTFETs

4. (2008) Nanotube transistor radios

SWCNT FETs were used to build Audio amplifiers, RF mixers, fixed RF amplifiers and resonant antennas.

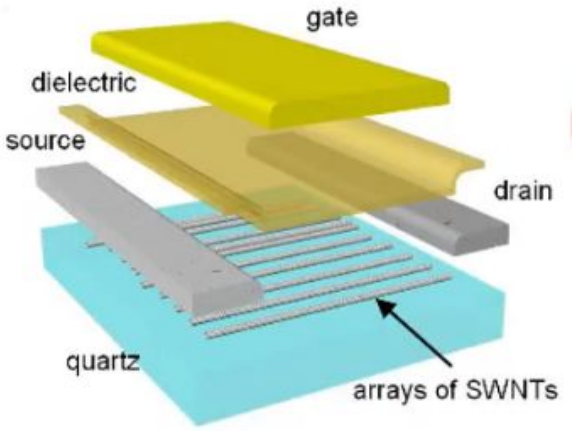
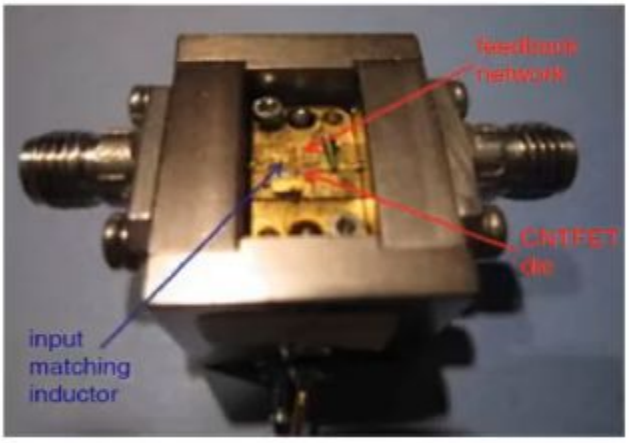
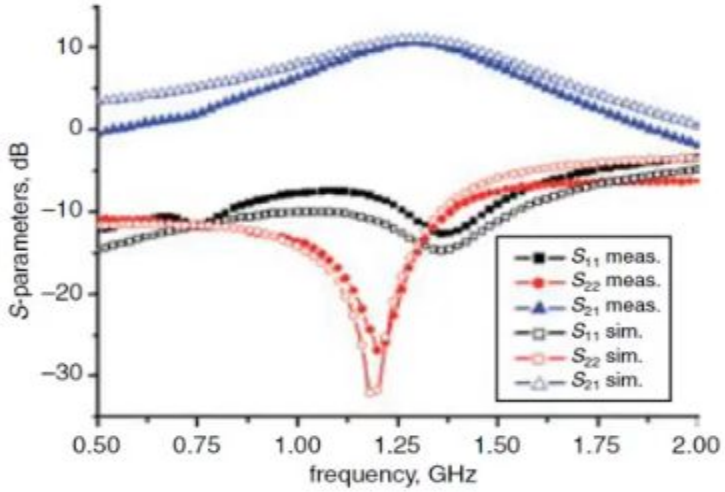


Figure-7

5. (2011) First CNTs based L-band RF amplifier

- Observed Gain > 11dB at a frequency of 1.3GHz.
- Input/Output return loss < 10dB.





L band amplifier with S-parameters |

Figure-8

6. (2013) CNT transistor based computer

- Integer sorting and counting at the same time
- Realization of future electronic systems with high energy efficiency.

7. (2017) Realization of nanotube transistors with 5nm gate length

- High on-state current
- Large conductance at room temperature
- CNTFETs used with graphene contacts, which leads to:
    1. Reduction of Drain/Source parasitic capacitances.
    2. Reduction of short channel effects.

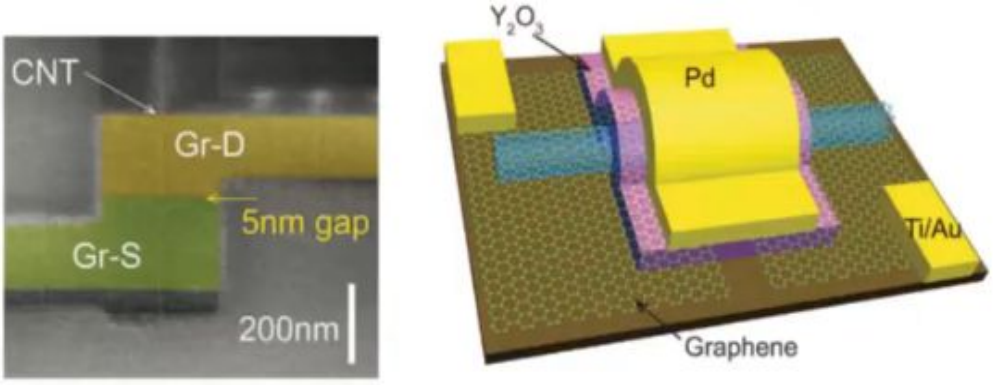


Figure-9: CNTFET with graphene contacts

8. (2017) First CNTFET with 40nm footprint

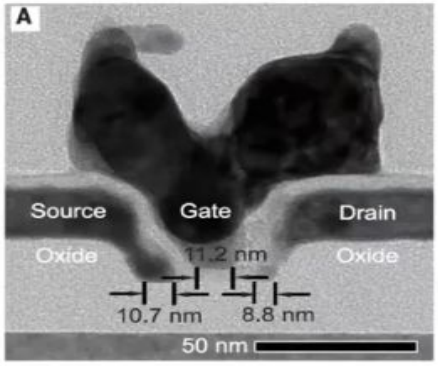


Figure-10: TEM image of the 40nm Footprint CNTFET

9. (2017) Fabrication of Five stage ring oscillator

- Built with complimentary carbon nanotubes.
- Switching frequency of 2.82 GHZ can be achieved.

Applications-

CNTFET-based devices offer high mobility for near-ballistic transport, high carrier velocity for fast switching, as well as better electrostatic control due to the quasi-one-dimensional structure of CNTs.

Therefore, these devices have tons of applications in the electronics industry, some of them are:

1. Digital logic design (taking place of the currently used CMOS).
2. SRAM design.
3. DRAM design(Figure-5).
4. High-frequency applications like RADAR and Satellite-communication.
5. Analog design: Design of analog devices like op-amps, which find applications in a wide range of electronics products and gadgets like TVs, stereos, computers, other ICs, etc.
6. CNTFET technology has a bright future in the area of Mobile and wireless RF applications.

Basically, CNTFETs can take the place of all the MOSFETs used in any device.There are lots of other applications of these CNTFET devices and there is a great scope of these devices and hopefully, we will see such devices replacing the conventional MOSFETs in the near future.

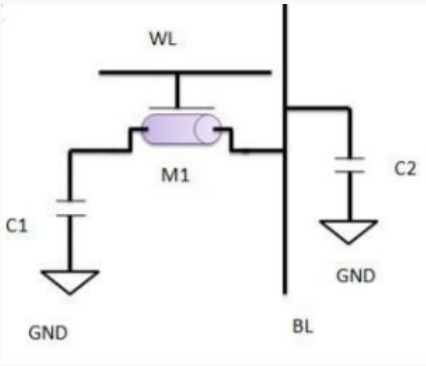


Figure-11: 1 Transistor DRAM cell

Figure Of Merits

- Better control over channel formation
- Better threshold voltage : The **threshold voltage**, commonly abbreviated as V_{th}, of a field-effect transistor (FET) is the minimum gate-to-source voltage $V_{GS\,(th)}$ that is needed to create a conducting path between the source and drain terminals. The threshold voltage of CNTFET is better than CMOS.
- High electron mobility : The **electron mobility** characterises how quickly an electron can move through a metal or semiconductor, when pulled by an electric field. Mobility is usually a strong function of material impurities and temperature, and is determined empirically. Mobility values are typically presented in table or chart form. Mobility is also different for electrons and holes in a given material. CNTFET have higher electron mobility as compared to other useful MOSFETs.
- High Performance : CNTFET have a high **Performance-to-power** ratio as compared to other MOSFETs which give CNTFET an upper hand over other MOSFETs and CMOS.
- High current density : **Current Density** is the amount of charge per unit time that flows through a unit area of a chosen cross section. Current density is important to the design of electrical and electronic systems.
- High transconductance : **Transconductance** also infrequently called mutual conductance, is the electrical characteristic relating the current through the output of a device to the voltage across the input of a device. Conductance is the reciprocal of resistance.

  The present generation CNTFET have recorded a very high transconductance with respect to CMOS and other used FET devices .
- Device Scaling : Device scaling is one of the most important factors while choosing a particular FET device. There have been various advancements in this field with respect to CNTFET and scaling to very small channel length(~9nm) have been recorded till now.

Disadvantages-

- Lifetime : Carbon nanotubes degrade in a few days when exposed to oxygen. There have been several works done on passivating the nanotubes with different polymers and increasing their lifetime.Carbon nanotubes have recently been shown to be stable in air for many months and likely more, even when under continual operation.

- Reliability : Carbon nanotubes have shown reliability issues when operated under high electric field or temperature gradients. Avalanche breakdown occurs in semiconducting CNT and joule breakdown in metallic CNT.

- Production cost : Although CNTs have unique properties such as stiffness, strength, and tenacity compared to other materials, especially silicon, there is currently no technology for their mass production and high production cost. To overcome the fabrication difficulties, several methods have been studied such as direct growth, solution dropping, and various transfer printing techniques.

Future Work-

As the scaling down of silicon MOSFET is approaching its utmost limit, different materials are effectively being examined in order to keep the scaling trend. Among these, carbon nanotubes (CNTs) have emerged as one of the most extensively studied materials due to their excellent performance properties such as minimal short channel effects, high mobility, and high normalized drive currents. CNTFET are looking forward as the future of nanoscale devices in the electronics industries.

The most desirable future work involved in CNTFETs will be the transistor with higher reliability, cheap production cost, or the one with more enhanced performances. For example, such efforts could be made: adding effects external to the inner CNT transistor like -

- Schottky barrier between the CNT and metal contacts
- multiple CNTs at a single gate
- channel fringe capacitances
- parasitic source/drain resistance
- series resistance due to the scattering effects.

Conclusion-

From the above report given with respect to Carbon Nanotube Field Effect Transistor(CNTFET) which include its introduction, working , fabrication and also its advantages/disadvantages it can be concluded that Carbon Nanotube Field Effect Transistor(CNTFET) are considered as the future for nanoscale devices in the electronic industry and various development in this field can be very crucial in the advancement of the electronic industry in the near future.

The evolution of CNTFET over the last two decades have made this CNTFET technology as a potential candidate to replace the traditional CMOS devices and various other FET devices.Also considering the advancement in the carbon nanotube industry , the CNTFET technology have the capability to go below 7nm node and scaling to a very small channel length measuring upto 9nm have been recorded as the recent activity in this field .Also the high frequency application due to high mobility ,thermal ruggedness and high possible linearity have made CNTFET a better choice over the traditional CMOS devices.

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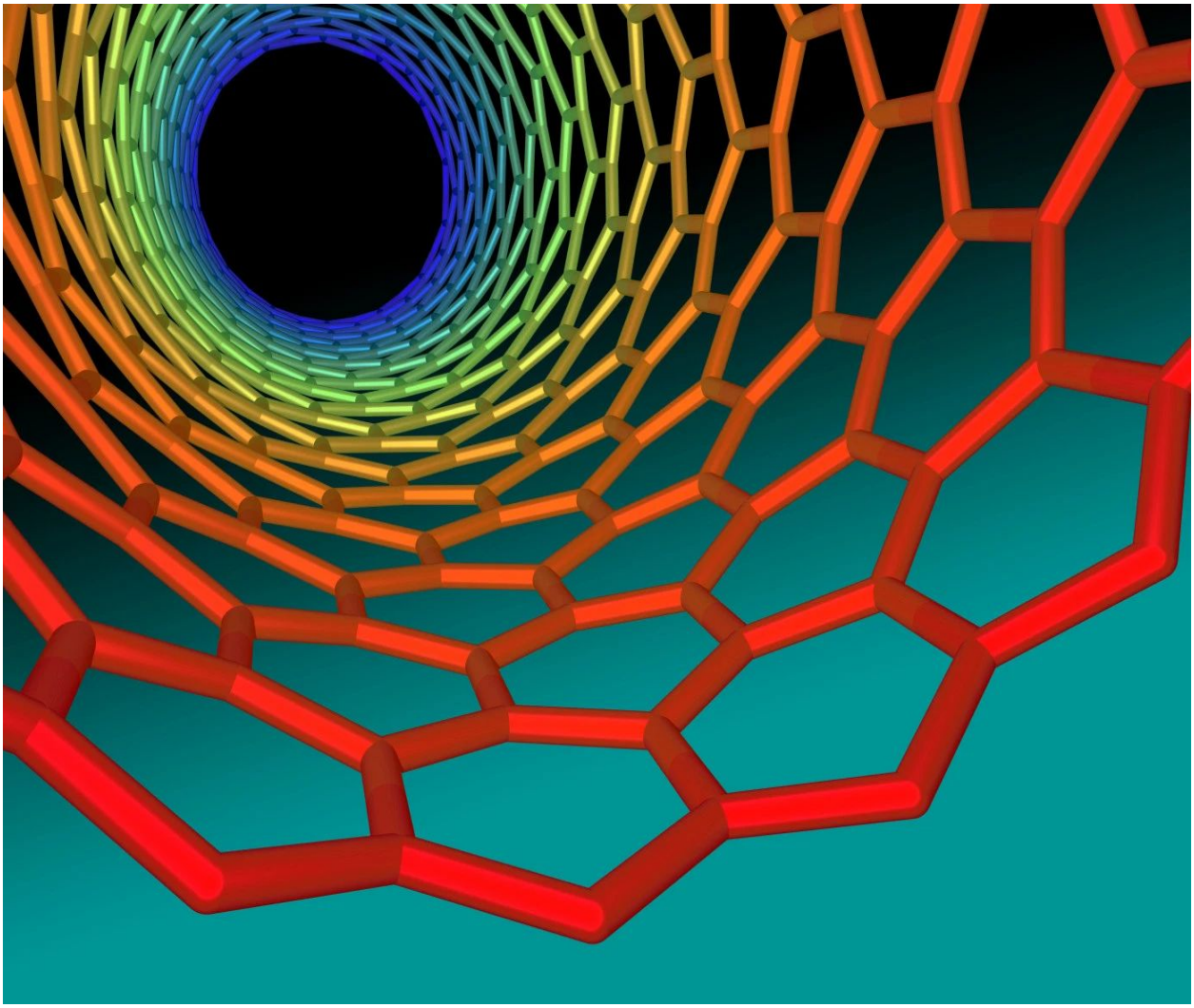

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