BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus First Semester 2020-2021

CS F342 Computer Architecture Lab-3

Implement Instruction Memory for the following instructions.

The instruction format is given as follows:

Type	Instruction	31	30 2	9 2	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	. ;	3	2	1	0
			O	осо	de					rs					rt					rd				s	han	nt	100			f	fun	ct		
	sub	000000			rs						rt					rd				00000						100010								
R	add	000000			rs					rt					rd				00000						100000									
	or	000000					rs					rt					rd					00000						100101						
1	addi	001000				rs						rt									immediate													

The following instructions are to be implemented (in the given order):

- 1) sub \$s2, \$s1, \$s0
- 2) add \$t3, \$t2, \$t0
- 3) or \$s1, \$t1, \$t4
- 4) addi \$t4, \$s0, 0x000D

The instruction format for R-type instructions is as follows:

instr rd, rs, rt

The instruction format for I-type instructions is as follows:

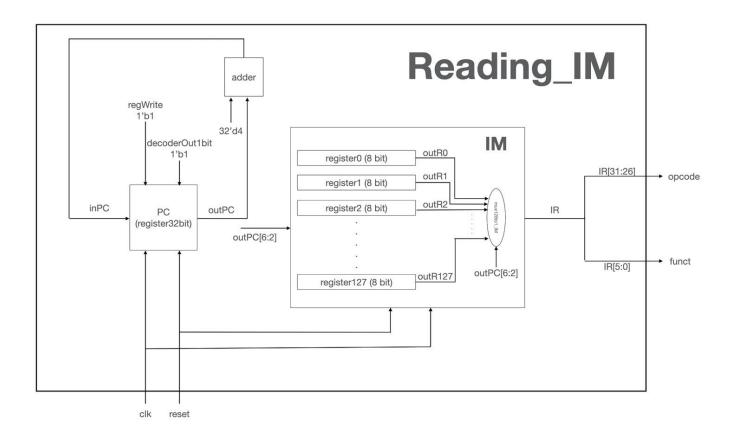
instr rt, rs, imm

The MIPS register numbers are as follows:

Name	Number	Use
\$0	0	the constant value 0
\$at	1	assembler temporary
\$v0-\$v1	2–3	function return value
\$a0-\$a3	4-7	function arguments
\$t0-\$t7	8-15	temporary variables
\$ s0 -\$ s7	16–23	saved variables
\$t8-\$t9	24–25	temporary variables
\$k0-\$k1	26–27	operating system (OS) temporaries
\$gp	28	global pointer
\$sp	29	stack pointer
\$fp	30	frame pointer
\$ra	31	function return address

Circuit diagram:

https://drive.google.com/file/d/1_ka7agWnAWveTYxppYHyg2366PSDrPu/view?usp=sharing



The required output signals to be tested for each instruction are:

- a) IR[31:26] (opcode) (2 marks)
- b) IR[5:0] (funct) (2 marks)

The expected waveform is as follows:

