

Practical – 05

Class: - B.E.E&TC

Subject: - VLSI Design and Technology

Aim: - To implement an inverter (not gate), NAND, NOR gate & 1 Bit Half Adder using CMOS technology

Theory :-

A] CMOS Inverter:

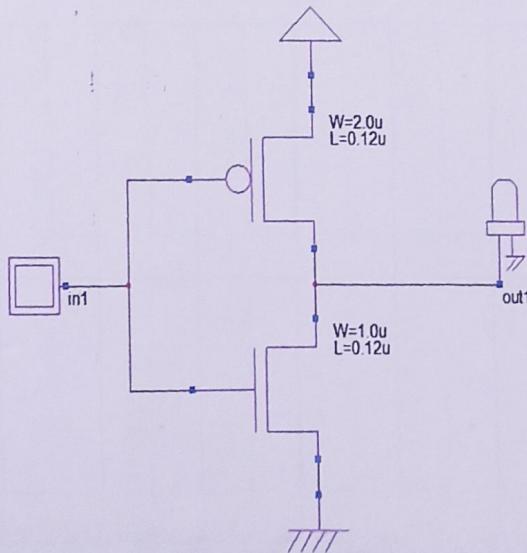
A logic inverter can be constructed by using one P-MOS and N-MOS inverter when there is '0' at input , then output is '1' and vice versa. In general a fully complementary always has n-Switch in pull down at output.

Truth table of Inverter:-

INPUT	OUTPUT
0	1
1	0

This is truth table of logic inverter where when there is a '0' at the input the output is '1' and when there is '1' at the input one output will zero.

Schematic of CMOS Inverter



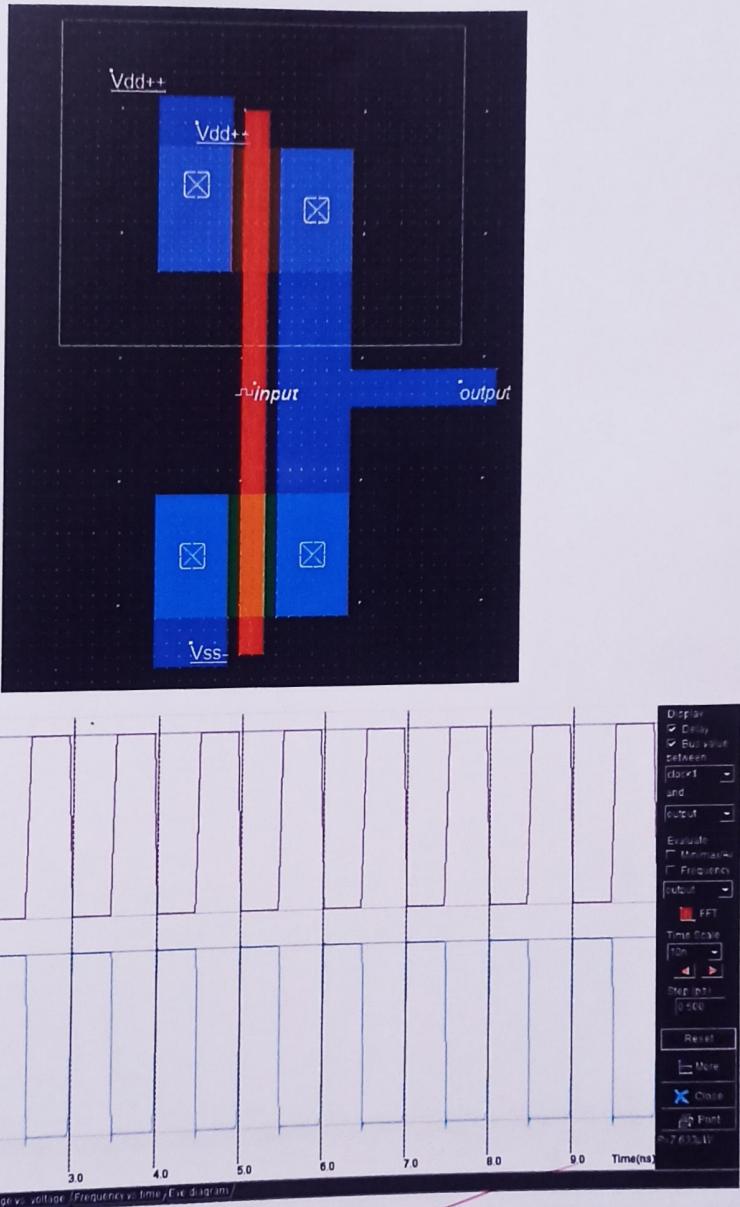
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Part A: $W_p=W_n=1 \mu\text{m}$, $L_n=L_p=0.2 \mu\text{m}$

Design Layout & Timing Diagram of CMOS Inverter



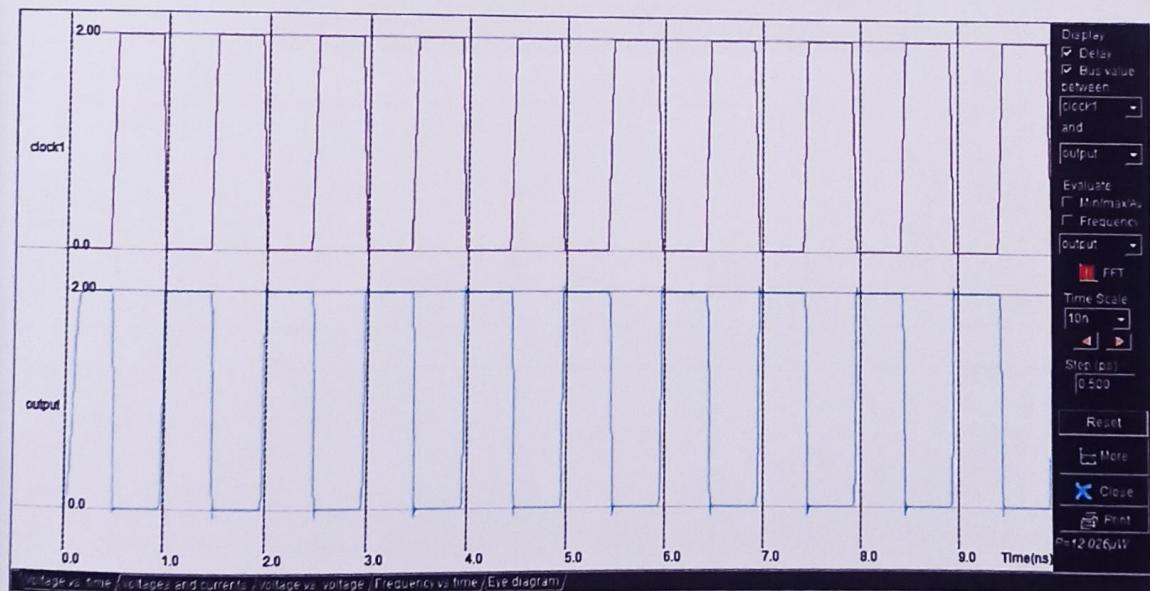
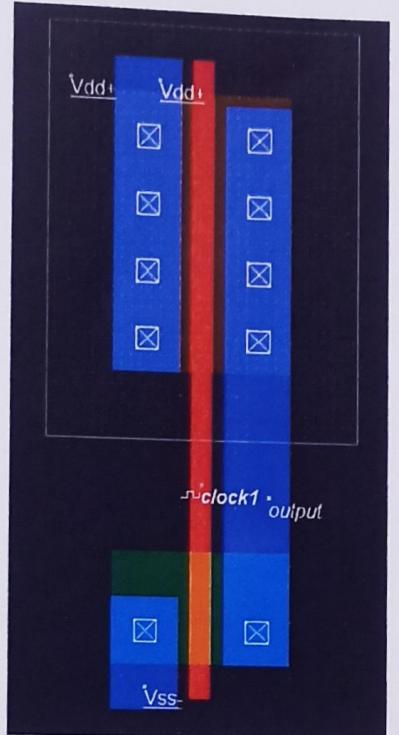
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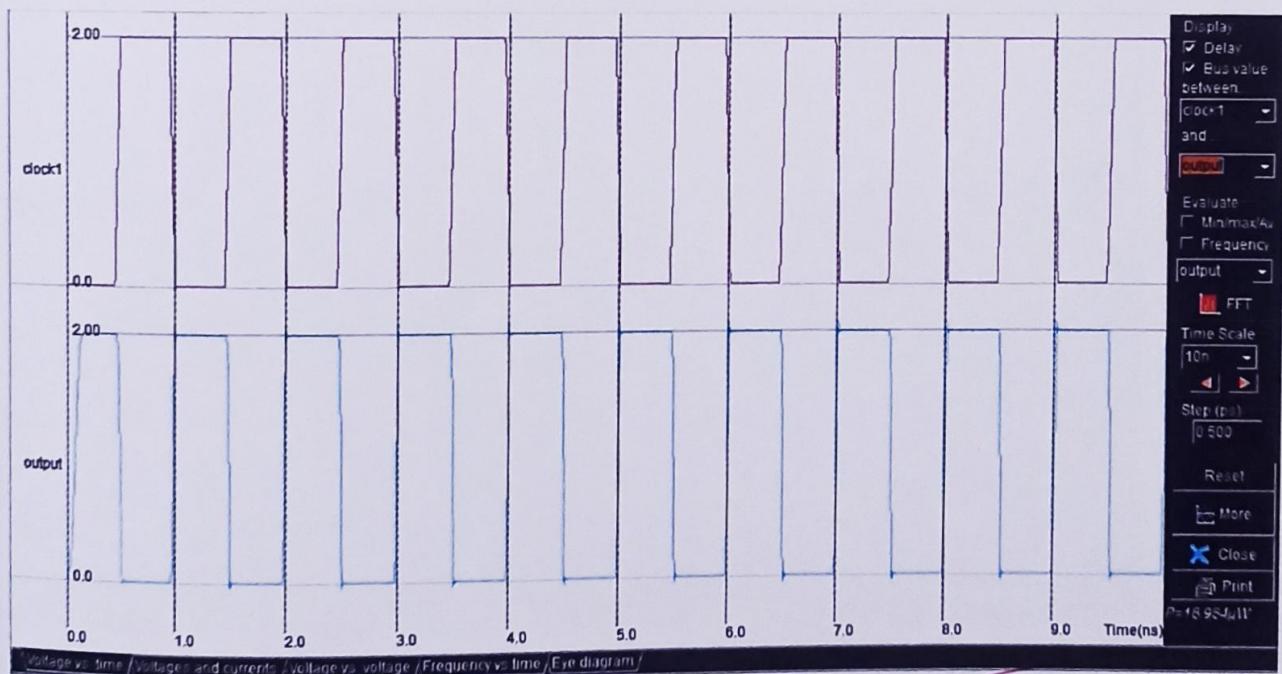
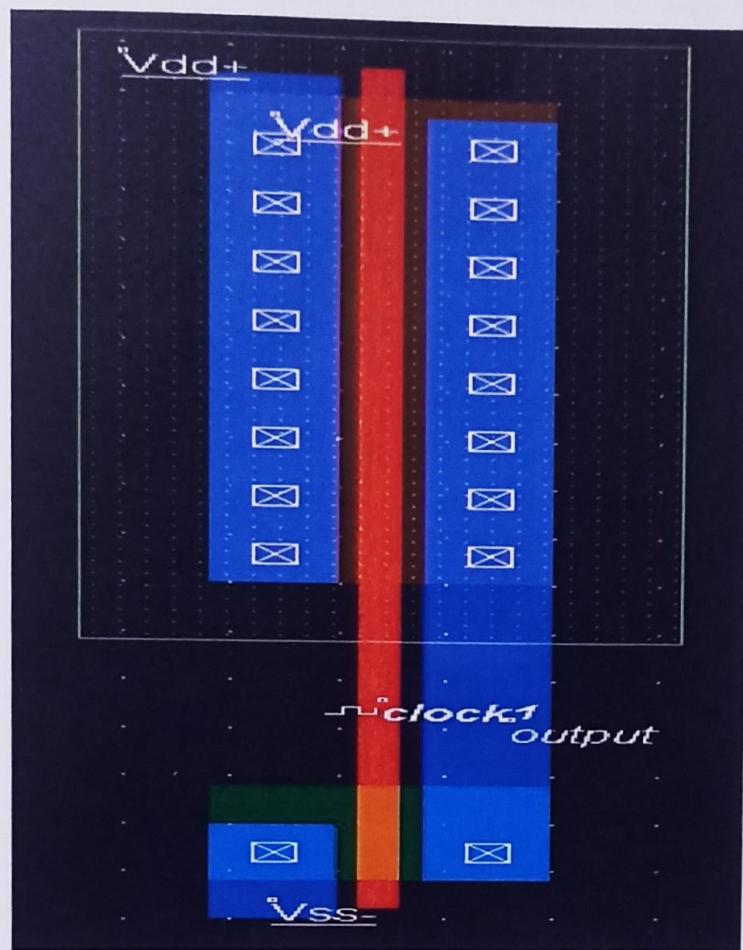
Part B: $W_p=2.5W_n$ ($W_n=1 \mu\text{m}$) , $L_n=L_p=0.2 \mu\text{m}$

Design Layout & Timing Diagram of CMOS Inverter



Part C: $W_p=5W_n$ ($W_n=1 \mu\text{m}$) , $L_n=L_p=0.2 \mu\text{m}$

Design Layout & Timing Diagram of CMOS Inverter



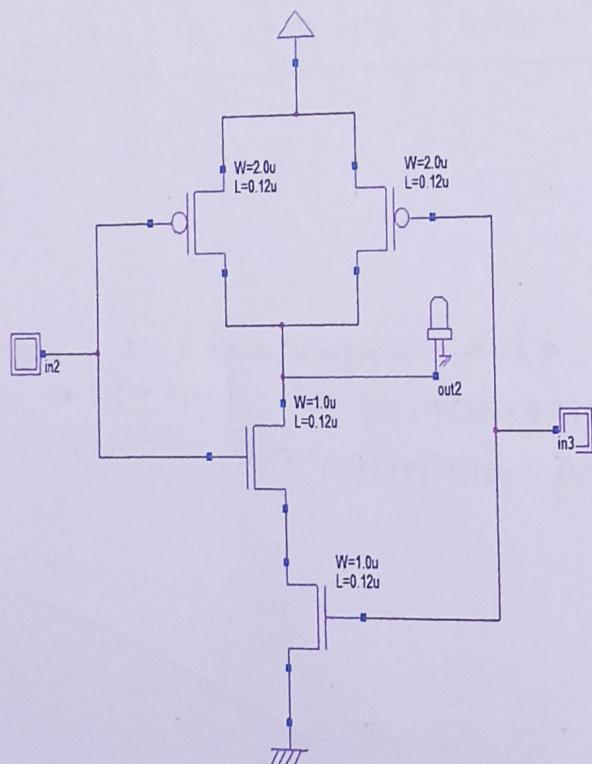
B] CMOS NAND Gate

Theory :- NAND Gate is formed by connecting an inverter i.e. NOT gate at the output of an AND gate

Truth Table:-

Input		Outputs
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Schematic of CMOS NAND Gate:



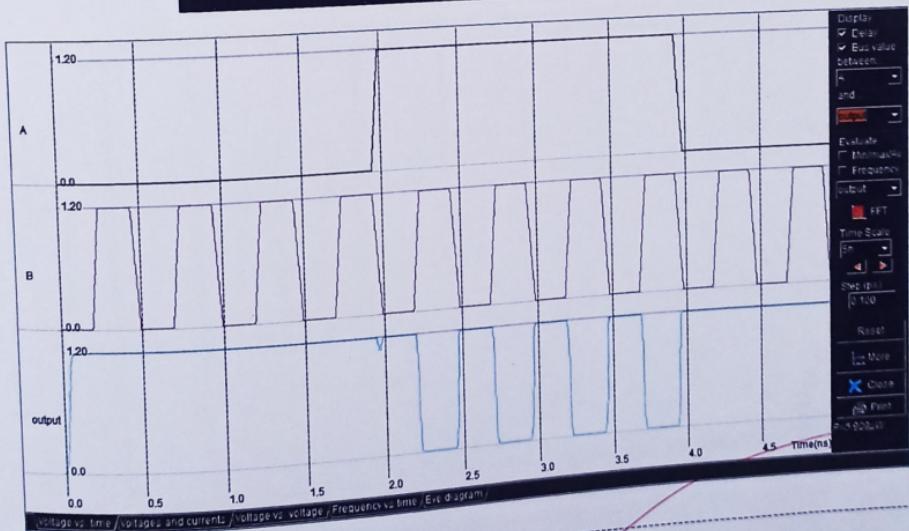
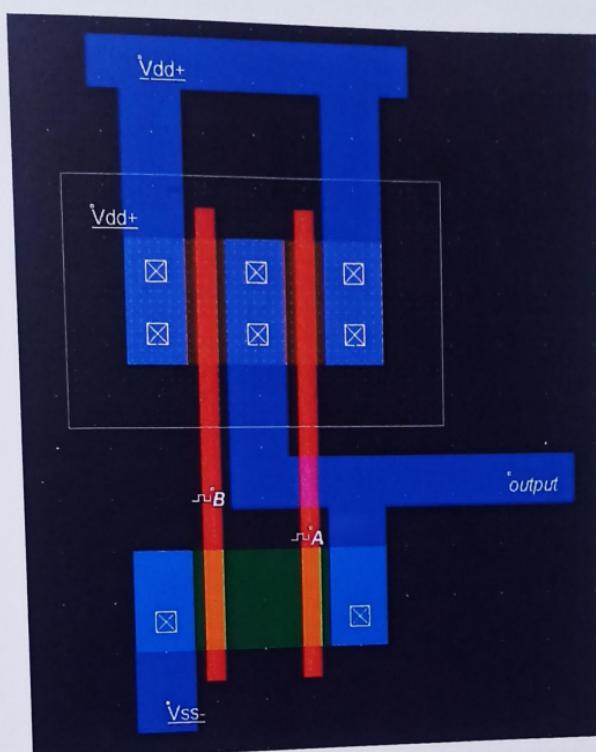
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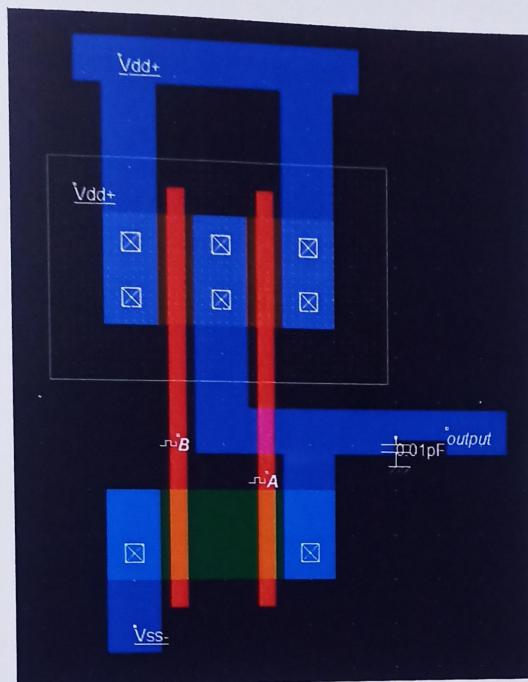
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Part A: Design Layout & Timing Diagram of CMOS NAND Gate without capacitor



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Part B: Design Layout & Timing Diagram of CMOS NAND Gate with capacitor



NAME OF THE STUDENT:

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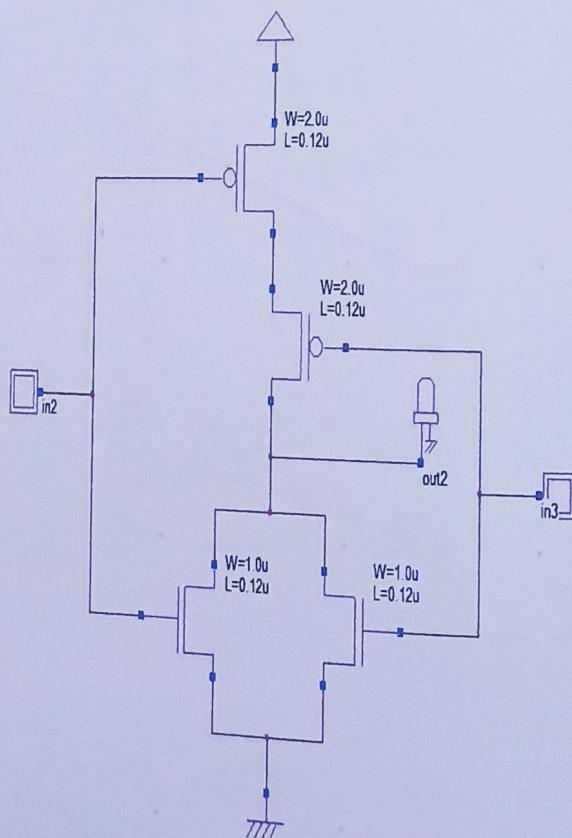
C] CMOS NOR Gate:

Theory :- A 2 input NOR gate can be constructed using NMOS & PMOS .

Truth Table:-

Input		Outputs
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

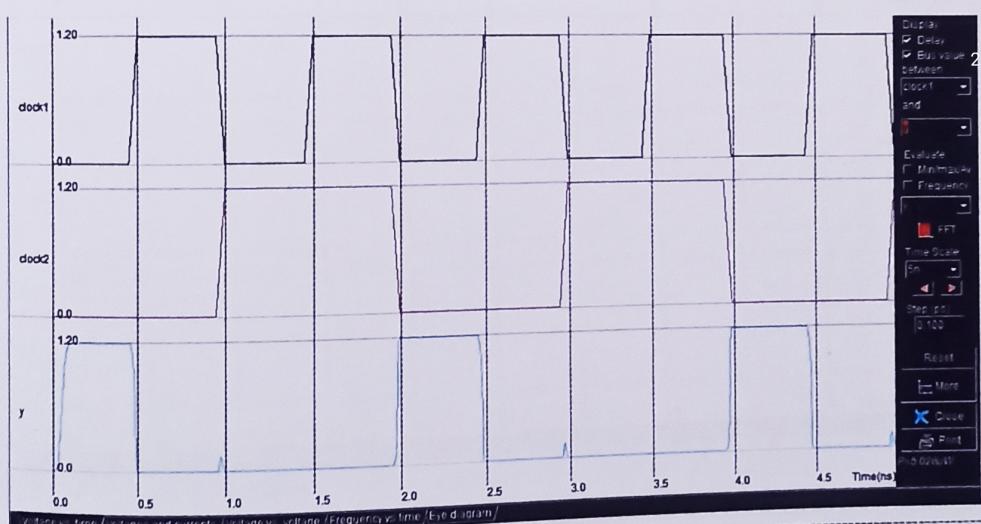
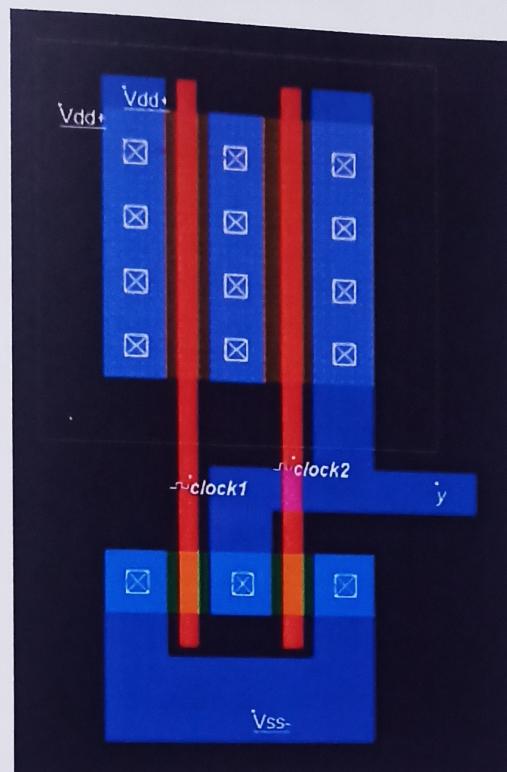
Schematic of CMOS NOR Gate:



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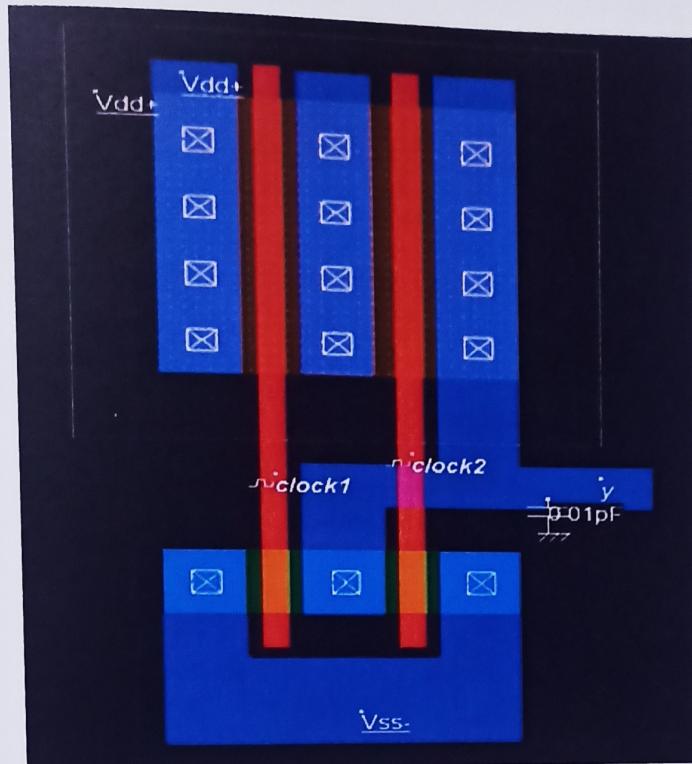
Part A: Design Layout & Timing Diagram of CMOS NOR Gate without capacitor



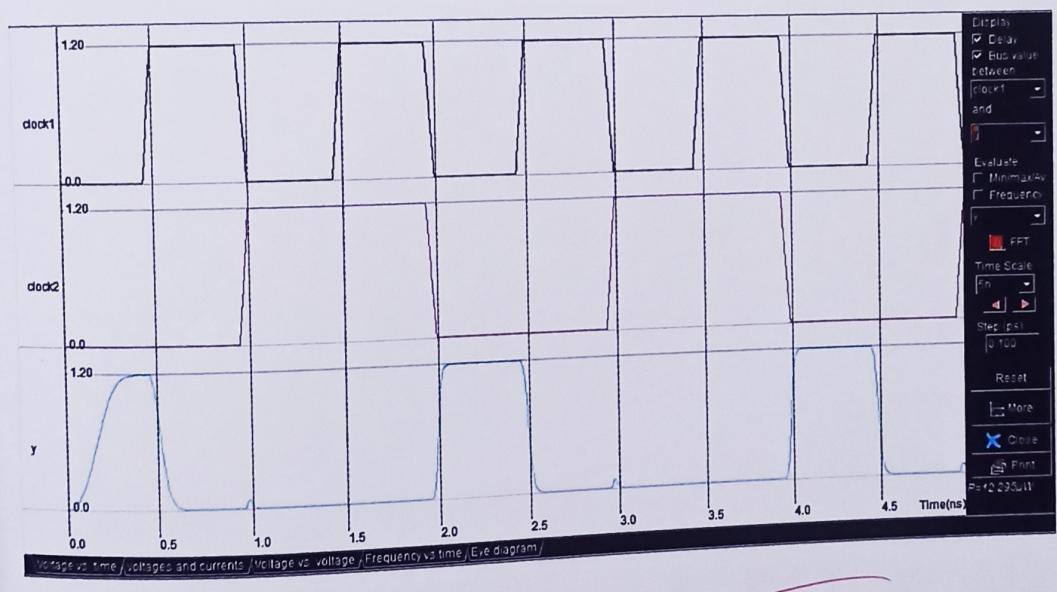
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Part B: Design Layout & Timing Diagram of CMOS NOR Gate with capacitor



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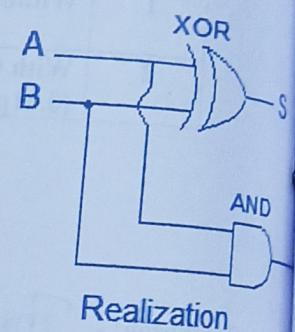
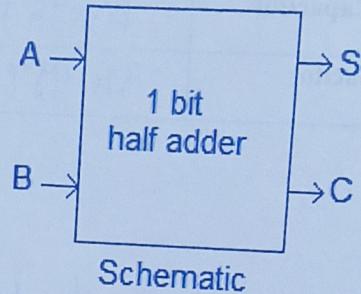


D) CMOS HALF ADDER:

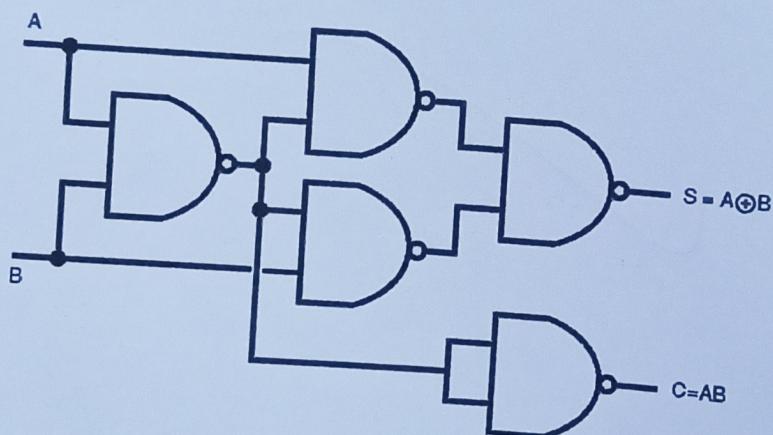
Theory: Half Adder is formed with the help of five CMOS NAND Gates.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

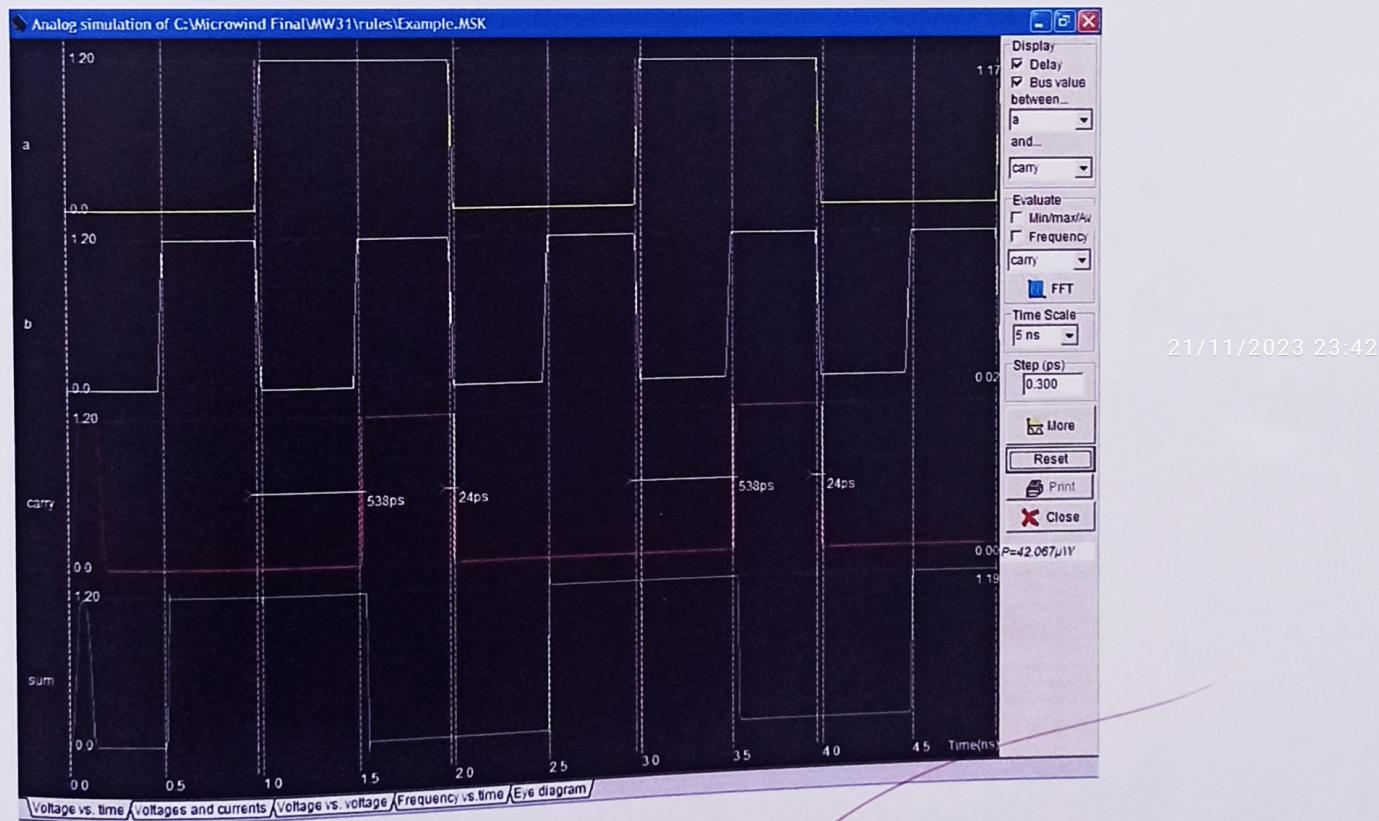
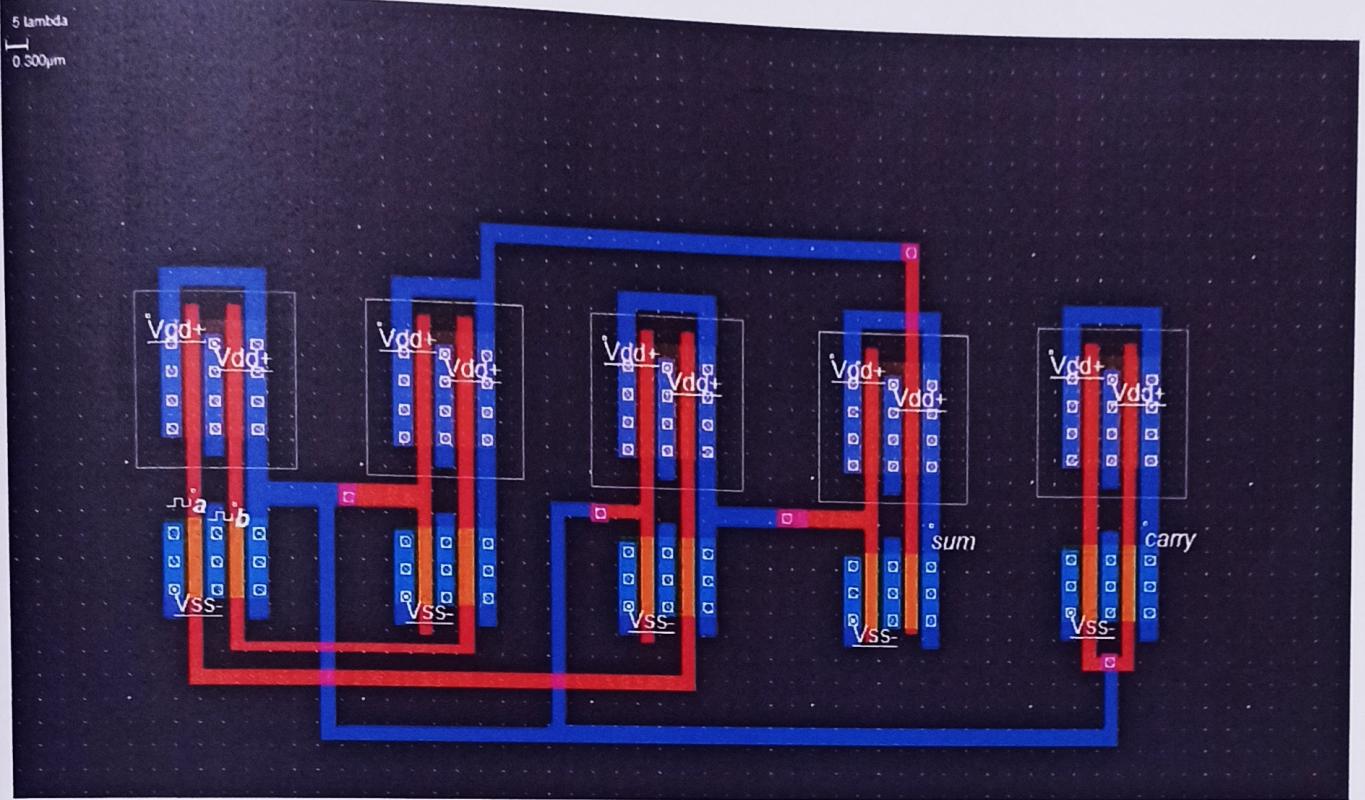
Truth table



Schematic :



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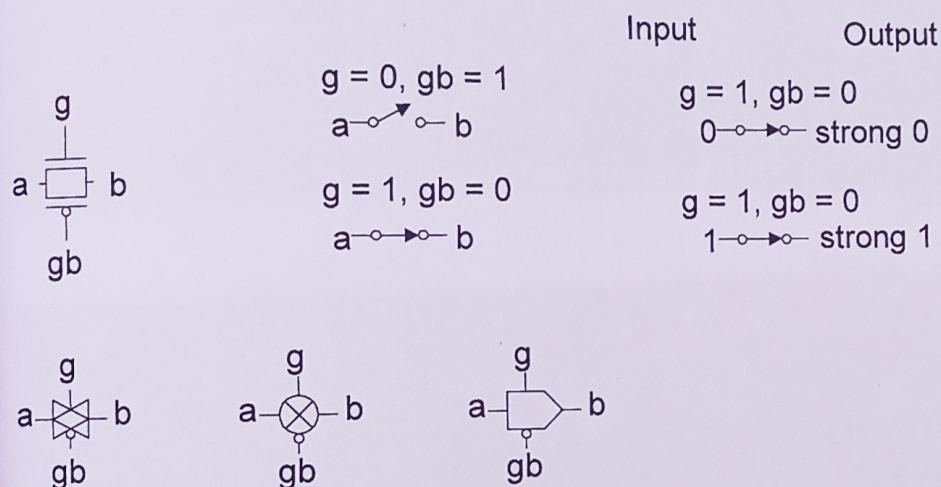
Subject: - VLSI Design and Technology

Aim: - To design and implement CMOS 2:1 multiplexer using Transmission gate & also comment on no. of pass transistors required to implement the same.

Theory: -

Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

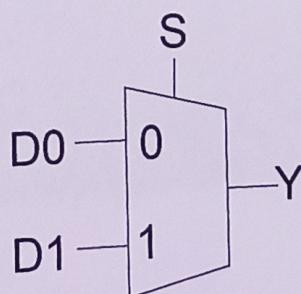


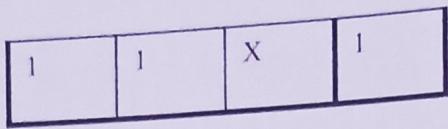
Multiplexers Using Transmission Gate

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- 2:1 multiplexer chooses between two inputs

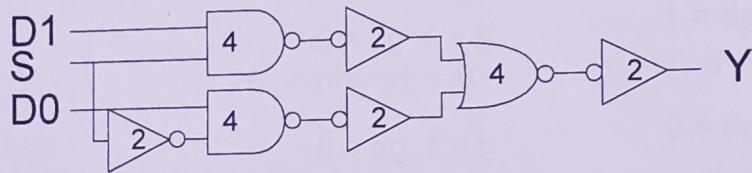
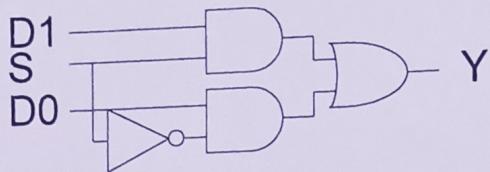
S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0



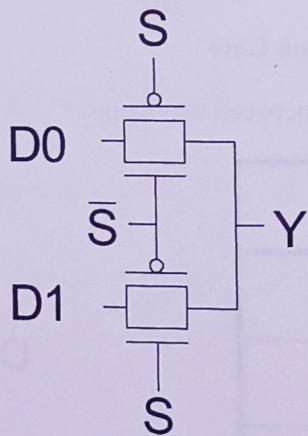


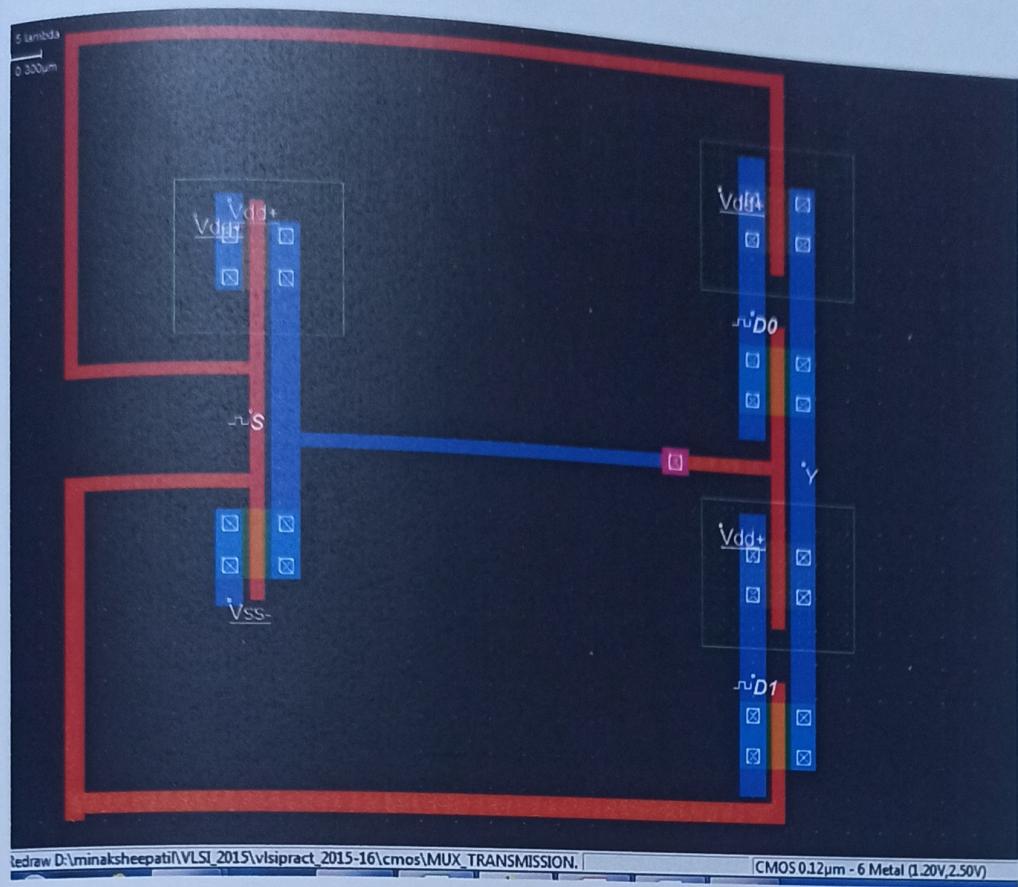
Gate-Level Mux Design:

$$Y = SD_1 + \overline{S}D_0 \text{ (too many transistors)}$$



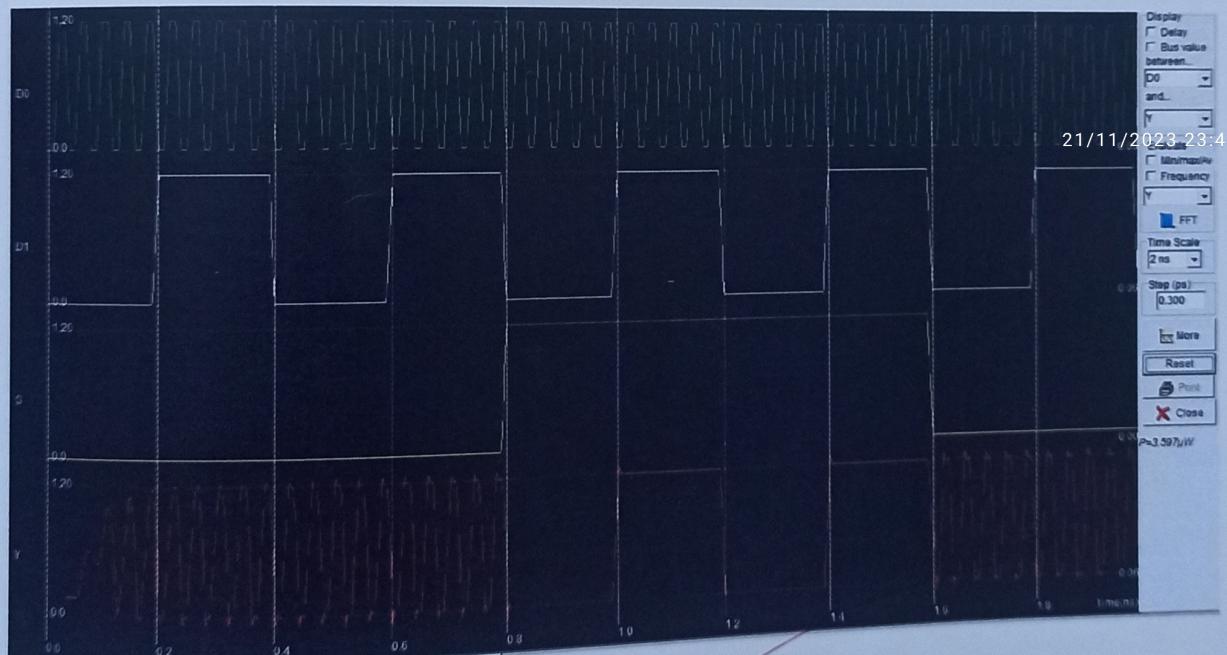
Transmission Gate Mux:





tedraw D:\minaksheepati\VLSI_2015\visipract_2015-16\cmos\MUX_TRANSMISSION.

CMOS 0.12μm - 6 Metal (1.20V,2.50V)



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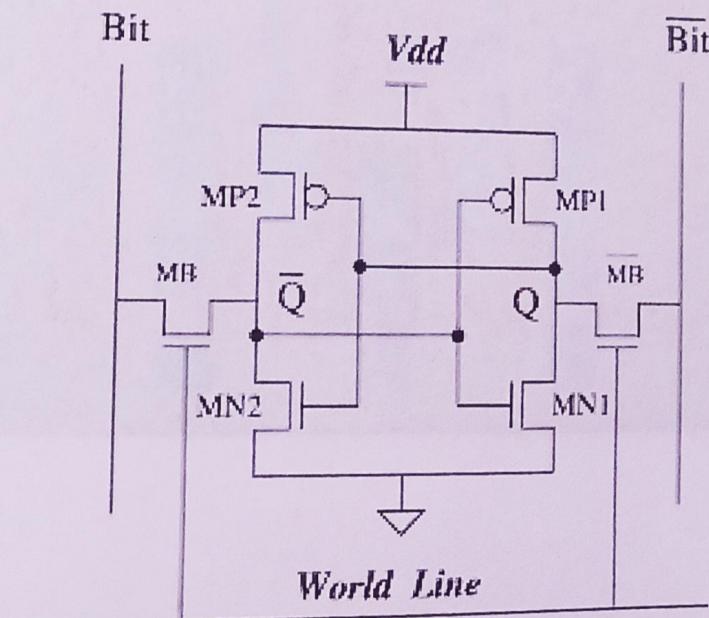
Subject: - VLSI Design and Technology

Aim: Design of CMOS single bit SRAM cell layout and verify the functionality by simulation

Procedure:

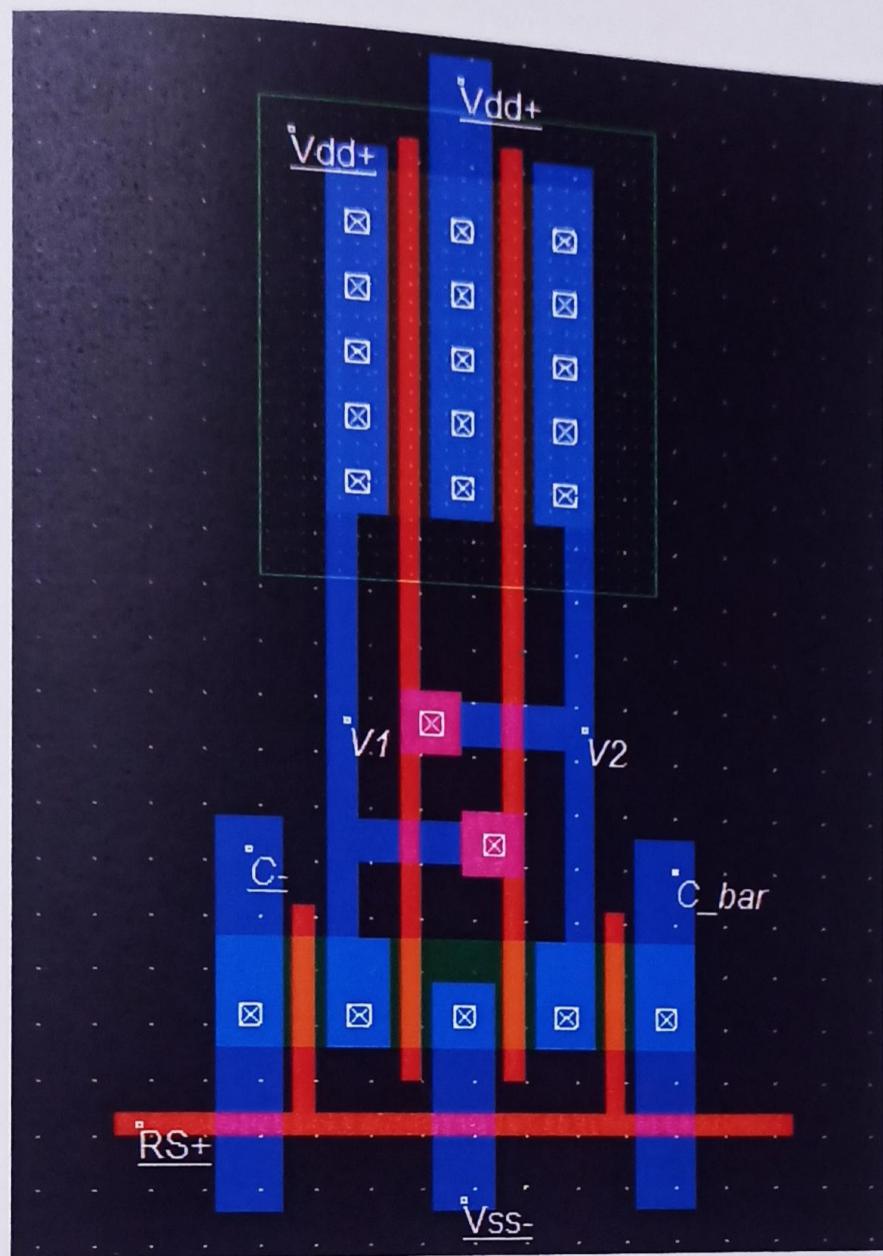
Prepare the CMOS layout of single bit SRAM cell. Do the functional simulation and verify the results.
Comment on the effect of no load and capacitive load on rise time and fall time.

Circuit Diagram:



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Layout Diagram:



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