154B Discussion 7

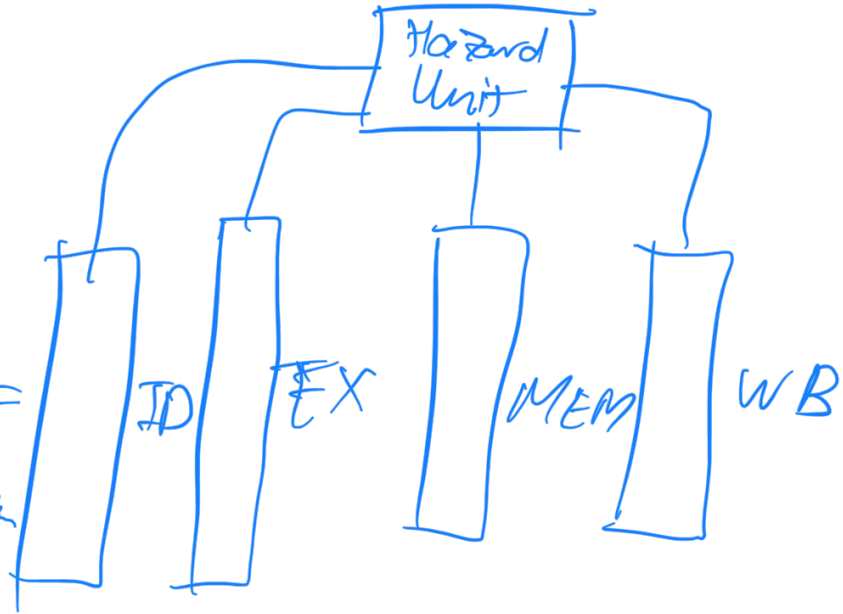
February 22nd, 2023

Outline

- Assignment 4
  - Multi-cycle memory components
  - Caching
- Cache Examples.
- Week 7 Quiz.

Assignment 4

* IF → output by Inst Mem
  ID → IF/ID stage reg
  EX → ID/EX stage reg
  MEM → EX/MEM stage reg
  WB → MEM/WB stage reg



imem_good : instruction in IF is correct
dmem_good
exmem_meminst : inst at mem stage is a memory inst

Assignment 4

Assignment 3: → branch misprediction (cond 1)

→ load-to-use hazard (cond 2)

Assignment 4 → !d_mem_good (cond 3) → data mem doesn't have correct data

→ !i_mem_good (cond 4) → i mem mem doesn't have correct instruction

* cond 1 & cond 3 do not happen at the same time

Assignment 4

	IF	ID	EX	MEM	WB
cond 1		flush	flush	flush	- - -
2		stall	flush	- - -	- - -
3		stall	stall	stall	flush
4		flush	- - -	- - -	- - -

cond 1: branch mispred

cond 2: load use

cond 3: !dmem_good

cond 4: !imem_good

	IF	ID	EX	MEM	WB
imem_good=0 →		add	- - -	- - -	- - -
imem_good=0 →		add	- - -	- - -	- - -

~~Quiz 7~~ Assignment 4

cond 1: branch mispred

cond 2: load use

cond 3: !dmem - good

cond 4: !imem - good

→ cond 1 & 3 do not happen at the same time

→ cond 1 : cond 2 doesn't matter
cond 4 //

cond 1	c2	c3	c4	nextpc	ID	EX	MEM	WB
0	0	0	0	pc+4	-	-	-	-
0	0	1	0	pcstall	stall	stall	stall	flush
0	1	1	0	pc stall	stall	stall	stall	flush
...								
0	0	0	1	pcstall	flush			

Quiz 7

imem == 0 ?

c1	c2	c3	c4	nextpc	ID	EX	MEM	WB
1	0	0	0 case2	pc+4	....	flush	flush	....
1	0	0	1 case1	PCfromtaken	flush	flush	~~jump~~ Stall	flush

	IF	ID	EX	MEM	WB
imem=0	garbage	...	...	jump	
case 1 → imem=0	pcfromtaken	flush	flush	jump	flush
case2 → imem=1	pc+4	...	flush	flush	jump