154B Discussion 10

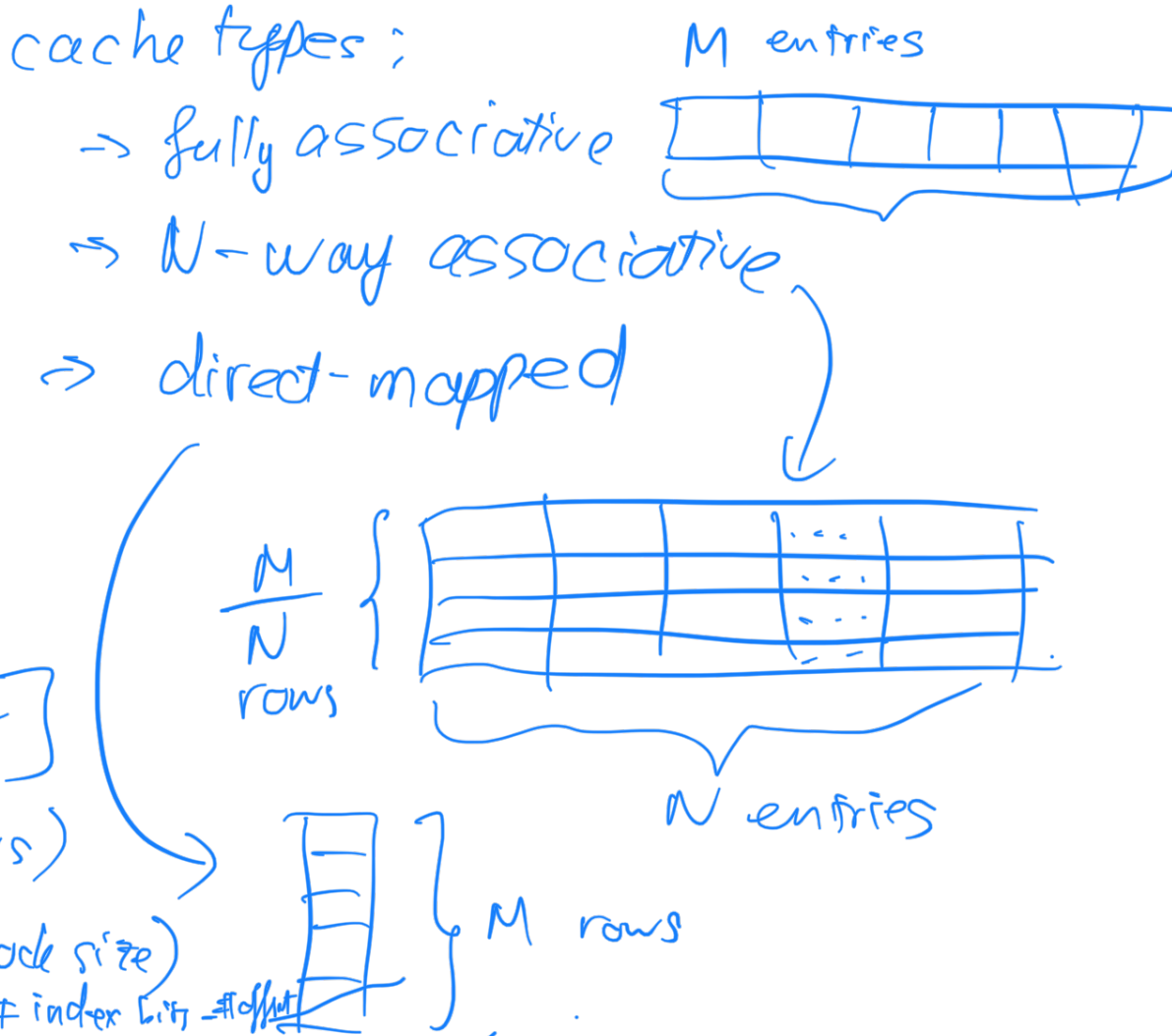
March 15th, 2023

Outline

- Review topics after the first midterm.
- Materials from last year's
  - https://github.com/jlpteaching/comparch/tree/main/_assets/wq22_154B_discussions

Topics

- Cache organizations
  - Cache types.
  - Cache parameters.
  - AMAT.
  - AMAT with TLBs.



Topics

- Virtual memory
  - Benefits. → process isolation,
  - Overheads. → translation cost
  - Physical Address / Virtual Address. → virtual address: [VPN0 | VPN1 | VPN2 | offset]
    physical address: [PFN | offset]
  - Address translation. translation(VPN0, VPN1, VPN2) → PFN
  - Paging, page tables, page walking.
  - TLB.
  - TLB organizations (similar to cache).
  - TLB miss penalty.

2GiB mem / 4KiB page size → 2^{31} / 2^{12} different pages

→ 2^{19} translation

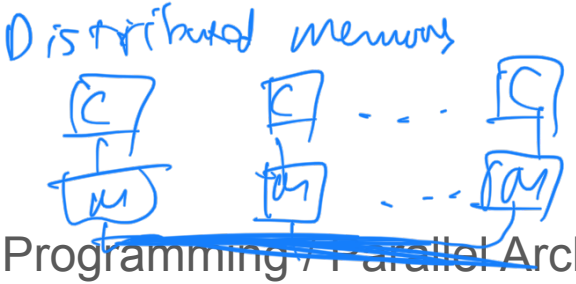
VPN

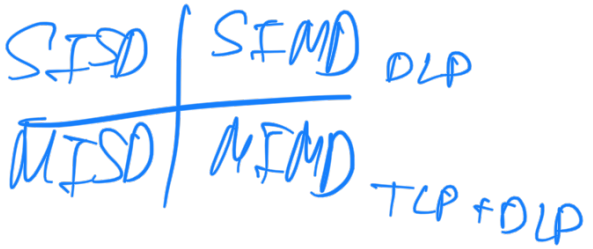
TLB

SATP/CR3 → address of level 1 page table

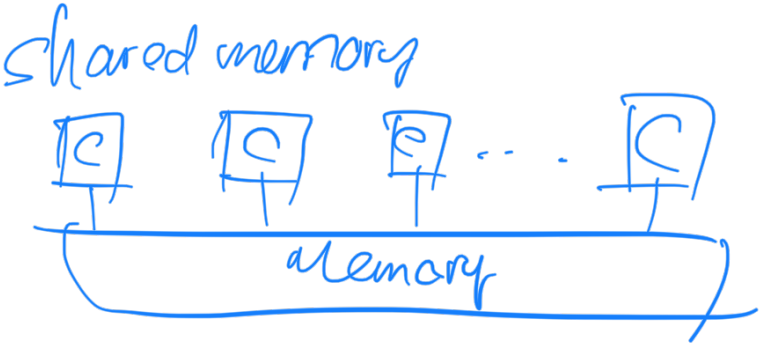
5 extra N mem accesses where N is the # of levels of page tables

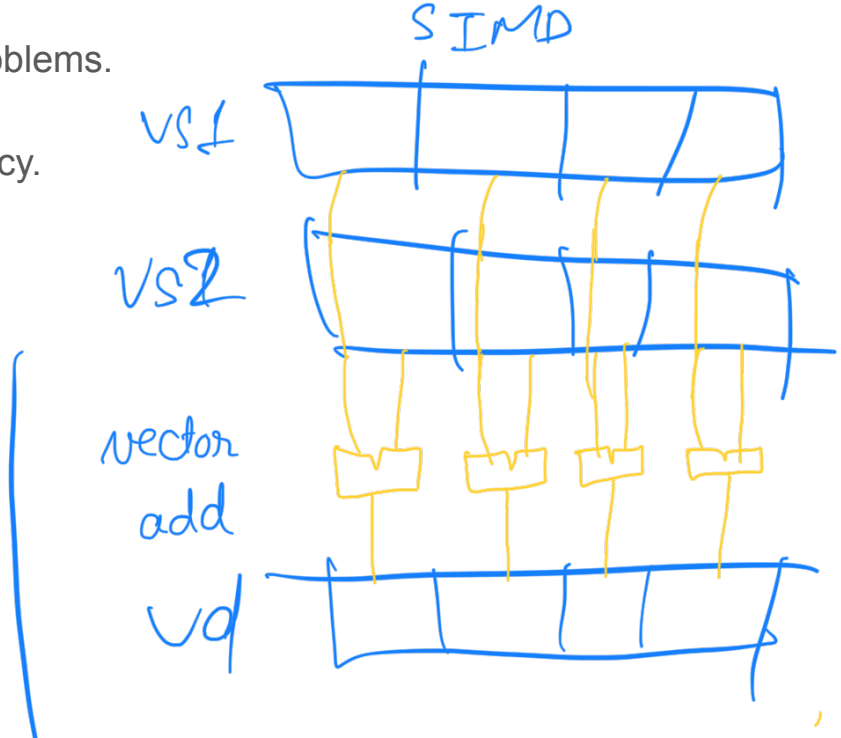
Topics





- Parallel Programming / Parallel Architectures.
  - Flynn's taxonomy.
  - Parallel processing and synchronization problems.
  - Cache coherence / False sharing.
  - Memory consistency / Sequential consistency.
  - Accelerators: GPUs, etc.
  - Shared memory / Distributed memory.
  - Levels of Parallelism: ILP, DLP, TLP.
  - Understanding Amdahl's Law.





Topics

- Security.

Topics

- This is not exhaustive list of topics covered in the lectures.

Quiz Review

Week 10 q8

program: 95% kernel + 5% serial

48-core GPU: speedup kernel 40x

96-core : 50x

speedup: $\frac{t_{48\text{-core}}}{t_{96\text{-core}}}$

Amdahl's law: p: portion that can be parallelized

N: # computing units

max speedup: $\frac{1}{(1-p) + \frac{p}{N}}$

(1-p): serial

assume that the speedup is Nx

Assume that program takes 1 second to run with 1 core

Kernel: 0.95s

serial: 0.05s

48-core

Kernel: $\frac{0.95s}{40}$

serial: 0.05s

96-core

kernel: $\frac{0.95s}{50}$

serial: 0.05s

Quiz Review

$$speedup = \frac{t_{old}}{t_{new}}$$

$$\rightarrow t_{new} = \frac{t_{old}}{speedup}$$

Quiz Review

Cache params

- # ways
- block size:

256 KiB cache used for blocks (not include metadata)

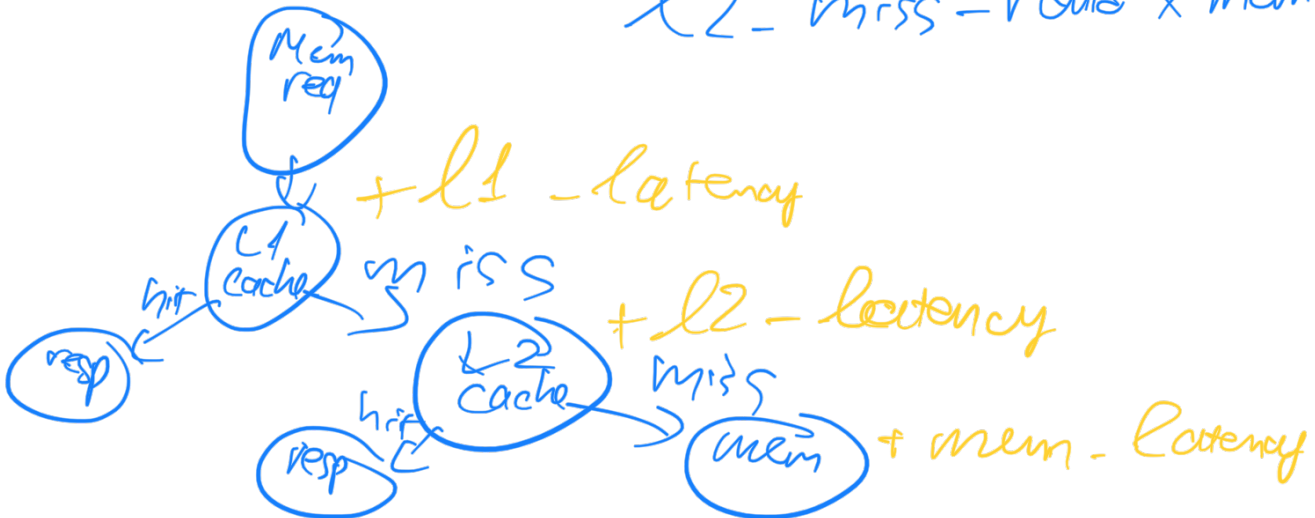
block size 64B

→ # entries = $\frac{256\ \text{KiB}}{64\text{B}}$

Quiz Review AMAT

AMAT 2-level cache

= l1_latency + l1_miss_ratio (l2_latency + l2_miss_rate x mem_latency)



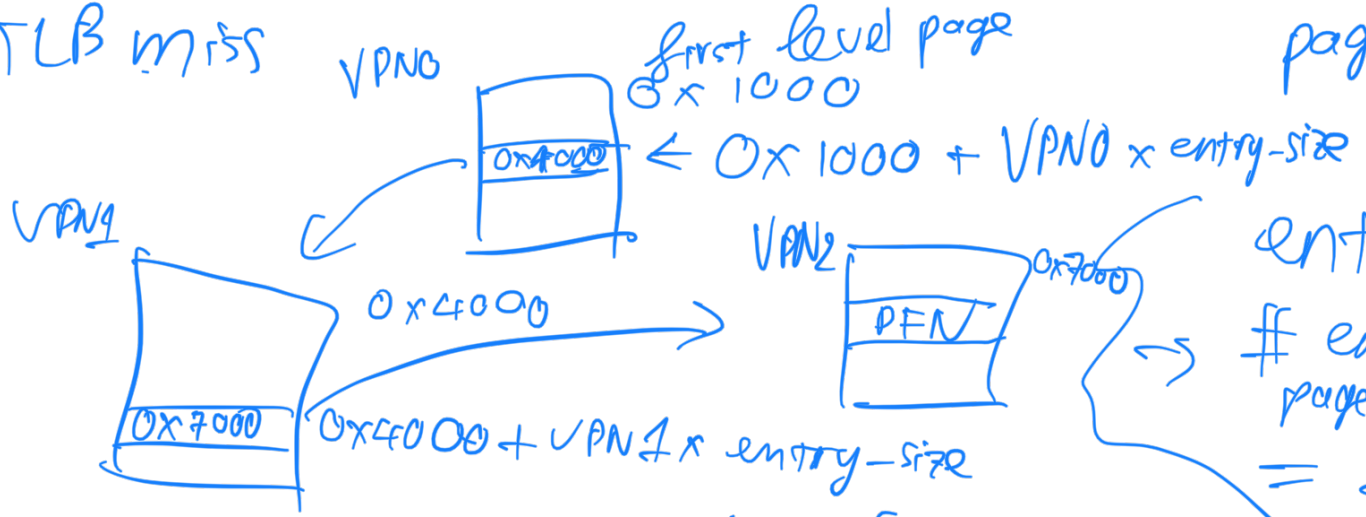
Quiz Review

Paging

virtual address [VPN0 | VPN1 | VPN2 | offset]

physical address [PFN | offset]

TLB miss



page_size : 4KiB, 2MiB, 1GiB

entry size = 4 bytes

entries per page table = $\frac{\text{page-size}}{\text{entry size}}$

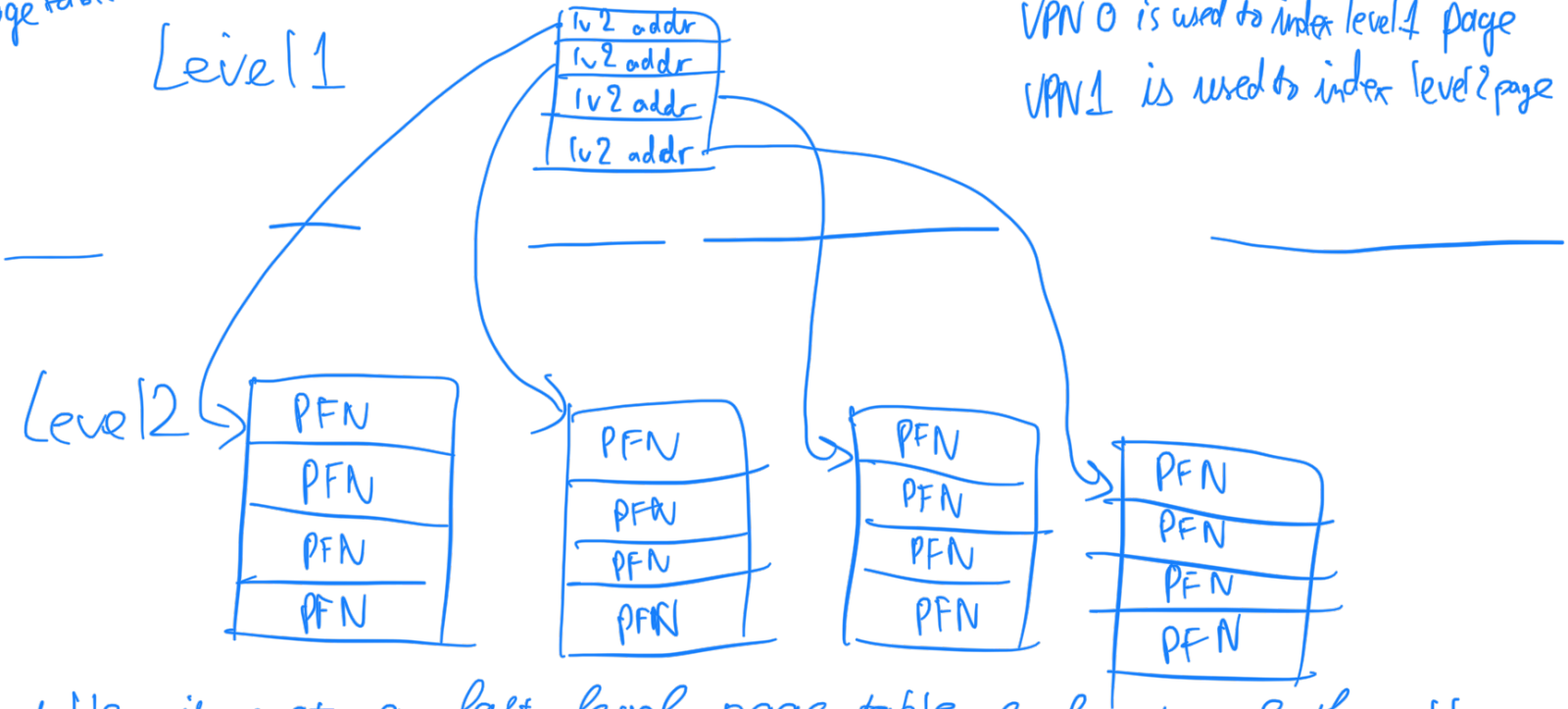
offset bits = $\log_2$ (page-size)

VPN-bits = $\log_2$ (# entries)

Quiz Review

Page Table Data Structure

Eg. 2-level page table.



If a page table is not a last level page table, each entry of the table has an address of the next level page. If a page table is a last level page, each entry contains a translation, i.e. PFN.