154B Discussion 7

February 25th, 2022

Goals

- Assignment 4.
- Examples of virtual-to-physical memory address translation.

Logistics

- Assignment 4 due date is now on Feb 28th.

Assignment 4: Question 1, 2, and 3

- You can use some multiple of seconds
  - E.g., seconds, milliseconds, microseconds, nanoseconds, picoseconds.

Assignment 4: Question 4 and 5

- qsort and rsort implementations:
  - qsort: https://github.com/jlpteaching/dinocpu-wq22/blob/main/src/test/resources/c/qsort/qsort_main.c#L67
  - rsort: https://github.com/jlpteaching/dinocpu-wq22/blob/main/src/test/resources/c/rsort/rsort.c#L32
  - Disassembled binaries are in *.dump files.

Assignment 4: Question 4 and 5

- Reasons for speedups/slowdowns
  - Instruction-level parallelism.
    - When two instructions can be issued simultaneously.
  - Number of branches/jumps/loads/stores.
    - From previous discussions: branch mispredictions and jumps waste CPU cycles.
    - Loads can stall the pipeline.
  - Branch misprediction rates.
  - From the algorithmic perspective,
    - quicksort vs radixsort: frequency of comparisons.
  - etc.
- You can pick one reason and explain that well for full credits.

Address formats

PPN → physical page number

VPN → virtual page number

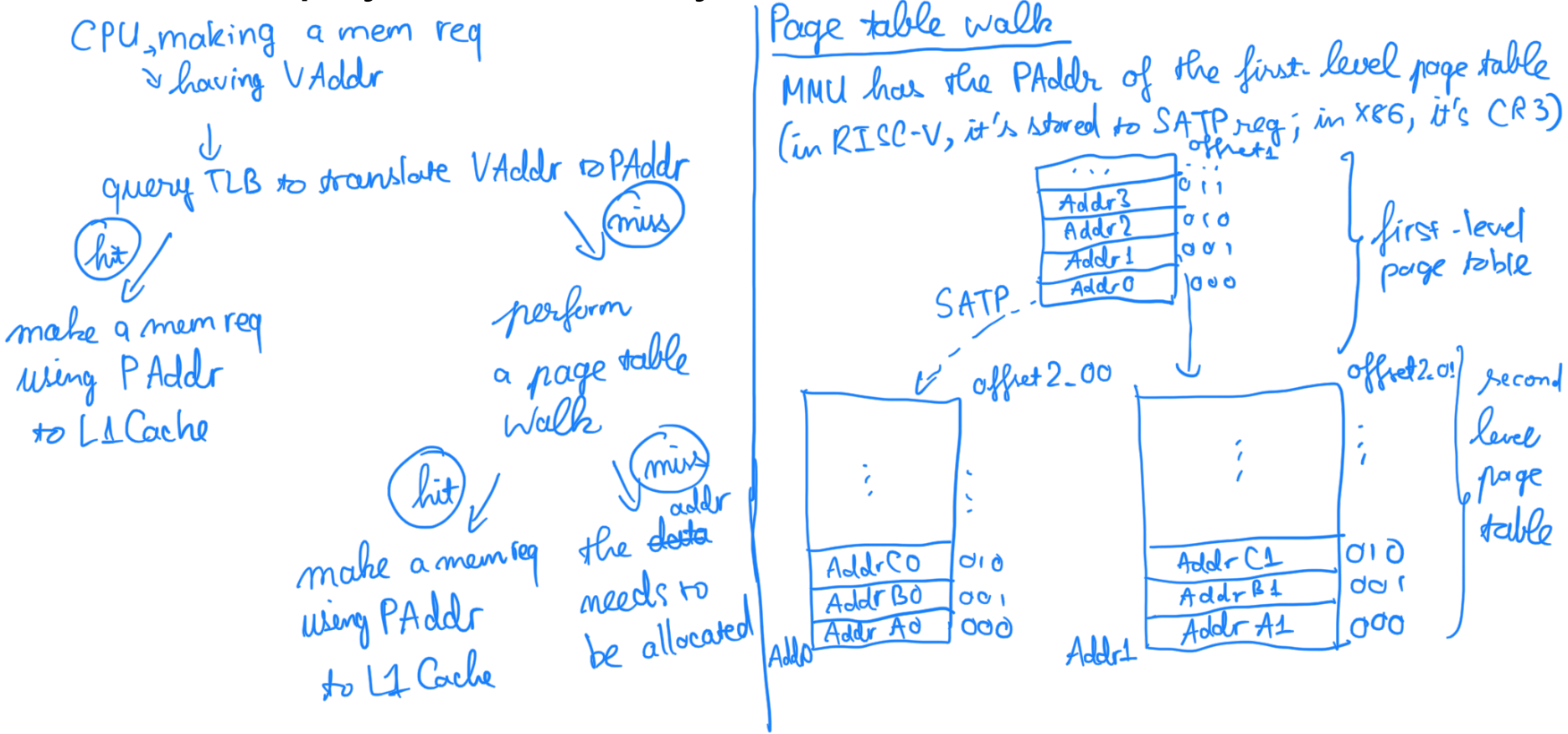
- Physical address
  - [PPN | offset]
- Virtual address
  - [VPN | offset]

- The *offset* parts of a virtual address and its physical address are the same (thus, have the same number of bits).
- So, the translation is essentially mapping a VPN to a PPN.
- Why the offset is preserved?
  - Preserving data locality!

Virtual-to-physical memory address translation

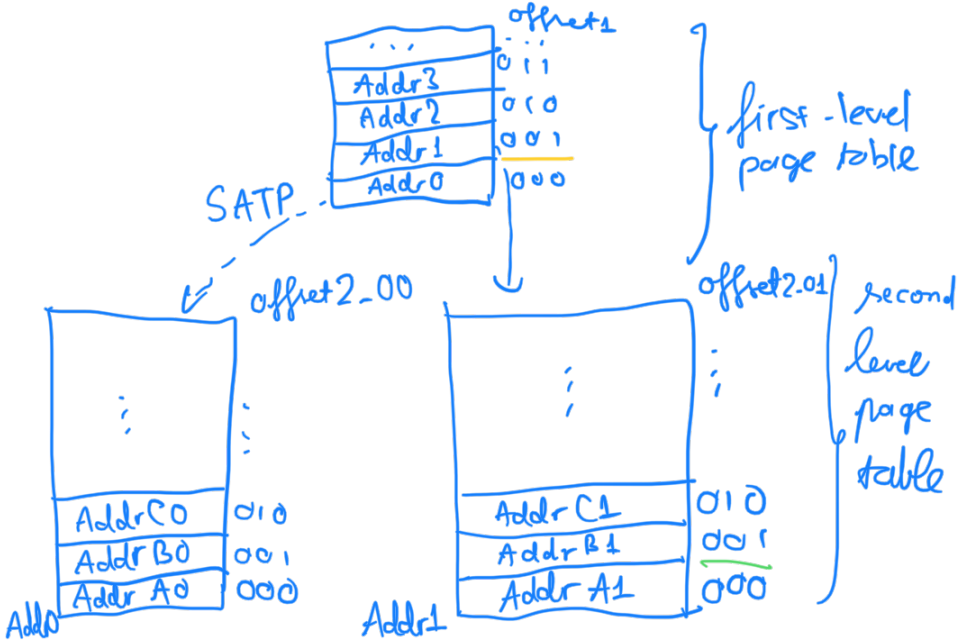
- Translation from a virtual address to the corresponding physical address.
- Translation is required for each memory request from CPU.
  - L1 Cache only works with physical addresses.
- TLB (translation lookaside buffer)
  - Caching the translation,
    - From a virtual address
    - To a physical address and associated metadata.

Virtual-to-physical memory address translation



Virtual Address : [VPN | offset] ← offset within a data block

VPN [offset_first_level | offset_second_level | ... | offset_k^th_level]



SATP: Paddr of 1st-level pagetable

data[SATP + offset_first_level] = Paddr of 2nd-level

data[data[SATP + offset_1st_level] + offset_2nd_level]

= Paddr of 3rd-level

→ how many bits for offset bits at each level?

$\#bits_{lvk} = \log_2(\#\text{entries at level k})$

→ recall from OS class: each process has its own vaddr space
→ TLB has to be flushed per switching process

VPN offset

VA 0: 0x03010004
VA 1: 0x
VA 2: 0x
VA 3: 0x

ld/st unit

PPN offset

PA 0: 0x02C72004
PA 1: 0x
PA 2: 0x
PA 3: 0x

Virtual address

16 bits for page offset

Virtual page number	Page offset

31 16 15 0

L2 Index	L1/PTE Index

31 24 23 16

<8 bits> <8 bits>

Page table entry

36 bits PAddr

PAddr [PPN (20 bits) | offset (=16 bits)] (= # bits for page offset from VAddr)

Physical page number	Valid	Present

21 2 1 0

MMU

SATP register: 0x7A2300000

TLB

VPN	PPN	V
0x0002	0x8588A	1
0x0301	0x02C72	1
0xABCD	0x741AC	1

8 bits for offset-2nd-level

2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages

8 bits for offset-1st-level

Physical address

Cache tag	Set index	Block offset

35 4 3 3 2 0

Cache

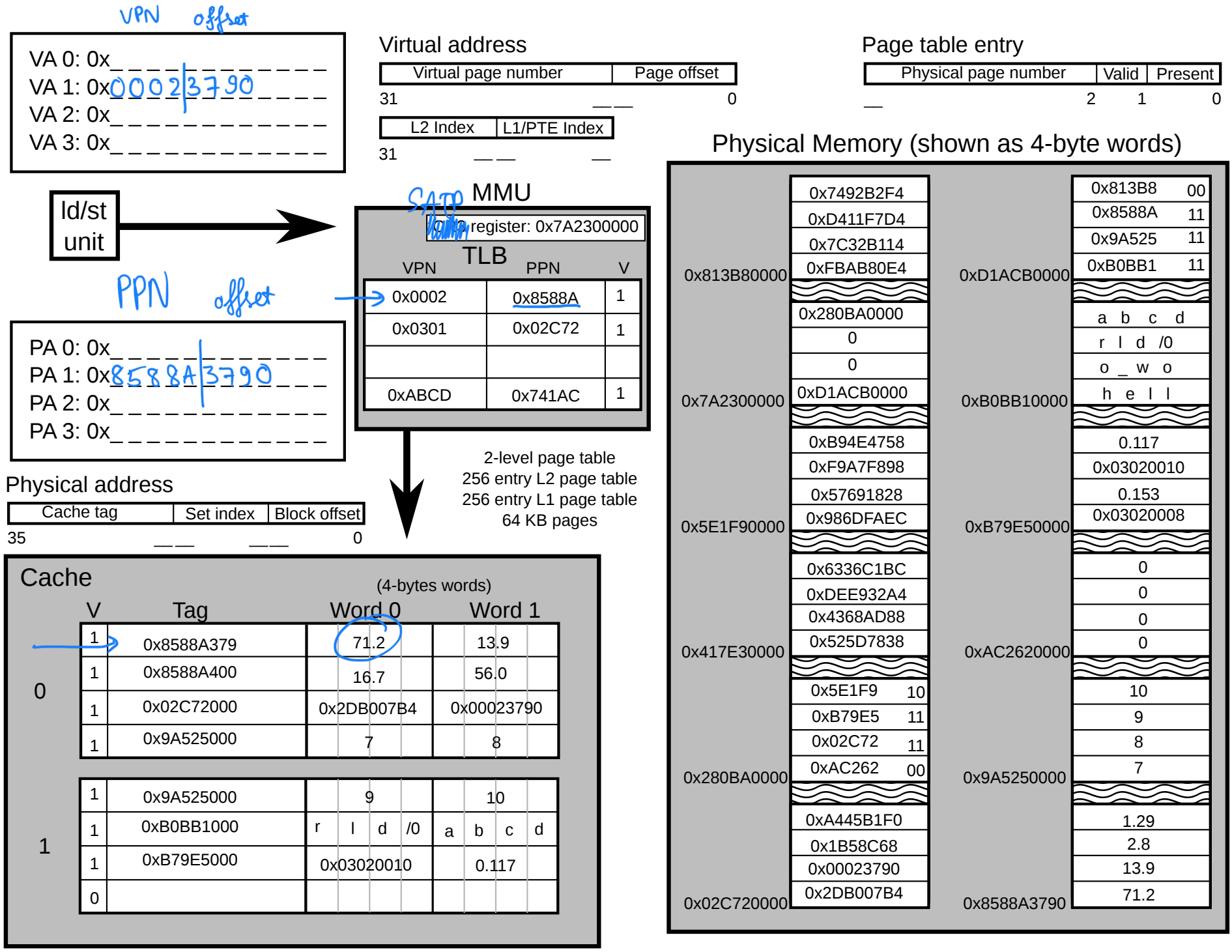
(4-bytes words)

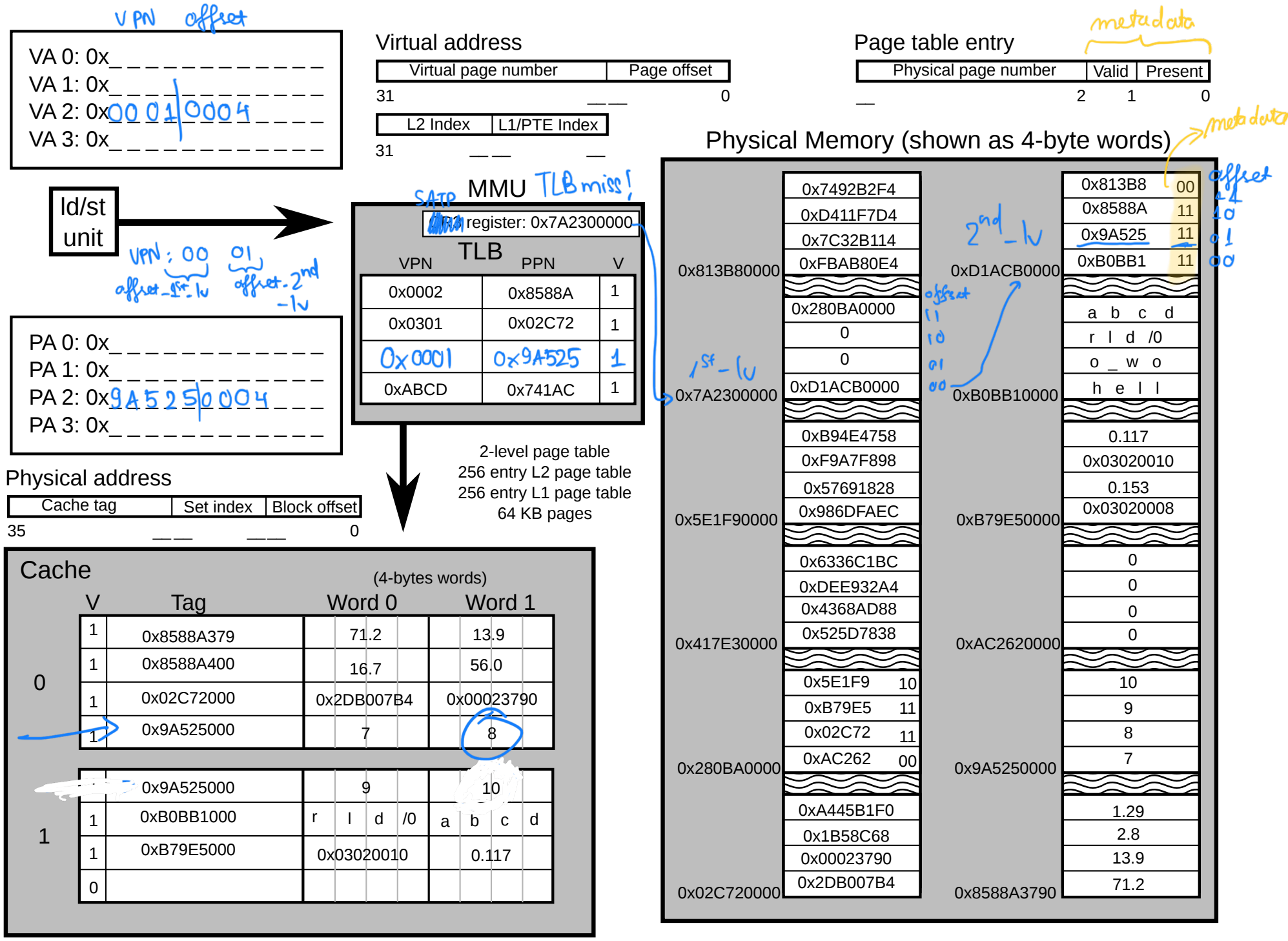
	V	Tag	Word 0	Word 1
0	1	0x8588A379	71.2	13.9
	1	0x8588A400	16.7	56.0
	1	0x02C72000	0x2DB007B4	0x00023790
	1	0x9A525000	7	8
1	1	0x9A525000	9	10
	1	0xB0BB1000	r l d /0	a b c d
	1	0xB79E5000	0x03020010	0.117
	0			

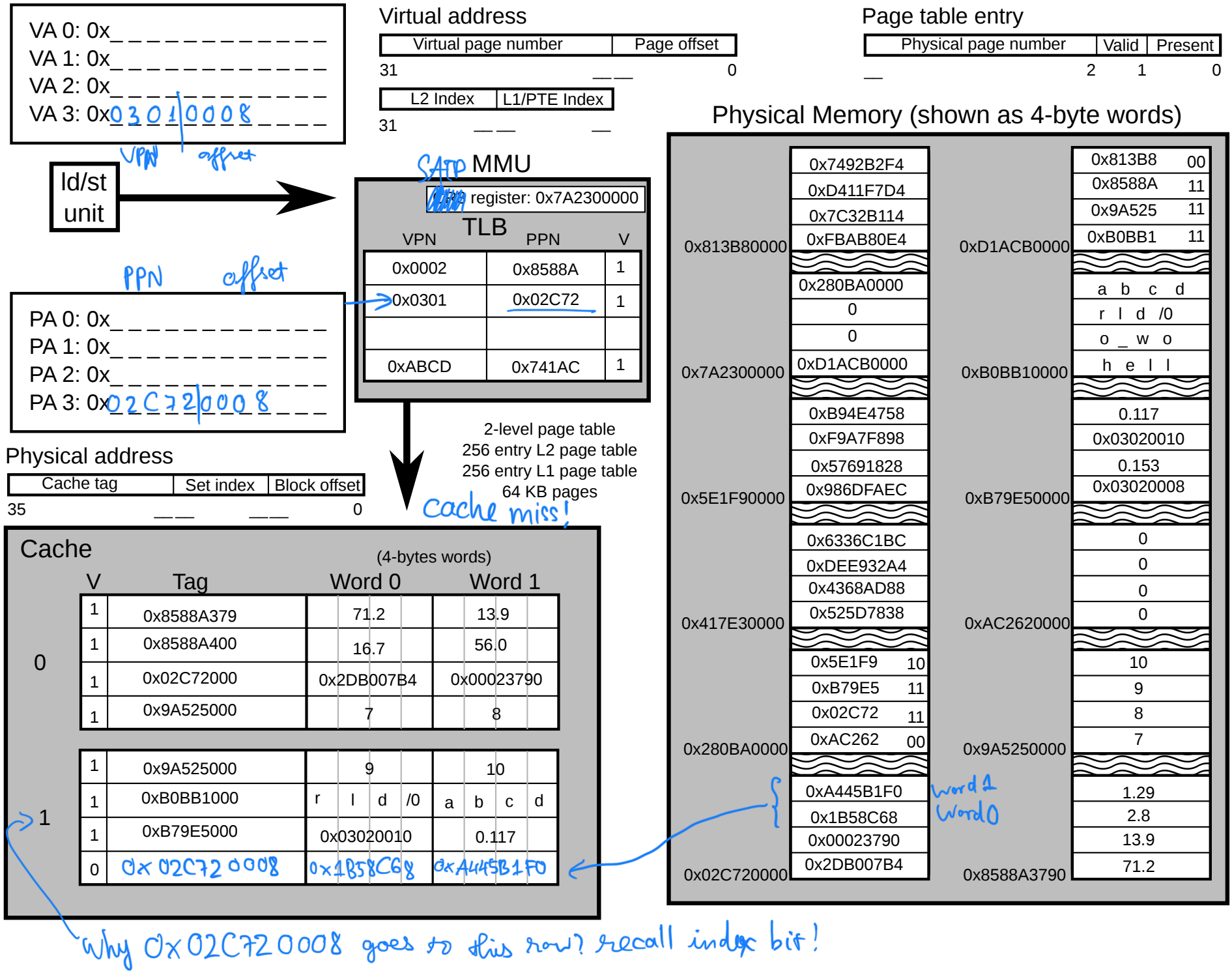
Physical Memory (shown as 4-byte words)

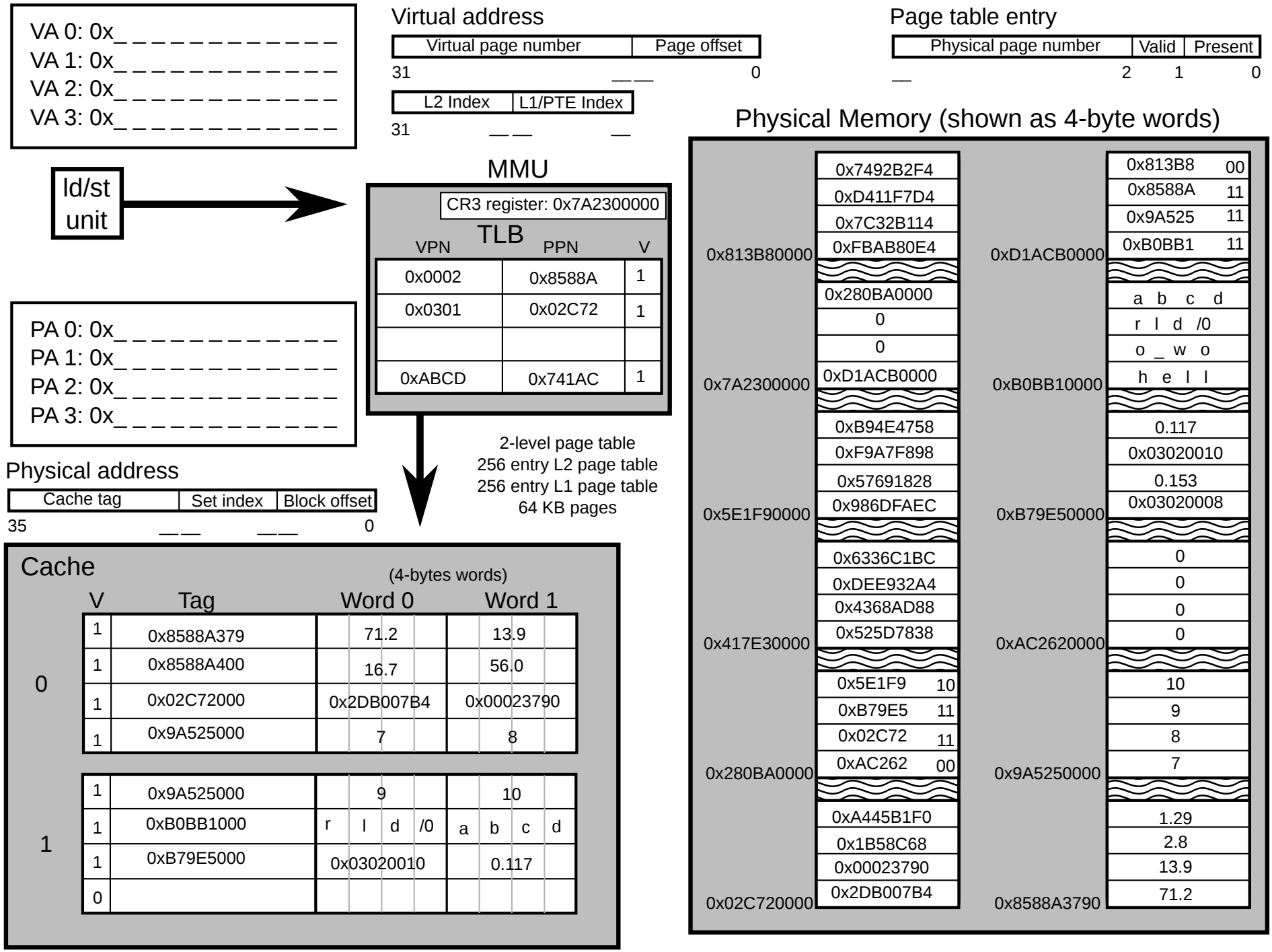
0x813B80000	0x7492B2F4	0xD1ACB0000	0x813B8 00
	0xD411F7D4		0x8588A 11
	0x7C32B114		0x9A525 11
	0xFBAB80E4		0xB0BB1 11
	0x280BA0000		a b c d
	0		r l d /0
	0		o _ w o
0x7A2300000	0xD1ACB0000	0xB0BB10000	h e l l
	0xB94E4758		0.117
	0xF9A7F898		0x03020010
	0x57691828		0.153
0x5E1F90000	0x986DFAEC	0xB79E50000	0x03020008
	0x6336C1BC		0
	0xDEE932A4		0
	0x4368AD88		0
0x417E30000	0x525D7838	0xAC2620000	0
	0x5E1F9 10		10
	0xB79E5 11		9
	0x02C72 11		8
0x280BA0000	0xAC262 00	0x9A5250000	7
	0xA445B1F0		1.29
	0x1B58C68		2.8
	0x00023790		13.9
0x02C720000	0x2DB007B4	0x8588A3790	71.2

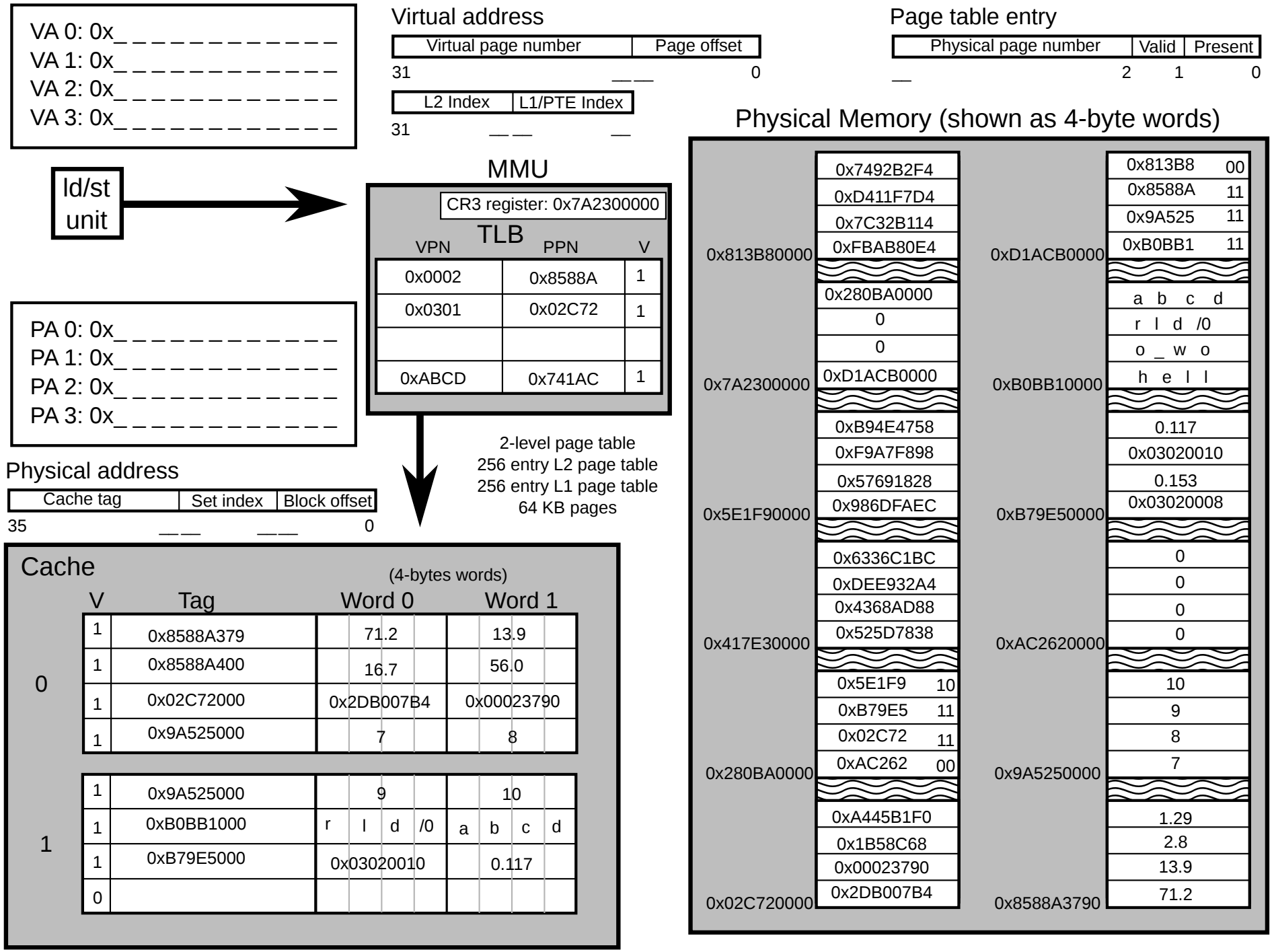
4-way associative, 1 bit for index bits, block-size = 8 B


VPN offset
VA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _
VA 1: 0x0002 3790
VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
31
Page table entry
Physical page number
Valid
Present
2
1
0
Physical Memory (shown as 4-byte words)
ld/st unit
MMU
SATP register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
0x741AC
1
PPN offset
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x8588A 3790
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical address
Cache tag
Set index
Block offset
35
0
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790


VPN offset
VA 0: 0x
VA 1: 0x
VA 2: 0x00010004
VA 3: 0x
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
31
Page table entry
metadata
Physical page number
Valid
Present
2
1
0
ld/st unit
MMU
TLB miss!
SATP register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0x0001
0x9A525
1
0xABCD
0x741AC
1
VPN: 00 01
offset-1st-lv
offset-2nd-lv
PA 0: 0x
PA 1: 0x
PA 2: 0x9A5250004
PA 3: 0x
Physical address
Cache tag
Set index
Block offset
35
0
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical Memory (shown as 4-byte words)
1st-lv
2nd-lv
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
0xB0BB10000
a b c d
r l d /0
o _ w o
h e l l
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
offset
11
10
01
00
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0


VA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _
VA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _
VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x03010008
VPN
offset
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x02C72008
PPN
offset
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
31
Page table entry
Physical page number
Valid
Present
2
1
0
MMU
SATP register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
0x741AC
1
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical address
Cache tag
Set index
Block offset
35
0
Cache miss!
Physical Memory (shown as 4-byte words)
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
word 1
word 0
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0 0x02C72000 0x1B58C68 0xA445B1F0
Why 0x02C72000 goes to this row? recall index bit!


VA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
Set index
Block offset
35
0
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
31
Page table entry
Physical page number
Valid
Present
2
1
0
MMU
CR3 register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
0x741AC
1
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical Memory (shown as 4-byte words)
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0


VA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
Set index
Block offset
35
0
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
31
Page table entry
Physical page number
Valid
Present
2
1
0
MMU
CR3 register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
0x741AC
1
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical Memory (shown as 4-byte words)
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0