154B Discussion 7

February 25th, 2022

Goals

- Assignment 4.
- Examples of virtual-to-physical memory address translation.

Logistics

- Assignment 4 due date is now on Feb 28th.

Assignment 4: Question 1, 2, and 3

- You can use some multiple of seconds
  - E.g., seconds, milliseconds, microseconds, nanoseconds, picoseconds.

Assignment 4: Question 4 and 5

- qsort and rsort implementations:
  - qsort: https://github.com/jlpteaching/dinocpu-wq22/blob/main/src/test/resources/c/qsort/qsort_main.c#L67
  - rsort: https://github.com/jlpteaching/dinocpu-wq22/blob/main/src/test/resources/c/rsort/rsort.c#L32
  - Disassembled binaries are in *.dump files.

Assignment 4: Question 4 and 5

- Reasons for speedups/slowdowns
  - Instruction-level parallelism.
    - When two instructions can be issued simultaneously.
  - Number of branches/jumps/loads/stores.
    - From previous discussions: branch mispredictions and jumps waste CPU cycles.
    - Loads can stall the pipeline.
  - Branch misprediction rates.
  - From the algorithmic perspective,
    - quicksort vs radixsort: frequency of comparisons.
  - etc.
- You can pick one reason and explain that well for full credits.

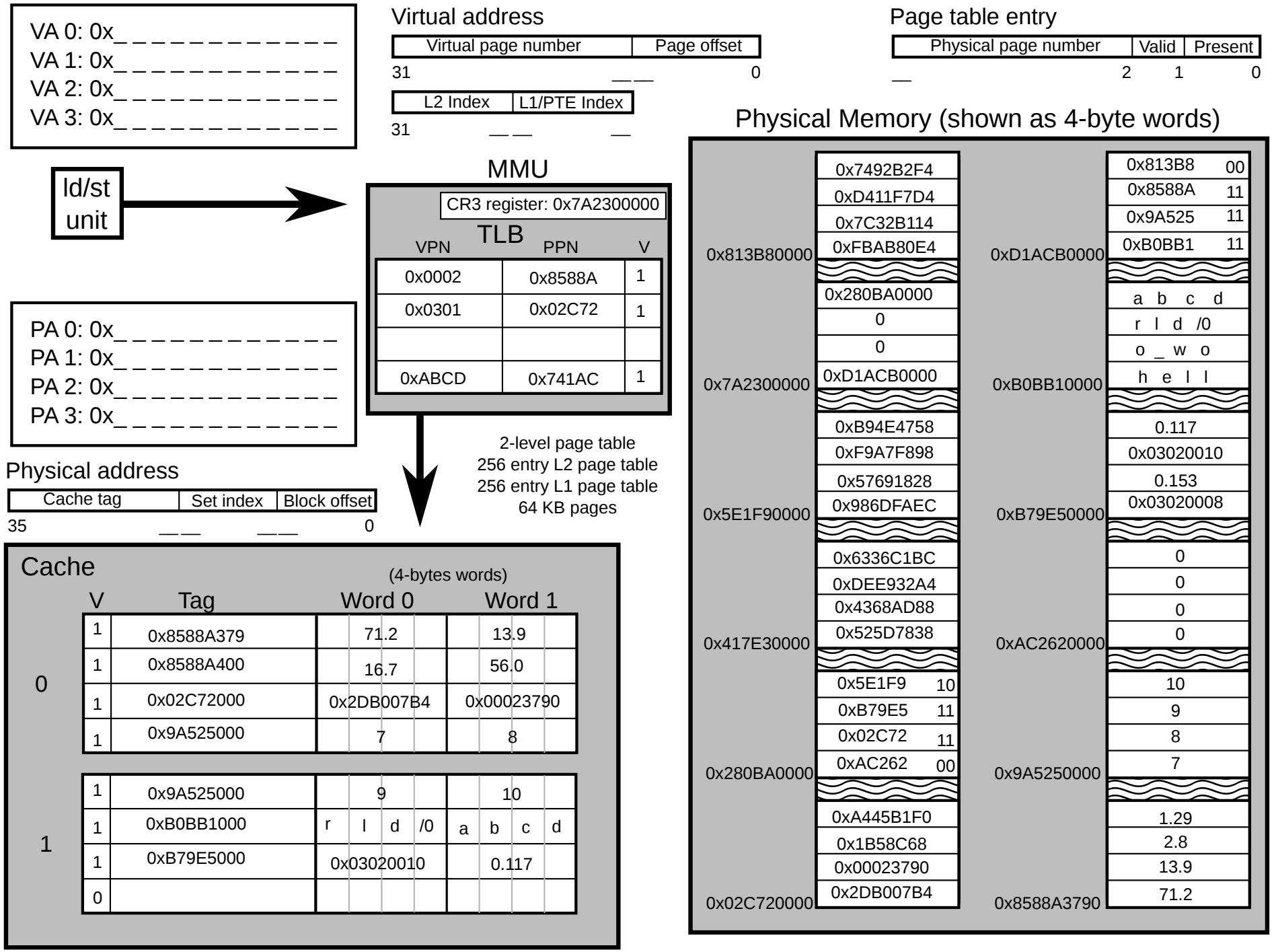
Address formats

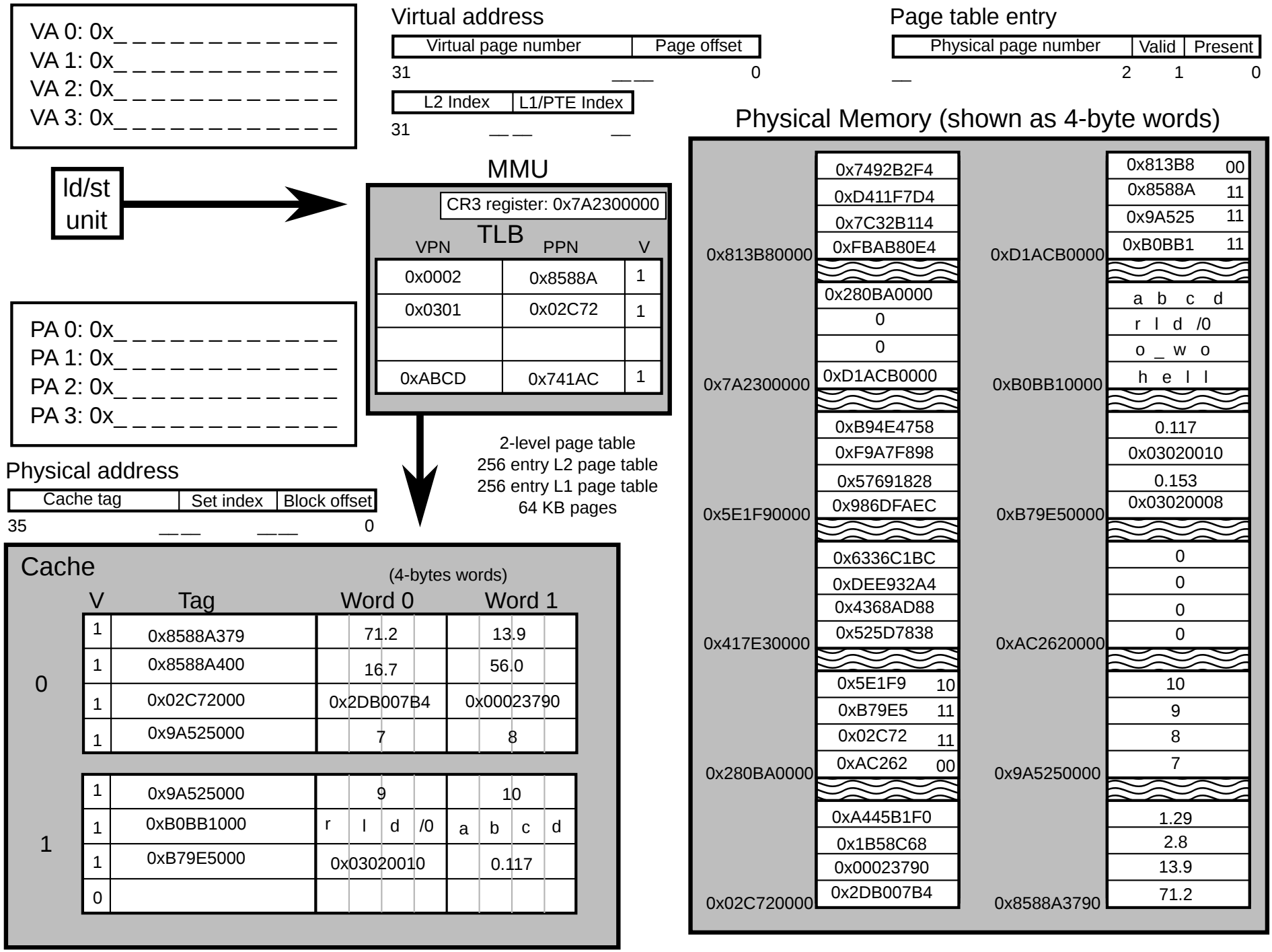
- Physical address
  - [PPN | offset]
- Virtual address
  - [VPN | offset]
- The *offset* parts of a virtual address and its physical address are the same (thus, have the same number of bits).
- So, the translation is essentially mapping a VPN to a PPN.
- Why the offset is preserved?
  - Preserving data locality!

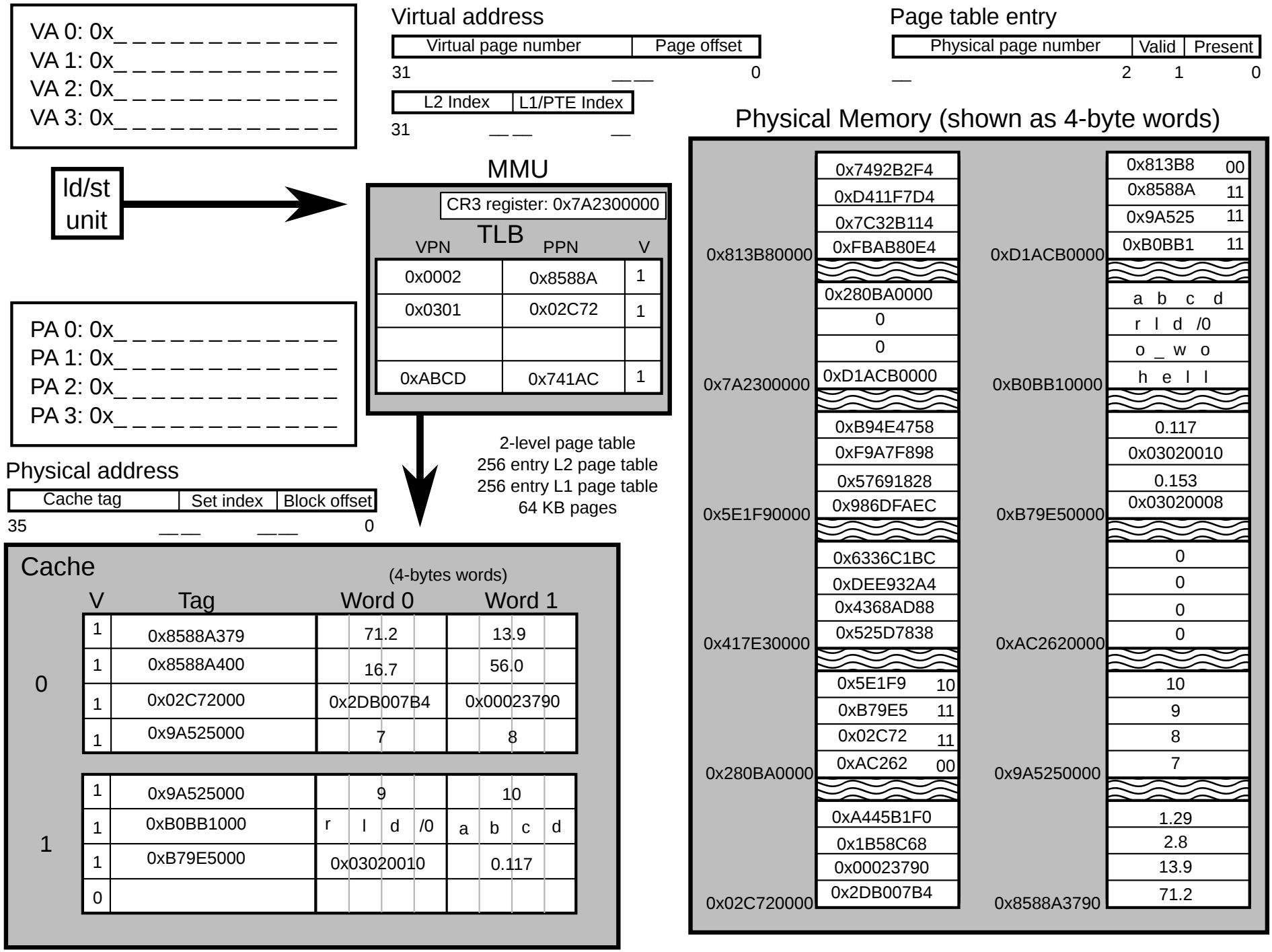
Virtual-to-physical memory address translation

- Translation from a virtual address to the corresponding physical address.
- Translation is required for each memory request from CPU.
  - L1 Cache only works with physical addresses.
- TLB (translation lookaside buffer)
  - Caching the translation,
    - From a virtual address
    - To a physical address and associated metadata.

Virtual-to-physical memory address translation


VA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
Set index
Block offset
35
0
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
31
Page table entry
Physical page number
Valid
Present
2
1
0
MMU
CR3 register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
0x741AC
1
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical Memory (shown as 4-byte words)
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0


VA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
Set index
Block offset
35
0
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
31
Page table entry
Physical page number
Valid
Present
2
1
0
MMU
CR3 register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
0x741AC
1
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical Memory (shown as 4-byte words)
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0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VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
Set index
Block offset
35
0
Virtual address
Virtual page number
Page offset
31
0
L2 Index
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Page table entry
Physical page number
Valid
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2
1
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MMU
CR3 register: 0x7A2300000
TLB
VPN
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0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
0x741AC
1
2-level page table
256 entry L2 page table
256 entry L1 page table
64 KB pages
Physical Memory (shown as 4-byte words)
0x813B80000
0x7492B2F4
0xD411F7D4
0x7C32B114
0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
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0x525D7838
0x417E30000
0x5E1F9 10
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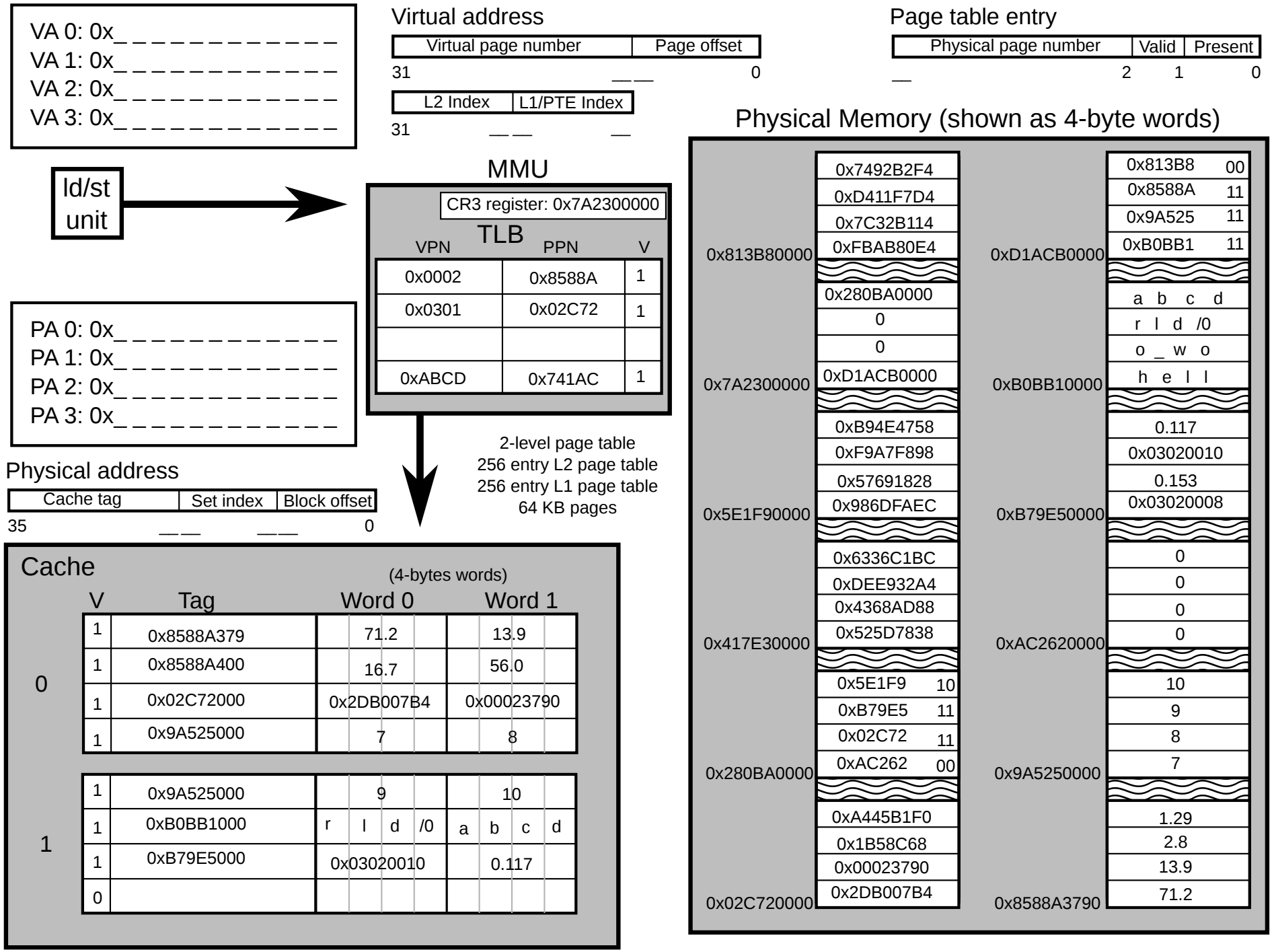
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0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VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
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Block offset
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Virtual address
Virtual page number
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0x9A525 11
0xB0BB1 11
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r l d /0
o _ w o
h e l l
0xB0BB10000
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0.153
0x03020008
0xB79E50000
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1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
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1 0x8588A379 71.2 13.9
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1 0x9A525000 9 10
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1 0xB79E5000 0x03020010 0.117
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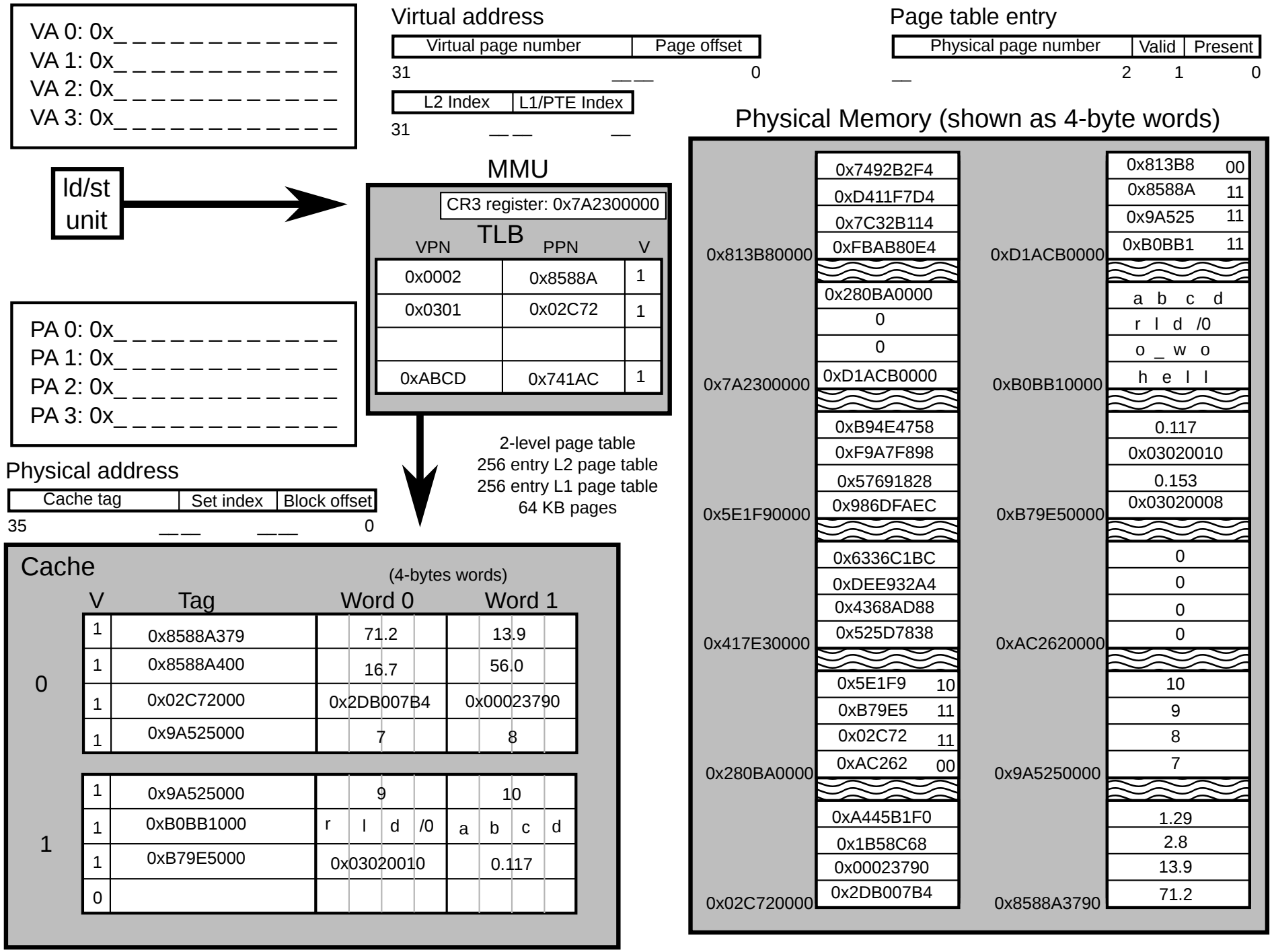
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VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
Set index
Block offset
35
0
Virtual address
Virtual page number
Page offset
31
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L2 Index
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Page table entry
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2-level page table
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0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
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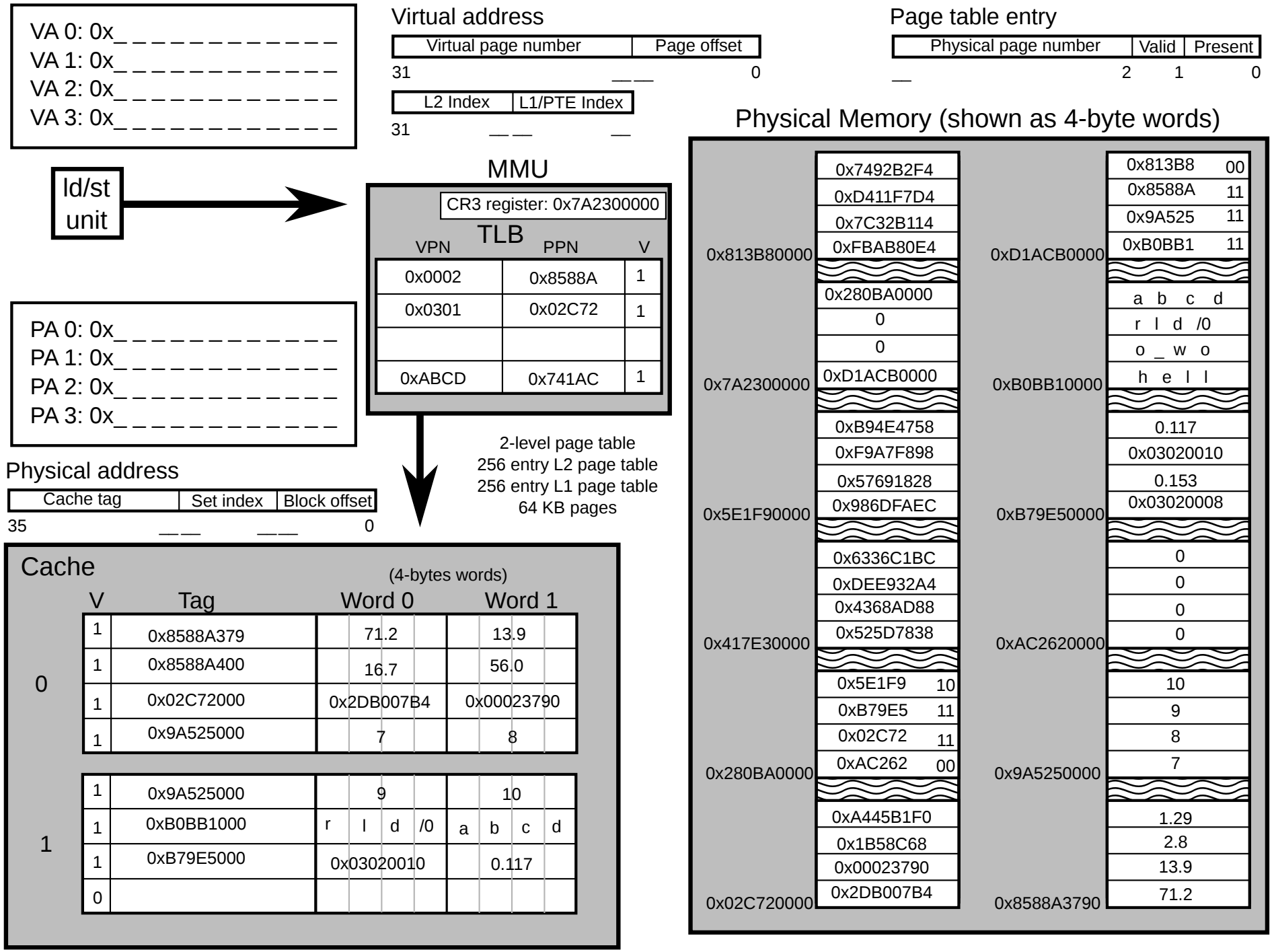
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0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VA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
VA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
ld/st unit
PA 0: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 1: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 2: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
PA 3: 0x_ _ _ _ _ _ _ _ _ _ _ _ _
Physical address
Cache tag
Set index
Block offset
35
0
Virtual address
Virtual page number
Page offset
31
0
L2 Index
L1/PTE Index
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Page table entry
Physical page number
Valid
Present
2
1
0
MMU
CR3 register: 0x7A2300000
TLB
VPN
PPN
V
0x0002
0x8588A
1
0x0301
0x02C72
1
0xABCD
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1
2-level page table
256 entry L2 page table
256 entry L1 page table
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Physical Memory (shown as 4-byte words)
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0x7492B2F4
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0xFBAB80E4
0x280BA0000
0
0
0xD1ACB0000
0x7A2300000
0xB94E4758
0xF9A7F898
0x57691828
0x986DFAEC
0x5E1F90000
0x6336C1BC
0xDEE932A4
0x4368AD88
0x525D7838
0x417E30000
0x5E1F9 10
0xB79E5 11
0x02C72 11
0xAC262 00
0x280BA0000
0xA445B1F0
0x1B58C68
0x00023790
0x2DB007B4
0x02C720000
0xD1ACB0000
0x813B8 00
0x8588A 11
0x9A525 11
0xB0BB1 11
a b c d
r l d /0
o _ w o
h e l l
0xB0BB10000
0.117
0x03020010
0.153
0x03020008
0xB79E50000
0
0
0
0
0xAC2620000
10
9
8
7
0x9A5250000
1.29
2.8
13.9
71.2
0x8588A3790
Cache
(4-bytes words)
V
Tag
Word 0
Word 1
0
1 0x8588A379 71.2 13.9
1 0x8588A400 16.7 56.0
1 0x02C72000 0x2DB007B4 0x00023790
1 0x9A525000 7 8
1
1 0x9A525000 9 10
1 0xB0BB1000 r l d /0 a b c d
1 0xB79E5000 0x03020010 0.117
0