Circuit Simulation Project

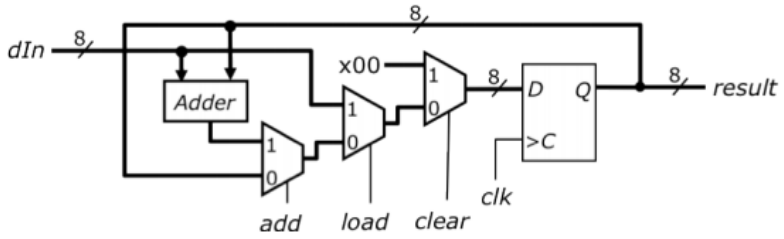
https://esim.fossee.in/circuit-simulation-project

Name of the participant: Shreyas Choudhary

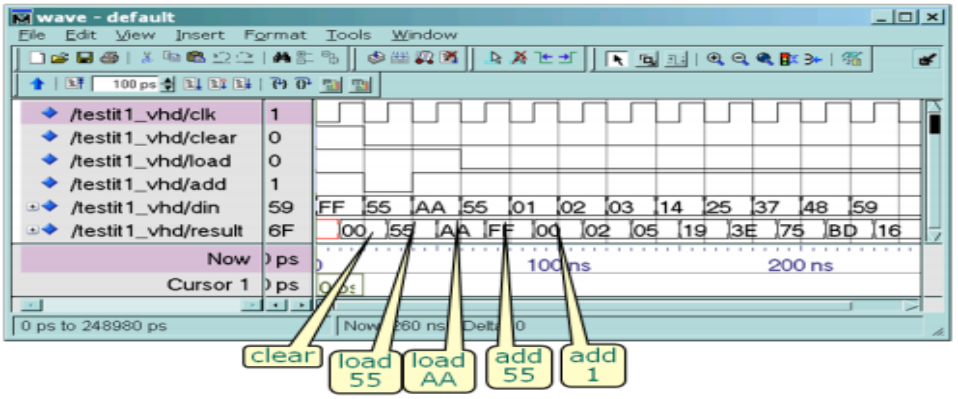
Title of the circuit: Calculator using VHDL

Theory/Description: The circuit has an 8 bit data input called dIn, an 8 bit data output called result and control inputs clear, load and add. It has an internal storage register that can store an 8 bit value. The result output is the value stored in this register. When the clear input is asserted, the stored value is cleared, when the load input is asserted the value of dIn is stored, and when the add input is asserted, the value of dIn is added to the stored value. The clk input controls when the circuit responds to control inputs.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :



Source/Reference(s):
https://www.tutorialspoint.com/vlsi_design/vlsi_design_vhdl_introduction.htm

Calculator VHDL code: https://github.com/Shreyas1308/FOSSEE_submission.git