

# Circuit Simulation Project

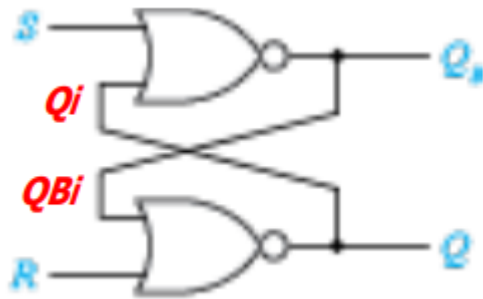
<https://esim.fossee.in/circuit-simulation-project>

Name of the participant: **Shreyas Choudhary**

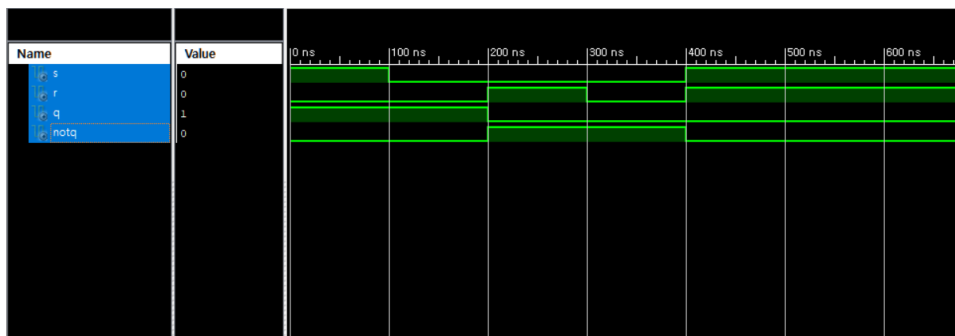
Title of the circuit: **SR Latch**

Theory/Description: An SR latch made from two NAND gates. An SR latch (Set/Reset) is an asynchronous device: it works independently of control signals and relies only on the state of the S and R inputs. In the image, we can see that an SR latch can be created with two NOR gates that have a cross-feedback loop.

Circuit Diagram(s): created using NGHDL



Results (Input, Output waveforms, and/or Multimeter readings) :



Source/Reference(s):

[https://www.tutorialspoint.com/vlsi\\_design/vlsi\\_design\\_vhdl\\_introduction.htm](https://www.tutorialspoint.com/vlsi_design/vlsi_design_vhdl_introduction.htm)

SR Latch VHDL code:- [https://github.com/Shreyas1308/FOSSEE\\_submission.git](https://github.com/Shreyas1308/FOSSEE_submission.git)