SHREYAS GAWALI

Email: shreyasgawali123@gmail.com | **Phone:** +1 682-283-4600 | **IMMIRGATION STATUS: F1 CPT till Dec 2026**
LinkedIn: https://www.linkedin.com/in/shreyasgawali/ | San Jose, CA

SUMMARY

Electrical Engineer with over 3 years of experience in functional validation and embedded systems, including post- and pre-silicon testing for server CPUs. I am skilled in C, Python, Bash, hardware debugging, and system-level validation using tools such as emulation platforms and hardware. Proven ability to work cross-functionally with design and test teams to drive quality and reliability of hardware products.

PROFESSIONAL EXPERIENCE

Intel Corporation — SoC Functional Validation Engineer
Chandler, AZ | Feb 2022 – June 2025

- IP and SoC-level functional validation and characterization for next-generation accelerator and memory subsystems integrated in server CPU architectures
- Platform and board level bring-up, validation and debug including verifying interactions between SoC blocks (e.g., DDR memory controller, PCIe) during stress and regression tests
- Develop and implement tests using C, Python and Bash scripting to introduce new features and enhance existing functionalities
- Modify existing code to address bug fixes and implement enhancement based on validation outcome
- Run comprehensive regression & stress tests in both pre-silicon emulation environment (Unix-based GUI) and post-silicon hardware (Linux OS)
- Automate post-silicon testing and data collection to improve validation efficiency and throughput
- Participate in cross-functional team discussions to address design changes and updates, ensuring alignment and effective communication
- Maintain detailed documentation of bug fixes and validation processes to support continuous improvement and knowledge sharing

Tata Consultancy Services — Engineer
Talent, OR | Jun 2021 – Feb 2022

- Software testing and validation of the Battery Management System (BMS) used in electric vehicles (EV)
- Hardware in Loop (HIL) testing to validate new and existing features
- Ensure code integrity and identify potential bugs
- Verification of BMS parameters using tools such as Vector CANalyzer and Vector CANape

EDUCATION

Westcliff University – MS, Engineering Management (Expected Dec 2026)
GPA: 4.0/4.0

The University of Texas at Arlington – MS, Electrical Engineering (May 2021)
GPA: 3.3/4.0

University of Mumbai – BE, Electronics Engineering (May 2018)
GPA: 6.87/10

SKILLSET

- **Programming Languages:** C, Python, Bash, Assembly
- **Lab Equipment:** Oscilloscope, Protocol analyzer, Multimeter
- **Operating Systems:** Windows, Linux
- **IDE:** Visual Studio Code, Vim, Eclipse
- **Protocols:** UART, SPI, I2C, CAN, PCIe
- **CI/CD Tools:** GitHub
- **Toolchains:** Makefiles, Assemblers, Linkers, GNU
- **Agile Methodology:** Jira – scrum and kanban

PROJECTS

- RTOS on M4F Controller – Implementation of a custom RTOS solution for ARM Cortex M4F based TM4C123GXL evaluation board that has preemptive scheduling with support for semaphores, yielding, sleep, priority scheduling, priority inheritance, and a shell interface
- Cache Architecture Optimization – Evaluated best architecture and total access time for interfacing 128kb cache in 16-bit microprocessor running Cholesky decomposition
- 32-bit RISC Microprocessor – Designed 4-stage pipelined RISC processor with full hazard resolution and Harvard architecture
- Programmable Pulse Generator – Developed a <$10 waveform generator using TM4C123GXL, supporting dual analog output at up to 40KHz. Virtual COM using 115200 baud rate and 8N1 protocol, with no hardware handshaking used to support waveform generation commands