

CS2323 Computer Architecture

HW-4

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- 1 The generalized formula for array multiplication(of n x n matrix) using systolic array is obtained to be:

$$(3n) - 2 \quad (\text{Ans})$$

This can be understood by realizing that $b_{0,0}$ will take n steps to reach from row 0, to row $n-1$. When $b_{0,0}$ would have reached the $n-1$ th row, $a_{n-1,0}$ would have entered 0th column with it. This $a_{n-1,0}$ will take $n-1$ further steps to reach the $n-1$ th column. When $a_{n-1,0}$ will reach $n-1$ th column, $a_{n-1,n-1}$ would have entered the 0th column. This $a_{n-1,n-1}$ will then take $n-1$ steps to reach the last column. Thus a total of $n + n-1 + n-1 = 3n-2$ steps are required to perform the entire multiplication.

2

```
1 for(row_big=0; row_big<R; row_big = row_big + B) //B is the blocking factor
2 for(col =0; col<C; col++)
3 for(to=0; to<M; to++)
4 for(ti =0; ti <N; ti++)
5 for(i =0; i<K; i++)
6 for(j =0; j<K; j++)
7 for(row=row_big; row_big<min(row_big+B,R); row++)
8 Output_fmaps[to][row][col] += Weights[to][ti][i][j] * Input_fmaps[ti][S*row+i]
   [S*col+j]
```

3

```
1 __device__ void addFunc1(int *a, int *b, int *c)
2
3 __global__ void addFunc2(int *a, int *b, int *c)
4
5 __host__ void random_ints(int* x, int size)
6
7 __host__ int main(void)
```

Variables	Location
x_{dim}	Register
y_{dim}	Register
iteration	Register
pqr	Local
ABC	Global
maxValue	Global

4

- 5 (a) Dimension of the matrix is 16 x 16. Cache size is 128 bytes.
 (b)

Unblocked Cache:

Hits: 192

Misses: 320

Input Matrix Misses = 64 | Output Matrix Misses = 256

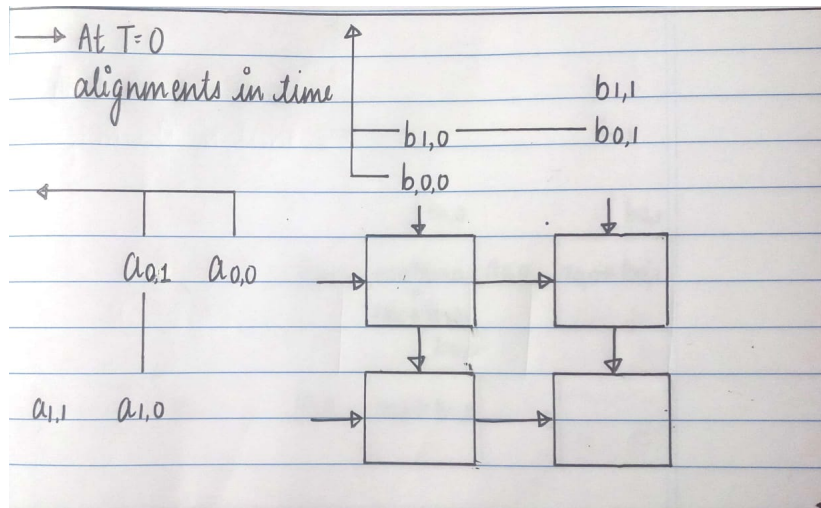
Blocked Cache:

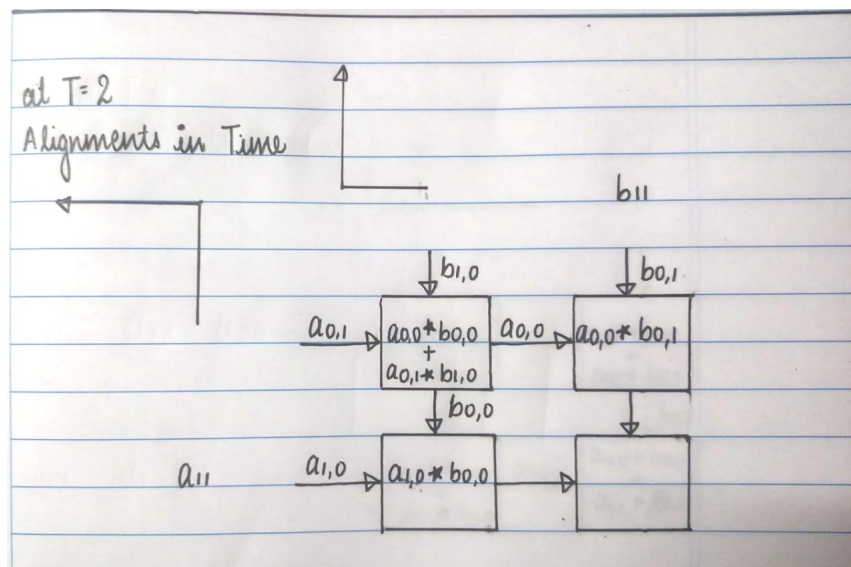
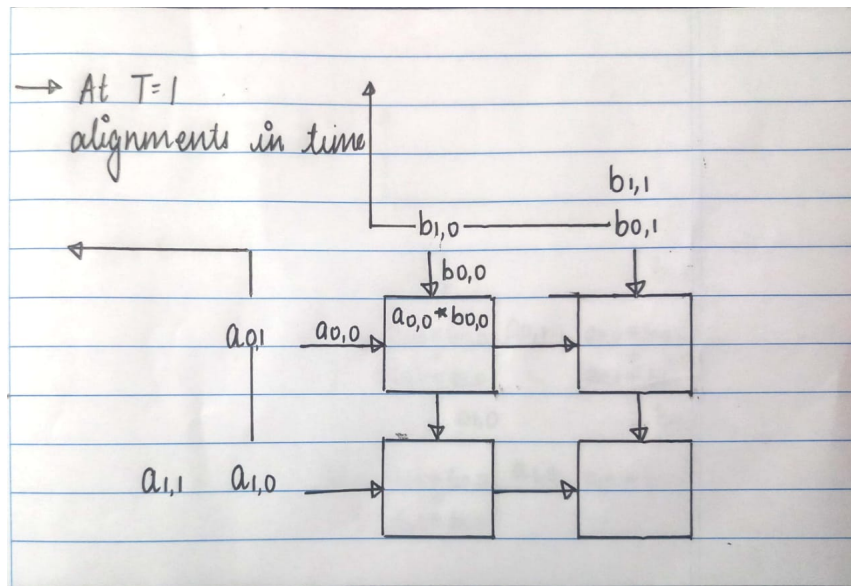
Hits: 384

Misses: 128

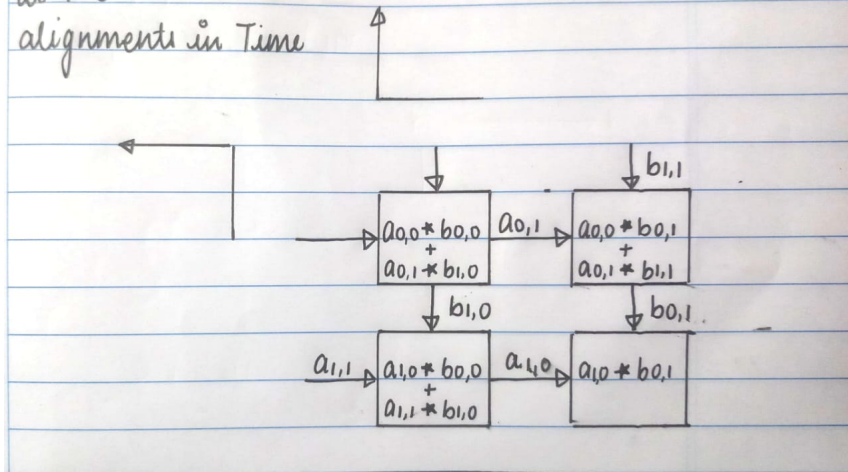
Input Matrix Misses = 64 | Output Matrix Misses = 64

-
- 6 Shown are the 5 stages for $\mathbf{A} \cdot \mathbf{B}$:

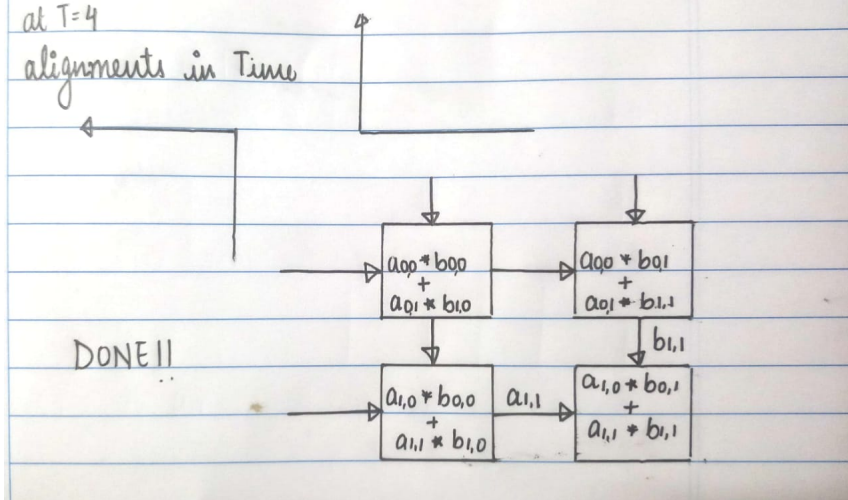




at $T=3$
alignments in Time



at $T=4$
alignments in Time



- 7 (a) 4
 (b) 5.5
 (c) 5.6875
 (d) 5.6953125

8	<table> <tr> <th>Instruction</th><th>Semantics</th></tr> <tr> <td>v.ld vr1, 20[r1]</td><td>vr1 $\leftarrow ([r1 + 20], [r1 + 28])$</td></tr> </table>	Instruction	Semantics	v.ld vr1, 20[r1]	vr1 $\leftarrow ([r1 + 20], [r1 + 28])$
Instruction	Semantics				
v.ld vr1, 20[r1]	vr1 $\leftarrow ([r1 + 20], [r1 + 28])$				

Note: 8byte doubles stored.

- 9 We know: $AI = \frac{TotalFLOPS}{TotalDRAMBytes}$

Note: Assuming 8 byte double elements in all the matrices.

(a)

Case 1:

$$Total\ Flops = n^2; Total\ DRAM\ Bytes = 3n^2 \times 8$$

$$AI = \frac{n^2}{3n^2 \times 8} = 1/24 \quad (Ans)$$

Case 2:

$$Total\ Flops = n^2/4; Total\ DRAM\ Bytes = 3n^2 \times 8$$

$$AI = \frac{n^2/4}{3n^2 \times 8} = 1/96 \quad (Ans)$$

(b)

Case 2:

$$Total\ Flops = n^2/4; Total\ DRAM\ Bytes = 3n^2/4 \times 8$$

$$AI = \frac{n^2/4}{3n^2/4 \times 8} = 1/24 \quad (Ans)$$

- 10 We know: $AI = \frac{TotalFLOPS}{TotalDRAMBytes}$

Note: Taking 1GB = 10^9 Bytes and 1MB = 10^6 Bytes wherever required.

(a)

$$Performance\ of\ ZU19EG\ FPGA\ obtained: \frac{75}{100} \times 66TOPS = 49.5TOPS$$

$$OPS\ to\ classify\ 1\ image = 1.5GOPS$$

$$\therefore TotalImagesClassssifiedIn1Second = \frac{49.5TOPS}{1.5GOPS} = \frac{49500}{1.5} = \mathbf{33000} \quad (Ans)$$

(b)

8bit fixed:

Total Flops = $1.5GFLOPS$; Total DRAM Bytes = $50MB$

$$AI = \frac{1.5G}{50M} = \mathbf{30} \quad (\text{Ans})$$

Binarized:

Total Flops = $1.5GFLOPS$; Total DRAM Bytes = $7.4MB$

$$AI = \frac{1.5G}{7.4M} = \mathbf{202.702} \quad (\text{Ans})$$

11 We know: Peak FLOP = AI \times Memory Bandwidth

Note: Taking $1GB = 10^9$ Bytes and $1MB = 10^6$ Bytes wherever required.

Peak FLOP = $2199GFLOP/s$

$$\therefore AI = \frac{PeakFLOP}{MemoryBandwidth}$$

MCDRAM

$$AI = \frac{2199GFLOP/s}{372GB/s} = \mathbf{5.9112} \quad (\text{Ans})$$

DRAM

$$AI = \frac{2199GFLOP/s}{77GB/s} = \mathbf{28.558} \quad (\text{Ans})$$
