CS2323 Computer Architecture
HW-1

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1 Total Energy = Leakage Energy + Dynamic Energy

(a)L1 Cache:

$LeakagePower_1 = 0.2W$

$$LeakageEnergy_1 = LeakagePower_1 \times TimeTaken = 0.2W \times 1000ns = 200nJ$$

Dynamic Access Energy for Each Access ($DEPA_1$) = 0.217nJ

$No.of Accesses(N_1) = HitRate_1 \times TotalAccesses_1 = 0.95 \times 10^6$

$$DynamicEnergy_1 = DEPA_1 \times N_1 = 0.217 \times 0.95 \times 10^6 = 206,150nJ$$

$$TotalEnergy_1 = 200nJ + 206,150nJ = 206,350nJ$$

$$\frac{DynamicEnergy_1 \times 100}{TotalEnergy_1} = \frac{206,150nJ \times 100}{206,350nJ} = \mathbf{99.903\ \%} \quad \text{(Ans)}$$

(b)L2 Cache:

$TotalAccesses_2 = (1 - HitRate_1) \times TotalAccesses_1 = 0.05 \times 10^6 = 5 \times 10^4$

$No.of Accesses(N_2) = HitRate_2 \times TotalAccesses_2 = 1 \times 5 \times 10^4 = 5 \times 10^4$

$LeakagePower_2 = 6.9W$

$$LeakageEnergy_2 = LeakagePower_2 \times TimeTaken = 6.9W \times 1000ns = 6900nJ$$

Dynamic Access Energy for Each Access ($DEPA_2$) = 1.47nJ

$$DynamicEnergy_2 = DEPA_2 \times N_2 = 1.47 \times 5 \times 10^4 = 73,500nJ$$

$$TotalEnergy_2 = 6900nJ + 73,500nJ = 80,400nJ$$

$$\frac{DynamicEnergy_2 \times 100}{TotalEnergy_2} = \frac{73,500nJ \times 100}{80,400nJ} = \mathbf{91.4179\ \%} \quad \text{(Ans)}$$

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2 On increasing associativity, only the conflict misses can be resolved but the compulsory and capacity misses still persist and constitute the majority of the misses. Therefore the decrease in the miss rate on increasing associativity is marginal.

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3 Total Address Space Bits = 8.

$OffsetBits = \log_2 4 = 2$

$SetBits = \log_2 8 = 3$

$TagBits = 8 - 2 - 3 = 3$

(a)

Cache 1

Sequence	**Tag**	**Set**	**Hit/Miss**
0	0	0	Miss
63	1	7	Miss
1	0	0	Hit
62	1	7	Hit
2	0	0	Hit
61	1	7	Hit
3	0	0	Hit
60	1	7	Hit
4	0	1	Miss
59	1	6	Miss
5	0	1	Hit
58	1	6	Hit
6	0	1	Hit
57	1	6	Hit
7	0	1	Hit
56	1	6	Hit
8	0	2	Miss
55	1	5	Miss
9	0	2	Hit
54	1	5	Hit
10	0	2	Hit
53	1	5	Hit
11	0	2	Hit
52	1	5	Hit

$$\textbf{Hit Ratio} = \frac{18}{24} = 0.75$$

Cache 2

Sequence	**Tag**	**Set**	**Hit/Miss**
0	0	0	Miss
63	7	7	Miss
1	1	0	Miss
62	6	7	Miss
2	2	0	Miss
61	5	7	Miss
3	3	0	Miss
60	4	7	Miss
4	4	0	Miss
59	3	7	Miss
5	5	0	Miss
58	2	7	Miss
6	6	0	Miss
57	1	7	Miss
7	7	0	Miss
56	0	7	Miss
8	0	1	Miss
55	7	6	Miss
9	1	1	Miss
54	6	6	Miss
10	2	1	Miss
53	5	6	Miss
11	3	1	Miss
52	4	6	Miss

$$\textbf{Hit Ratio} = \frac{0}{24} = \mathbf{0}$$

(b)

Cache 1

Sequence	**Tag**	**Set**	**Hit/Miss**
0	0	0	Miss
64	2	0	Miss
128	4	0	Miss
192	6	0	Miss
1	0	0	Miss
65	2	0	Miss
129	4	0	Miss
193	6	0	Miss
11	0	2	Miss
75	2	2	Miss
139	4	2	Miss
203	6	2	Miss
9	0	2	Miss
137	4	2	Miss
201	6	2	Miss
73	2	2	Miss

$$\textbf{Hit Ratio} = \frac{0}{16} = \mathbf{0}$$

Cache 2

Sequence	**Tag**	**Set**	**Hit/Miss**
0	0	0	Miss
64	0	0	Hit
128	0	0	Hit
192	0	0	Hit
1	1	0	Miss
65	1	0	Hit
129	1	0	Hit
193	1	0	Hit
11	3	1	Miss
75	3	1	Hit
139	3	1	Hit
203	3	1	Hit
9	1	1	Miss
137	1	1	Hit
201	1	1	Hit
73	1	1	Hit

$$\textbf{Hit Ratio} = \frac{12}{16} = \mathbf{0.75}$$

4 Given:
Total Instructions $= 10^6$
$I_A = 0.3 \times 10^6, CPI_{A_1} = 2, CPI_{A_2} = 2$
$I_B = 0.2 \times 10^6, CPI_{B_1} = 2, CPI_{B_2} = 1$
$I_C = 0.35 \times 10^6, CPI_{C_1} = 4, CPI_{C_2} = 2$
$I_D = 0.15 \times 10^6, CPI_{D_1} = 4, CPI_{D_2} = 3$
Clock Rate of Processor 1 $=$ 2.2GHz and Clock Rate of Processor 2 $=$ 1.6GHz

$$Cycles_{total} = \sum(Instructions \times CPI)$$

For Processor 1: $Cycles_1 = (I_A \times CPI_{A_1}) + (I_B \times CPI_{B_1}) + (I_C \times CPI_{C_1}) + (I_D \times CPI_{D_1})$
For Processor 2: $Cycles_2 = (I_A \times CPI_{A_2}) + (I_B \times CPI_{B_2}) + (I_C \times CPI_{C_2}) + (I_D \times CPI_{D_2})$

$$Cycle_1 = ((0.3 \times 2) + (0.2 \times 2) + (0.35 \times 4) + (0.15 \times 4)) \times 10^6 = 3 \times 10^6 cycles$$

$$Cycle_2 = ((0.3 \times 2) + (0.2 \times 1) + (0.35 \times 2) + (0.15 \times 3)) \times 10^6 = 1.95 \times 10^6 cycles$$

$$t_1 = \frac{Cycles_1}{ClockRate_1} = \frac{3 \times 10^6}{2.2 \times 10^9} = 1.3636 \times 10^{-3} s \qquad \text{(Ans)}$$

$$t_2 = \frac{Cycles_2}{ClockRate_2} = \frac{1.95 \times 10^6}{1.6 \times 10^9} = 1.21875 \times 10^{-3} s \qquad \text{(Ans)}$$

$\therefore$ **Processor 2** is faster for this program.

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5 Initial State: $\boxed{0}\boxed{0}\boxed{0}\boxed{0}\boxed{\mathbf{0}}$
Rightmost Bit is exclusive bit.

i	0	1	0	0	**0**
ii	0	0	1	0	**1**
iii	1	0	0	0	**1**
iv	1	0	0	1	**0**
v	0	0	0	1	**1**
vi	0	0	1	1	**0**

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6 Let m_1 and w_1 be the L2 Cache misses and ways respectively for Application 1. Let m_2 and w_2 be the L2 Cache misses and ways respectively for Application 2.
Given that linear interpolation applies, the misses and ways can be related as follows:

$$\textbf{Application 1: } m_1 = 4000 - (\tfrac{(4000-3600)}{4} \times (w_1 - 2)) = 4200 - 100w_1$$

$$\textbf{Application 2: } m_2 = 2040 - (\tfrac{(2040-1600)}{4} \times (w_2 - 2)) = 2260 - 110w_2$$

Given that L2 Cache has total 8 ways. Let Application 1 use x ways and Application 2 use $(8-x)$ ways. As an application needs at least 2 ways; $x \geq 2$ and $(8-x) \geq 2$.

$$\therefore 8 - x \geq 2 \implies x \leq 6 \implies 2 \leq x \leq 6$$

$$\therefore m_1 = 4200 - 100x \therefore m_2 = 2260 - 110(8-x)$$

To minimize $m_1 + m_2$:

$$\implies Minimize : 4200 - 100x + 2260 - 110(8-x) \implies 5580 + 10x$$

As linear relation with positive slope of total misses with x, minimize x
$\therefore x = 2$ and $8 - x = 6$

$\therefore$ **Application 1: 2** ways and **Application 2: 6** ways

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7 **(a)**Let transaction rate be $T_P = 44/min, T_Q = 77/min, T_R = 91/min$
Time Taken for i^{th} Transaction $= \dfrac{600}{T_i}$
$TotalTransactions = 600 + 600 + 600 = 1800$

$$Avg(Transactions/min) = \frac{TotalTransactions}{TotalTime} = \frac{1800}{\frac{600}{T_P} + \frac{600}{T_Q} + \frac{600}{T_R}}$$

$$Avg(Transactions/min) = \frac{3}{\frac{1}{T_P} + \frac{1}{T_Q} + \frac{1}{T_R}} \equiv HM(Transactions/min)$$

$$\implies Avg(Transactions/min) = \frac{3}{\frac{1}{44} + \frac{1}{77} + \frac{1}{91}} = \mathbf{64.23529}(Transactions/min) \quad \text{(Ans)}$$

$\therefore$ We will use **Harmonic Mean** to get the average.
(b) Given:
$I_1 = 70, C_1 = 45$
$I_2 = 80, C_2 = 35$
$I_3 = 90, C_3 = 40$
$I_{total} = 240, C_{total} = 120$

Note: Calculating Mean for Instructions per Cycle(IPC)
Weighted AM:
$W_1 = 45/120, W_2 = 35/120, W_3 = 40/120$

$$WAM = \sum W_i \frac{I_i}{C_i} = (\frac{45}{120} \times \frac{70}{45}) + (\frac{35}{120} \times \frac{80}{35}) + (\frac{40}{120} \times \frac{90}{40}) = \frac{70 + 80 + 90}{120} = 2 \quad \text{(Ans)}$$

Weighted HM:
$W_1 = 70/240, W_2 = 80/240, W_3 = 90/240$

$$WHM = \frac{1}{\sum \frac{W_i}{\frac{I_i}{C_i}}} = \frac{1}{(\frac{\frac{70}{240}}{\frac{70}{45}}) + (\frac{\frac{80}{240}}{\frac{80}{35}}) + (\frac{\frac{90}{240}}{\frac{90}{40}})} = \frac{1}{\frac{45}{240} + \frac{35}{240} + \frac{40}{240}} = \frac{240}{45 + 35 + 40} = 2 \quad \text{(Ans)}$$

$\therefore$ Answer is **2** using both WAM and WHM.

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8 Let time taken by System 1 be t_1 and System 0 be t_0.
Given:
$t^1_{init} = t^0_{init}$ and $t^1_{vision} = \dfrac{t^0_{vision}}{7}$ and $t^1_{signal} = \dfrac{t^0_{signal}}{12}$
$t_{init} = 0.29t$ and $t_{vision} = 0.39t$ and $t_{signal} = (1 - 0.29 - 0.39) = 0.32t$

$$\therefore Speedup = \frac{Exec.TimeBefore}{Exec.TimeAfter} = \frac{t_0}{t_1} = \frac{t_0}{0.29t_0 + \dfrac{0.39t_0}{7} + \dfrac{0.32t_0}{12}} = \frac{1050}{391} = \mathbf{2.6854} \qquad \text{(Ans)}$$

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9 Given:
$0.8 \leq Voltage(V) \leq 1.2$
$f_0 = 3GHz$ and $V_0 = 1V$
$P^0_{total} = 150W$
$P^0_{leakage} = 40W$
$P^0_{dynamic} = 150 - 40 = 110W$
$t_0 = 40s$

$$Frequency(f) \propto V \therefore f = 3 \times 10^9 V$$

(i)

$$t \propto \frac{1}{f} \implies t = \frac{t_0 \times f_0}{f} \implies t = \frac{40 \times 3 \times 10^9}{3 \times 10^9 V}$$

$$\implies t = \frac{40}{V}$$

Given V_{max} = 1.2V

$$t_{min} = \frac{40}{1.2} = \mathbf{33\frac{1}{3}}s \qquad \text{(Ans)}$$

$$\boxed{\text{at V = 1.2V, f = 3.6GHz}}$$

(ii) We Know: $P_{total} = P_{dynamic} + P_{leakage}$

Dynamic Power:

$$P_{dynamic} \propto V^2 f \implies P_{dynamic} \propto V^3 \implies P_{dynamic} = \frac{P^0_{dynamic} \times V^3}{V_0^3}$$

$$\implies P_{dynamic} = \frac{110 \times V^3}{1}$$

Leakage Power:

$$P_{leakage} \propto V \implies P_{leakage} = \frac{P^0_{leakage} \times V}{V_0}$$

$$\implies P_{leakage} = \frac{40 \times V}{1}$$

Overall Power:

$$\text{Given } V_{min} = 0.8\text{V}$$

$$P_{total} = 110 \times V^3 + 40 \times V$$

$$P_{total_{min}} = 110 \times 0.8^3 + 40 \times 0.8 = \mathbf{88.32W} \qquad \text{(Ans)}$$

$$\boxed{\text{at V = 0.8V, f = 2.4GHz}}$$

(iii) We Know: $E_{total} = P_{total} \times t$ and $t \propto \frac{1}{V}$

$$E_{total} = (110 \times V^3 + 40 \times V) \times \frac{t_0}{V}$$

$$\implies E_{total} = (110 \times V^2 + 40) \times t_0$$
$$\text{Given } V_{min} = 0.8\text{V}$$

$$E_{total_{min}} = (110 \times 0.8^2 + 40) \times 40 = \mathbf{4416J} \qquad \text{(Ans)}$$

$$\boxed{\text{at V = 0.8V, f = 2.4GHz}}$$

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10 Access Sequence: P, Q, R, S, P, Q, R, S, P, Q, R, S

(a)

(a) LRU Policy:

- P: Miss
- Q: Miss
- R: Miss
- S: Miss
- P: Miss
- Q: Miss
- R: Miss
- S: Miss
- P: Miss
- Q: Miss
- R: Miss
- S: Miss

Total Misses = 12

(b) MRU Policy:

- P: Miss
- Q: Miss
- R: Miss
- S: Miss
- P: Hit
- Q: Hit
- R: Miss
- S: Hit
- P: Hit
- Q: Miss
- R: Hit
- S: Hit

Total Misses = 6
(b)

Access Element	Access Outcome	L1 Cache State	Victim Cache State
		MRU...LRU	
P	Miss	P	-
Q	Miss	Q, P	-
R	Miss	R, Q, P	-
S	Miss	S, R, Q	P
P	Hit	P, S, R	Q
Q	Hit	Q, P, S	R
R	Hit	R, Q, P	S
S	Hit	S, R, Q	P
P	Hit	P, S, R	Q
Q	Hit	Q, P, S	R
R	Hit	R, Q, P	S
S	Hit	S, R, Q	P

Total Misses = 4

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11 Given:
$CPI_{base} = 3$
$MissPenalty_1 = 60ns$
$Loads = 20\%$
$Stores = 10\%$
$ClockFrequency = 2GHz$

$$MissPenalty_{global} = 60 \times 10^{-9} \times 2 \times 10^9 = 120Cycles$$

Case 1:

Given:
No. of Levels = 1
I - Cache Miss Rate = 1%
D - Cache Miss Rate = 3%

CPI increase due to I - Cache Miss = Miss Rate × $MissPenalty_{global}$
= 1% × 120 = 1.2
CPI increase due to D - Cache Miss = Miss Rate × $MissPenalty_{global}$ × (Load+Stores) %
= 3% × 120 × 30% = 1.08

$$CPI_{new} = CPI_{base} + CPI_{total-increase} = 3 + 1.2 + 1.08 = \mathbf{5.28} \qquad \text{(Ans)}$$

Case 2:

Given:
No. of Levels = 2
L1:
I - Cache Miss Rate = 1%
D - Cache Miss Rate = 3%

L2:
L1 miss and L2 hit:

Access Time = 6ns

$$MissPenalty_{local} = 6 \times 10^{-9} \times 2 \times 10^{9} = 12 Cycles$$

CPI increase due to I - L1 - Cache Miss = Miss Rate ×$MissPenalty_{local}$
= 1% × 12 = 0.12
CPI increase due to D - L1 - Cache Miss = Miss Rate ×$MissPenalty_{local}$ × (Load+Stores) %
= 3% × 12 × 30% = 0.108

L1 miss and L2 miss:
L2 Cache Local Miss Rate = 4%
L2 Cache Global Miss Rate = L1-D miss rate × L2 Cache Local Miss Rate = 3%×4% = 0.12 %
CPI increase due to D - L2 - Cache Miss = Miss Rate ×$MissPenalty_{global}$ × (Load+Stores) %
= 0.12% × 120 × 30% = 0.0432

$$CPI_{new} = CPI_{base} + CPI_{total-increase} = 3 + 0.12 + 0.108 + 0.0432 = \mathbf{3.2712} \qquad \text{(Ans)}$$