

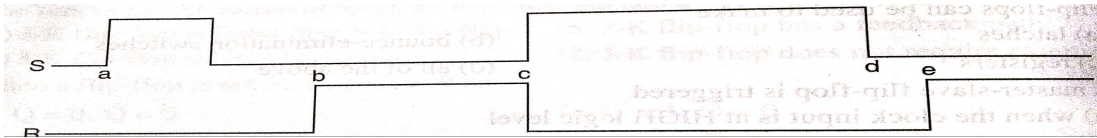
# IIIT Vadodara-International Campus Diu (IIITV-ICD)

Satellite Campus of IIIT Vadodara  
Education Hub, Kevdi, Diu PIN:362520

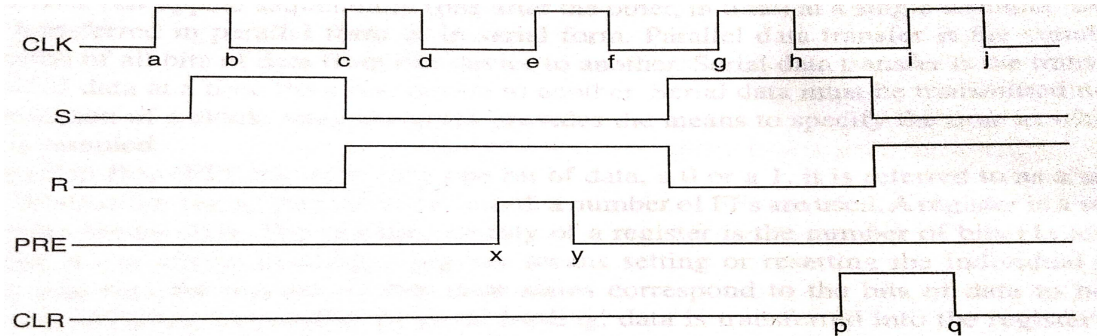
Subject: Digital Logic Design Lab    Branch: CSE  
Course Code:EC261    Semester: III

6 Write a program to generate the output for the following waveform

(a) An active HIGH S-R latch



(b) Negative edge triggered S-R flip flop with active HIGH PRESET and CLEAR.



(c) Positive edge-triggered J-K FF with active LOW PRESET and CLEAR.

