Shreyas Narayanan

248-938-2231 | nshreyas@umich.edu | www.github.com/ShreyasNarayanan06 |

Education

University of Michigan College of Engineering Ann Arbor, MI

B.S.E in Computer Engineering | GPA: 3.7 *Aug 2024 – May 2027*

- **Honors**: Deans List, Regents Scholar, National Merit Semifinalist
- **Relevant Coursework**: Introduction to Logic Design, Computer Organization, Data Structures and Algorithms, Digital IC Design, Discrete Math

Experience

Interactive Sensing and Computing Lab Jan 2025 – Present

Embedded Systems Research Assistant

- Implemented a real time magnetic signature detection algorithm written in C and implemented on a custom PCB to determine and classify the movement of an eyedropper cap under realistic conditions to support a Glaucoma study.
- Applied low pass filtering and derivatives to remove noise over an overlapping sliding window, enabling a threshold based state machine to classify cap events and achieve reliable performance under varying magnetic interference.
- Utilized Python and Matplotlib to create a live modeling tool that identified the magnetic signatures of cap events.
- Developed a rapid PCB prototyping process using a fiber laser, achieving accuracies down to 0.25mm and reducing development times from weeks to under 1.5 hours, enabling same day iteration from design to functional prototype.

Michigan Mars Rover Team Sept 2024 – Present

Embedded Hardware Subteam Member

- Designed schematics and PCB layouts in Altium for 18/12V buck converters powering LDOs and CAN transceivers.
- Validated buck converter performance through load testing, oscilloscope measurements, and multimeter verification, ensuring reliable voltage and current delivery under varying operating conditions from the rover's main battery.
- Maintained and organized schematic libraries using DigiKey, JLCPCB, and TI Power Designer, ensuring accurate component selection, consistent documentation, and efficient design reuse for ongoing and future hardware projects.

Instructional Aide - EECS 270 Introduction to Logic Design Aug 2025 – Present

University of Michigan, College of Engineering

- Led weekly lab sessions of 30+ undergraduates with presentations on Verilog and digital logic design.
- Tutored 20+ students weekly in office hours by providing support on lecture content, project debugging and assistance, providing feedback on assignment and replying to discussion board posts on Piazza.

Projects

Pipelined CPU Simulator

- Designed and implemented a 5-stage pipelined CPU simulator with internal forwarding, stall insertion, and predict not taken branch handling to resolve data and control hazards.
- Developed a comprehensive assembly test suite to validate correctness and edge cases across data dependencies and control hazards.

Traffic Light Controller in Verilog

- Researched, designed, and implemented an 8-bit adder/accumulator in Cadence Virtuoso, creating two custom adder topologies, one optimized for low power using static CMOS logic and one optimized for high speed using CPL, to evaluate performance trade-offs.
- Built supporting datapath components, including custom registers and multiplexers enabling load/clear operations, and verified circuit functionality and timing through detailed SPICE waveform analysis to assess speed, power, and signal integrity.

Technical Skills

Programming: C/C++, Verilog, Assembly, Java, Python, Matlab, Bash, Git, React JS, HTML/CSS, JavaScript
Hardware: Altium, Cadence Virtuoso, FPGAs, LTSpice, Quartus, ModelSim, Arduino IDE, Nordic SDK