Literature review of the paper: InAs-Al Hybrid Devices Passing the Topological Gap Protocol

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Introduction to Topological Quantum Computing and Quantum Computing in General

With the advancement of computing technology, a new frontier has opened: quantum computing. With the growing need for more computational power, we have reduced the size of transistors per unit length to the atomic level. For example, the smallest transistor is 100 times smaller than our blood cells, thus hitting a limit in the real world. Hence, to continue further, we rely on the strange properties of the quantum world to build the transistor equivalent called a quantum bit, also known as a qubit. A qubit is like a regular bit but increases by (2^n) computation this allows us to reach very high computational power with just a few qubits, with n being the number of quantum bits, and instead of taking a position of 1 or 0 in a single qubit, it takes a superposition of both, allowing for simultaneous calculations thus making the most complex calculation which would takes ages of universe to complete reduced to minutes. The potential of the quantum computer is from simulations and breaking encryption, allowing us to solve complex problems. But we have reached a new challenge, which is to sustain the quantum bits, as these are very delicate and can even be missed or disturbed by just room temperature or even the constant cosmic radiation that passes through us every day without us noticing it. Due to this delicate nature, we must create extreme conditions to sustain the devices, particularly the qubits, with the temperature near zero, and a perfect vacuum along complete thermal isolation. Even with all this, there is still a lot of interference, which is countered by another set of qubits dedicated to errors, thus wasting more of the possible computation energy or bits. With this problem, it is difficult to address the need for quantum computers in the world. To provide solutions for this problem, The Microsoft scientists has come up with a topological quantum chip mixing the ability of topological maths with the quantum world.

The Topological Quantum Chip

To understand the topological quantum chip, we need to set the ground rules, which involve understanding the topological property and the quasi-state of the electrons called Majorana topology. Let's start with understanding the Topological aspect of the quantum chip. Topology is the branch of mathematics that deals with geometric surfaces, to give the intuition Let's take the classic example of the donut and coffee mug, which can appear as two different objects but are the same in terms of topology as there is only on hole in both the objects and on can be morphed into another without any tear or cutting but a donut and a pretzel are different as there are three holes in it. Where does this fit in the quantum chip? to answer the question, it's in the Majorana particles. The objective is to design a chip that will tune the energy gap in such a way that it is resilient to the changes around it and still does not lose its quantum property, and this can be achieved by attaining the topological superconductivity.

To further understand the chip, let's understand the Majorana particle, which is more accurately a quasiparticle. A quasiparticle is a particle that exists due to the collective behaviour of the particles in the solid state around it example, a hole in semiconductors. In this case, it is due to the electrons arranged in the superconductors. The Majorana particle is such an example with quantum properties, such as the ability to retrieve data even if half of the structure is damaged due to the properties of quantum entanglement making it critical to storing the qubits for a sustained computation.

In conclusion, the primary objective of the paper is to create and sustain a Majorana particle that has resistance against the noise(disturbances). To prove this, there is the topological gap protocol, which is the protocol through which the process can be verified.

To address this issue, let’s see the challenges in store for such a chip:

1) Disorder

The structure the material of the semiconductor and superconductor must be such that there is minimum disorder, especially in terms of the material combinations and device design

2) Detecting the topological phase

The topological phase is unconventional; hence, it has a complicated mechanism to detect it, as certain measurements may not properly indicate the existence of the phase.

To address the issue, the paper has built the semiconductor in order of the following order,

With a superconductor with a barrier connecting the semiconductor, hence the top to bottom being

1) superconductor – aluminium

2) dielectric

3) InAs (quantum well)

4)buffer

5) substrate

This is done to address the challenges before, as the Al can be widened to prevent the disturbance from spreading, and to consider that the barrier thickness is crucial, so as not to stop the superconductivity is further measured by 4 junctions by measuring the length of trans conductance for purity

For the second challenge to detect the topological phase, we use the Topological gap protocol, which is described as the following parameters and principles,

Local and Non-Local Conductance Measurement:

Measure local (at one end of the device) and non-local (across both ends) differential conductance to observe the presence and extent of low-energy modes.

Zero-Bias Peak Identification:

Observe the emergence of simultaneous zero-bias conductance peaks at both ends of the nanowire that mark potential Majorana zero modes.

Energy Gap Evaluation:

Confirm the presence of a hard energy gap around the zero-bias peaks, showing that low-energy modes are still far from higher excited states.

Parameter Stability Check:

Ensure that these features persist over a continuous range of control parameters (e.g., magnetic field, gate voltages), indicating a stable topological phase and not accidental or trivial states.

Considering the following criteria with a 96% accuracy between the simulation and the experimental data, along with the increase and decrease the temperature to reestablish the topological state after the increase, the paper clearly shows the critical achievement in the field of quantum computing.

Critics and Conclusion

The critics of the paper can be said as the paper is presented as the chip itself is built and a possible hypothetical design for the chip, but attaining the Majorana state is just the beginning, as building the qubits in the chip will be the new problem, but,

The fact that they were able to attain a previous theoretical state shows the possible advancement in quantum computing that can be done, but the growing demand for AI and increasing computer complexity and uncertainty in the world technologies like quantum computing will pave the way for a brighter future.