IMPLEMENTATION OF DRAM USING CADENCE

Mini Project - Report submitted by

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In partial fulfillment of the requirements for the award of

the Degree of

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CERTIFICATE

Certified that the Mini project work entitled

"Implementation of DRAM using Cadence"

is a bonafide work carried out by

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during the year 2023-2024.

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Viva Voce Examination

Name of the Examiners	**Signature with Date**
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ACKNOWLEDGMENT

We like to share our sincere gratitude to all those who help us in completion of this project. During the work we faced many challenges due to our lack of knowledge and experience but these people help us to get over from all the difficulties and in final compilation of our idea to a shaped sculpture.

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ABSTRACT

Dynamic Random Access Memory (DRAM), is a vital part of contemporary computer systems for storing temporary data since it is a sort of memory that stores data in capacitors. The project's goal is to use Cadence's integrated circuit (IC) design tools to design and simulate a DRAM circuit, giving participants a hands-on understanding of memory circuit design and the difficulties involved.

Design of different types of DRAM will be carried out using Cadence Virtuoso in 180nm technology. Cadence, a leading electronic design automation (EDA) tool, provides a comprehensive platform for designing and validating CMOS circuits. Here cadence is used to model and simulate the intricate electrical characteristics of different DRAM cells, ensuring efficient read and write operations.

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CHAPTER 1

INTRODUCTION

As the main temporary data storage medium in contemporary computing systems, Dynamic Random-Access Memory (DRAM) has played a crucial role in the constantly changing field of computer technology. Because DRAM can store and retrieve large amounts of data quickly, it is an essential part of many applications, ranging from embedded systems and mobile devices to personal computers and servers.

The use of capacitors to store discrete data bits is the basic idea underlying DRAM. A capacitor and an access transistor make up each DRAM cell, which enables data storage and retrieval through the charging and discharging of the capacitor. To preserve the stored data, DRAM cells must periodically be refreshed because their capacitors are prone to leaking.

Not only will the effective construction of a DRAM circuit utilizing Cadence's EDA tools show how theoretical ideas can be put into practice, but it will also offer important insights into the difficulties involved in designing memory circuits. Through simulation and validation of DRAM functionality, this study will advance knowledge of an essential part of contemporary computer systems.

1.1 Aim

The aim of the project is to implement a Dynamic Random-Access Memory (DRAM) module using Cadence Virtuoso tools. Some popular DRAM topologies are 1T, 3T and 4T cells, concerned cells are implemented, simulated and read and write operations will be studied.

1.2 Objectives

To successfully implement DRAM using Cadence tools. First, to grasp the intricacies of DRAM architecture, encompassing its operational principles and functionality. This foundational understanding facilitates the subsequent stages.

Following this, familiarize oneself with Cadence design tools, particularly Cadence Virtuoso, to proficiently navigate the process of circuit design, simulation, and implementation. Also explore the capabilities of Cadence tools in designing and optimizing DRAM circuits for power and area efficiency

Subsequently, embark on designing the DRAM circuitry, intricately crafting components like memory cells using Cadence tools. This stage involves detailed schematic capture. We employ techniques such as hierarchical design and transistor-level simulation to ensure the robustness and reliability of the DRAM circuitry

Where in the DRAM chip's physical structure is meticulously crafted, taking into account factors like routing, signal integrity, and spatial constraints. This phase involves translating the circuit-level design into a physical layout while optimizing for factors such as area, power, and manufacturability.

Finally, conduct rigorous simulations to validate the DRAM design's functionality and performance across diverse operational scenarios and potential edge cases. This involves extensive simulation and verification, including writing operation to ensure that the DRAM design meets specifications and performs reliably under varying conditions.

CHAPTER 2

LITRATURE REVIEW

Dynamic Random-Access Memory (DRAM) has been a fundamental component in modern computing systems, providing high-speed data storage and retrieval capabilities crucial for various applications ranging from personal computers to data centers. With the increasing demand for higher memory densities and faster access times, the efficient design and implementation of DRAM circuits have become essential.

DRAM is organized as a matrix of memory cells, typically consisting of a capacitor and an access transistor. These cells store binary information in the form of charge, which must be periodically refreshed to maintain data integrity. The read and write operations in DRAM involve complex signaling schemes and timing constraints to ensure reliable data access. [1]

Computer-Aided Design play a crucial role in the design and verification of DRAM circuits. Cadence Design Systems offers a comprehensive suite of tools for memory design, including Cadence Virtuoso for schematic capture and layout, Specter for circuit simulation, and encounter for physical implementation. [2]

Despite significant advancements in DRAM technology, several challenges remain, including the impact of process variations, signal integrity issues, and the emergence of alternative memory technologies such as High Bandwidth Memory and Magneto-Resistive RAM.

In conclusion, the implementation of DRAM using Cadence tools presents a promising avenue for designing high-performance and energy-efficient memory subsystems. By leveraging advanced CAD techniques and insights from the existing literature, researchers can continue to push the boundaries of DRAM technology and unlock new opportunities for computing innovation.

CHAPTER 3

IMPLEMENTATION

3.1 Components

Transistor (NMOS):

The NMOS transistor, a fundamental building block in semiconductor circuits, is crucial in DRAM design for its role in data storage and access. By controlling the flow of electrons between the source and drain terminals, NMOS transistors enable the implementation of memory cells.

Capacitor:

Capacitors in DRAM store electrical charge, essential for retaining data in memory cells. Their ability to store charge enables DRAM to maintain information temporarily, facilitating rapid data access and manipulation.

VPULSE:

VPULSE, a voltage pulse source in Cadence Virtuoso, is indispensable for simulating dynamic behaviors in DRAM circuits. It generates voltage waveforms with specified characteristics, mimicking real-world operating conditions.

GND:

The ground (GND) node serves as the reference point for voltage in DRAM circuits, establishing a common voltage level for all components. It provides stability and ensures proper functioning of the circuit by maintaining a constant reference potential.

Labelling Pins:

Labelling pins in Cadence Virtuoso facilitate organization and documentation of circuit designs. By assigning labels to specific nodes or components, designers can easily identify and reference them during the design process.

3.2 Software

Cadence Virtuoso, a leading electronic design automation (EDA) software suite, serves as an indispensable tool in the implementation of Dynamic Random-Access Memory (DRAM) modules. Renowned for its comprehensive features and powerful simulation capabilities, Virtuoso provides engineers with a robust platform for designing and optimizing complex semiconductor circuits. With its intuitive user interface and extensive library of design elements, Virtuoso streamlines the development process, enabling engineers to efficiently create detailed circuit models and perform thorough simulations. Moreover, Virtuoso offers advanced analysis tools that facilitate in-depth exploration of DRAM architecture and performance metrics, empowering designers to identify optimization opportunities and refine their designs for enhanced functionality and efficiency. Through its seamless integration with semiconductor fabrication processes, Virtuoso enables designers to translate their conceptual designs into physical layouts, ensuring compatibility with industry-standard manufacturing techniques. In the context of DRAM implementation, Virtuoso plays a pivotal role in accelerating development cycles, enabling engineers to deliver high-performance memory solutions that meet the stringent demands of modern computing systems.

3.3 Schematics

1T DRAM, or one-transistor DRAM, employs a single transistor per memory cell as shown in Figure 3.1, for data storage. This minimalist design offers simplicity and compactness, making it suitable for high-density memory applications. However, 1T DRAM suffers from low retention times and susceptibility to leakage currents, necessitating frequent refresh operations to maintain data integrity.

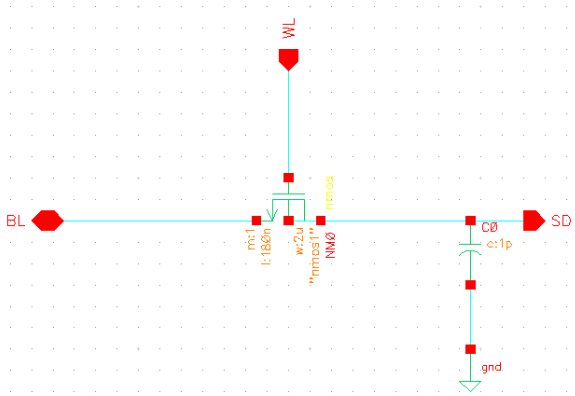

Figure 3.1 Schematic of 1T DRAM

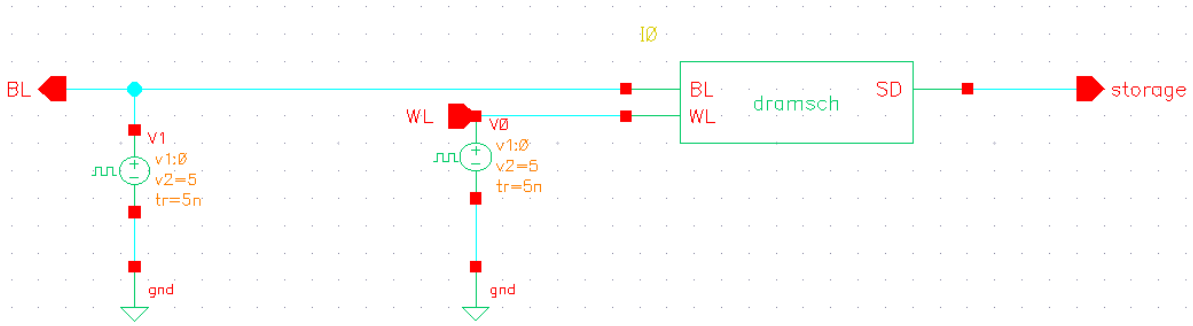

Figure 3.2 Test circuit of 1T DRAM

3T DRAM incorporates three transistors per memory cell: one access transistor and two storage transistors arranged in a flip-flop configuration as shown in Figure 3.3. This design balances performance and area efficiency, providing enhanced data retention and access speed compared to 2T DRAM. However, 3T DRAM still faces challenges related to leakage currents and cell stability, particularly at smaller process nodes.

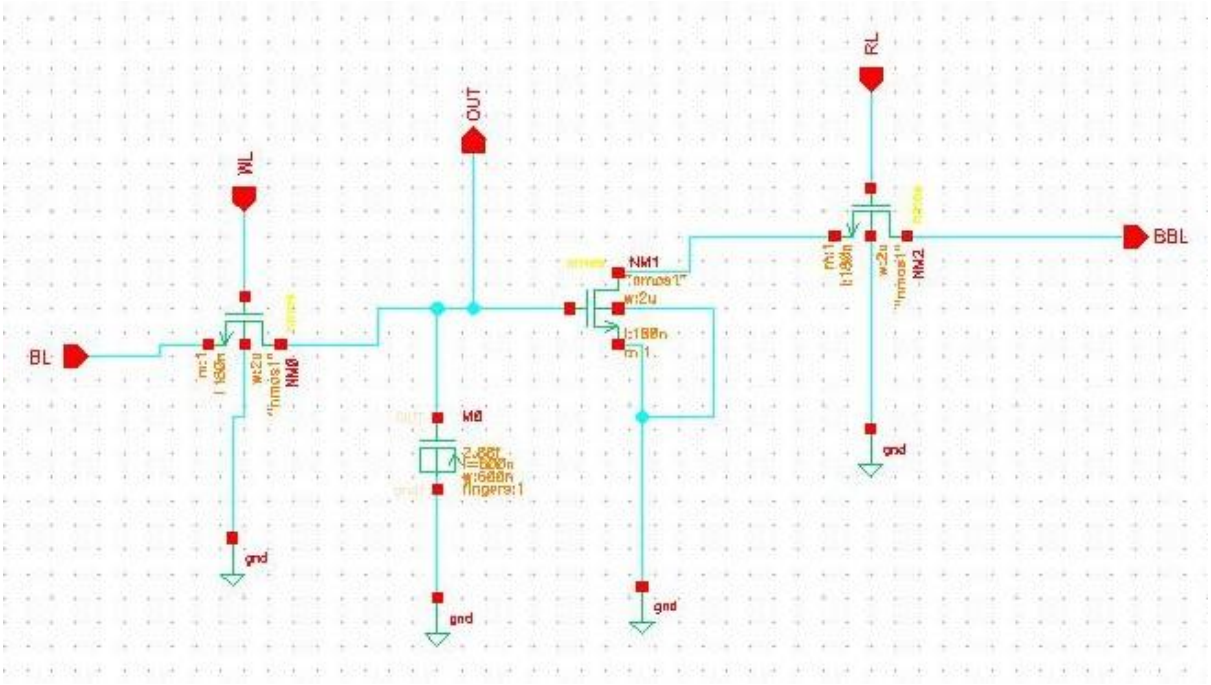

Figure 3.3 Schematic of 3T DRAM

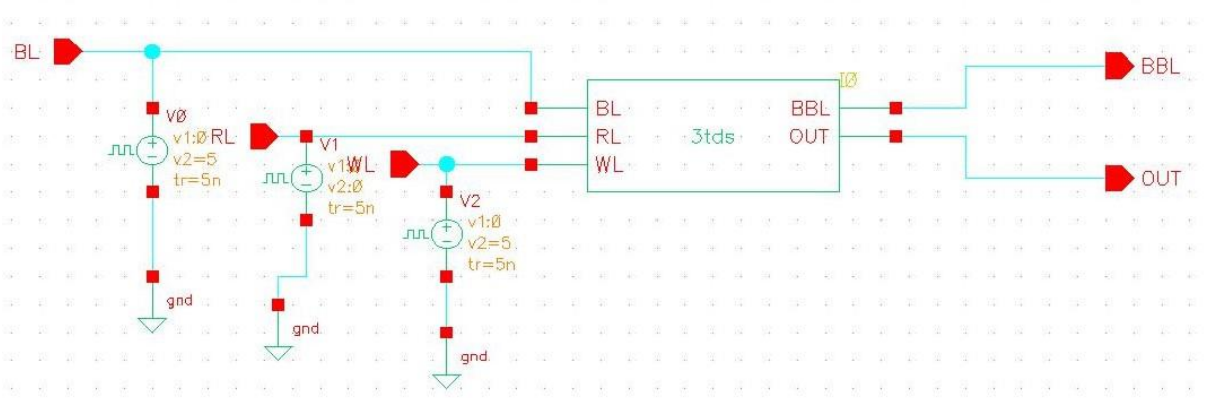

Figure 3.4 Test circuit of 1T DRAM

4T DRAM features four transistors per memory cell, including two access transistors and two storage transistors as shown in figure 3.5. This architecture offers superior data retention and robustness, making it well-suited for high-performance computing applications. Despite its advantages, 4T DRAM requires more complex circuitry and consumes additional silicon area, limiting its practicality for certain memory density requirements.

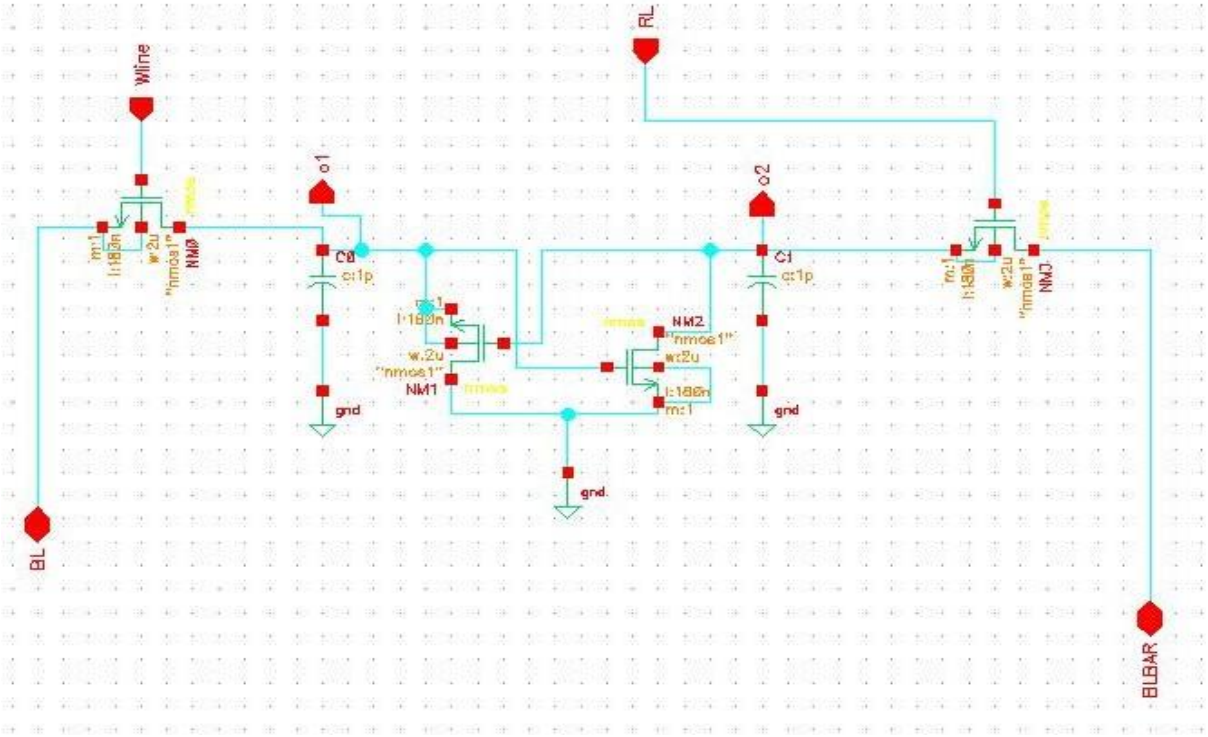

Figure 3.5 Schematic of 4T DRAM

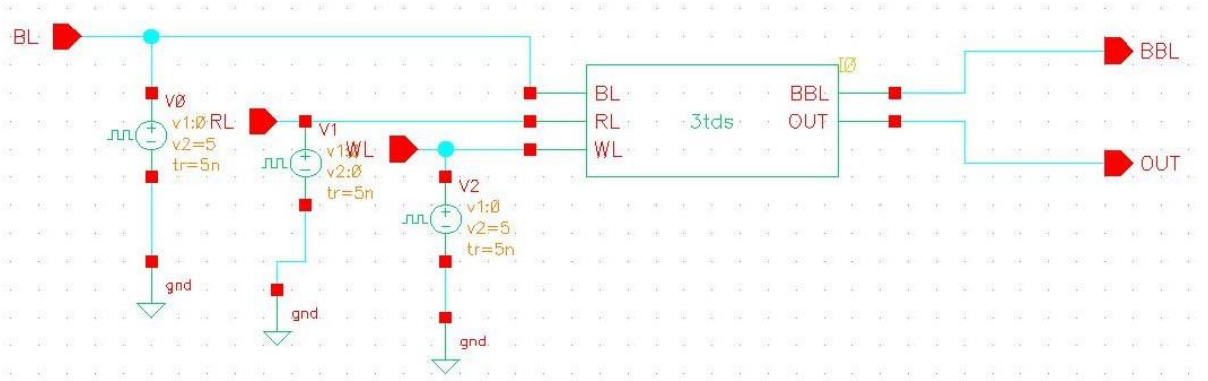

Figure 3.5 Test circuit of 1T DRAM

3.4 Working

In 1T DRAM architecture, a single transistor is utilized per memory cell, simplifying the structure. During a read operation, the transistor acts as both an access transistor and a storage element. To read data, the word line is activated, allowing charge stored in the capacitor to pass through the transistor to the bit line as shown in figure 3.2, indicating the stored data. For write operations, the word line is activated while the bit line is charged or discharged, modifying the charge on the capacitor to write new data.

In 3T DRAM architecture, three transistors are employed per memory cell, providing enhanced read and write capabilities. During a read operation, one transistor acts as an access transistor as shown in Figure 3.4, connecting the capacitor to the bit line, while the other two transistors function as pass transistors, allowing the stored charge to be read without disturbance. For write operations, the access transistor is utilized to modify the charge on the capacitor, updating the stored data.

4T DRAM utilizes four transistors per memory cell, offering increased control and flexibility in read and write operations. During a read operation, one transistor functions as an access transistor as shown Figure 3.6, connecting the capacitor to the bit line, while the other three transistors serve as pass transistors, enabling efficient data retrieval. For write operations, the access transistor and one pass transistor are utilized to modify the charge on the capacitor, facilitating data updates while maintaining data integrity.

RESULT

The diverse architectures of 1T, 3T, and 4T DRAM offer unique trade-offs between complexity, performance, and efficiency in write operations. 1T DRAM's simplicity allows for straightforward read and write processes as shown in Figure 4.1 and figure 4.2, with a single transistor serving dual roles for both access and storage. 3T DRAM further refines this approach, providing improved read stability by utilizing additional pass transistors as shown in figure 4.3. Finally, 4T DRAM offers the highest level of control and data integrity with dedicated access and storage transistors, enabling precise write operations as shown in Figure 4.4. Each architecture presents distinct advantages, catering to diverse application requirements and performance needs in dynamic random access memory implementations.

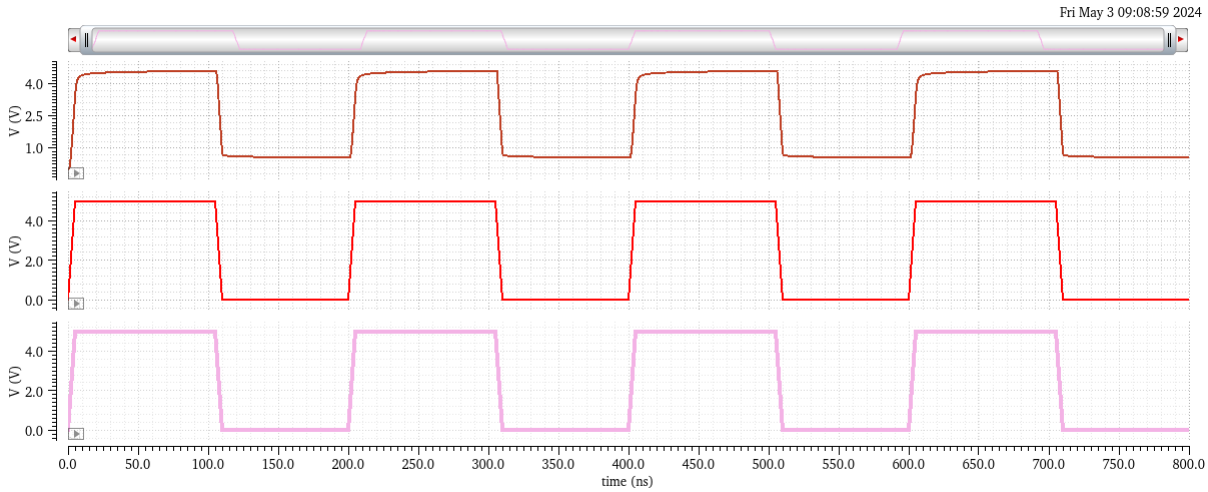

Figure 4.1 Write Operation of 1T DRAM

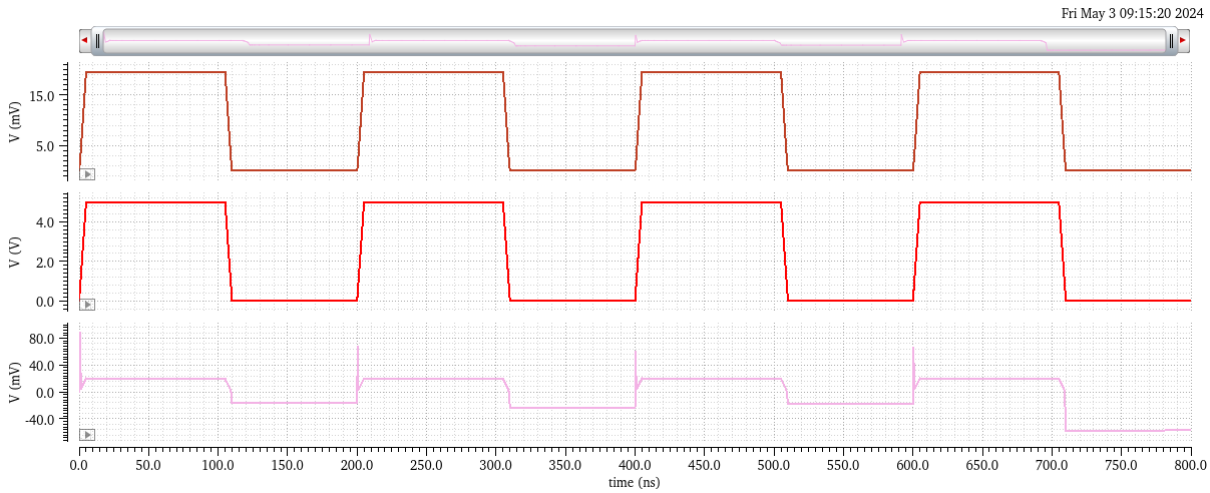

Figure 4.2 Read Operation of 1T DRAM

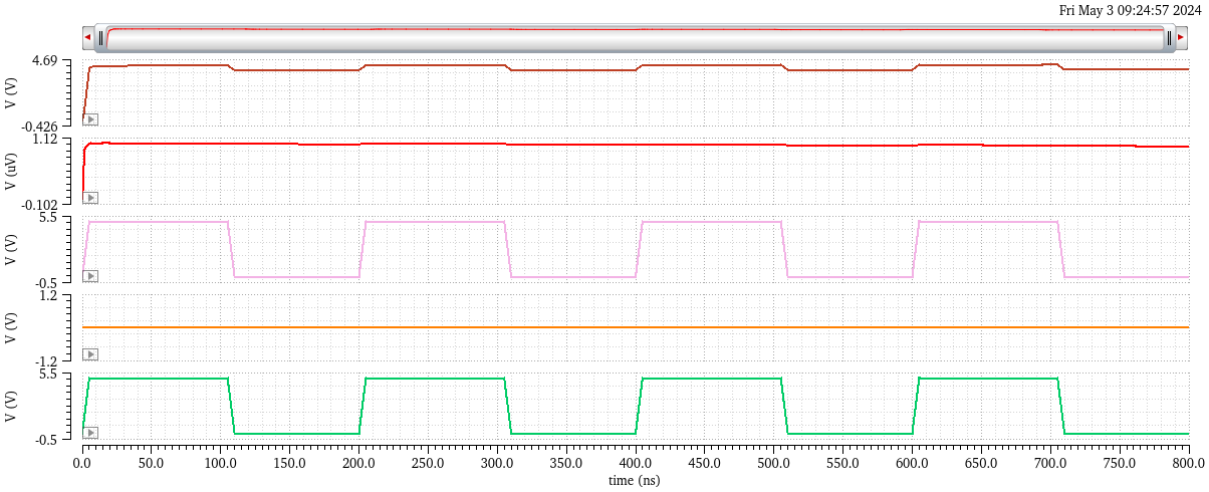

Figure 4.3 Write Operation of 3T DRAM

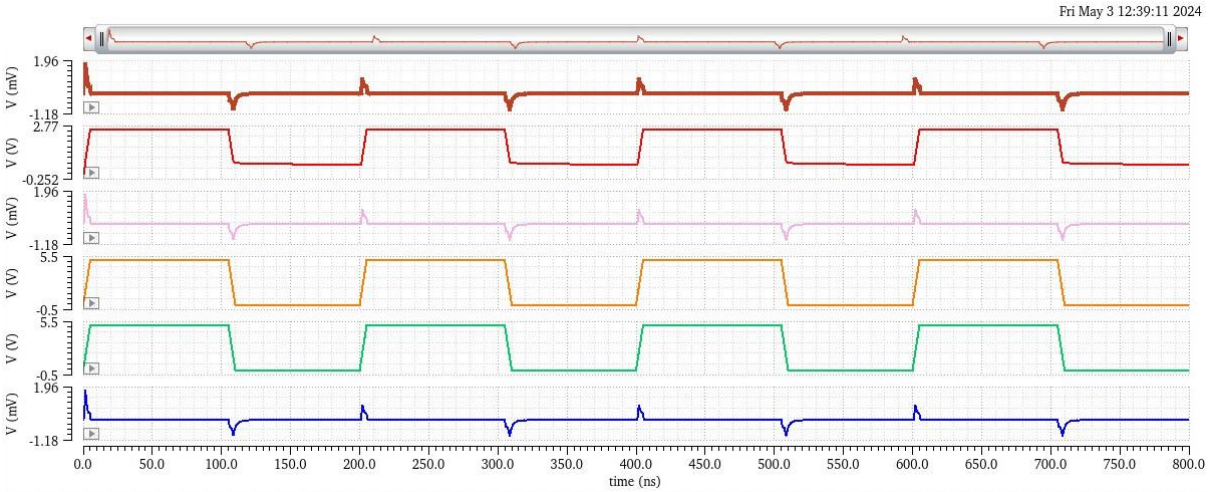

Figure 4.4 Write Operation of 4T DRAM

CONCLUSION

In conclusion, the implementation of DRAM using Cadence Virtuoso presents a promising avenue for advancing memory technology. Through comprehensive analysis, optimization, and simulation using Virtuoso tools, designers can achieve significant improvements in DRAM performance metrics such as access time, power consumption, and data integrity. By leveraging the capabilities of Virtuoso, we can explore innovative design strategies, optimize circuit layouts, and validate performance enhancements, ultimately delivering high-performance and energy-efficient DRAM solutions. Furthermore, the versatility and scalability of Virtuoso enable seamless integration with semiconductor fabrication processes, ensuring compatibility with industry standards and facilitating the transition from design to production. As the demand for high-performance memory solutions continues to grow across various applications, the utilization of Cadence Virtuoso in DRAM implementation holds immense potential for addressing evolving challenges and driving technological innovation in the field of semiconductor design.

SCOPE FOR FUTURE WORK

Future research on the implementation of DRAM using Cadence Virtuoso could explore several avenues to further advance memory technology. Firstly, investigating novel circuit architectures and design methodologies could lead to the development of DRAM modules with enhanced performance and energy efficiency. Additionally, research focusing on the integration of emerging technologies, such as resistive RAM (RRAM) or phase-change memory (PCM), into DRAM designs could unlock new possibilities for improving storage density and reliability. Furthermore, exploring advanced manufacturing techniques and materials could enable the fabrication of DRAM modules with reduced feature sizes and increased scalability. Moreover, research into techniques for mitigating common challenges in DRAM design, such as reducing leakage current and enhancing data retention, could contribute to the development of more robust and reliable memory solutions. Overall, future research efforts should aim to push the boundaries of DRAM technology, addressing current limitations and driving innovation to meet the growing demands of modern computing systems.

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