University of Central Florida

Department of Computer Science

CDA 5106: Fall 2022

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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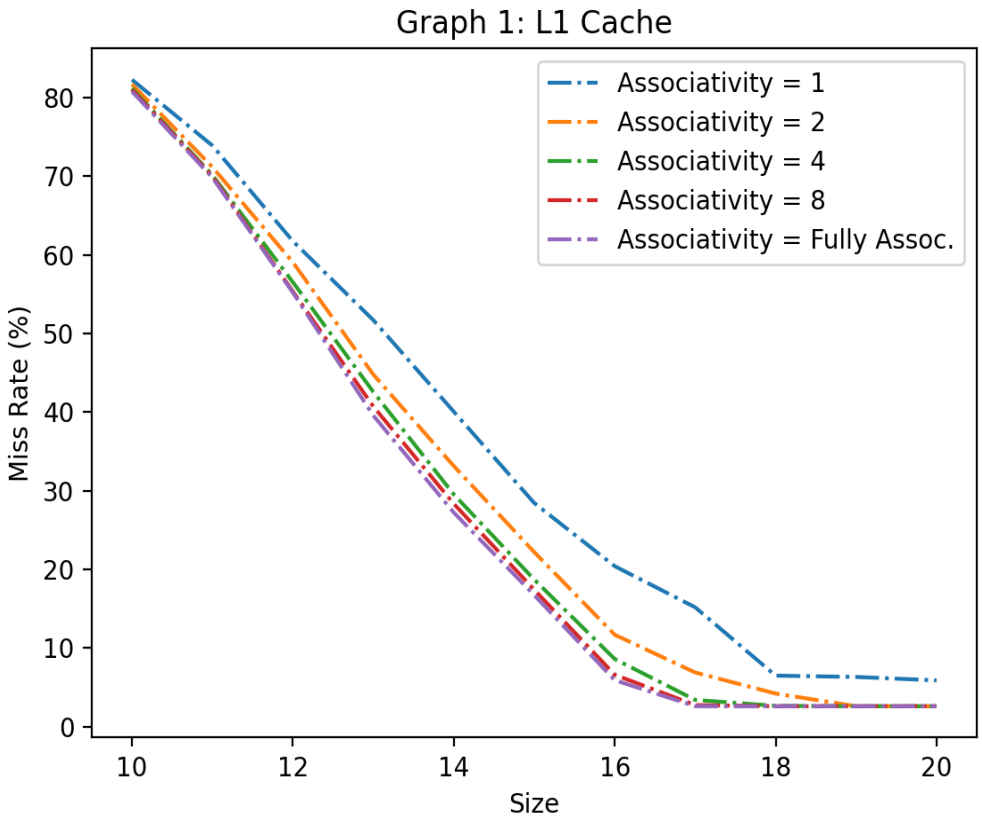
Sample cover page for MP1.

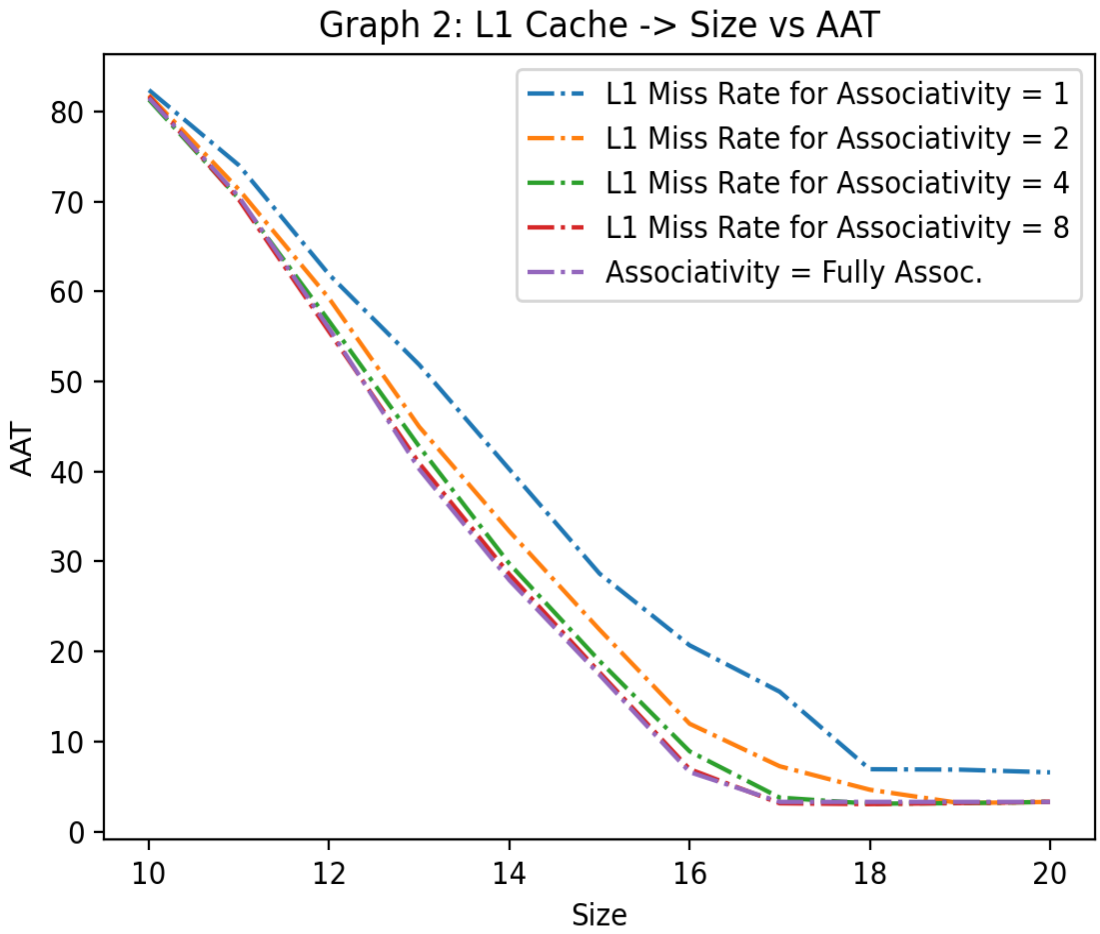
1. L1 cache exploration: SIZE and ASSOC



- It's clearly evident from the curve above that for fixed associativity if the cache size is increased miss rate decreases very drastically but after a saturation point, it becomes constant so increasing cache size can only reduce the miss rate to a point after that it's not beneficial.

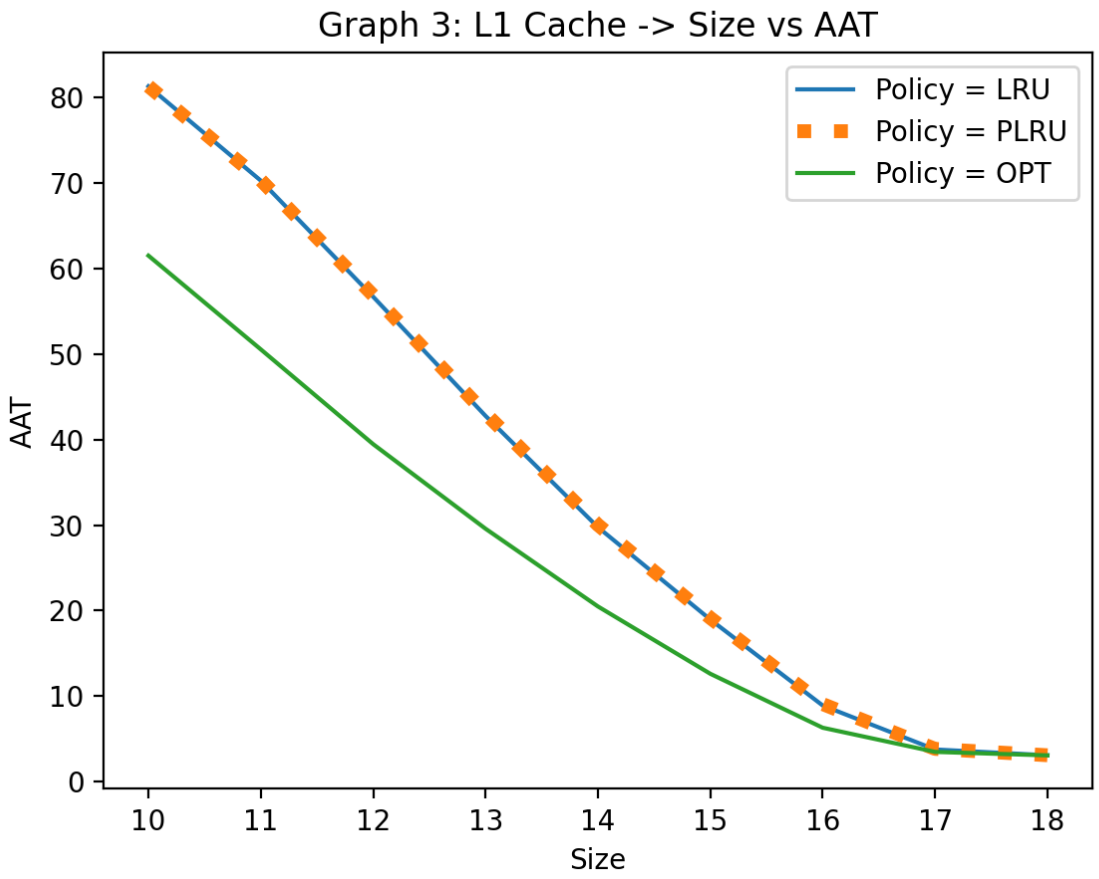
- Increasing the associativity for the constant cache size will slightly diminish the miss rate. The difference in the miss rate between the 1-way associative and fully associative is high if the cache size is large.

2. L1 cache exploration: SIZE and Associativity vs AAT



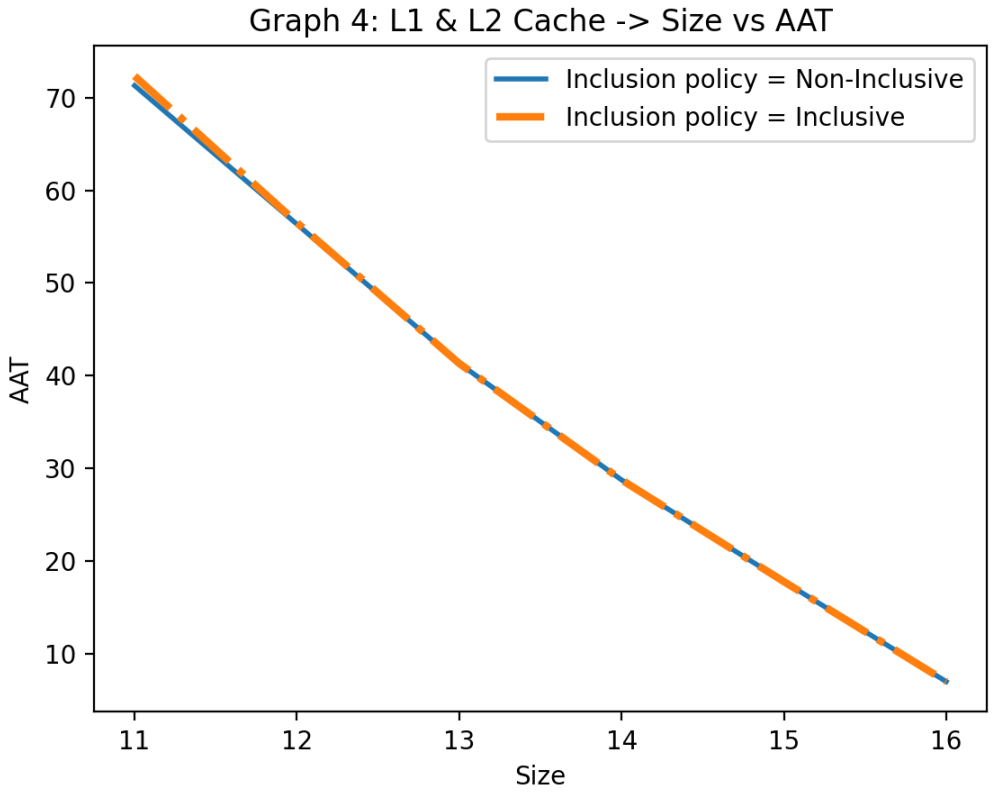
- We can observe from the above graph that the 8-way associative and fully associative have almost the same AAT but full associative being having slightly lower AAT(better) than 8-way associative and again the AAT decreases with the increase in cache size.

3. REPLACEMENT POLICY



- For the 4-way associativity and blocksize 32, it's clearly evident from the figure above that the optimal policy yields the lowest AAT whereas pseudoLRU and the LRU policies have the almost same AAT and with being slightly higher than the optimal policy in case of almost all the cache sizes just the larger cache size(near to 256kb) being outlier where all the three policies have almost the same AAT.

4. INCLUSION PROPERTY



- From what we can observe from the above graph is that changing the inclusion policies doesn't make much difference in the Average Access Time though the trend we can observe is that increasing the cache size does make the AAT linearly lower, though the non-inclusive property might have a slighter advantage in case of small cache size.