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Department of Information Technology

Computer Organization and Architecture

Online Examination Question Bank

UNIT I and UNIT II

1. In Booth's non-restoring division algorithm, after performing left shift operation on A, Q registers, if magnitude of A < 0 then?
   a. Q0=0, A=A+M
   b. A=A+M
   c. Q0=1
   d. A=A-M
2. In Booth's bit-pair recoding, what version of multiplicand will be selected if consecutive multiplier bits are 011?
   a. 0*M
   b. 1*M
   c. -1*M
   d. +2*M
3. What will be the result of Booth's bit-pair recoding operation on this multiplier 111010?
   a. 0-1-2
   b. 0+2-1
   c. 0+1+2
   d. 0-10
4. In Booth's restoring division algorithm, after performing operations (1) left shift operation on A,Q and (2) A=A-M, if MSB of A is 0?
   a. Q0=0, A=A+M
   b. A=A+M
   c. Q0=1
   d. A=A-M
5. In Booth's non restoring division algorithm, for Dividend=10000 and Divisor=100. How many numbers of cycles are required to get the correct division result
   a. 4
   b. 5
   c. 3
   d. 6
6. In Booth's algorithm, if Multiplicand = +22 and Multiplier = -5, what is content of A, Q and Q-1 register after third cycle?

a. A=001000, Q=010111, Q-1=0

b. A=111001, Q=010111, Q-1=0

c. A=000001, Q=010111, Q-1=1

d. A=001000, Q=010111, Q-1=1

7. In Booth's algorithm, if Multiplicand = +15 and Multiplier = -6, what is content of A, Q and Q-1 register after fourth cycle?

a. A=11010, Q=01101, Q-1=0

b. A=11010, Q=01101, Q-1=1

c. A=11010, Q=11010, Q-1=1

d. A=10100, Q=11010, Q-1=1

8. In restoring division algorithm, if Dividend = 1010 and Divisor = 0011, what is content of A and Q register after third cycle ?

a. A=10001, Q=0001

b. A=00010, Q=0011

c. A=00010, Q=0001

d. A=01001, Q=0101

9. In restoring division algorithm, if Dividend = 17 and Divisor = 03, what is content of A and Q register after fourth cycle ?

a. A=111111, Q=10010

b. A=000010, Q=10010

c. A=000011, Q=00010

d. A=101001, Q=00101

10. In non-restoring division algorithm, if Dividend = 1100 and Divisor = 0011, what is content of A and Q register after third cycle ?

a. A=11101, Q=0010

b. A=00001, Q=0010

c. A=00010, Q=0001

d. A=00000, Q=0011

11. In non-restoring division algorithm, if Dividend = 1011 and Divisor = 0101, what is content of A and Q register after fourth cycle ?

a. A=11100, Q=0010

b. A=00001, Q=0010

c. A=00000, Q=0010

d. None of these

12. What will be the result of Booth recoding operation on 0011110?

a. 0+1000-10

b. 0+1000+10

c. 0+10000

d. 0-1000-10

13. In Booth's bit-pair recoding, what version of multiplicand will be selected if consecutive multiplier bits are 001?

a. 0*M

b. +1*M

c. -1*M

d. +2*M

14. n Booth's bit-pair recoding, what version of multiplicand will be selected if consecutive multiplier bits are 011?
    a. 0*M
    b. +1*M
    c. -1*M
    d. +2*M
15. In Booth's bit-pair recoding, what version of multiplicand will be selected if consecutive multiplier bits are 100?
    a. 0*M
    b. +1*M
    c. +2*M
    d. -2*M
16. In Booth's bit-pair recoding, what version of multiplicand will be selected if consecutive multiplier bits are 101?
    a. 0*M
    b. +1*M
    c. -1*M
    d. +2*M
17. In Booth's bit-pair recoding, what version of multiplicand will be selected if consecutive multiplier bits are 110?
    a. 0*M
    b. +1*M
    c. -1*M
    d. +2*M
18. What will be the result of Booth's bit-pair recoding operation on this multiplier 111010?
    a. 0-1-2
    b. 0+2-1
    c. 1-2
    d. 0-1-0
19. What will be the result of Booth's bit-pair recoding operation on this multiplier 11010?
    a. 0-1-2
    b. 0+2-1
    c. 12
    d. 0-10
20. Calculate the CPU time of the system having CPI 1.43, clock rate 100MHz, and instruciton count of 7*106 ?
    a. 0.01sec
    b. 0.1sec
    c. 0.02sec

d. 0.2sec

21. Calculate the CPU time of the system having CPI 1.25, clock rate 100 MHz, and instruciton count of 12*106 ?
    a. 0.12sec
    b. 0.125sec
    c. 0.15sec
    d. 0.2sec
22. Calculate the CPU time of the system having CPI 1.25, clock rate 100 MHz, and instruciton count of 12millions ?
    a. 0.12sec
    b. 0.125sec
    c. 0.15sec
    d. 0.2sec
23. Calculate the CPU time of the system having CPI 1.43, clock rate 100MHz, and instruciton count of 7 millions?
    a. 0.01sec
    b. 0.1sec
    c. 0.02sec
    d. 0.2sec
24. Calculate the CPI of the system having CPU time of 0.1sec, clock rate 100MHz, and instruciton count of 7 millions?
    a. 1
    b. 1.1
    c. 1.43
    d. 1.7
25. Calculate the CPI of the system having CPU time of 0.1sec, clock rate 100MHz, and instruciton count of 7*106 ?
    a. 1
    b. 1.1
    c. 1.43
    d. 1.7

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26. Which is the fastest memory in computer system?
    a. Registers
    b. RAM
    c. ROM
    d. Cache
27. What are the basic components of the CPU?
    a. Registers
    b. ALU
    c. Control Unit
    d. All of these

28. Which registers shows the status of the CPU?
    a. Status /Flag Register
    b. General Purpose Register
    c. Special Purpose Register
    d. Stack
29. What is mean by op-code?
    a. Operation code
    b. Output code
    c. Organized code
    d. Optional code
30. What are the sources of the operand?
    a. Main memory
    b. CPU registers and I/O devices
    c. CPU register and ALU
    d. Both 1 and 2
31. What is the correct sequence of execution of an instruction?
    a. Decode-Fetch-Execute
    b. Execute-Fetch-Decode
    c. Fetch-Decode-Execute
    d. None of these
32. What is the function of data movement instructions?
    a. Processing of data
    b. Movement of data
    c. Mange the program flow control
    d. Both 1 and 2
33. What is the function of data processing instructions?
    a. Processing of data
    b. Movement of data
    c. Mange the program flow control
    d. Both 1 and 2
34. Which instruction has one of the operand as an accumulator?
    a. 1 address
    b. 2 address
    c. 3 address
    d. 0 address
35. Which instruction has all implicit addresses?
    a. 1 address
    b. 2 address
    c. 3 address
    d. 0 address
36. How many addresses do the stack related instructions use?
    a. 1 address

b. 2 address
c. 3 address
d. 0 address

37. Which of the following is a memory addressing mode?
    a. Register addressing
    b. Direct addressing
    c. In-direct addressing
    d. Both b and c
38. Which of the following is a fastest addressing mode?
    a. Register addressing
    b. Direct addressing
    c. Immediate addressing
    d. None of these
39. In which of the following addressing modes one of the operand is data?
    a. Register addressing
    b. Direct addressing
    c. Immediate addressing
    d. None of these
40. The instruction that are used to move the data among CPU registers are in the group of
    a. Data Transfer Instruction
    b. Logical Instrcution
    c. Control Transfer Instruction
    d. None of these
41. How many memory reference are required to fetch single indirection instuction ?
    a. 1
    b. 2
    c. 3
    d. 0
42. Next instruction reference is
    a. explicitly in instruction
    b. implicitly in instruction
    c. Both a and b alternatively
    d. Completely
43. The operation of the CPU is determined by the instruction it exectutes, referred to as
    a. Computer instruction
    b. Machine instruction
    c. Next instruction
    d. Both a and b
44. In instuction cycle state diagram, which is next step after instruction/ operation decoding?
    a. Date operation
    b. Operatnd fetch
    c. Operand address calculation

d. Instruction address calculation

45. In instuction cycle state diagram, which is next step after instruciton address calculation?
    a. Date operation
    b. Instruction fetch
    c. Operand address calculation
    d. Instruction address calculation
46. In case of which instruction, system discard the next consecutive instruction?
    a. Interupt
    b. Branch
    c. Jump
    d. All of these
47. The ALU is that part of computer that actually performs arithmetic and logical operation on …..
    a. Instructions
    b. Data
    c. Both data and instruction
    d. None of these
48. Each instruction is represented by
    a. Operand
    b. Opcode
    c. Both a and b alternatively
    d. Sequence of bits
49. Logical instructions operate on,
    a. Numeric data
    b. Bits of word
    c. Character data
    d. Both numeric and character data
50. Branch instruction are used,
    a. Branch to same set of instruction depending on addition
    b. Branch to a different set of instructions depending on the decision made
    c. Branch to different set of data based on decsion made
    d. None of these
51. In case of one address instructions, which register is used as second operand ?
    a. IR
    b. AC
    c. MQ
    d. MBR
52. Which of the following is fastest instructi on?
    a. Three Address
    b. Two Address
    c. One Address
    d. None of these
53. Which of the following is slowest instruciton?

a. Three Address
b. Two Address
c. One Address
d. None of these

54. Which kind of instructions are widely used?
    a. Three Address
    b. Two Address
    c. One Address
    d. None of these
55. Which kind of instructions uses stack as memory?
    a. Three Address
    b. Two Address
    c. One Address
    d. None of these
56. Which is common representation for representing character data?
    a. ASCII
    b. EBCDIC
    c. Unicode
    d. All of these
57. PUSH and POP are,
    a. Arithmetic operations
    b. Data transfer operations
    c. Logical operations
    d. Transfer of control
58. Set and Reset are,
    a. Arithmetic operations
    b. Data transfer operations
    c. Logical operations
    d. Transfer of control
59. Test is,
    a. Arithmetic operations
    b. Data transfer operations
    c. Logical operations
    d. Transfer of control
60. Halt is,
    a. Arithmetic operations
    b. Data transfer operations
    c. Logical operations
    d. Transfer of control
61. Which kind of operations are performed in privileged state?
    a. Input/ Output
    b. Transfer of control

c. System control
d. All of these

62. In case of branch instructions,
    a. One of its operands is the address of the next instructions.
    b. One of its operand is AC
    c. One of its operand is numeric
    d. One of its operand in NULL
63. Procedure call instructions uses which type of memory
    a. Stack memory
    b. Sequential memory
    c. Both a and b alternatively
    d. None of these
64. Which kind of addressing mode do not require any memory reference?
    a. Immediate
    b. Register
    c. Both a and b
    d. Register indirect
65. Which kind of addressing mode do not require any memory reference?
    a. Immediate
    b. Register
    c. Stack
    d. All of these
66. Which kind of displacement based addressing uses PC as register?
        a. PC addressing
        b. Relative Addressing
        c. Base register
        d. Index
67. Incrementation operation uses which kind of displacement based addressing?
    a. Base addressing
    b. Index
    c. Relative addressing
    d. All of these
68. The CPU reads an instruction from memory is,
    a. Decode operation
    b. Fetch operation
    c. Fetch data
    d. Write data
69. Which registers helps to minimize the main memory references?
    a. User-visible registers
    b. Control registers
    c. Status registers
    d. Invisible registers

70. Which registers are partially visible to the programmer?
    a. Address
    b. Data
    c. Stack pointer
    d. Condition codes
71. Indirect cycle take place in case of which addressing modes?
    a. Indirect
    b. Relative addressing
    c. Post indexing
    d. All of these
72. Which of the following is correct sequence in case of indirect instructions?
    a. Fetch-Decode-Execute
    b. Fetch-Decode-Execute-Indirect
    c. Fetch-Indirect-Decode-Execute
    d. None of these
73. Contents of which register is used to fetch an instruction?
    a. IR
    b. PC
    c. MAR
    d. MBR
74. Which register stores the output of fetch cycle?
    a. IR
    b. PC
    c. MAR
    d. MBR
75. During which cycle contents of the PC must be saved to memory?
    a. Fetch
    b. Decode
    c. Interrupt
    d. Execute
76. Which of the following cycle calculate the effective address of each source operand?
    a. Fetch operand
    b. Decode operand
    c. Calculate operand
    d. Write operand
77. The PC will be updated. If there is,
    a. Unconditional Branch
    b. Conditional Branch
    c. Interrupt
    d. All of these
78. After updating PC, system should
    a. Fetch instruction

b. Empty pipe and fetch instruction
c. Empty pipe
d. None of these

79. Machine cycle is,
    a. Time taken to fetch operand.
    b. Time taken to fetch operand and performa ALU operations.
    c. Time taken to fetch operand, perform ALU operations and stores result in a registers.
    d. None of these
80. The length of program is smaller in case of ,
    a. CISC
    b. RISC
    c. Both of these
    d. None of these
81. Which kind of architecture uses simpler addressing modes?
    a. CISC
    b. RISC
    c. Both of these
    d. None of these
82. Which kind of architecture uses simpler addressing modes?
    a. CISC
    b. RISC
    c. Both of these
    d. None of these
83. Which kind of architecture uses complex addressing modes?
    a. CISC
    b. RISC
    c. Both of these
    d. None of these
84. Which kind of architecture uses simpler instruction format?
    a. CISC
    b. RISC
    c. Both of these
    d. None of these
85. Which kind of architecture uses complex instruction format?
    a. CISC
    b. RISC
    c. Both of these
    d. None of these
86. How many registers are supported in case of MIPS?
    a. 30
    b. 31
    c. 32

d. 33

87. What is size of cache in case of MIPS?
    a. 124bytes
    b. 128MB
    c. 128Kbytes
    d. 128kbits
88. MIPS R4000 support,
    a. IEEE single precision format
    b. IEEE dobule precision format
    c. Both a and b
    d. None of these
89. Which is first commercially available RISC processor?
    a. MIPS
    b. MPPS
    c. VAX
    d. MPIS