

DE1-SOC: Altera Cyclone V SoC

Version-1.0

Revision History:

| Date | Version | Authors | Revision Description | Reviewers | Status |
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| Dec 14 th 2023 | 1.0 | Satish Sankella, Ruthvik R Chanda, Harinarayan Gajapathy, Shrinithi Venkatesan | Documented the initial technical report of project using DE1- SOC, Altera CycloneV system on chip | Prof. Timothy Lee Scherr Aamir Suhail Burhan Daniel Mendez | Drafted |

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1. Executive Summary

This report summarizes the detailed project broken down into four modules, each with a specific objective of learning different aspects of DE1-SOC Altera Cyclone-V FPGA development flow particularly in the case of learning and exploring an advanced approach of interfacing hard processor system, on-chip peripherals and IPs and advanced designs utilizing bigger amount of logic elements on the fabric. The scope covers the objectives, procedure, test results and learning outcome.

| Module | Description | Learning Outcome |
|----------------------------------|---|---|
| FPGA Architecture | DE1-SOC KIT is a FPGA evaluation kit which adopts Altera's Cyclone-V SOC FPGA is used for the entire project which integrates a range of features, including programmable logic elements, ARM Cortex-A9 processor, DSP blocks, and various peripherals. | Hands-on familiarity with the Cyclone V FPGA, gaining insights into its architecture, dual-core ARM Cortex-A9 hard processor, and the integration of programmable logic and embedded processing capabilities. |
| Quartus Prime Design Suite | The project utilizes the Quartus Prime design suite for hardware development, offering a cohesive toolset with IP cores and reference designs. | Learning the utilization of Quartus Prime to develop, design, analyze, synthesize, and simulate diverse hardware implementations tailored to the DE1-SOC platform. |
| Design Flow | The programmable logic implementation is achieved through Hardware Description Languages (HDLs) such as Verilog and VHDL, incorporating Quartus Prime tools for synthesis, simulation, and verification. | Mastering the design flow, encompassing the use of HDLs, system-level design, synthesis, and simulation, ensuring compliance with project requirements. |
| Qsys/System Integration | Utilizing Qsys, an integral part of Quartus Prime, for system integration and peripheral configuration, streamlining the design process for complex system-on-chip (SoC) implementations. | Integrating peripherals and configuring the system using Qsys to meet project objectives, enhancing efficiency in SoC design on the DE1-SOC platform. |
| IP Catalog/Libraries | Explored the Audio Codec, HPS timer, high bandwidth interconnect, clocks, PLLs. | Learnt and explored the usage libraries and different core implementations. |
| Timing Analysis & Timing Closure | Implementing timing analysis techniques to validate design performance, identifying, and resolving timing violations to achieve timing closure. | Performing timing analysis, setting clock constraints, and ensuring timing closure for each design iteration, recording, and optimizing Fmax. |
| Simulation | Utilizing ModelSim for design simulation, encompassing script generation, model compilation, simulation execution, and results analysis. | Proficiency in using ModelSim to verify design functionality through simulation, ensuring alignment with expected behavior before programming the FPGA. |
| Intel-FPGA Monitor Program | The Monitor Program is a complete software development environment for the ARM Cortex-A9 processor and Nios II processor. One can develop both assembly-language and C code on DE-series boards using the Monitor Program. | Programmed HPS on SoC system using assembly and C programming without the need of soft-core processor flow due to the added advantage with this tool. |

Conclusion: The overall learning objectives of advanced development flow of programmable logic design are met successfully by working on this project using DE1-SOC and Quartus prime tool. The project explored FPGA and embedded systems, advanced concepts, including C programming for tasks like determining maximum values, successful integration of FPGA with HPS, audio codec, FIR filters showcased a comprehensive understanding of the hardware-software relationship. These project modules showcase the capability of Cyclone-V SoC with large logic

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elements capacity and a powerful HPS processor and provides ease of use with lot of onboard peripherals on DE1-SOC makes it a solid board for learning foundational programmable logic.

2. Objectives

1. Gain proficiency in Quartus and the System-on-Chip Embedded Design Suite (SoC EDS) development flow for seamless integration of hardware and software components.
2. Utilize Quartus to design and implement various combinational and sequential digital circuits on the DE1-SoC board, demonstrating expertise in hardware development.
3. Incorporate the Real-Time Clock into the system using Verilog, with a focus on displaying relevant data on the 7-segment display for effective time representation.
4. Integrate the Audio CODEC into a higher-level system, enabling processing of input audio signals. Implement a filtering mechanism to reduce noise in the audio signal and transmit the filtered output back to the Audio CODEC.
5. Perform Embedded Software Development using the Monitor Program software, employing the C programming language. Develop programs for tasks such as data computation, real-time clock integration, and state machine implementation for 7-segment display messages.
6. Gain a comprehensive understanding of the connection between the Hard Processor System (HPS) and FPGA fabric. Execute cross-compilation of source files to obtain executable files for running on the target device.
7. Employ the arm-linux-gnueabihf cross compiler to compile the project, ensuring compatibility and functionality when executed on the DE1-SoC board.
8. Develop audio filters using on chip audio codec flow and interfacing the audio ADC-DAC flow with digital FIR filters in the middle.

The objective is to finish each module meeting the objectives in a step-by-step manner against specified requirements criteria and provide the analysis and this technical report.

3. Procedure

The approach is formulated to perform each module of the project to meet its requirements and capture test results in the below steps.

- Already installed Quartus for DE1-SOC development.
- Prepared for each project by acquiring the base files and tools required.
- Examined the Verilog/ VHDL design.
- System designed using DE1-SOC.
- Created pin assignments wherever necessary.
- Compiled each project to check each phase of Synthesis, Fitter (Place & Route), Timing Analysis, Simulations are successful.
- Verified Fmax meets its requirements and timing analysis is done. If timing analysis fails, set timing constraints and re-run.
- Programmed the FPGA fabric.
- Captured the system functional behavior and test results to use them in the report.
- Created software programs to run on the synthesized core to interact with peripherals.

4. Modules

4.1 Module 1

4.1.1 Description

In Module 1, we focused on designing various combinational and sequential digital circuits using Verilog HDL on the DE1-SoC board. This included creating a switch-LED, 2:1 & 3:1 MUX circuits, a 2-input selector, and displaying outputs on a 7-segment display. For sequential circuits, we designed a modulo-k counter, a 3-digit BCD counter, and integrated the Real-Time Clock (RTC) present on the board. Module 1 resulted in successful implementation and display of various digital circuits on the DE1-SoC board,

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demonstrating proficiency in Verilog HDL.

Section 1: Combinatorial Circuits

Submodule 1: Simple Switch-LED Mapping Create a foundational design illustrating the mapping of switches to LEDs. Showcase the entire project creation process, from HDL design to pin assignment and physical device programming.

Submodule 2: 4-Bit 2-to-1 Multiplexer Develop a 4-bit-wide 2-to-1 multiplexer leveraging the first eight switches as inputs, with SW9 serving as the selector. Map the output to the initial four LEDs.

Submodule 3: 2-Bit 3-to-1 Multiplexer Apply principles of code reusability to transform the 4-bit 2-to-1 multiplexer design into a 2-bit-wide 3-to-1 multiplexer. Map the selected output to the first two LEDs.

Submodule 4: 2-Input Selector for 7-Segment Display Craft a 2-input selector tailored for 7-segment displays, utilizing SW0-1. Configure the display content to showcase characters 'd', 'E', '1', or a blank space.

Section 2: Sequential Circuits

Submodule 1: Modulo-k Counter Implement a versatile modulo-k counter, configurable with variable parameters for different modulos and bit widths. Validate functionality using a clock sourced from a user push button (PB1), with the counter value displayed on LED0-7 and rollover indication on LED9.

Submodule 2: 3-Digit BCD Counter Develop a 3-digit Binary-Coded Decimal (BCD) counter building upon the modulo-k counter. Conduct a timing-aware analysis to ensure robust performance and closure of the design.

Submodule 3: Real-Time Clock (RTC) Transform the 3-digit BCD counter into a real-time clock capable of counting to 60 minutes with a precision of 10ms. Integrate user-friendly features such as presetting minute values using SW0-7 and PB1 and implementing a stop function with PB0.

4.1.2 Fmax of the design

For Lab5Part1: Fig.9.1.1 shows the Fmax recorded in SmartTime

| Fmax | Restricted Fmax | Clock Name |
|------------|-----------------|------------|
| 454.75 MHz | 454.75 MHz | clock |

For Lab5Part2: Fig.9.1.2 shows the Fmax recorded in SmartTime

| Fmax | Restricted Fmax | Clock Name |
|------------|-----------------|-------------|
| 271.52 MHz | 271.52 MHz | Clk_50 |
| 438.2MHz | 438.2MHz | CLK_DIVIDER |
| 447.03Mhz | 447.03Mhz | TENS |
| 447.23MHz | 447.23MHz | ONES |

For Lab5Part3: Fig.9.1.3 shows the Fmax recorded in SmartTime

| Fmax | Restricted Fmax | Clock Name |
|-------------|-----------------|------------|
| 281.934 MHz | 281.934 MHz | Clk_50 |
| 300.48Mhz | 300.48Mhz | Clk_100 |

4.1.3 FPGA Utilization

For Lab1Part1: Fig.9.1.4 shows the resource utilization.

| | |
|-----------------|---------------------|
| Total LE | 1 / 32,070 (< 1 %) |
| Total Registers | 0 |

For Lab1Part2: Fig.9.1.5 shows the resource utilization.

| | |
|-----------------|---------------------|
| Total LE | 3 / 32,070 (< 1 %) |
| Total Registers | 0 |

For Lab1Part3: Fig.9.1.6 shows the resource utilization.

| | |
|-----------------|---------------------|
| Total LE | 3 / 32,070 (< 1 %) |
| Total Registers | 0 |

For Lab1Part4: Fig.9.1.7 shows the resource utilization.

| | |
|-----------------|---------------------|
| Total LE | 1 / 32,070 (< 1 %) |
| Total Registers | 0 |

For Lab5Part1: Fig.9.1.8 shows the resource utilization.

| | |
|-----------------|---------------------|
| Total LE | 7 / 32,070 (< 1 %) |
| Total Registers | 14 |

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For Lab5Part2: Fig.9.1.9 shows the resource utilization.

| | |
|------------------------|----------------------|
| Total LE | 41 / 32,070 (< 1 %) |
| Total Registers | 65 |

For Lab5Part3: Fig.9.1.10 shows the resource utilization.

| | |
|------------------------|-----------------------|
| Total LE | 258 / 32,070 (< 1 %) |
| Total Registers | 59 |

4.1.4 Board Behavior

For Lab1Part1, the circuit functionality was tested by toggling the switches and observing the corresponding LED responses.

For Lab1Part2, the LEDs reflect the values of the selector and the output of the four-bit wide 2-to-1 multiplexer. Toggling switches SW3-0 and SW7-4 will influence the LED displays, demonstrating the dynamic response of the circuit to input changes.

ForLab1Part3, toggling the switches will dynamically influence the LED displays, providing a visual representation of the two-bit wide 3-to-1 multiplexer's functionality.

For Lab1Part4, the 7-segment decoder module processes a two-bit input (c1c0) to generate seven outputs, enabling the display of characters (d,E,1) on a 7-segment display.

For Lab5Part1, Key 0 resets the counter, Key 1 increments it manually, and upon reaching the mod value, the rollover LED lights up. Subsequent key presses reset the counter, turning off the rollover LED for a fresh counting cycle.

For Lab5Part2, the board observations for this setup involve utilizing three modulo counters, interconnected through the rollover counter serving as the clock source. The status of this BCD counter is then visually displayed on the 7-segment display.

ForLab5Part3, a 3-digit BCD counter is implemented into a real-time clock capable of counting to 60 minutes with a precision of 10ms (1/100th of second) which is displayed on a 7-segment display. Onboard timer is measured against a stopwatch timer.

4.2 Module 2

4.2.1 Description

Part 1: Audio CODEC Development

Submodule 1.1: Integration of Audio CODEC into Higher-Level System

The primary objective in this submodule is to seamlessly integrate the audio CODEC into the higher-level system. This involves configuring internal circuitry to receive inputs from the audio CODEC, transmitting them back without substantive signal processing. The complexity lies in managing the dual channels (left and right) of the audio codec, ensuring synchronization with the CODEC's readiness signals (read_ready & write_ready), and subsequently programming the DE1-SoC board. A practical application involves connecting a microphone to the MIC_IN audio jack and a speaker to the LINE_OUT audio jack for testing the successful integration.

Submodule 1.2: Implementation of Averaging FIR Filter

The focus of the second submodule is on implementing an averaging Finite Impulse Response (FIR) filter within the circuitry to effectively reduce noise from the incoming audio signal. This phase involves creating instances of the FIR filter for both left and right channels, addressing frequency discrepancies between the system clock and the audio codec clock, and ensuring data integrity by adhering to CODEC's signals (read ready & write ready). After compiling the project and programming the DE1-SoC board, testing includes speaking into the connected microphone to verify a noticeable reduction in noise, affirming the successful incorporation of the filter circuitry.

Part 2: Embedded Software Development using C

Submodule 2.1: Maximum Value in List of Integers

In the first submodule, a C program is created to read a predefined list of eight integers from memory and determine the integer with the maximum value. This program demonstrates the integration of C programming with memory management and arithmetic operations.

Submodule 2.2: Real-Time Clock (RTC) Interface

The focus of the second submodule is on writing a C program to interface with a real-time clock (RTC) and

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display the current time on a 7-segment display. The program updates the time every 10 milliseconds and configures the timer, keys, and display to achieve this functionality.

Submodule 2.3: Scrolling Message Display

The final submodule in embedded software development involves creating a program that displays the text "DE1-SOC" on a 7-segment display. The program manages the sequence of characters to create a scrolling message effect. It ensures continuous updating of the display, creating the illusion of a leftward-scrolling message. The display ceases its animation upon detection of any key press among the four available keys on the board.

4.2.2 Fmax of the design

Figure 9.2.2 shows the Fmax of the design part-1.1.

| Fmax | Restricted Fmax | Clock Name |
|------------|-----------------|------------|
| 257.33 MHz | 257.33 MHz | CLOCK_50 |

Figure 9.2.5 shows the Fmax of the design part-1.2.

| Fmax | Restricted Fmax | Clock Name |
|------------|-----------------|------------|
| 130.96 MHz | 130.96 MHz | CLOCK_50 |

4.2.3 FPGA Utilization

Figure 9.2.1 shows the utilization of the design part-1.1.

| | |
|-----------|-------------------|
| Total LE | 217/ 32070 < (1%) |
| Total I/O | 11/457 |

Figure 9.2.4 shows the utilization of the design part-1.2.

| | |
|----------|-------------------|
| Total LE | 340/ 32070 < (1%) |
|----------|-------------------|

| | |
|-----------|--------|
| Total I/O | 11/457 |
|-----------|--------|

4.2.4 Board Behavior

Figure 9.2.1 shows successful compilation and figure 9.2.3 shows successful programming of the board.

On flashing the board, audio can be taken in through LINE-IN connected to a MIC and the same audio along with some noise can be heard on LINE-OUT which is connected to a speaker.

Figure 9.2.4 shows successful compilation and figure 9.2.6 shows programming success. On flashing the board, audio in which is taken in through a MIC which is connected to LINE-IN is passed through a filter which operates at 48KHz and gives a noise removed audio output through LINE-OUT which is connected to a speaker.

Figure 9.2.7 shows the successful execution of part-2.1 which is printing the largest number on the console of Intel FPGA Monitor Program.

Figure 9.2.8, 9.2.9 and 9.2.10 shows the successful expected behavior of HPS private timer displaying MM:SS on 7-segment display and pausing the clock on press of any push buttons KEY0-KEY3.

Figure 9.2.11 and figure 9.2.12 shows successful expected behavior of scrolling "dE1-SOC" message on the 7-segment display continuously.

NOTE: Due to board not available after the module4-demo, these images are captured on cpulator which emulates the exact behavior of ARMV-7 cortex A9 hard processor on DE1-SOC system.

4.3 Module 3

4.3.1 Description

The FPGA-HPS connection relies on two key components: the HPS-to-FPGA Bridge and the Lightweight HPS-to-FPGA Bridge. The Lightweight HPS-to-FPGA Bridge interfaces with peripherals using the Parallel Input Output (PIO) module, establishing a

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direct link to the lightweight master bridge of the HPS system. This bridge controls the memory device managing the behavior of DE1-SOC board LEDs.

After obtaining the HDL file from the Qsys module, the DE1-SOC board loads the hardware configuration. To validate the system, a C project is created, leveraging predefined addresses in Qsys modules. Cross-compilation, using arm-linux-gnueabihf as the compiler, produces an executable transferred to the DE1-SOC board via scp.

The outcome is dynamic LED behavior, confirming successful HPS-FPGA integration and validating hardware and software configurations. This blinking pattern serves as a tangible indicator of system efficacy.

4.3.2 Fmax of the design

Fig. 9.3.4 shows the Fmax recorded at Slow 1200mV 85C Model.

| Fmax | Restricted Fmax | Clock Name |
|-------------|-----------------|---------------------|
| 63.45 MHz | 63.45 MHz | Altera_reserved_tck |
| 81.95 Mhz | 81.95 Mhz | Clock_50_1 |
| 1184.83 MHz | 717.36 Mhz | Soc_System_pll |

4.3.3 FPGA Utilization

Fig.9.3.5. shows the resource utilization.

| | |
|-----------------|----------------------|
| Total LE | 2,215 / 32,070 (7 %) |
| Total pins | 368 / 457 (81 %) |
| Total registers | 3318 |

4.3.4 Board Behavior

Figure 9.3.1 shows the default Qsys file and figure 9.3.2, 9.2.3 shows the parallel IO addition to the design connected to HSP and exported as conduit for interfacing with fabric.

Figure 9.3.6 shows the board behavior after the executable is copied into the HPS linux through secure

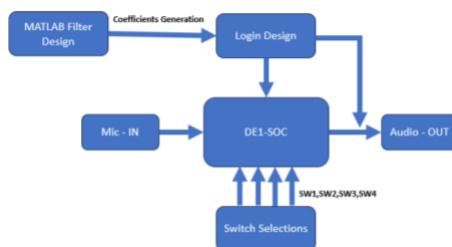
copy and executed. The board shows the LEDs turning on in a sequential pattern.

4.4 Module 4

4.4.1 Description

Module4 is an implementation of audio filters Unfiltered, Low-Pass, High-Pass, Band-Pass, within the existing audio codec RTL implementation given as a starter kit on project-3 module-2. These filters will be switched between the audio input and output based on the user input switch selection using SW0-SW2.

4.4.2 System Block Diagram



4.4.3 Implementation and Validation

Figure 9.4.1, 9.4.2, 9.4.3 shows the filter design using MATLAB by selecting certain parameters such as type of filtering, stop frequency and pass frequency and generated co-efficients for each type of filter.

These co-efficients are plugged into the filter and routed between the audio codec output and audio codec loopback input. Figure 9.4.4 shows the RTL viewer of the same and figure 9.4.5 shows the RTL viewer of a low pass filter.

Figure 9.4.6 shows the logic utilization of the implementation.

| | |
|------------------|----------------------|
| Total LE | 5164 / 32,070 (16 %) |
| Total pins | 17 / 457 (4 %) |
| Total registers | 10475 |
| Total DSP Blocks | 87/87 (100%) |

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| | |
|-------------------------|----------------|
| Total block memory bits | 12288/ 4065280 |
|-------------------------|----------------|

4.4.4 Validation and Results

Each filter is verified by using specific frequency tones which lie both in and out of cut-off frequency zones. Also the testing is carried out using audio sweep tune of 20Hz to 20KHz tone which showed the results of each implemented filter. Low-pass filter showed successful cut-off of higher frequencies whereas the other filters didn't behave as expected but allowed the audio tones out beyond the cut-off levels.

4 List of Project Deliverables

1. Hardware implementation files for each module
2. Software modules zipped for each module
3. Executive Summary
4. Documentation
5. Module Test Results Screenshots
6. Demonstration of each module

5 Lessons Learnt

- Using DSP Builder for Intel FPGA would have provided better filter design support and direct conversion of real-point and fixed-point coefficient formats.
- Project-3 Module2 could have been done better with identifying the sampling frequency from the codec properly.
- Use of cpulator emulator provided a great opportunity to emulate the entire DE1-SOC board which would have helped more if known earlier.
- Modelsim verification could have been better utilized by writing test bench files for bigger design verification.
- Utilize University FPGA program efficiently to look at existing references which gives a better idea of existing IP or implementations.
- Latches were added for the design of real-time clock due to mixing combinational and sequential logic, which could have been avoided.

6. Conclusions

The project involved a thorough exploration of FPGA development and embedded systems, covering fundamental aspects like combinatorial and sequential circuits, as well as advanced topics such as the integration of audio CODEC and FIR filtering. The utilization of C for embedded software development showcased its versatility, tackling diverse tasks like determining maximum values and implementing a scrolling message display. The crucial phase of connecting FPGA with HPS demanded careful validation through the execution of C projects. The dynamic LED behavior, following a predefined pattern, served as a tangible confirmation of the successful integration of HPS and FPGA. In summary, this project provided a comprehensive understanding of the intricate relationship between hardware and software in embedded systems, contributing to a well-rounded skill set in FPGA development.

6 References

1. Project guide files
2. <https://www.mathworks.com/help/signal/ug/introduction-to-filter-designer.html>
3. <https://www.rfwireless-world.com/source-code/VERILOG/Low-pass-FIR-filter-verilog-code.html>
4. <https://cpulator.01xz.net>

7 Project Team

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9 Appendix

9.1 Appendix for Module-1 Test Results

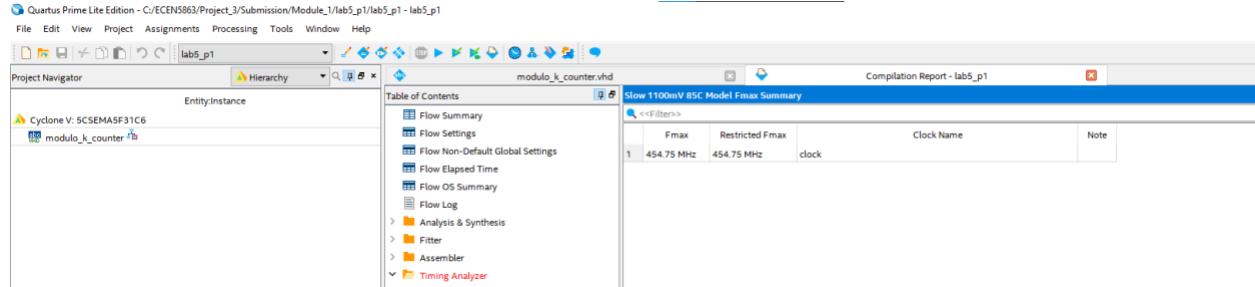


Fig 9.1.1: Fmax for Lab5Part1

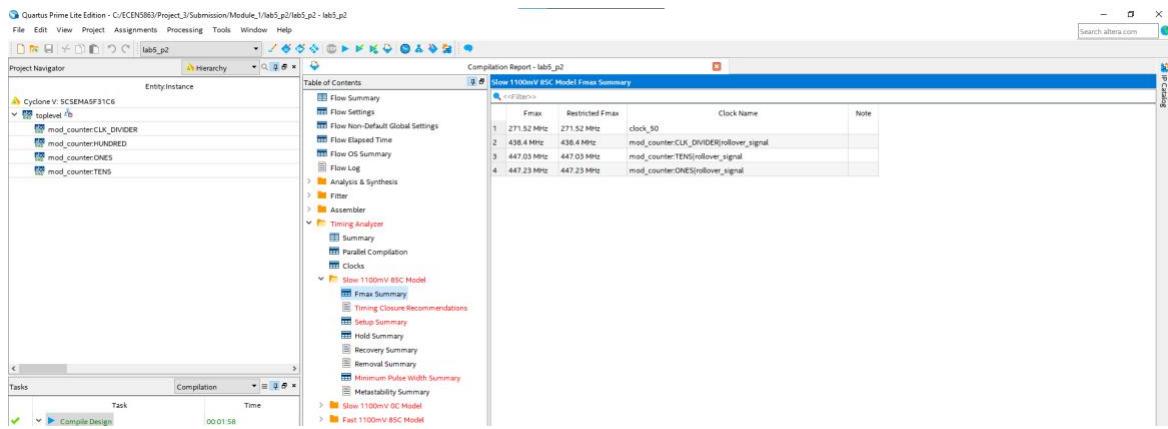


Fig 9.1.2: Fmax for Lab5Part2

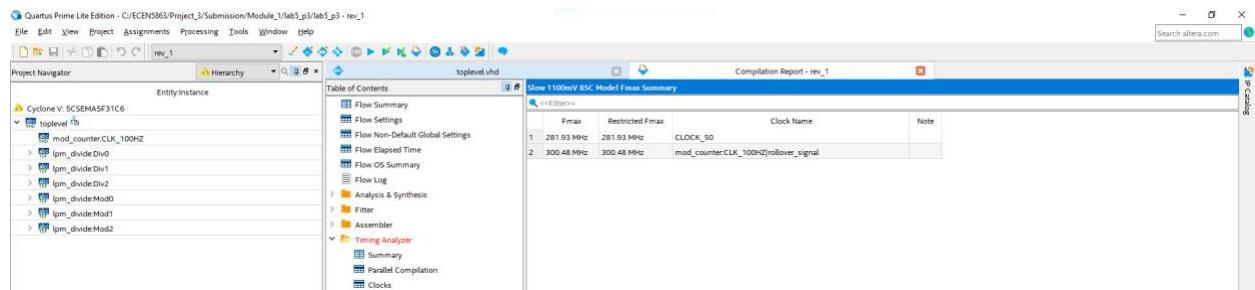


Fig 9.1.3: Fmax for Lab5Part3

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Fig 9.1.4: Resource Utilization for Lab1Part1

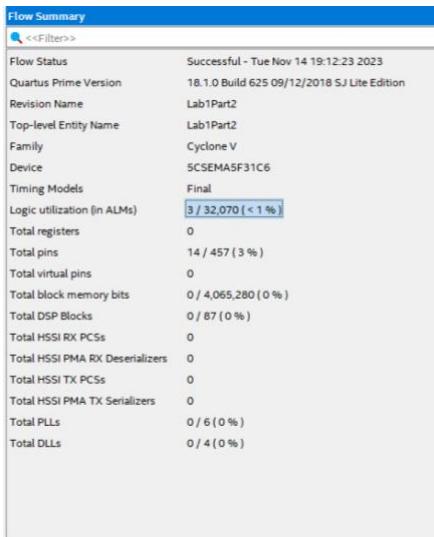


Fig 9.1.5: Resource Utilization for Lab1Part2

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| Flow Summary | |
|---------------------------------|---|
| <<Filter>> | |
| Flow Status | Successful - Tue Nov 14 19:07:19 2023 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | Lab1Part3 |
| Top-level Entity Name | Lab1Part3 |
| Family | Cyclone V |
| Device | 5CSEMA5F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 3 / 32,070 (< 1 %) |
| Total registers | 0 |
| Total pins | 10 / 457 (2 %) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 (0 %) |
| Total DSP Blocks | 0 / 87 (0 %) |
| Total HSSI RX PCSS | 0 |
| Total HSSI PMA RX Deserializers | 0 |
| Total HSSI TX PCSS | 0 |
| Total HSSI PMA TX Serializers | 0 |
| Total PLLs | 0 / 6 (0 %) |
| Total DLLs | 0 / 4 (0 %) |

Fig 9.1.6: Resource Utilization for Lab1Part3

| Flow Summary | |
|---------------------------------|---|
| <<Filter>> | |
| Flow Status | Successful - Tue Nov 14 19:37:31 2023 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | Lab1Part4 |
| Top-level Entity Name | Lab1Part4 |
| Family | Cyclone V |
| Device | 5CSEMA5F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 1 / 32,070 (< 1 %) |
| Total registers | 0 |
| Total pins | 9 / 457 (2 %) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 (0 %) |
| Total DSP Blocks | 0 / 87 (0 %) |
| Total HSSI RX PCSS | 0 |
| Total HSSI PMA RX Deserializers | 0 |
| Total HSSI TX PCSS | 0 |
| Total HSSI PMA TX Serializers | 0 |
| Total PLLs | 0 / 6 (0 %) |
| Total DLLs | 0 / 4 (0 %) |

Fig 9.1.7: Resource Utilization for Lab1Part4

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| Fitter Summary | |
|---------------------------------|---|
| <<Filter>> | |
| Filter Status | Successful - Thu Dec 14 11:31:54 2023 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | lab5_p1 |
| Top-level Entity Name | modulo_k_counter |
| Family | Cyclone V |
| Device | 5CSEMA5F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 7 / 32,070 (< 1 %) |
| Total registers | 14 |
| Total pins | 11 / 457 (2 %) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 (0 %) |
| Total RAM Blocks | 0 / 397 (0 %) |
| Total DSP Blocks | 0 / 87 (0 %) |
| Total HSSI RX PCSS | 0 |
| Total HSSI PMA RX Deserializers | 0 |
| Total HSSI TX PCSS | 0 |
| Total HSSI PMA TX Serializers | 0 |
| Total PLLs | 0 / 6 (0 %) |
| Total DLLs | 0 / 4 (0 %) |

Fig 9.1.8: Resource Utilization for Lab5Part1

| Fitter Summary | |
|---------------------------------|---|
| <<filter>> | |
| Filter Status | Successful - Thu Dec 14 12:10:20 2023 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | lab5_p2 |
| Top-level Entity Name | toplevel |
| Family | Cyclone V |
| Device | 5CSEMA5F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 41 / 32,070 (< 1 %) |
| Total registers | 65 |
| Total pins | 23 / 457 (5 %) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 (0 %) |
| Total RAM Blocks | 0 / 397 (0 %) |
| Total DSP Blocks | 0 / 87 (0 %) |
| Total HSSI RX PCSS | 0 |
| Total HSSI PMA RX Deserializers | 0 |
| Total HSSI TX PCSS | 0 |
| Total HSSI PMA TX Serializers | 0 |
| Total PLLs | 0 / 6 (0 %) |
| Total DLLs | 0 / 4 (0 %) |

Fig 9.1.9: Resource Utilization for Lab5Part2

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| Filter Summary | |
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| <>Filter>> | |
| Filter Status | Successful - Thu Dec 14 12:29:41 2023 |
| Quartus Prime Version | 18.1.0 Build 625 09/12/2018 SJ Lite Edition |
| Revision Name | rev_1 |
| Top-level Entity Name | toplevel |
| Family | Cyclone V |
| Device | 5CSEMA5F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 258 / 32,070 (< 1 %) |
| Total registers | 59 |
| Total pins | 53 / 457 (12 %) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 (0 %) |
| Total RAM Blocks | 0 / 397 (0 %) |
| Total DSP Blocks | 0 / 87 (0 %) |
| Total HSSI RX PCSS | 0 |
| Total HSSI PMA RX Deserializers | 0 |
| Total HSSI TX PCSS | 0 |
| Total HSSI PMA TX Serializers | 0 |
| Total PLLs | 0 / 6 (0 %) |
| Total DLLs | 0 / 4 (0 %) |

Fig 9.1.10: Resource Utilization for Lab5Part3

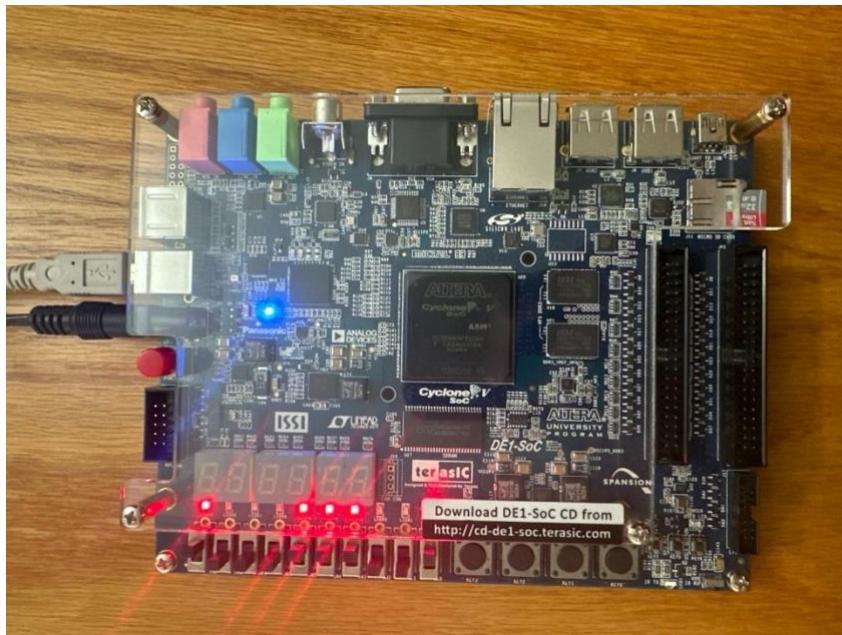


Fig 9.1.11: Lab1-Part1 LED-SW behavior

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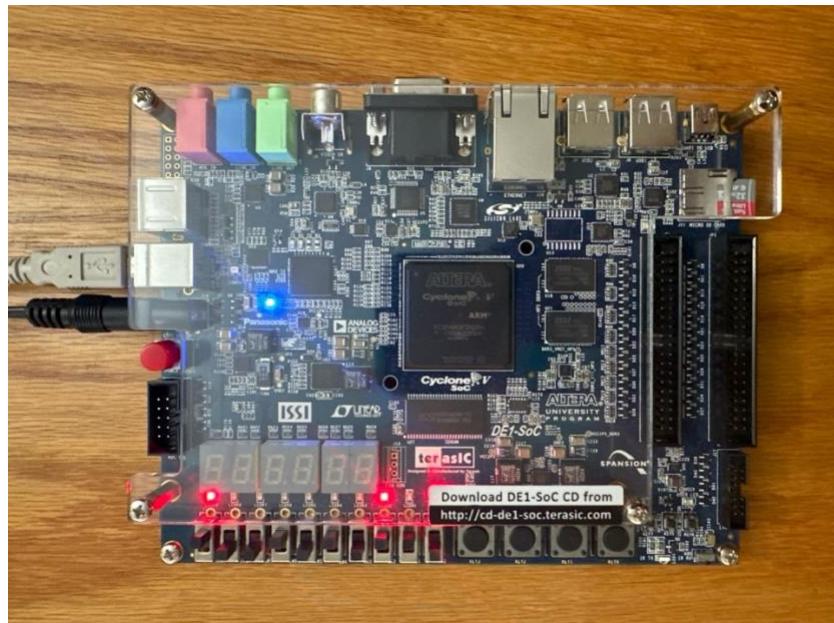


Fig 9.1.12: Lab1-Part2 MUX-Y (SW4-SW7) selected based on SW9-ON

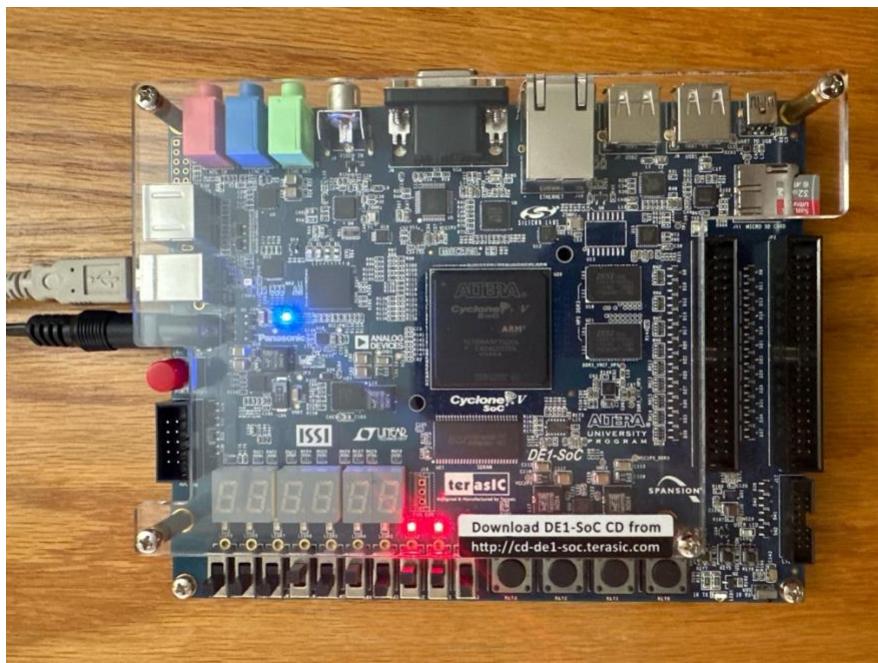


Fig 9.1.12: Lab1-Part2 MUX-X (SW0-SW3) selected based on SW9-OFF

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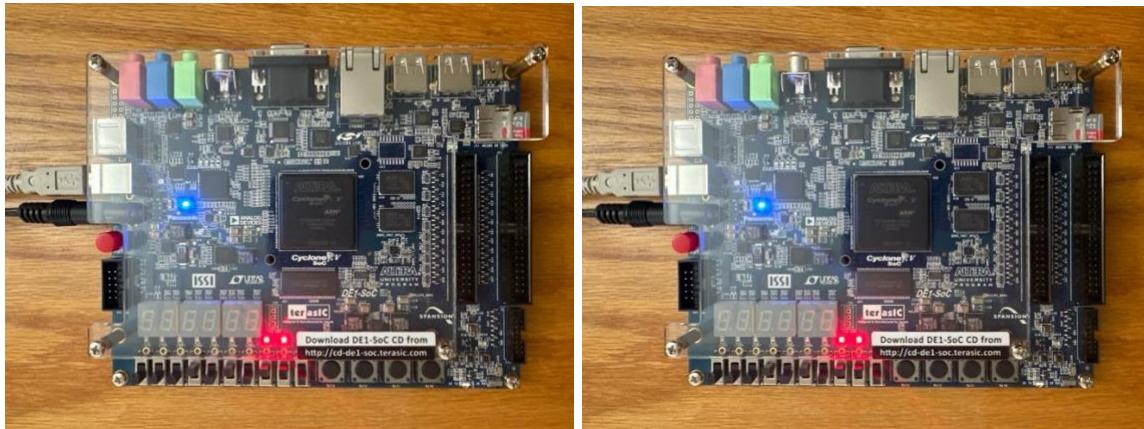


Fig 9.1.13: Lab1-Part3 MUX-U (SW0-SW1) selected based on SW9-8 (00)



Fig 9.1.14: Lab1-Part4 d,E,1 display on 7-segment based on MUX



Fig 9.1.15: Lab5-Part1 1-20 count display on LED0-LED7 on KEY1 press

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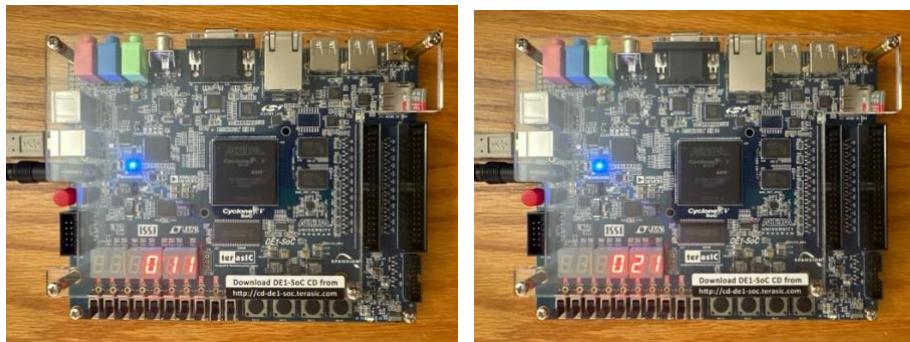


Fig 9.1.16: Lab5-Part2 BCD Counter display on 7-segment display from 0-999

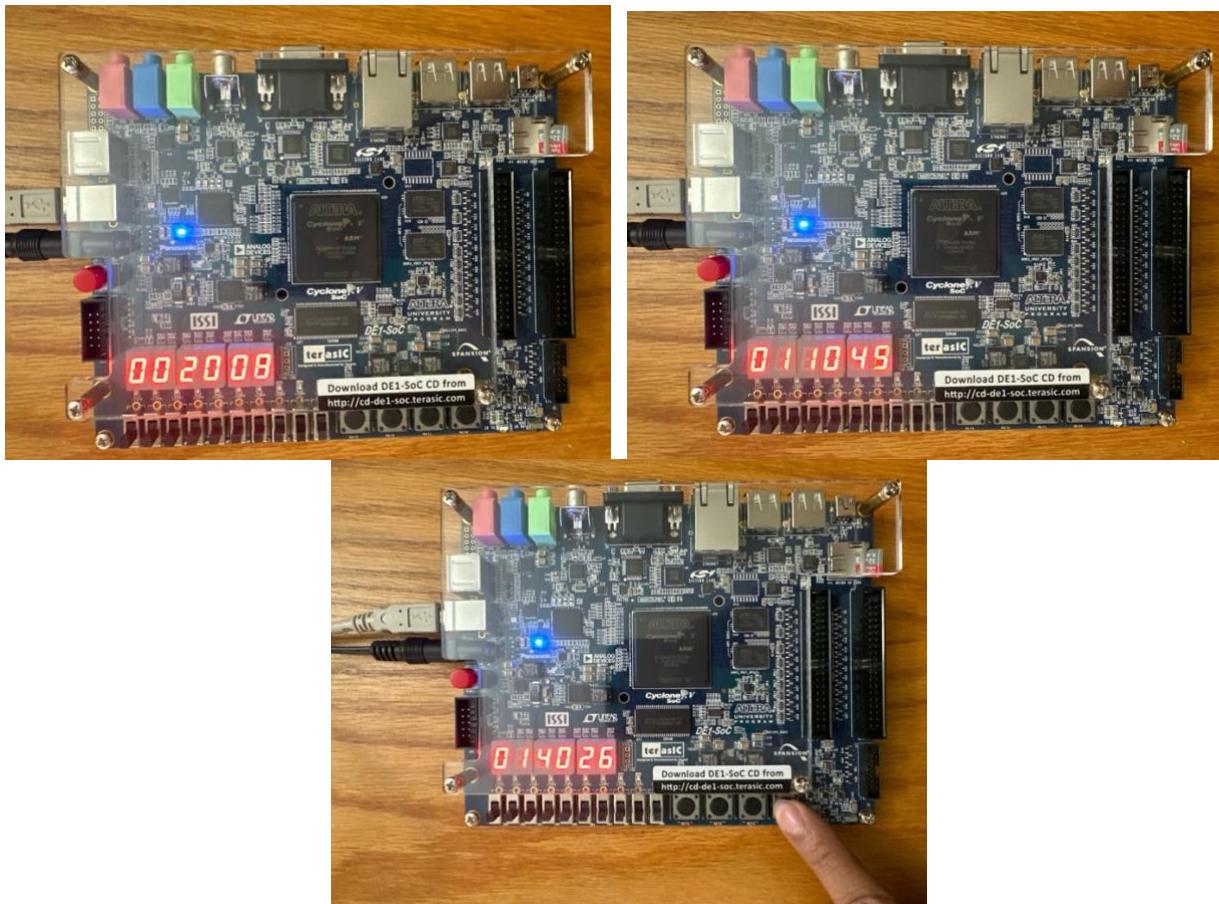


Fig 9.1.16: Lab5-Part3 Real Time Clock

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9.2 Appendix for Module-2 Test Results

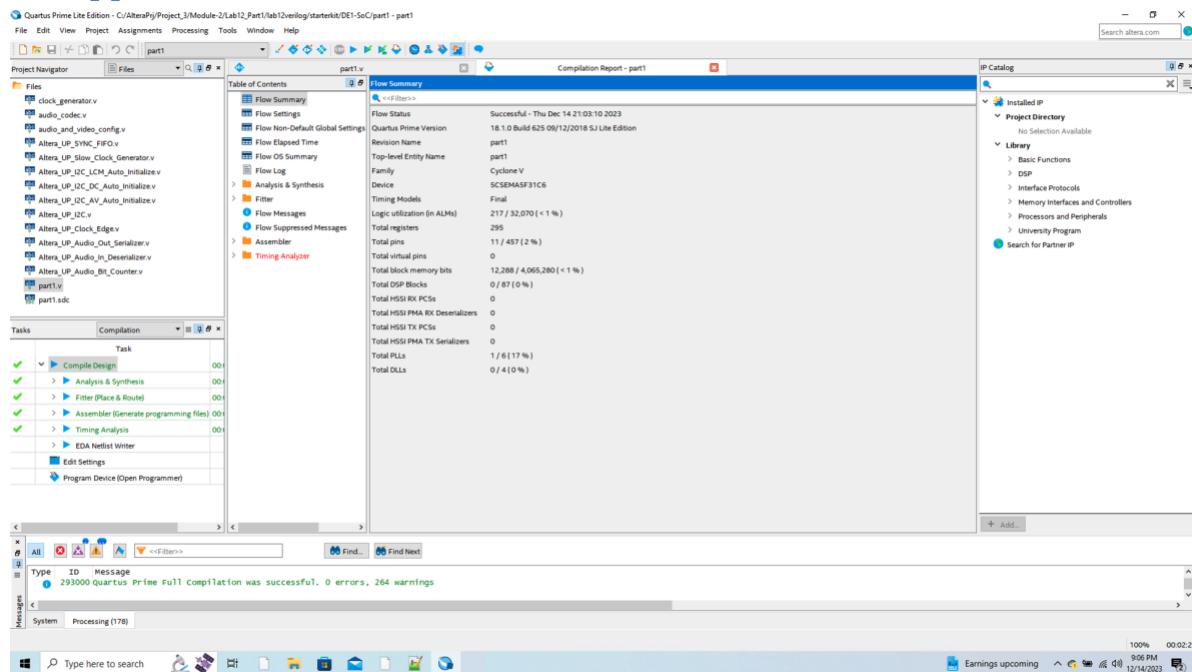


Fig:9.2.1: Resource Utilization for Lab12 Part-1

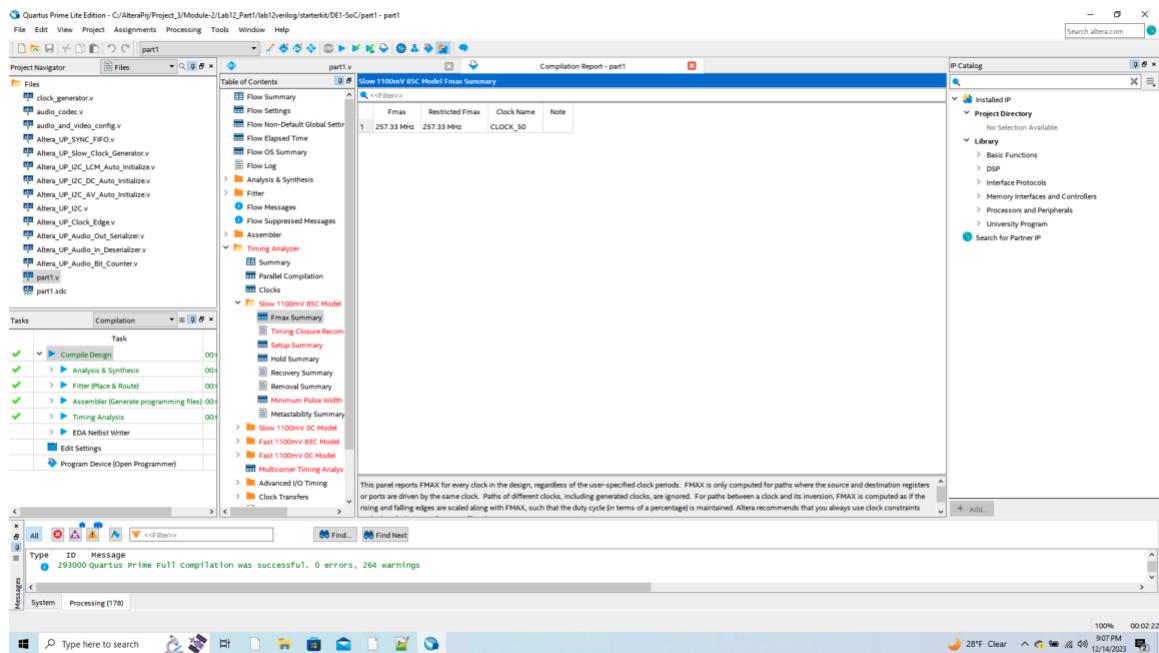


Fig:9.2.2: Fmax for Lab12 Part-1

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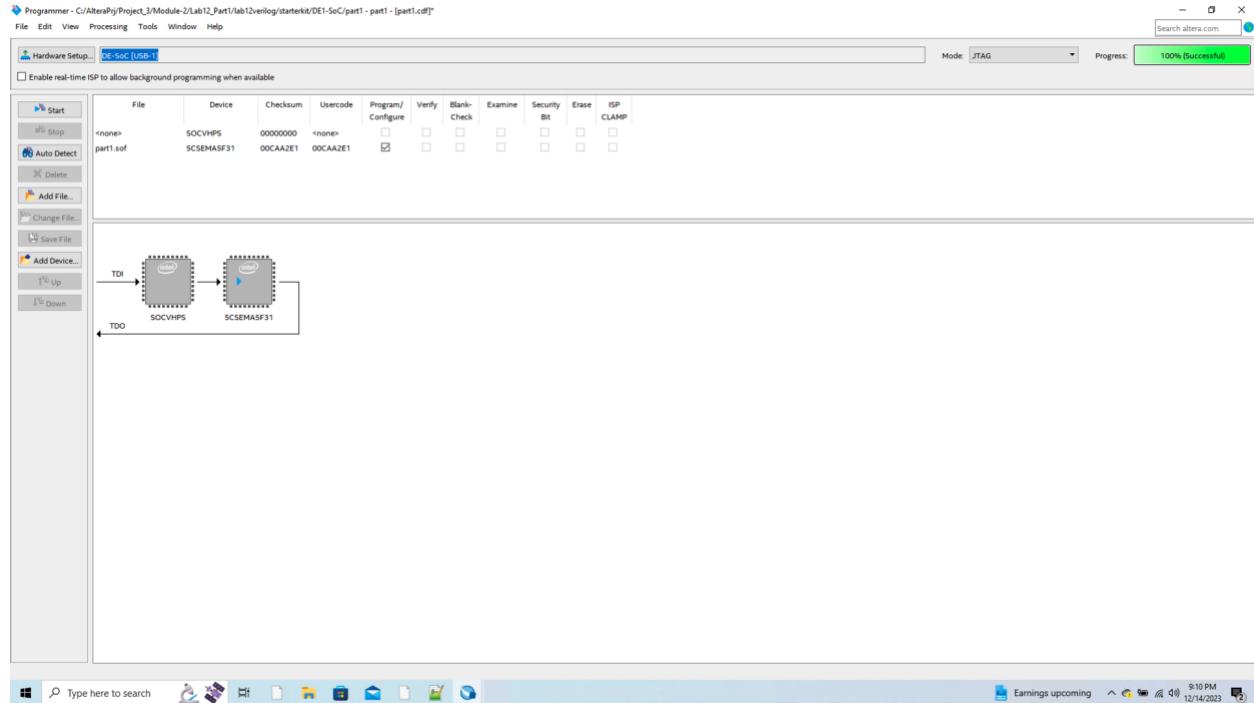


Fig 9.2.3: Programming success for Lab12 part-1

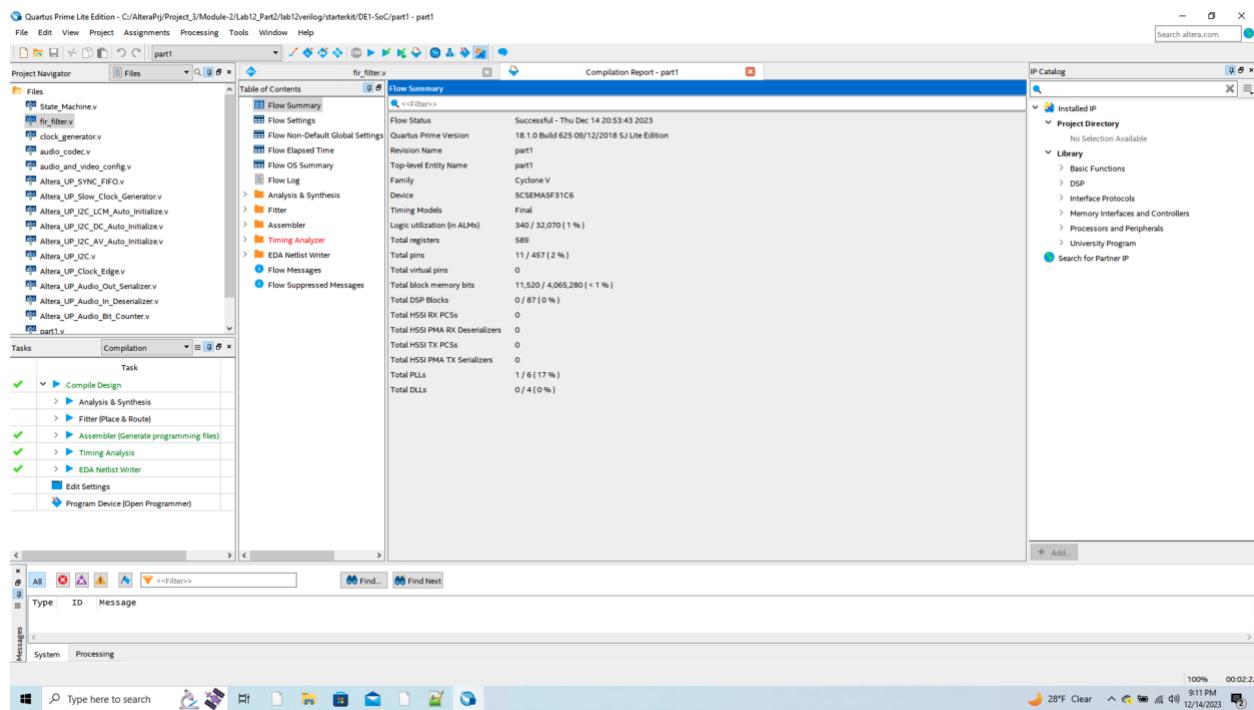


Fig 9.2.4: Resource Utilization for Lab12 Part-2

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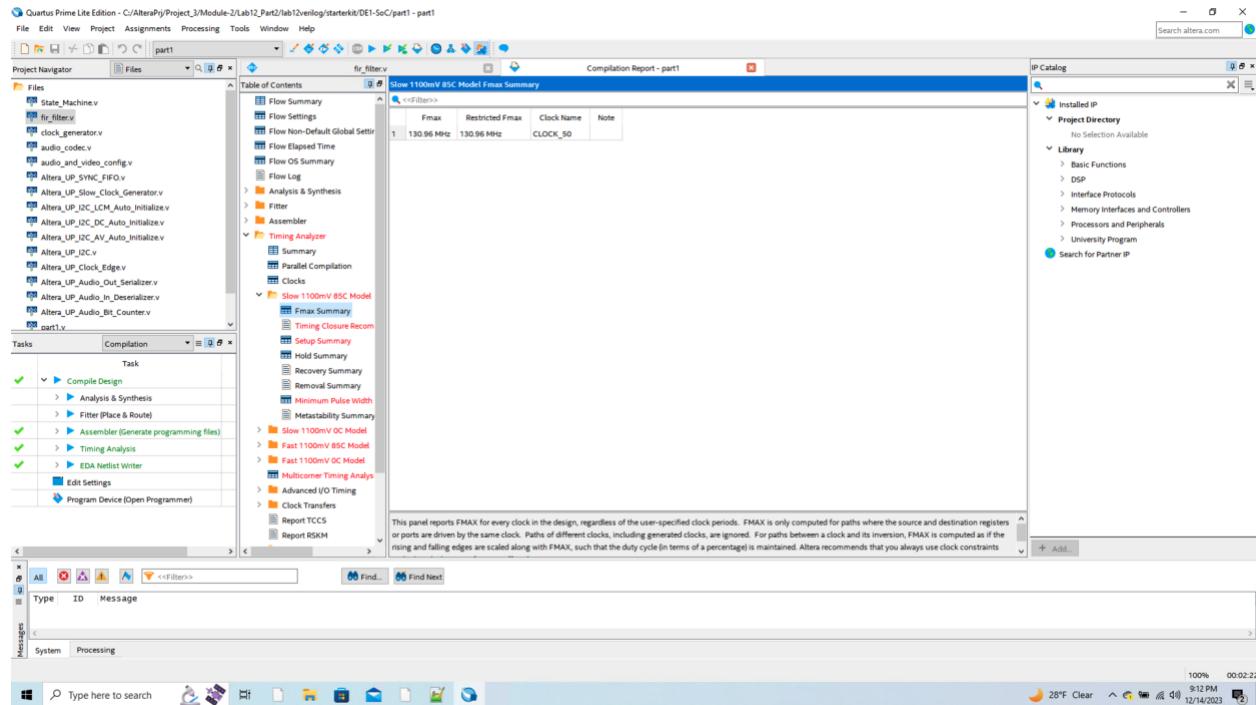


Fig 9.2.5: Fmax for Lab12 Part-2

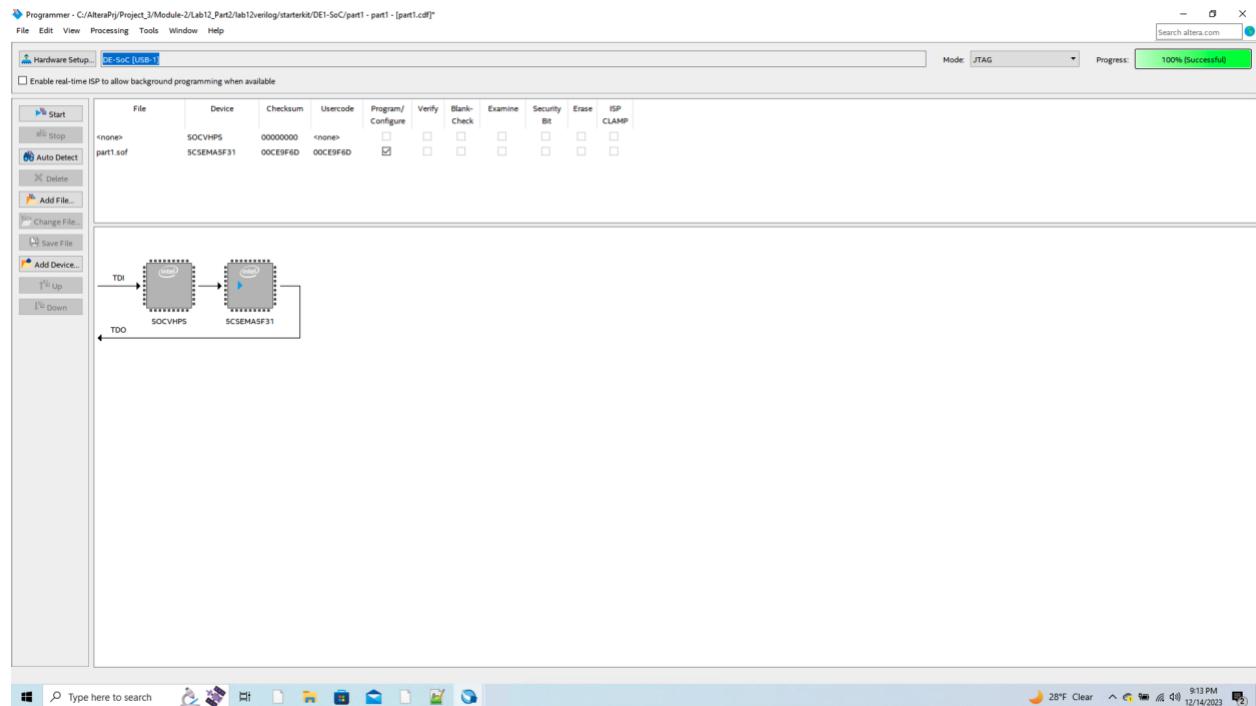


Fig 9.2.6: Programming success for Lab12 part-2

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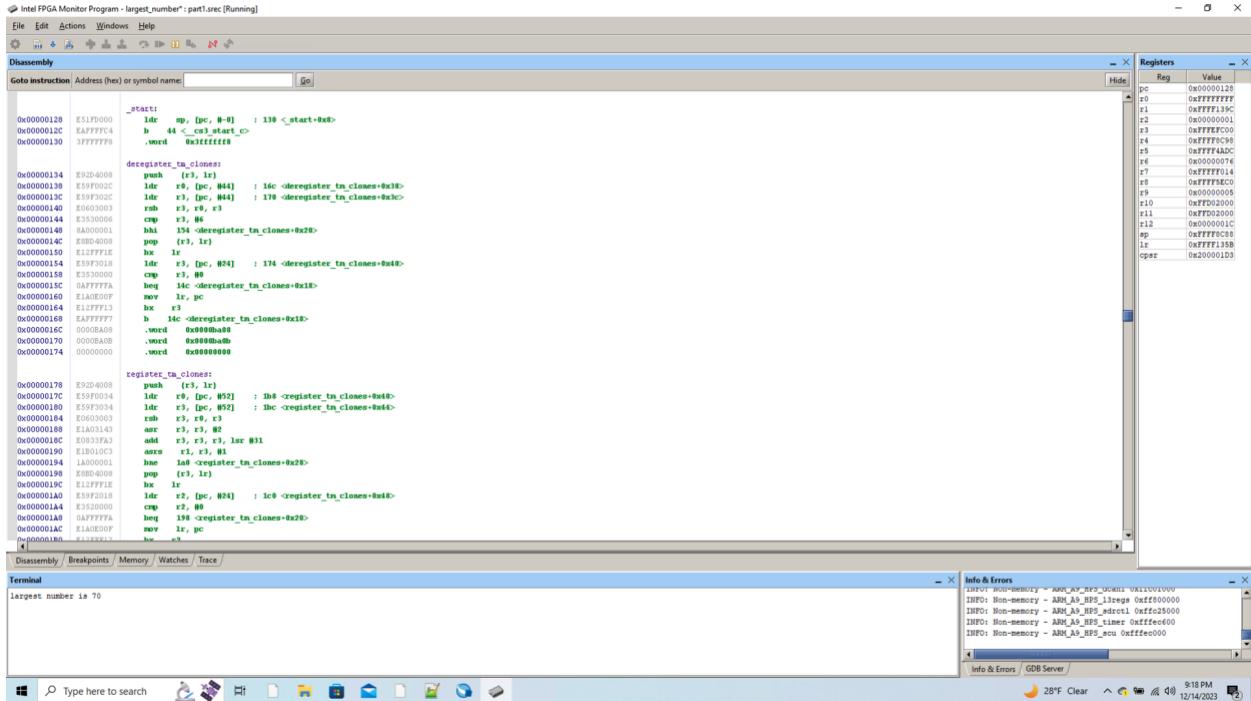


Fig 9.2.7: Successful execution of module2-part-3

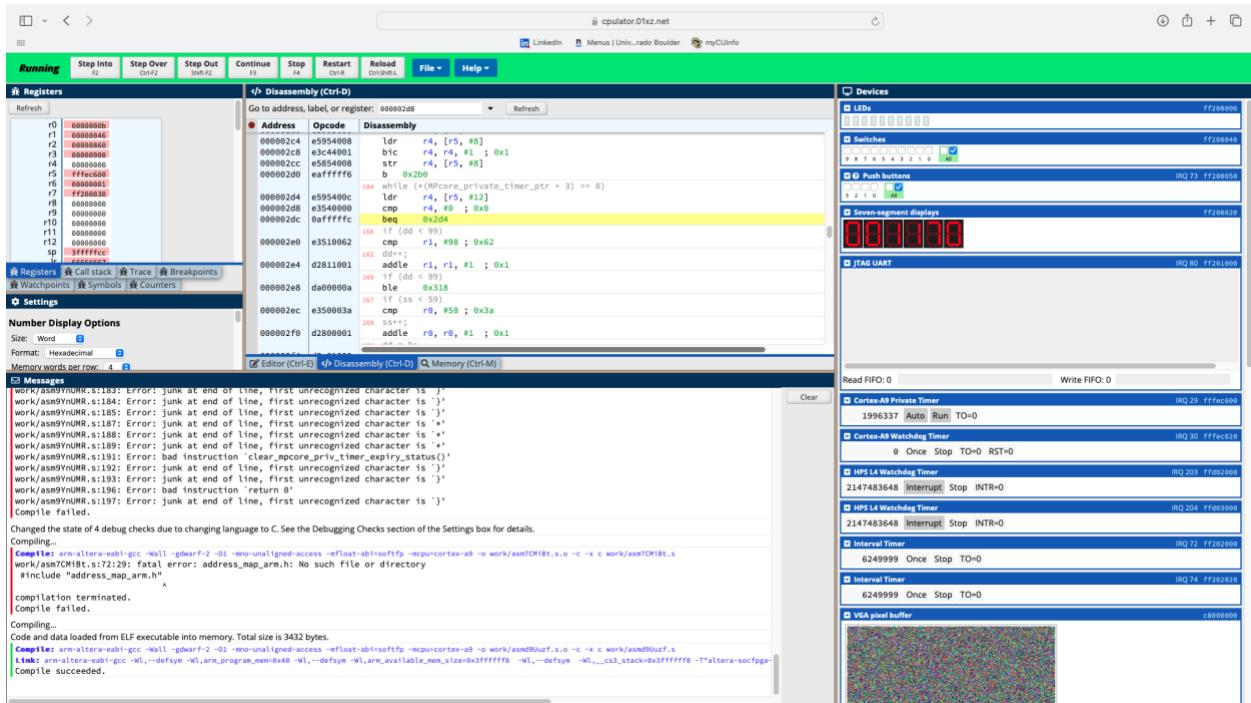


Fig 9.2.8: Successful execution of module2-part-4 running timer

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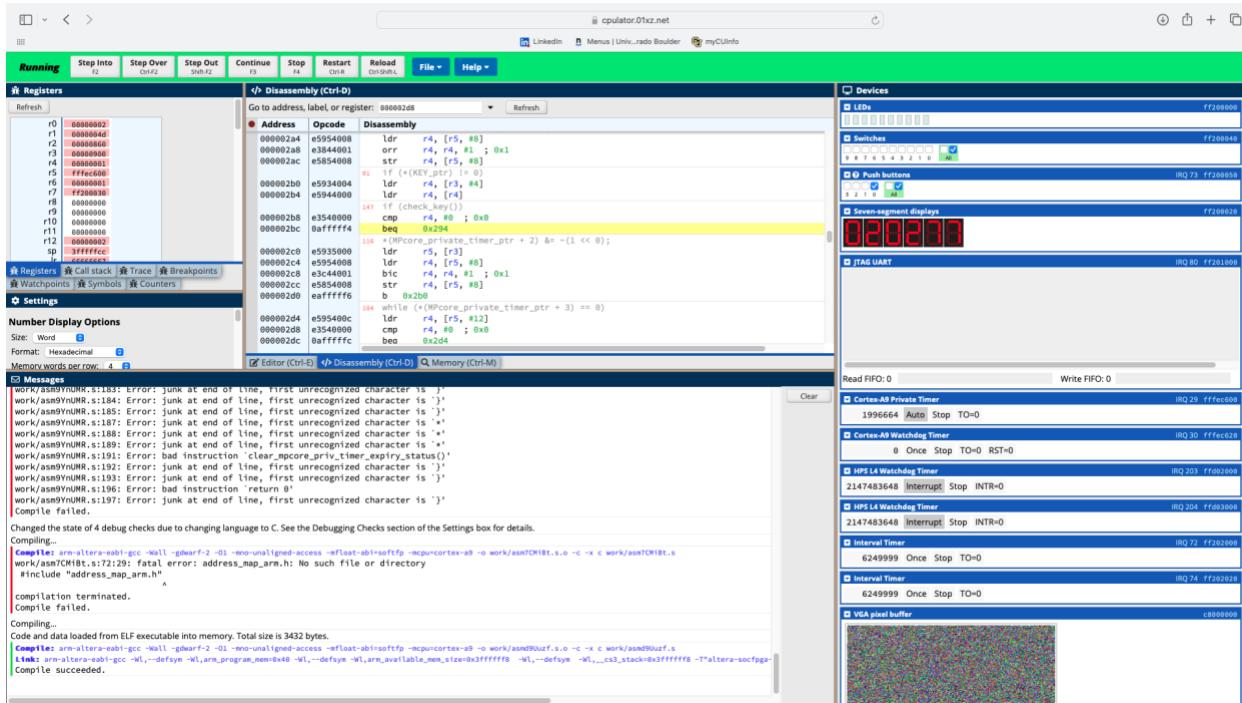


Fig 9.2.9: Successful execution of module2-part-4 running timer(push button pressed)

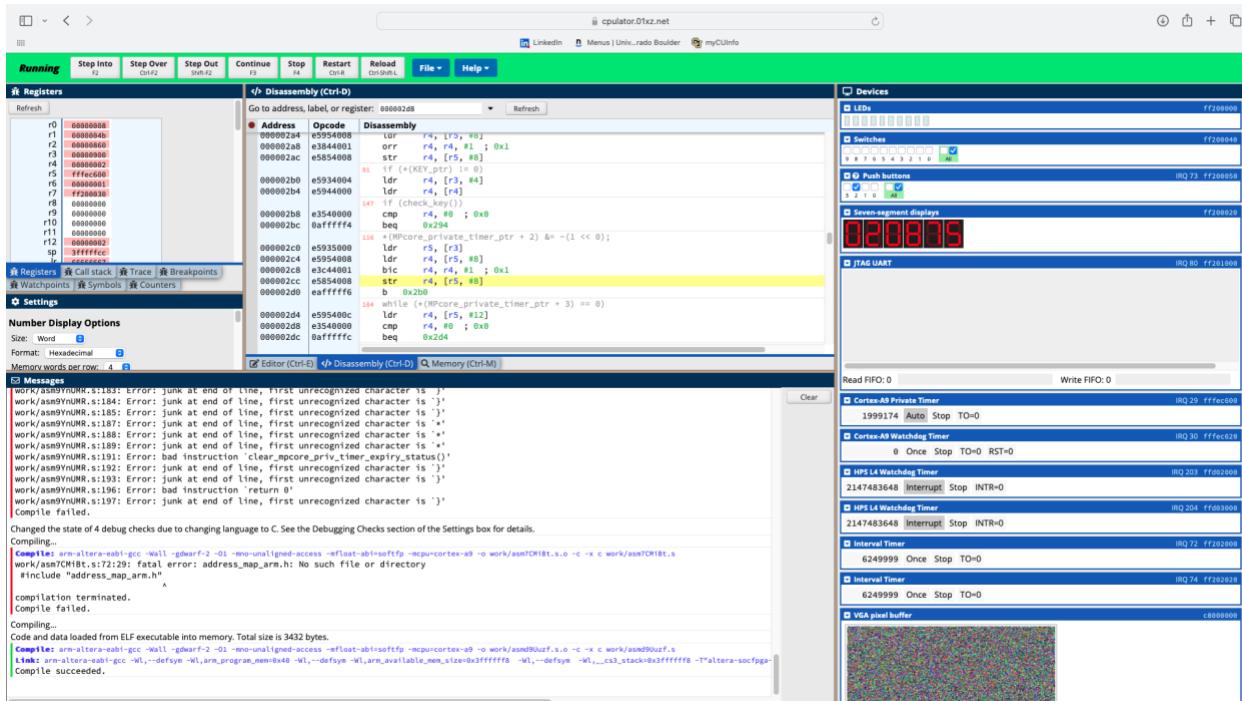


Fig 9.2.10: Successful execution of module2-part-4 running timer(2nd push button pressed)

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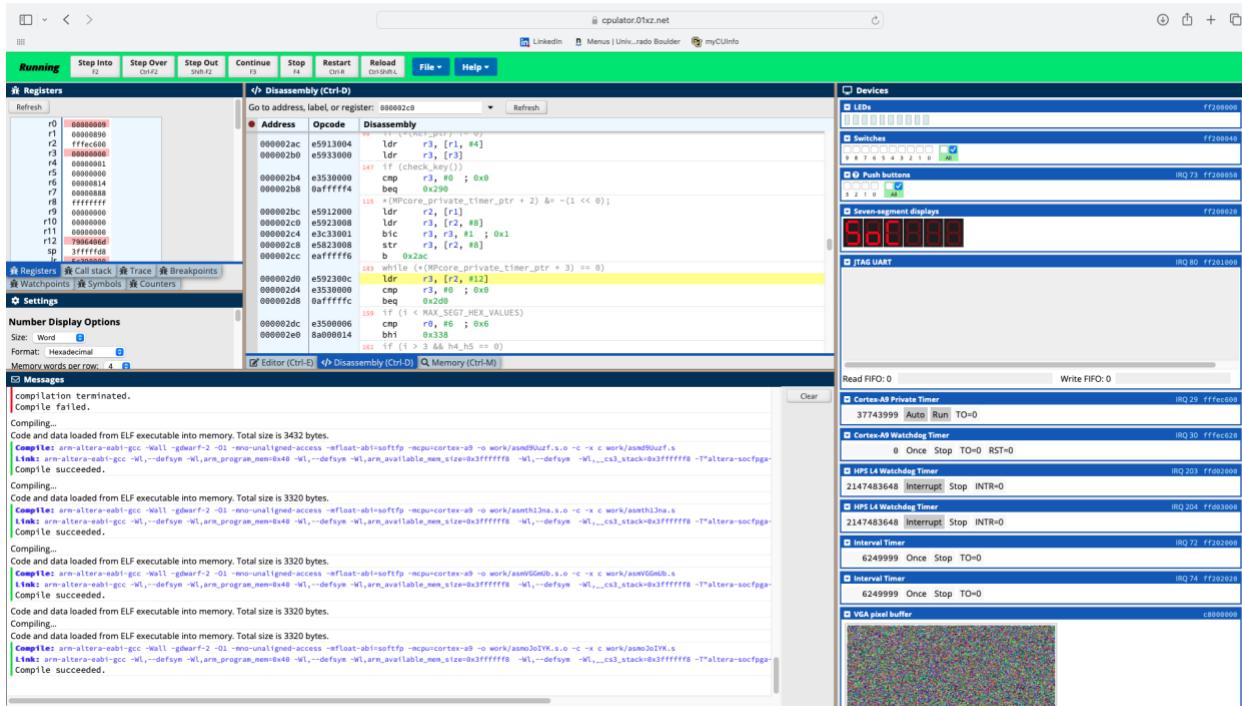


Fig 9.2.11: Successful execution of module2-part-5 showing scrolling message

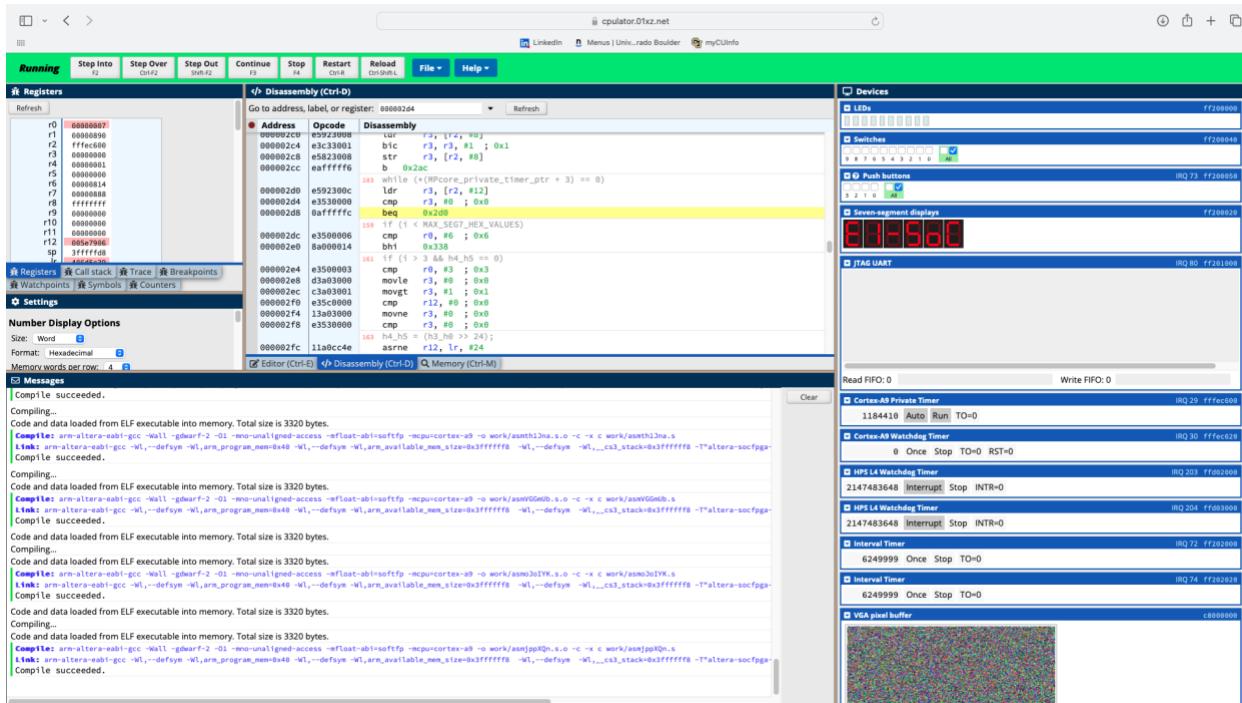


Fig 9.2.12: Successful execution of module2-part-5 showing scrolling message

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9.3 Appendix for Module-3 Test Results

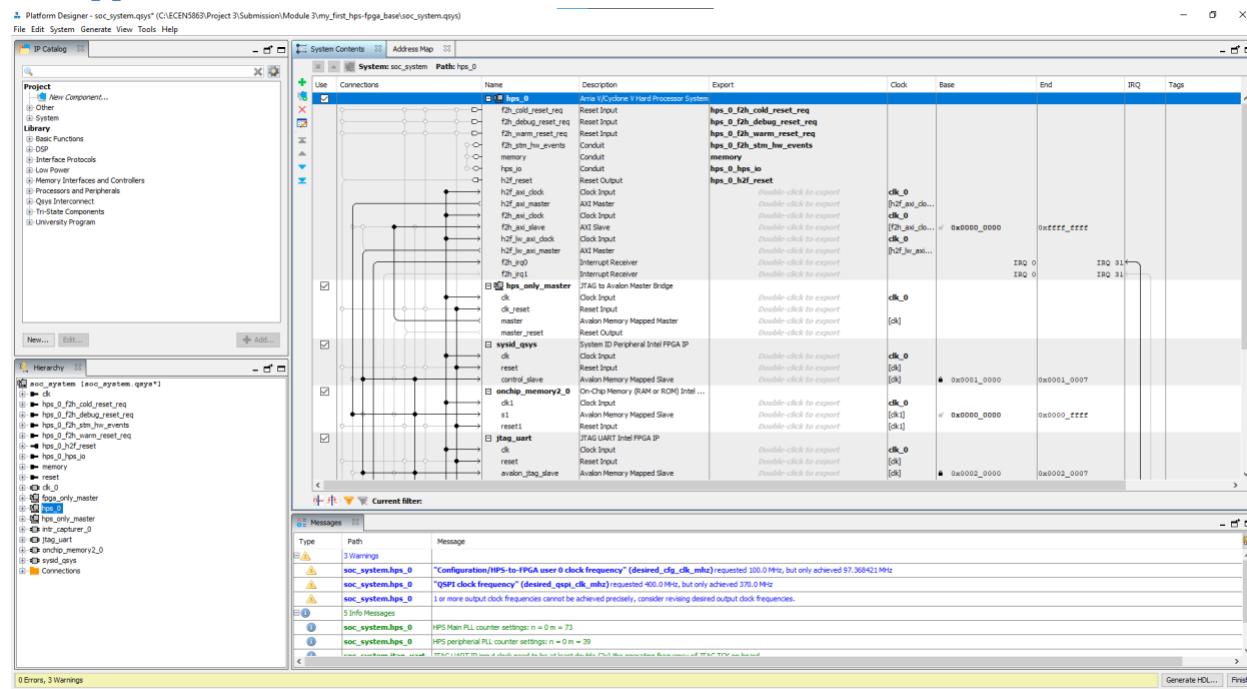


Fig 9.3.1 Qsys platform designer containing hardware peripheral integrations

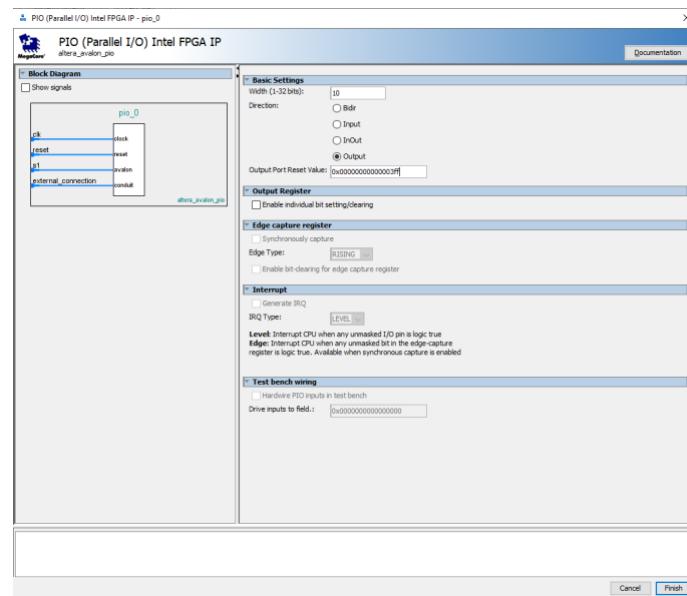


Fig 9.3.2 Setting for PIO IP

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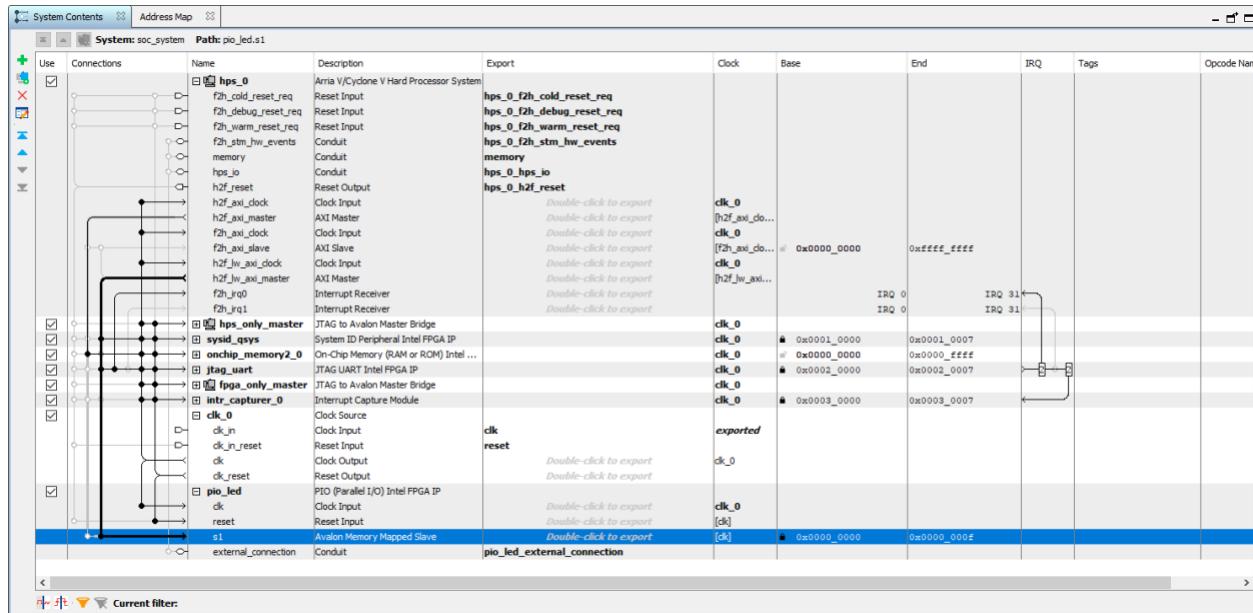


Fig 9.3.3 Qsys configuration after adding PIO slave and connecting the master bridge

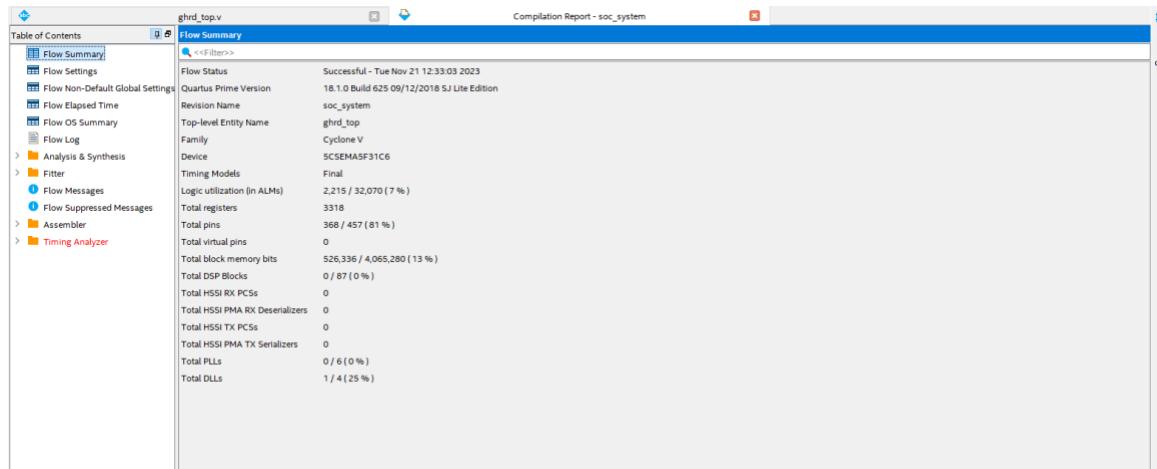


Fig 9.3.4 Compilation Report determining the resource utilization

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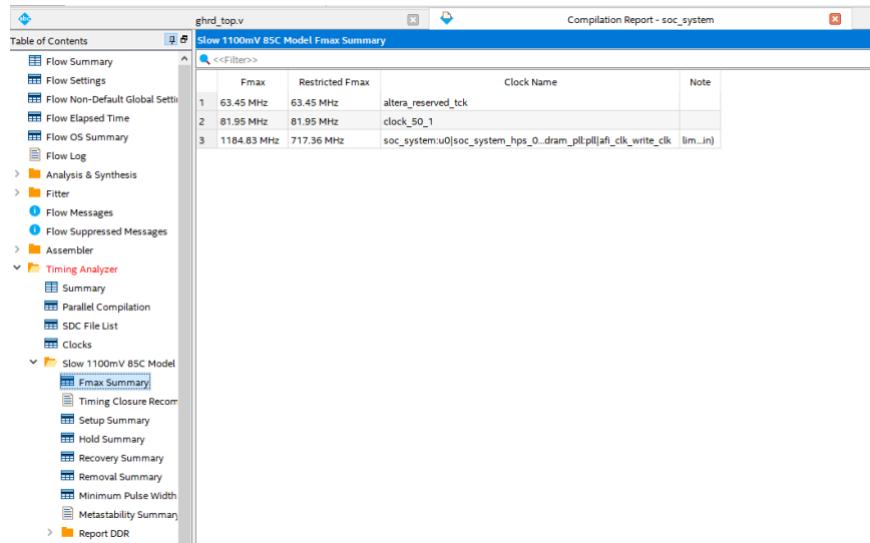


Fig 9.3.5 Fmax report

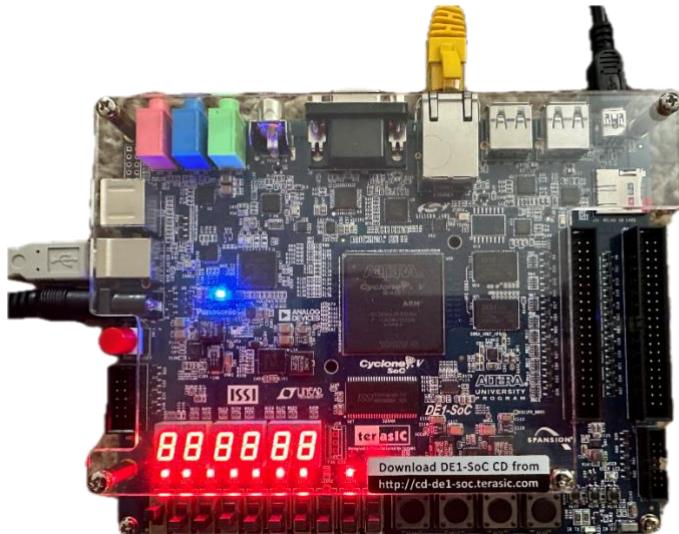


Fig 9.3.6 Board output after executing my_first_hps-fpga

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9.4 Appendix for Module-4 Test Results

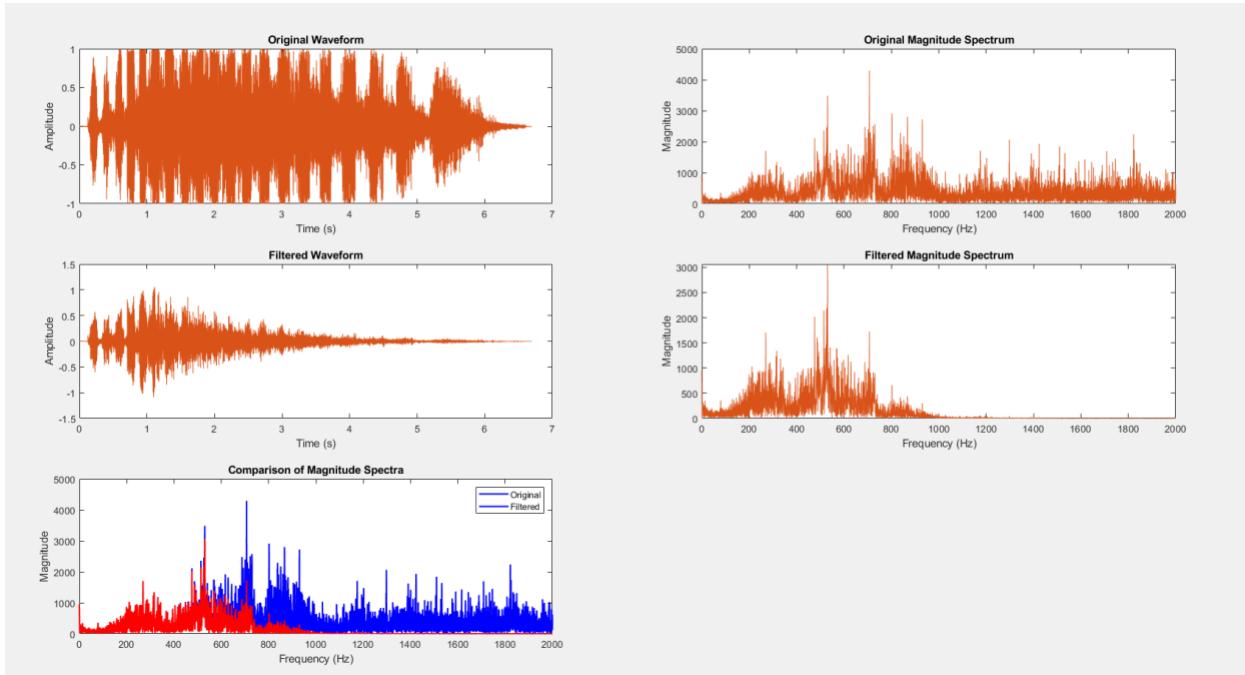


Figure 9.4.1 : Low Pass Filter Characteristics: Cutoff Frequency: 600Hz, Filter Order: 50 Filter Functionality: Permits frequencies below 600Hz. Attenuates frequencies beyond the cutoff.

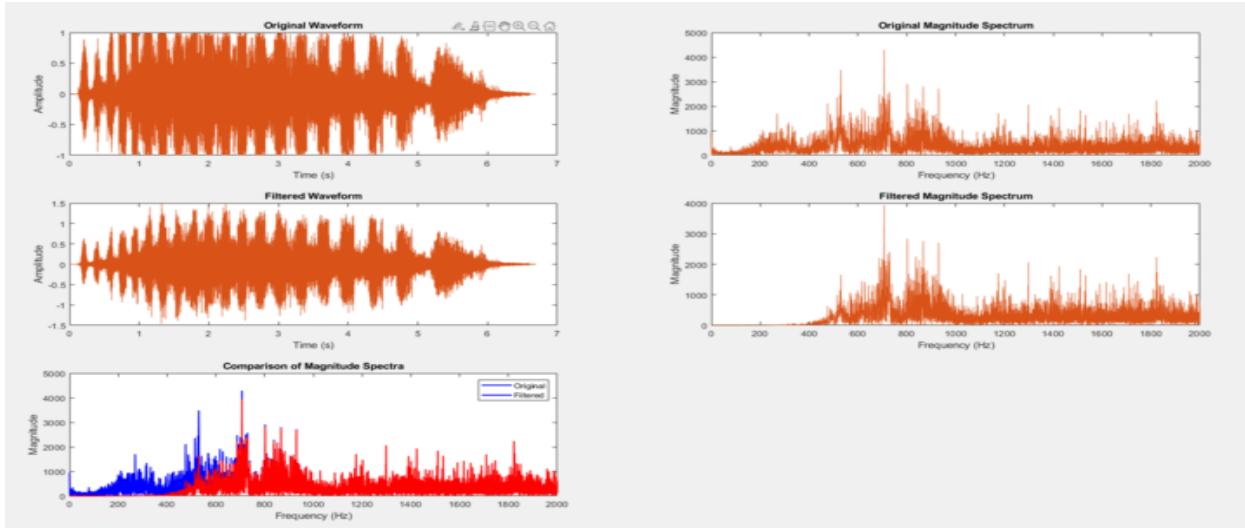


Figure 9.4.2 : High Pass Filter Characteristics: Cutoff Frequency: 600Hz, Filter Order: 50, Filter Functionality: Permits frequencies above 600Hz. Attenuates frequencies below the cutoff.

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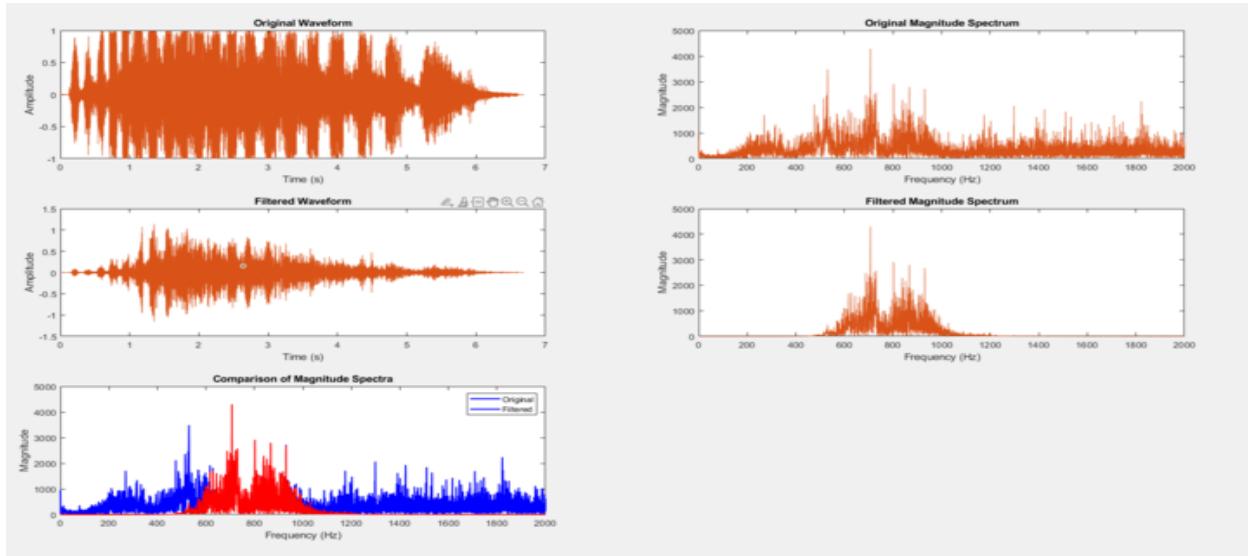


Figure 9.4.3: Band Pass Filter Characteristics: Cutoff Frequency1: 600Hz, Cutoff Frequency2: 1000Hz, Filter Order: 50 Filter Functionality: Permits frequencies below 600Hz. Attenuates frequencies beyond the cutoff.

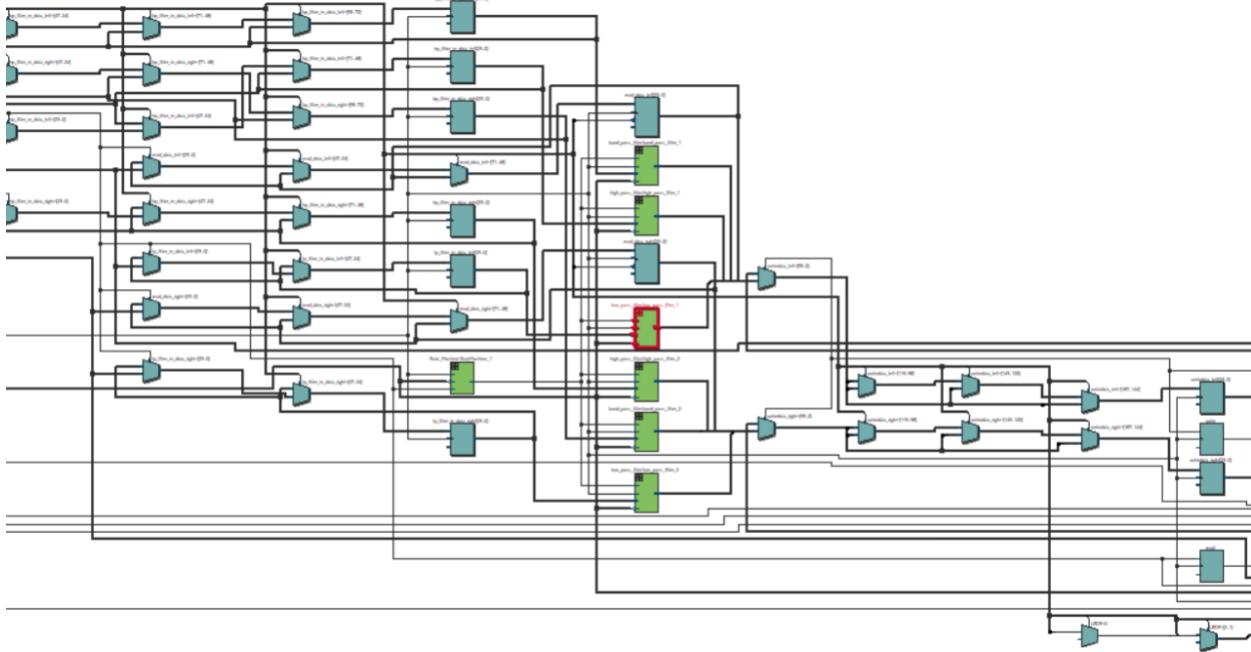


Figure 9.4.4: RTL Viewer of the designed interface between filters and codec

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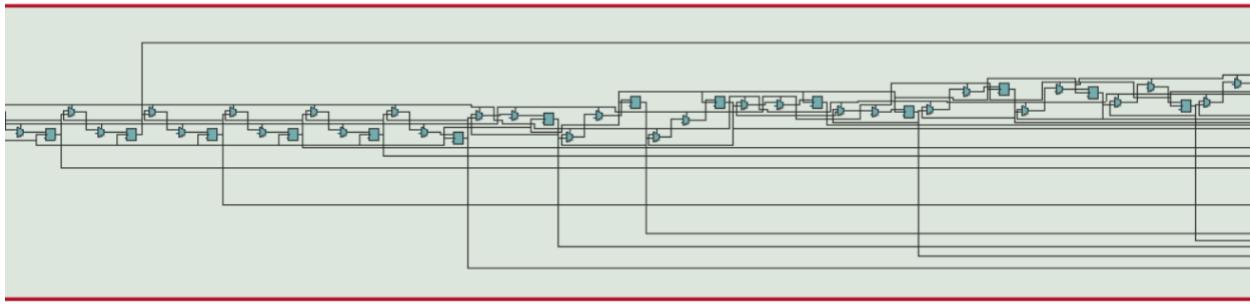


Figure 9.4.5: RTL Viewer of a low pass filter

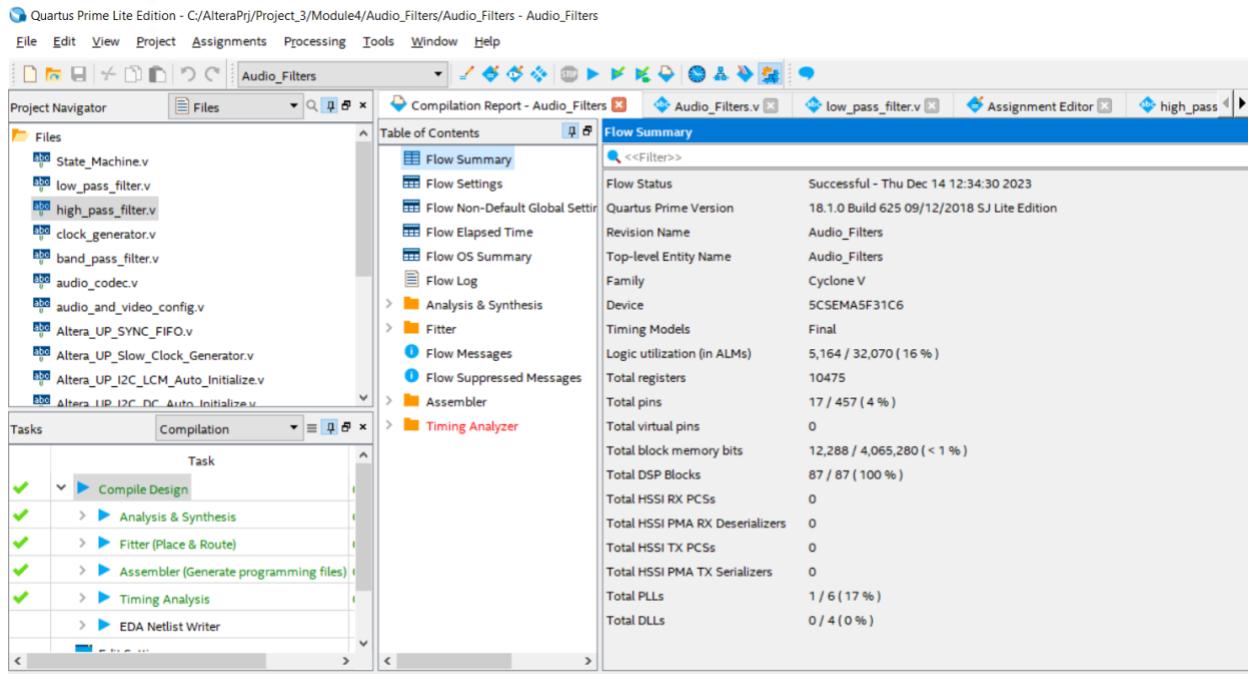


Figure 9.4.6: FPGA Utilization of the entire design

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