Analysis of Transmission Line Discontinuities using Time Domain Reflectometry

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***Abstract*—This paper presents a methodology to address the effects of return path discontinuities induced by slots in transmission lines and proposes a solution to mitigate them. By introducing additional capacitance through strategically positioned patches above slots in the transmission line, impedance stabilization is achieved. Through careful dimension selection, the transmission line exhibits consistent impedance characteristics, as demonstrated by Time Domain Reflectometry (TDR) responses. In high-frequency electronic systems, this method shows potential for improving signal integrity and reducing impedance variability.**

***Index Terms*—TDR, Time Domain Reflectometer, Return Path Discontinuity**

I. Introduction

As technological advancements drive clock frequencies higher and rise times faster, the design of transmission lines on PCBs becomes increasingly critical to maintaining signal integrity. Discontinuities such as vias and slots in the ground plane can significantly impact signal quality [4] [7]. Among these, return path discontinuity (RPD) arises when conduction current in the return path is non-uniform, leading to the flow of return current as displacement current to close the loop. In planar interconnects, slots on the return path are a common cause of RPD [5].

Time Domain Reflectometry (TDR) and its corresponding instrument, the Time Domain Reflectometer, serve as indispensable tools for characterizing passive transmission line traces on PCBs [1] [6]. By generating brief, fast-rising voltage pulses and measuring the reflected signal, TDR allows for the assessment of spatial properties such as characteristic impedance, time delay, and uniformity of transmission lines [2] [4] [8]. In this project, TDR is employed to investigate transmission line parameters and analyze the nature of discontinuities.

To experimentally study the effects of return path discontinuities, a 1-port TDR demonstration board for controlled impedances was constructed. By introducing a return path discontinuity in the form of a slot in the ground plane, the project aims to observe the resulting increase in transmission line impedance due to the discontinuity.

II. Theoretical Development

In practical design scenarios, it is often unavoidable to have discontinuities such as vias or slots in the return path, leading to impedance mismatches and potential signal reflections. To address this challenge, two options are considered:

A. Making the Discontinuity Transparent

One approach to address return path discontinuities is to make them transparent to the signal. If the geometry of the discontinuity can be reduced to less than 1/3 of the spatial extent of the signal edge, it is possible for the discontinuity to appear transparent to the signal [3]. The spatial extent of a signal edge is defined as the product of the signal speed (in inches/nanosecond) and the rise time of the signal (in nanoseconds). Therefore, the spatial edge is a length typically measured in inches. For instance, consider a FR4 PCB with a dielectric constant of 4. According to the Rule of Thumb, the signal speed is approximately 6 inches/nanosecond. Assuming a rise time of 1 nanosecond, the spatial extent of the signal edge would be 6 inches. Consequently, for this signal, any discontinuity greater than two inches would be noticeable. This approach underscores the importance of carefully managing the dimensions of discontinuities relative to the signal characteristics to ensure minimal impact on signal integrity.

B. Additional Capacitance

As previously discussed, the introduction of a return path discontinuity in the design results in added inductance in the return path, thereby increasing the characteristic impedance of the line. To mitigate this increase in impedance, extra capacitance can be incorporated into the transmission line. The formula for the capacitance of a parallel plate capacitor is:

$$C = \frac{A \times \epsilon}{d} \tag{1}$$

where, C = Capacitance of the parallel plates,
A = Area of the plates of the capacitor,
ϵ = Permittivity of the material,
d = Distance between the parallel plates of the capacitor.

From the above formula, it is evident that if the Area of the parallel plate capacitor is increased, its capacitance increases. Extending this logic to the transmission line, the width of the transmission line accounts for the area. This concept extends to transmission lines, where the width of the line corresponds to the area. By enlarging the width of the transmission line at the specified location, capacitance is increased, thereby reducing the overall characteristic impedance of the transmission line.

III. Project Flow

The Project flow is be given as follows in Fig 1:

Fig. 1. Project Flow of the Experiment

Each step in the project is explained as follows:

1) Simulation: Utilize Ansys HFSS to simulate transmission lines with desired impedance and acquire design parameters.
2) Board Design: Employ Altium Designer to design the PCB, incorporating parameters obtained from the simulation for transmission lines. Additionally, obtain 1-Port Measurements on the designed board through VNA.
3) TDR Measurements: Use Keysight ADS to import s1p files obtained from 1 port measurements, plot, and analyze Time Domain Reflectometry (TDR) data for the measured results.
4) Reverse engineer to compare and analyze simulated results, observing details closely.
5) Compare the plots for Measured and Simulated Data.
6) Verify the best design and measurement practices.

IV. Experimental Setup

For this experiment, the most prevalent transmission line impedance values were selected: $25\,\Omega$, $50\,\Omega$, and $75\,\Omega$. Initially, a microstrip structure was crafted for a $25\,\Omega$ transmission line, followed by the introduction of a slot in the return path. Several critical design parameters were meticulously considered and outlined below. The slot dimensions were computed based on the criterion that for the discontinuity to be detectable, it should be at least 1/3 of the spatial extent.

Size of Slot:

$$
\begin{aligned}
&\text{Length of the line (assumed)} && = 4 \text{ inches} \\
&\text{Speed of the signal} && = \frac{11.8}{\sqrt{4.4}} \\
& && = 5.625 \text{ in/nsec} \\
&\text{Rise Time} && = 0.05\text{nsec} \\
&\text{Spacial Extent of a signal} && = 5.625 * 0.05\text{inches} \\
& && = 0.28125 \text{ inches} \\
&\text{Size of discontinuity} && >= \frac{0.28125}{3}\text{inches} \\
& && >= 0.09375 \text{ mm} \\
& && >= 2.381 \text{ mm}
\end{aligned}
$$

Consequently, the minimum slot parameters should be 2.381 mm for the discontinuity to be discernible, hence the slot dimensions were rounded off to 3 mm.

To counteract the introduced discontinuity, supplementary capacitance was incorporated through a patch. An Optimetric sweep on the width of the patch was conducted to obtain a flat impedance profile and from there, the patch parameters were determined.

TABLE I
Analysis Setup for HFSS Design

Parameters	Values
Solution Frequency	Single
Frequency	20 GHz
Maximum Number of Passes	30
Maximum Delta S	0.02
Do Lambda Refinement	Yes
Maximum Refinement Per Pass	30%

TABLE II
Sweep Parameters and Values

Sweep Parameters	Values
Sweep Type	Interpolating
Type	Linear Step
Start Frequency	20 MHz
Step Frequency	20 MHz
Stop Frequency	20 GHz

By aligning the results with the impedance of the $25\,\Omega$ transmission line, the length and width of the patch were determined. This procedure was replicated for all transmission line impedance values and the design characteristics for the three impedances $25\,\Omega$, $50\,\Omega$, and $75\,\Omega$ were obtained. Fig 2 shows the transmission line parameters obtained from the above simulation.

Parameters	Variable Names used in HFSS	Evaluated values for 25 Ω Transmission line	Evaluated values for 50 Ω Transmission line	Evaluated values for 75 Ω Transmission line
Length of the Board	Length_Board	4 inches	4 inches	4 inches
Width of the Board	Width_Board	840 mil	290 mil	120 mil
Width of the Microstrip line	Microstrip_W	42 mil	14.5 mil	6 mil
Thickness of the signal trace	Microstrip_Thickness	0.035 mm	0.035 mm	0.035 mm
Thickness of the dielectric	Dielectric_Thickness	8.28 mil	8.28 mil	8.28 mil
Width of the slot	Gap_W	3 mm	3 mm	2 mm
Length of the slot	Gap_L	3 mm	3 mm	2 mm
Thickness of the ground plane	Layer2_Thickness	0.6 mil	0.6 mil	0.6 mil
Width of the patch	Patch_L	4.5 mm	2.5 mm	1 mm
Length of the patch	Patch_W	3mm	3mm	2 mm

Fig. 2. Design Properties of Transmission Lines

A snapshot of the $50\,\Omega$ transmission line as designed in Ansys HFSS is given below in Fig 3:

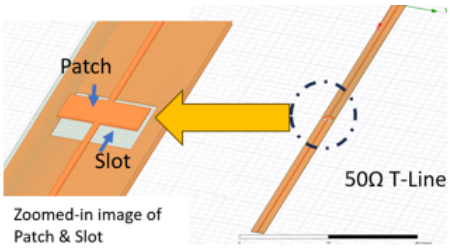

Fig. 3. A $50\,\Omega$ transmission line model designed in Ansys HFSS with both slot and patch placed in the middle of the transmission line.

V. Board Design

The transmission line parameters obtained from the simulation setup were utilized to design the printed circuit board (PCB) using Altium Designer. Three sets of transmission lines, each with a patch, slot, and a combination of both, were designed for $25\,\Omega$, $50\,\Omega$, and $75\,\Omega$ impedance values. The detailed PCB layout, focusing on the $50\,\Omega$ transmission line design illustrated in Fig 4:

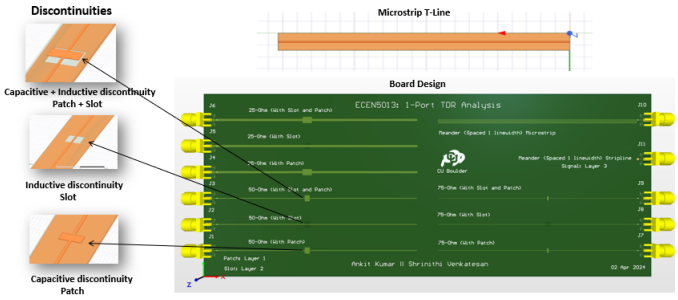

Fig. 4. Printed Circuit Board Layout in Altium Designer

The board was meticulously assembled, incorporating edge-connected SMA to ensure robust connectivity. Subsequently, precise 1-port measurements were conducted using a Vector Network Analyzer (VNA). This comprehensive analysis facilitated the acquisition of S-parameter data, stored in .s1p files, providing invaluable insights into the transmission line's impedance, reflection, and transmission properties across various frequencies. The assembled Printed Circuit Board with SMA Connectors is shown in Fig 5:

Fig. 5. Assembled Printed Circuit Board with SMA Connectors

VI. The Results

The S-parameter files obtained through the VNA measurements for 1-port are imported into Keysight ADS to analyze the measured results. Subsequently, the detailed analysis of measured TDR plots is carefully conducted for the $25\,\Omega$ transmission line and then compared with simulated results. Additionally, for the $50\,\Omega$ and $75\,\Omega$ transmission lines, comparison results with measured and simulated TDR plots are presented and discussed. This comprehensive comparative analysis enables a thorough evaluation of the performance and accuracy of the designed transmission lines across different impedance values.

A. Measured TDR Plot for $25\,\Omega$

The TDR Plot for the $25\,\Omega$ transmission line with the slot, patch, and slot-patch combination is depicted in Figure 6. Upon examination of Figure 6, characteristic impedance at $25\,\Omega$ is evident, followed by noticeable impedance differences at 1 nanosecond, indicative of the introduced discontinuities. Subsequently, the impedance profile follows the $25\,\Omega$ characteristic until the end of the transmission line, where it rises to infinity due to the absence of terminating resistance.

Close observation of the plots reveals distinct features corresponding to the different components:

- The purple plot exhibits a peak in impedance around $37\,\Omega$, indicating the presence of the slot and its inductive behavior.
- The blue plot displays a dip in impedance around $15\,\Omega$, signifying the presence of the patch and its capacitive behavior.
- The red plot showcases a compensated impedance around $24\,\Omega$, slightly skewed towards capacitive characteristics, representing the combination of slot and patch.

Additionally, various sections of the TDR plot reveal supplementary information:

- An initial segment signifies the 50 picoseconds rise time, followed by an impedance at $50\,\Omega$ for 0.2 nanoseconds, incorporated to observe the Device under Test (DUT) in detail at $25\,\Omega$.
- A launch discontinuity at the beginning of the DUT results indicates the absence of slots in the SMA pads on our board design, attributed to their capacitive behavior.

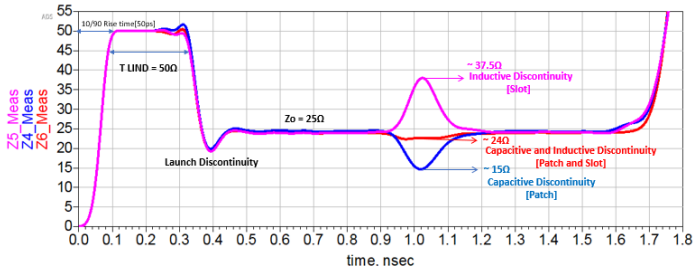

Fig. 6. Measured TDR Plot for 25 Ω transmission line

B. Measured and Simulated TDR Plots for 25 Ω

Comparing these results to the obtained simulation results from Ansys HFSS, we analyze the measured and simulated TDR plots for the compensated design with a combination of patch and slot. Figure 7 illustrates the TDR Plot for the 25 Ω transmission line with the slot, patch, and slot-patch combination. Additionally, the green plot in Figure 7 represents the simulated results from the HFSS design files for the compensated design with a combination of patch and slot.

Upon examination, the simulated plot exhibits a characteristic impedance of 24.8 ohms, closely matching the desired value of 25 ohms. This close correspondence underscores the appropriateness of the simulated design, which benefits from controlled parameters. Comparing the measured and simulated characteristic impedances, the discrepancy is minimal, with an error percentage of only 0.4%. Notably, in the case of the measured results with a compensated patch and slot design, the maximum discontinuity is reduced to as low as approximately 8% compared to the measured characteristic impedance.

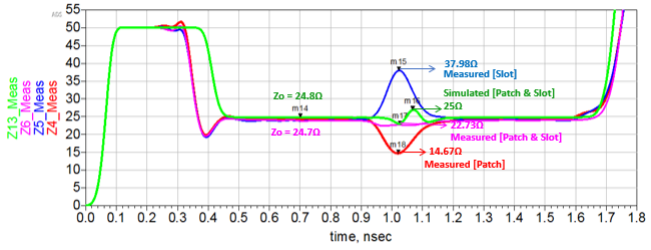

Fig. 7. Simulated and Measured TDR Plots for 25 Ω transmission line

C. Measured and Simulated TDR Plots for 50 Ω

The TDR Plot for the 50 Ω transmission line with the slot, patch, and slot-patch combination is depicted in Figure 8. Upon examination of Figure 8, a characteristic impedances of measured and simulated plots are observed, followed by noticeable impedance differences at 1 nanosecond, indicative of the introduced discontinuities.

Close observation of the plots reveals distinct features corresponding to the different components:

- The green plot represents the simulated results for the compensated design with a combination of patch and slot from the HFSS results. The characteristic impedance is observed at approximately 49.9 Ω, very close to the desired impedance at 50 Ω due to better control over the design parameters.
- The measured plots (blue, purple, red) show a characteristic impedance at approximately 46.8 Ω, differing from the simulated result (green plot) at approximately 42.4 Ω by 6.2%.
- The blue plot exhibits a peak in impedance around 62.4 Ω, indicating the presence of the slot and its inductive behavior.
- The red plot displays a dip in impedance around 27.5 Ω, signifying the presence of the patch and its capacitive behavior.
- The purple plot showcases a compensated impedance around 42.4 Ω, slightly skewed towards capacitive characteristics, representing the combination of slot and patch. Notably, in the case of the measured results with a compensated patch and slot design, the maximum discontinuity is reduced to as low as approximately 9% compared to the measured characteristic impedance.

The TDR Plot for 50 Ω transmission line with the slot and patch is given below in Fig 9:

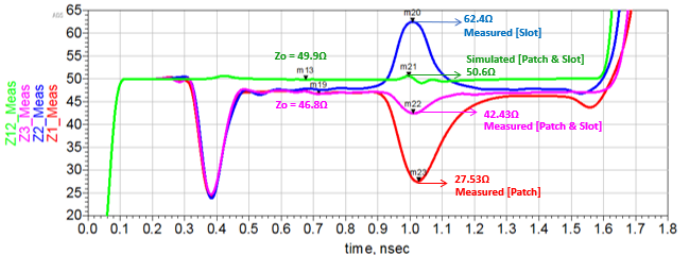

Fig. 8. Simulated and Measured TDR Plots for 50 Ω transmission line

D. Measured and Simulated TDR Plots for 75 Ω

The TDR Plot for the 75 Ω transmission line with the slot, patch, and slot-patch combination is depicted in Figure 9. Upon examination of Figure 9, a characteristic impedance for measured results and simulated results are observed and followed by noticeable impedance differences at 1 nanosecond, indicative of the introduced discontinuities.

Close observation of the plots reveals distinct features corresponding to the different components:

- The green plot represents the simulated results for the compensated design with a combination of patch and slot from the HFSS results. The characteristic impedance is observed at approximately 75.6 Ω,very close to the desired impedance at 75 Ω due to better control over the design parameters.
- The measured plots (blue, purple, red) show a characteristic impedance at approximately 67.5 Ω, differing from the simulated result (green plot) at approximately 75.6 Ω by 12%.
- The blue plot exhibits a peak in impedance around 75.13 Ω, indicating the presence of the slot and its inductive behavior.

- The red plot displays a dip in impedance around $54.37\,\Omega$, signifying the presence of the patch and its capacitive behavior.
- The purple plot showcases a compensated impedance around $64.45\,\Omega$, slightly skewed towards capacitive characteristics, representing the combination of slot and patch. Notably, in the case of the measured results with a compensated patch and slot design, the maximum discontinuity is reduced to as low as approximately 4.5% compared to the measured characteristic impedance.

The TDR Plot for $75\,\Omega$ transmission line with the slot and patch is given below in Fig 9:

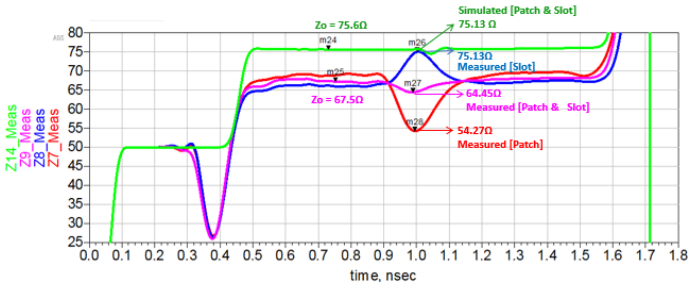

Fig. 9. TDR Plot for $75\,\Omega$ transmission line

E. Reverse Engineering the measured plots for $25\,\Omega$ transmission line

To obtain the values of inductance and capacitance in the transmission lines, reverse engineering of the measured TDR plots were conducted, focusing on the detailed analysis of the 25-ohm transmission line with slot, patch and a combination of slot-patch. Through this process, the intricate characteristics of the transmission line, including its inductance and capacitance values, were meticulously examined and evaluated.

The TDR Plot for $25\,\Omega$ transmission line with the just the slot is given below in Fig 10. The value of inductance was measured as 0.7 nH (approx.).

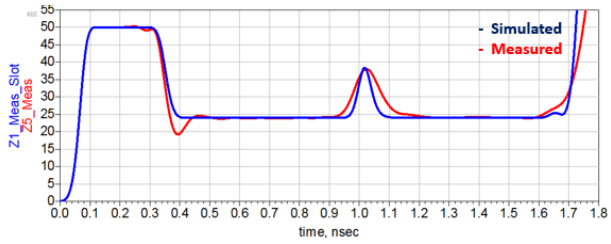

Fig. 10. TDR Plot for $25\,\Omega$ transmission line with Slot

The TDR Plot for $25\,\Omega$ transmission line with the just the patch is given below in Fig 11. The value of capacitance was measured as 1.05 pF (approx.).

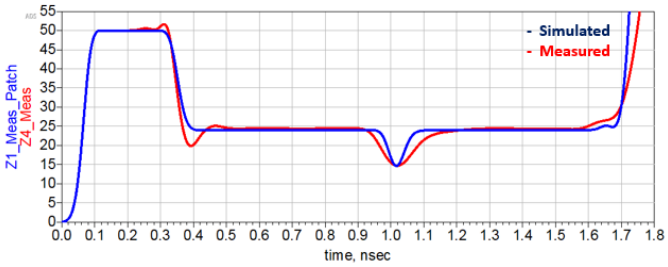

Fig. 11. TDR Plot for $25\,\Omega$ transmission line with Patch

The TDR Plot for $25\,\Omega$ transmission line with the combination of slot-patch is given below in Fig 12. The value of inductance and capacitance were measured at 0.1 nH (approx.) and 0.27 pF (approx.) respectively.

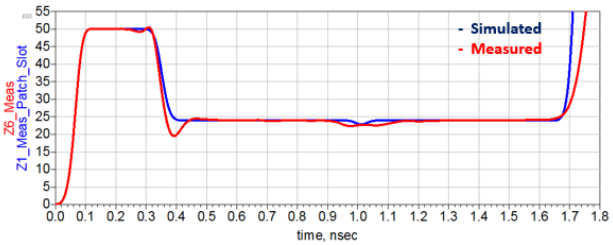

Fig. 12. TDR Plot for $25\,\Omega$ transmission line with Slot-Patch

VII. Conclusions

In conclusion, the paper sheds light on the impact of return path discontinuities, such as those induced by slots and countered by patches, on transmission line behavior. Capacitive discontinuities are found to result in a dip of impedance in the Time Domain Reflectometry (TDR) profile, whereas inductive discontinuities result as peaks of impedance in the TDR profile. By carefully controlling the geometries of both slots and patches, it becomes evident that characteristic impedance of the transmission line can be strategically managed. The application of the Rule of Thumb for assessing the transparency of discontinuities highlights the importance of considering the spatial extent of signal edges. Additionally, the study underscores the necessity of maintaining a uniform, continuous return path while minimizing the length of any unavoidable discontinuities. Lastly, the experiment asserts the critical role of return current alongside signal current in ensuring optimal signal integrity in high-frequency electronic systems. These findings offer valuable insights and practical guidelines for transmission line design.

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