

Analysis of Transmission Line Discontinuities using Time Domain Reflectometry

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AGENDA

Background

Project Flow

Transmission Line Simulation with Discontinuities

1 Port Measurement on PCB

Measured TDR Plots

Hacked TDR Plots

Observations

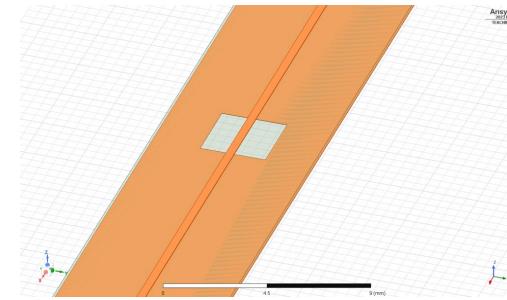


Key Definitions:

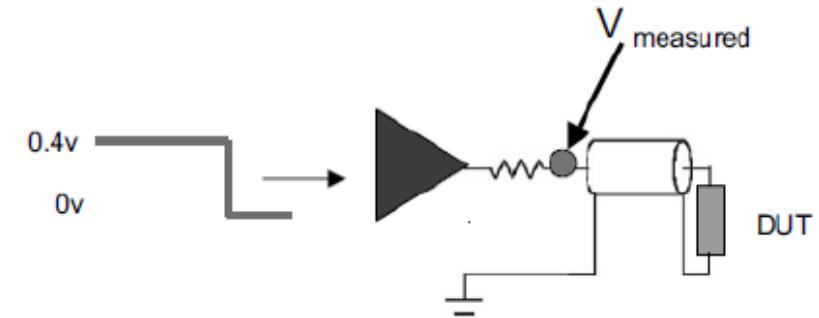
Return Path Discontinuity (RPD):

- Path of the returning conduction current of an interconnect is “discontinuous”.
- Causes the return-current to continue as displacement current, to close the loop.
- Capacitance and inductance Discontinuity.
- Analyze -> Time Domain Reflectometry (TDR)

TDR Internal Schematic.



Discontinuity in Return Path



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Design Flow and Project Goals:



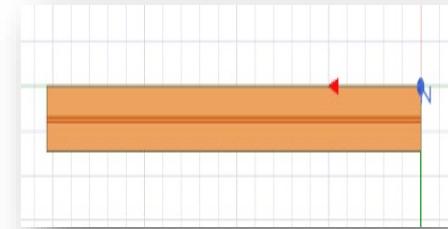
HFSS



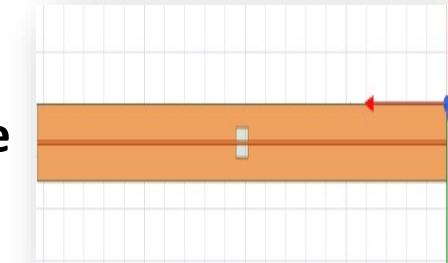
- | | | | | |
|---|---|--|--|--|
| <ul style="list-style-type: none">• Simulate Transmission Lines 25/50/75 Ω• Obtain Design Parameters | <ul style="list-style-type: none">• Design PCB using parameters from Simulation for Transmission Lines 25/50/75 Ω<ul style="list-style-type: none">• Obtain 1-Port Measurements | <ul style="list-style-type: none">• Import s1p files, plot and analyse the TDR for Measured Data | <ul style="list-style-type: none">• Reverse Engineer and plot the TDR for Simulated Data | <ul style="list-style-type: none">• Compare the plots for Measured and Simulated Data.• Verify the best design and measurement practices. |
|---|---|--|--|--|

Simulation setup in HFSS

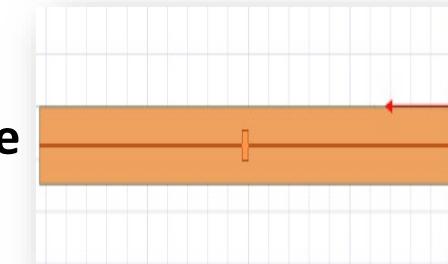
Microstrip T-Line
 50Ω



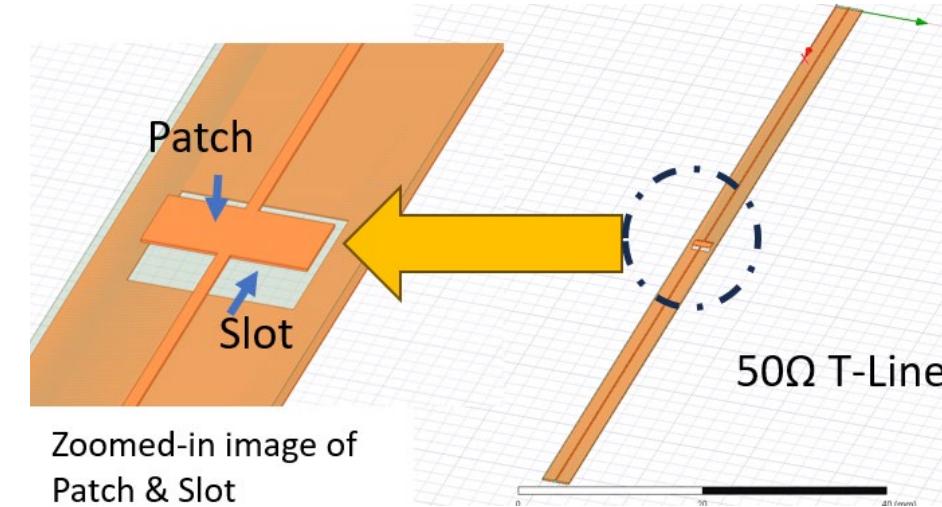
Slot in return plane



Patch in signal plane



Slot + Patch (Compensated to 50Ω)



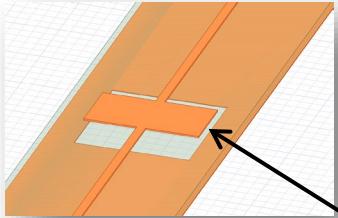
The Design Properties for Slot and Patch

Parameters	Evaluated values for 25Ω Transmission line	Evaluated values for 50Ω Transmission line	Evaluated values for 75Ω Transmission line
Width of the slot	3 mm	3 mm	2 mm
Length of the slot	3 mm	3 mm	2 mm
Width of the patch	4.5 mm	2.5 mm	1 mm
Length of the patch	3mm	3mm	2 mm

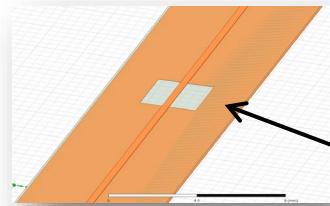
5

Board Setup:

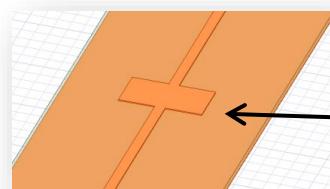
Discontinuities



Capacitive + Inductive discontinuity
Patch + Slot

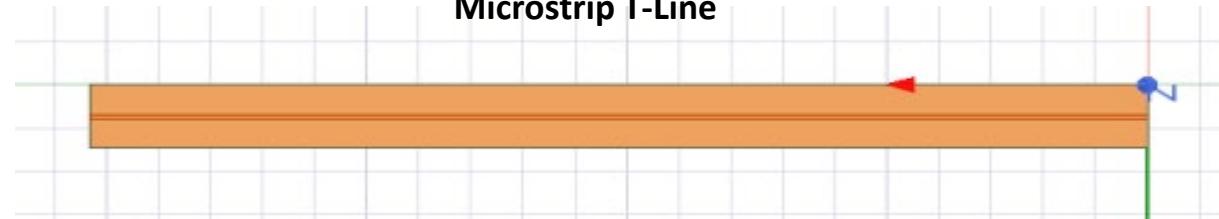


Inductive discontinuity
Slot

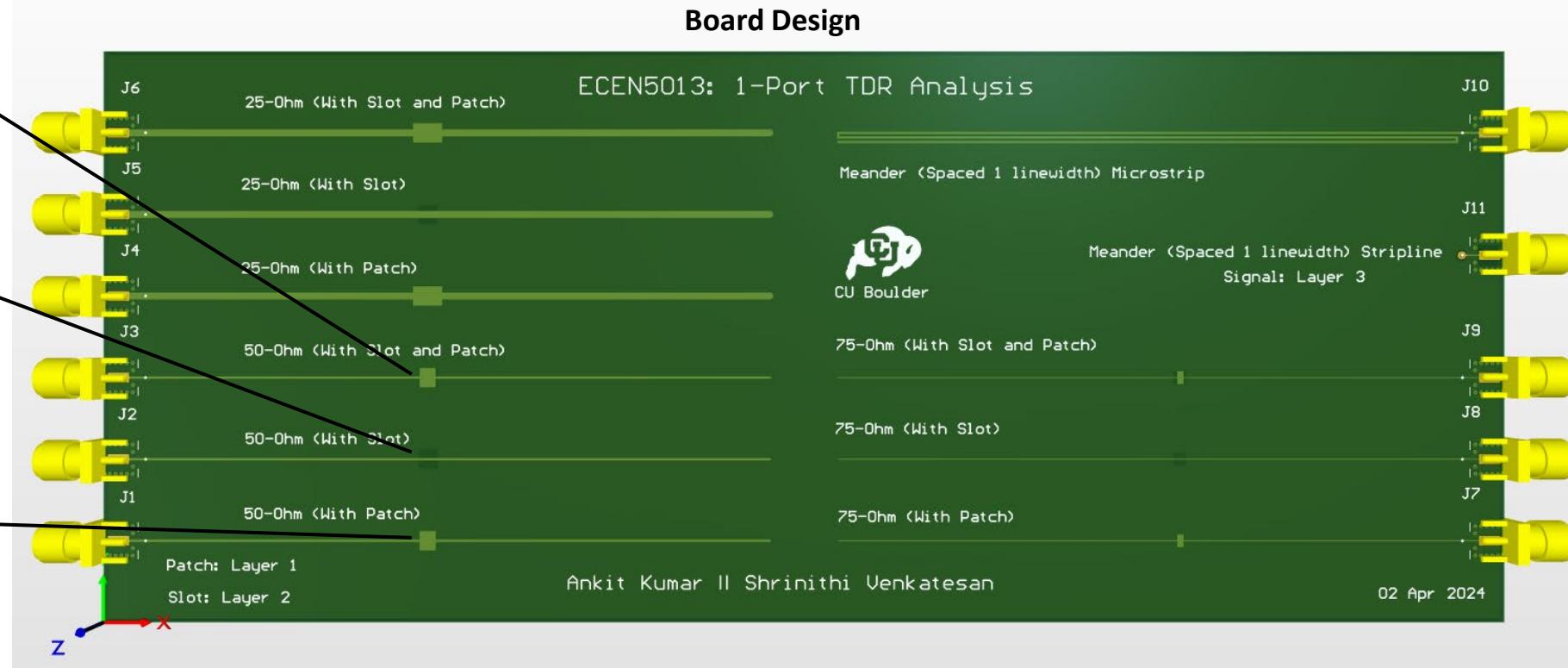


Capacitive discontinuity
Patch

Microstrip T-Line



Board Design



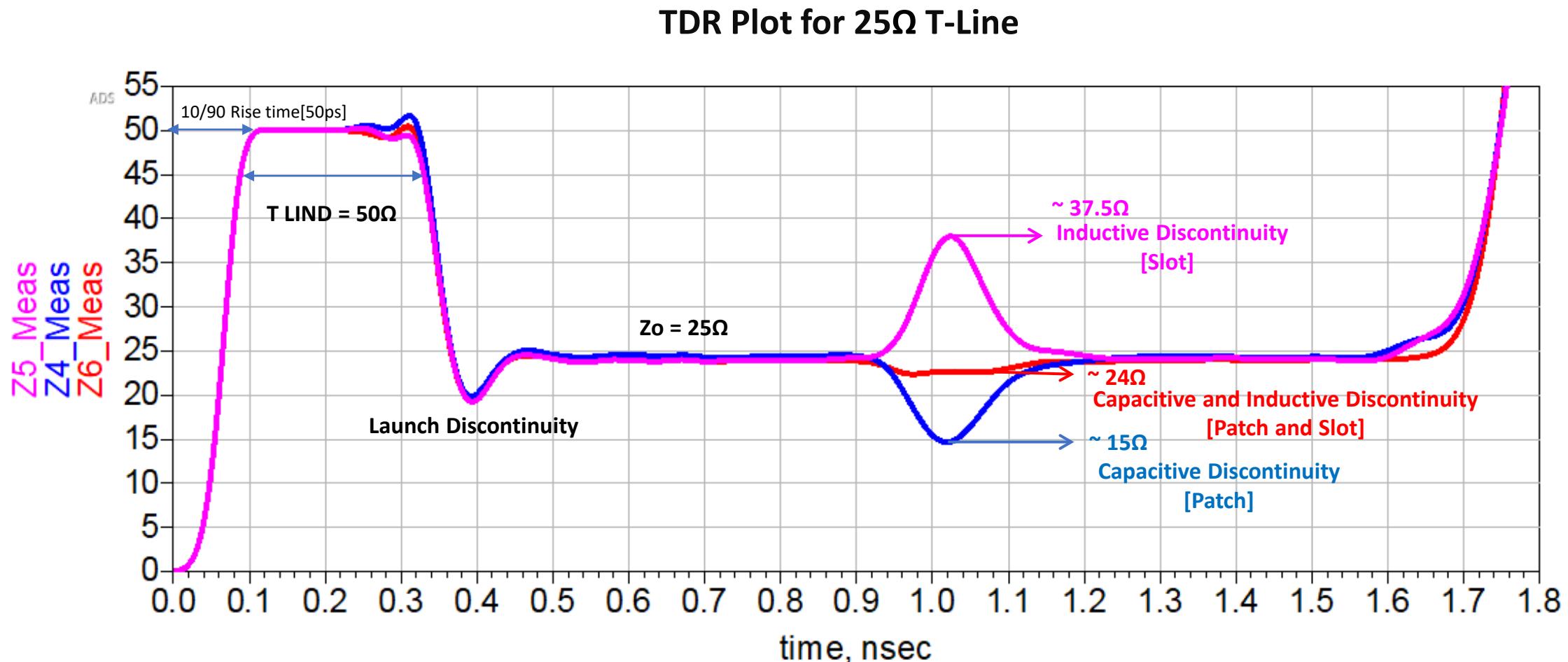
1-Port VNA Measurements:



Plan of Record for the Measurement:

- 1-Port VNA measurement.
- Obtained s1p files.
- Export to Keysight ADS.

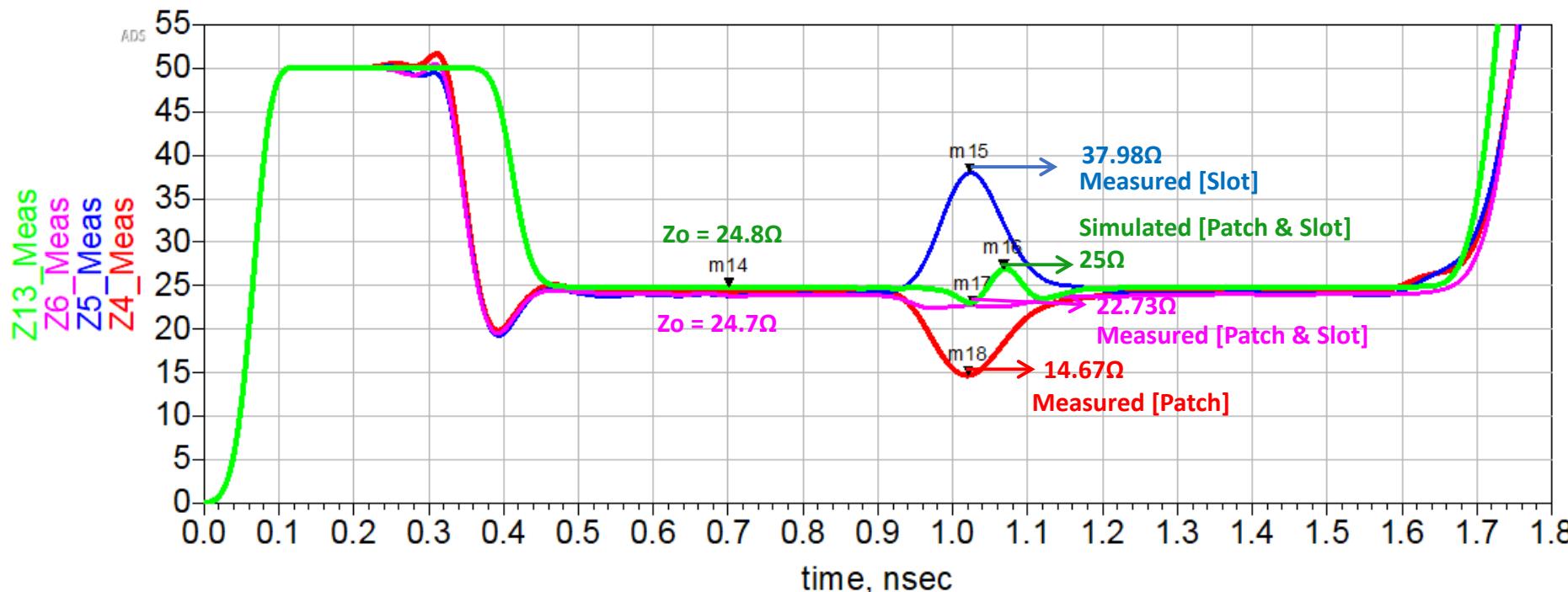
Measured TDR Analysis in Keysight ADS (25Ω)



Comparison of the Measured Vs. Simulated values for 25Ω Transmission Line:

TDR Plot for 25Ω T-Line

Maximum Discontinuity in case of compensated (Slot & Patch) is reduced to as low as ~8%



Measured Results ($Z_0 = 24.7\Omega$):

Plot	Error % (wrt Measured)
Patch	-40.6%
Slot	53.7%
Patch & Slot	-7.9%

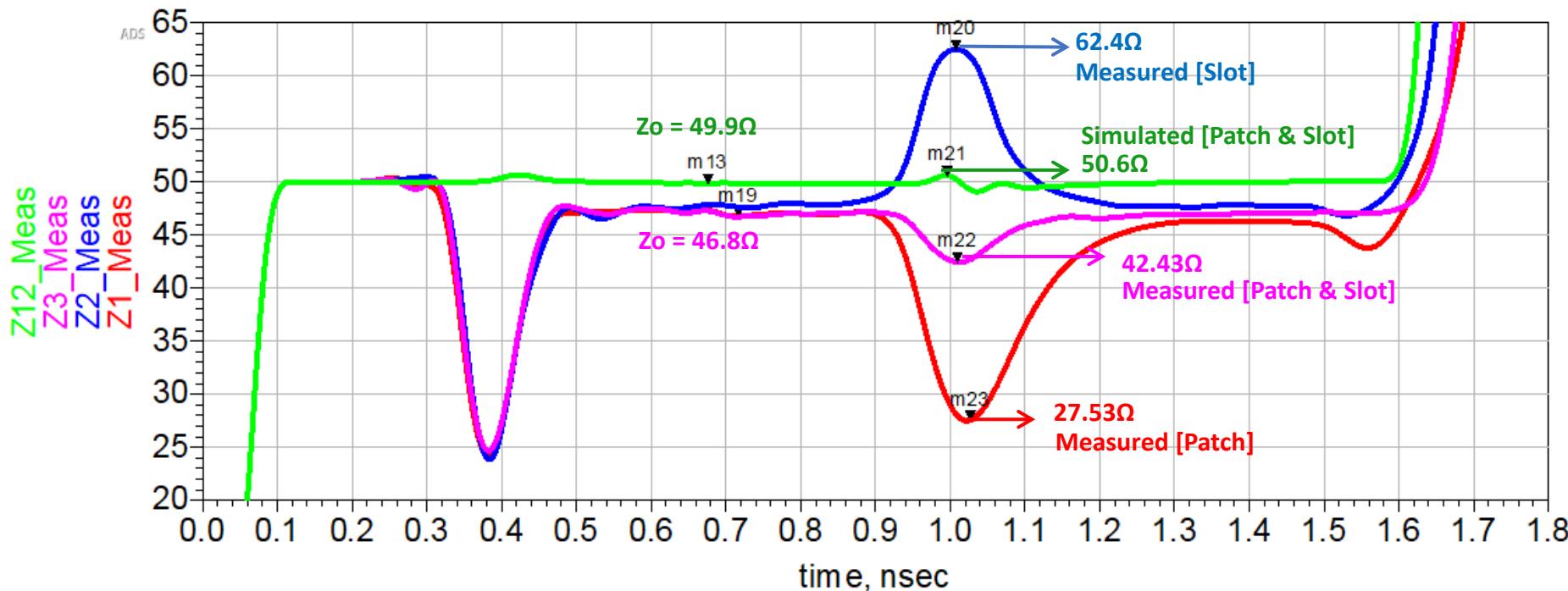
Simulated Results ($Z_0 = 24.8\Omega$):

Error = 0.4%

Comparison of the Measured Vs. Simulated values for 50Ω Transmission Line:

TDR Plot for 50Ω T-Line

Maximum Discontinuity in case of compensated (Slot & Patch) is reduced to as low as ~9%



Measured Results ($Z_0 = 46.8\Omega$):

Plot	Error % (wrt Measured)
Patch	-41.1%
Slot	33.3%
Patch & Slot	-9.3%

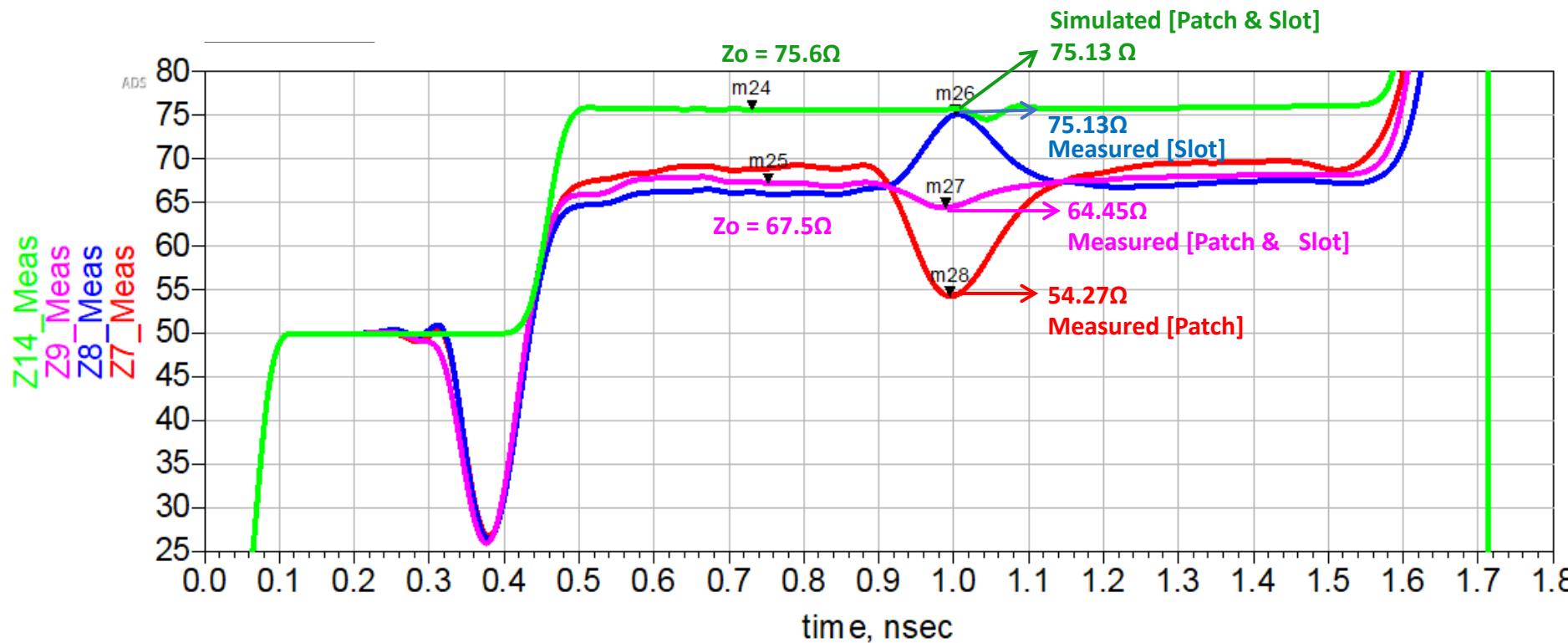
Simulated Results ($Z_0 = 49.9\Omega$):

Error = 6.2%

Comparison of the Measured Vs. Simulated values for 75Ω Transmission Line:

TDR Plot for 75Ω T-Line

Maximum Discontinuity in case of compensated (Slot & Patch) is reduced to as low as ~4.5%



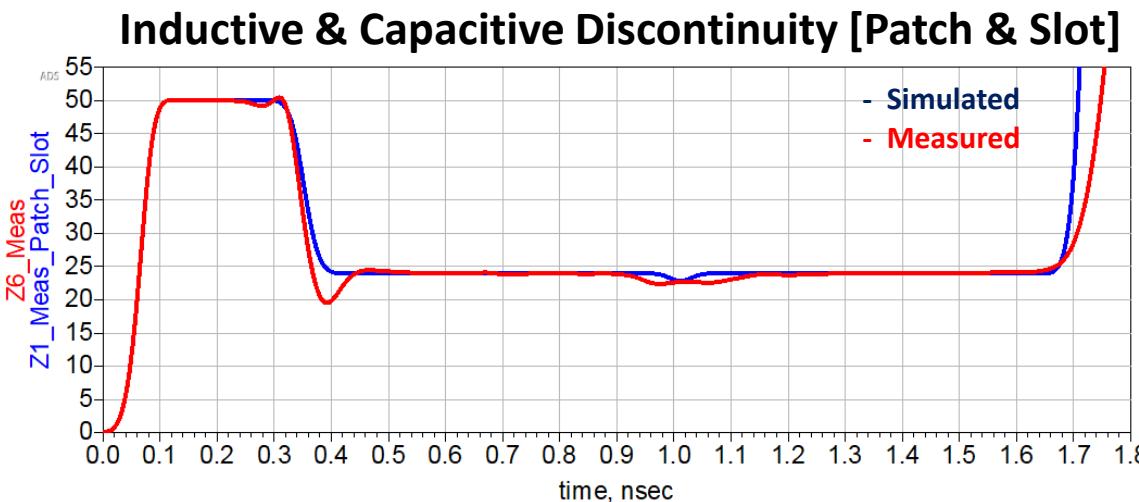
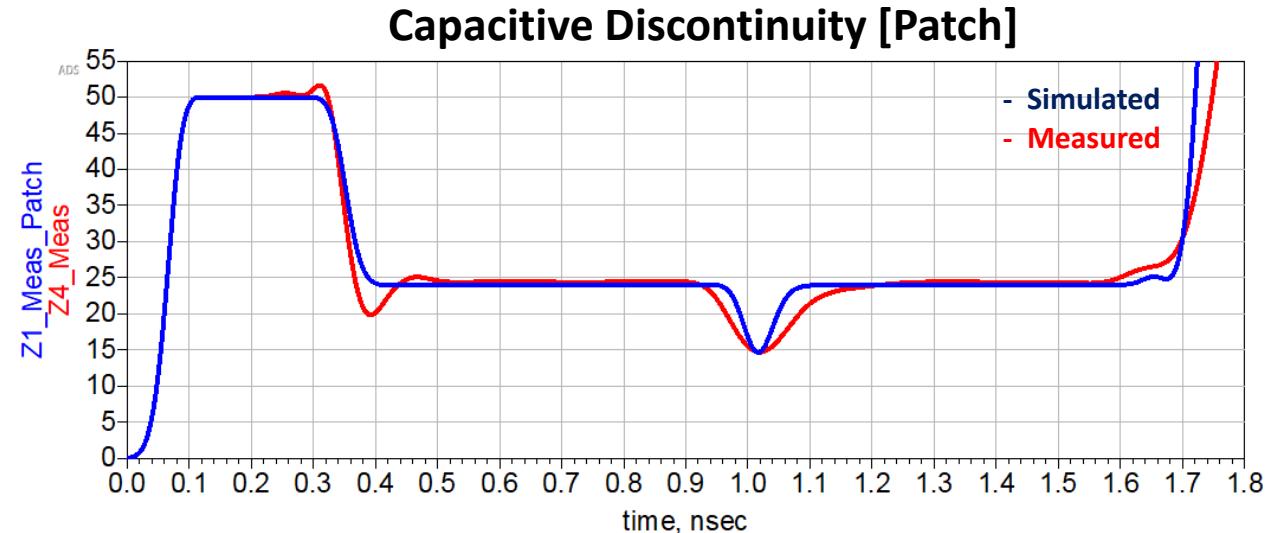
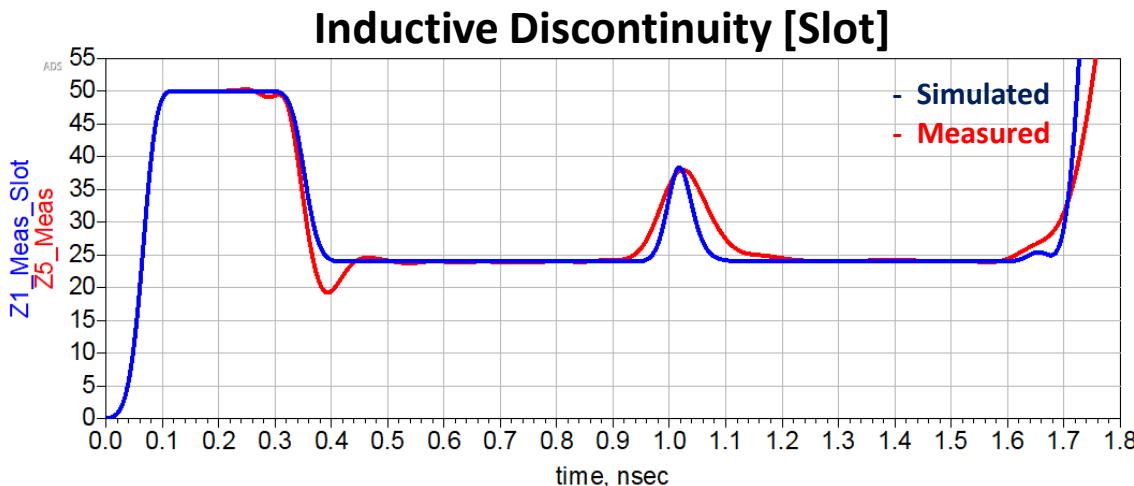
Measured Results ($Z_0 = 46.8\Omega$):

Plot	Error % (wrt Measured)
Patch	-19.6%
Slot	11.3%
Patch & Slot	-4.5%

Simulated Results ($Z_0 = 49.9\Omega$):

Error = 12%

Reverse Engineering the Design (25Ω)



Estimated values of Capacitance and Inductance present in the slot and patch

Plot	C (pF)	L (nH)
Patch	1.05	-
Slot	-	0.7
Patch & Slot	0.27	0.1



University of Colorado **Boulder**



High Speed Digital Engineering Group

Key Takeaways:

- Slot -> Increase in inductance, elevates the impedance value -> peak.
- Patch -> Enlarges the trace area, increase in capacitance -> dip.
- Control the geometries of the slot and the patch -> control the characteristics impedance of the transmission line.

Best Design Practice:

If allowed, Always use uniform, wide and continuous return path because:

“Return current is as important as signal current.”

Thank You!

