

Experiment No: - 4

Experiment Name: - STUDY & DESIGN OF FLIP-FLOPS

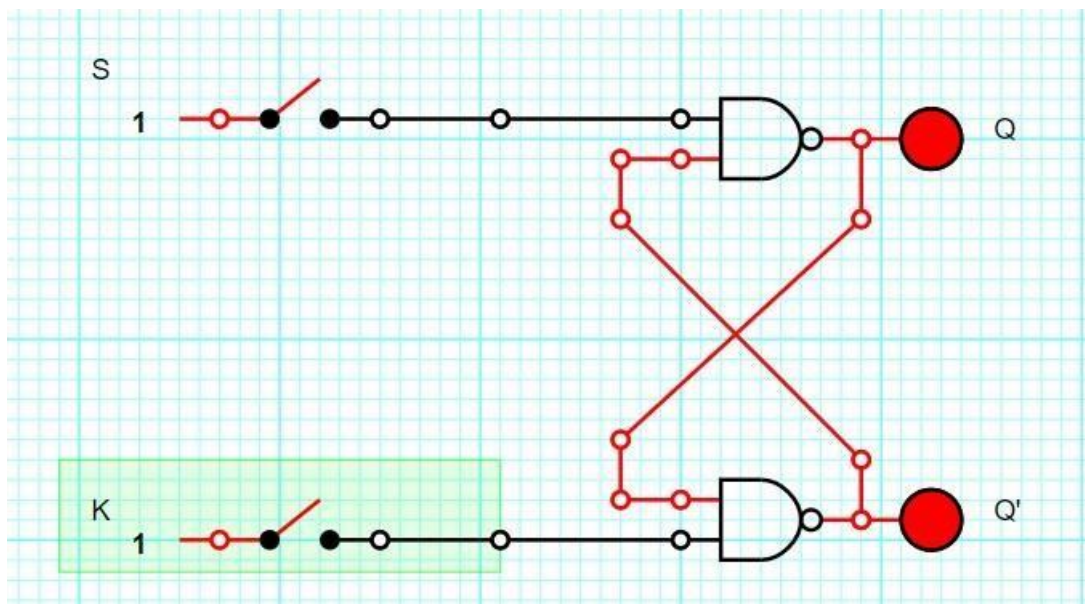
Name: - Shrikrushna C Gundre

Roll No: - DCSE 12

PRN No: - 2122010191

1. S-R Flip-Flop

- **Construction**



- **Truth Table**

S	R	Q	Q'
0	0	Latch	Latch
0	1	0	1
1	0	1	0
1	1	Invalid	Invalid

- **Applications**

1. These circuits are known for storing the information in the form of bits. These are known as memory elements.
2. The usage of pulse latches follows the same behavior of flip-flops but good enough to generate a quick response.
3. It is widely used to store the data and the codes for computations.

- **Significance**

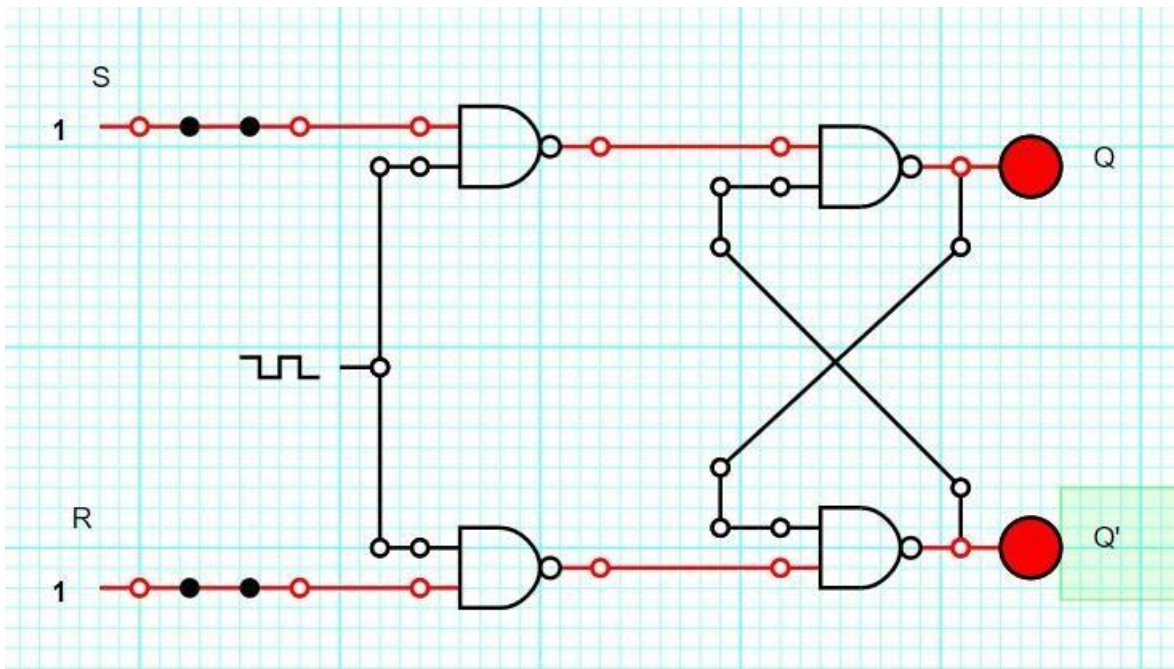
1. It is used to keep a record of different values of variable state like intermediate, input or output.
2. It is mainly used to store data or information.
3. Wherever operations, storage and sequencing are required these signal circuits are used.
4. They are also used for exercising control over the way the circuit has to function, like for changing the operation of a circuit to a different state.

- **Limitation**

1. The main problem associated with these circuits is that they work on simple 1bit memory, so if set input is first taken as 0 then taken back to logic, and then the further change does not have any effect on logic 0 pulses of set input (S).

2. Clocked S-R Flip-Flop

- **Construction**



- **Truth Table**

Inputs			Outputs	
CLK	S	R	Q_{n+1}	$Q_{n'+1}$
↑	0	0	Q_n	Q_n'
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	X	X

- **Applications**

1. These circuits are known for storing the information in the form of bits. These are known as memory elements.
2. The usage of pulse latches follows the same behaviour of flip-flops but good enough to generate a quick response.
3. It is widely used to store the data and the codes for computations.

- **Significance**

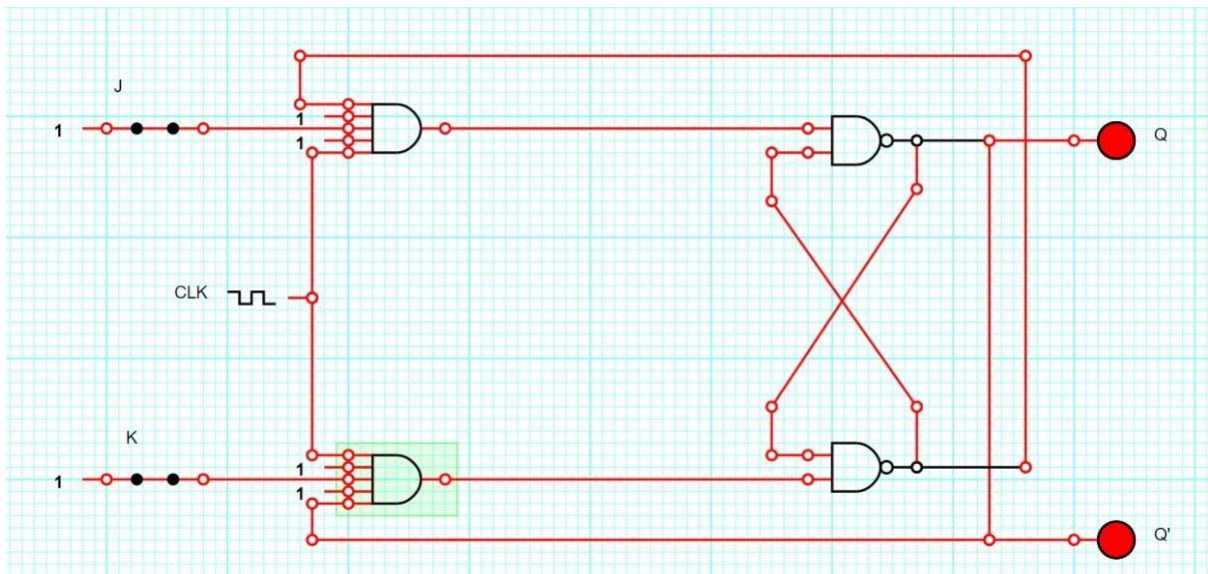
1. It contains an additional input called Clock which is used to control the circuit.
2. It is used to design the counters.

- **Limitations**

1. It contains the state which is called the INVALID.
2. The INVALID condition occurs when $S=1$ & $R=1$.
3. Because of that the output is not generated in SR Flipflop.

3. J-K Flip-Flop

- **Construction**



•

Truth Table

Inputs			Outputs	
CLK	S	R	Q_{n+1}	$Q_{n'+1}$
↑	0	0	Q_n	Q_n'
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Toggle	Toggle

•

Applications

1. Registers.
2. Counters.
3. Event Detectors.
4. Data Synchronizers.
5. Frequency Dividers.

•

Significance

1. In J-K flipflop the INVALID condition is not occurs.
2. In J-K flipflop TOGGLE condition occurs.
3. When $J=1$ & $K=1$ J-K flipflop toggles continuously.

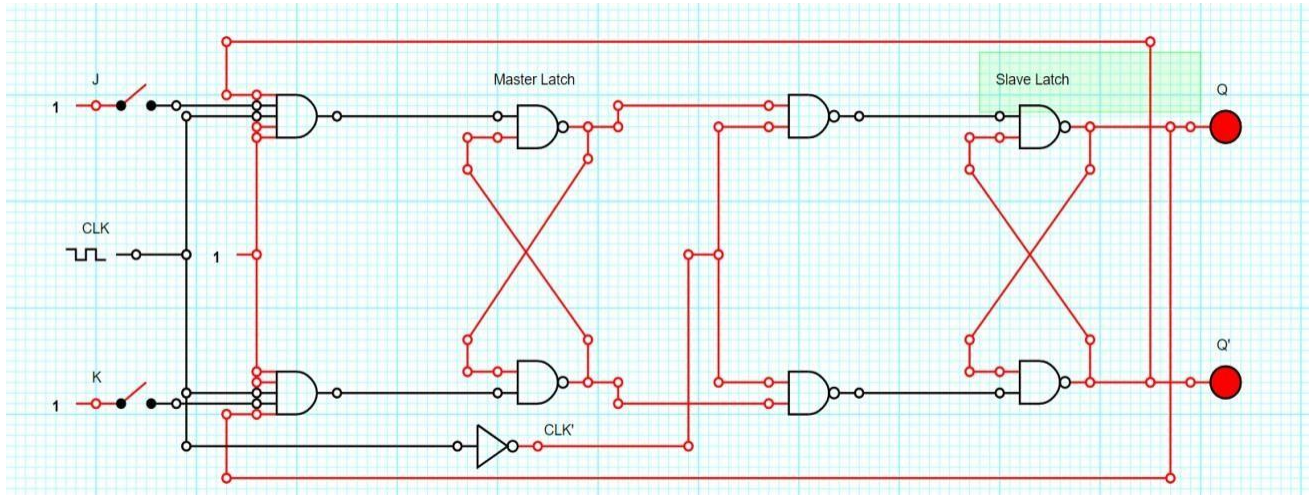
•

Limitations

1. When $J=1$ & $K=1$ J-K flipflop toggles continuously.
2. There is no Controlled toggling happens in J-K flipflop.

4. Master-Slave J-K Flip-Flop

- **Construction**



- **Truth Table**

Inputs			Outputs		Remark
CLK	J	K	Q_{n+1}	$Q_{n'+1}$	
X	0	0	Q_n	Q_n'	No Change
↑	0	0	Q_n	Q_n'	No Change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Q_n'	Q_n	Toggle

- **Applications**

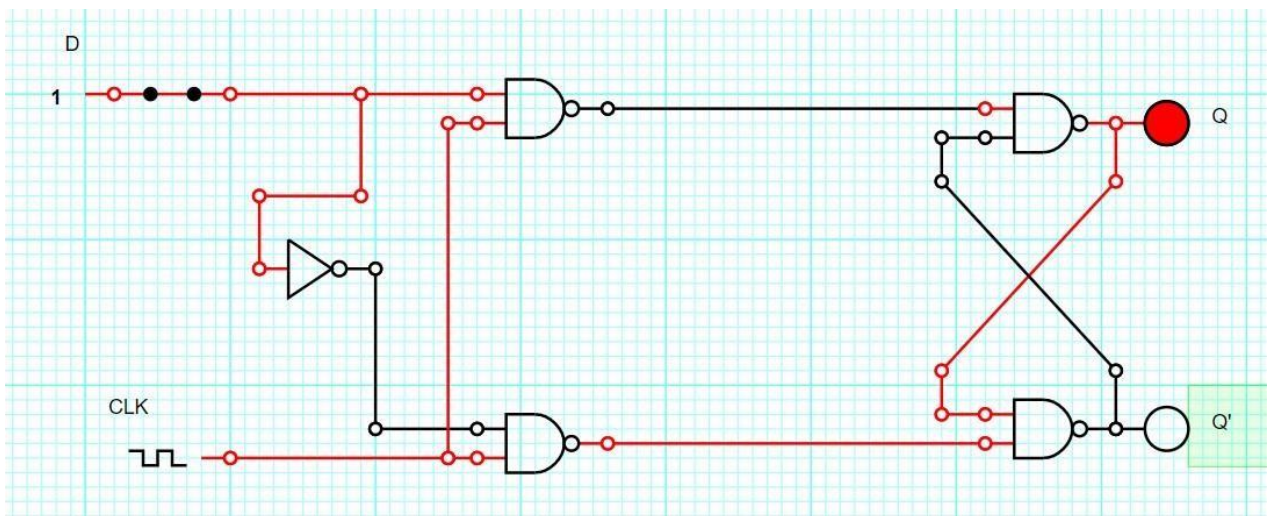
1. JK flip flop master slave overcome the limitation of SR flip flop, in SR flip flop when $S = R = 1$ condition arrives the output becomes uncertain. Still, in the JK master slave, when $J = K = 1$, then the output toggles, the output of this state keeps changing with the clock pulse.

Significance

1. A sequential circuit with an edge-controlled flip flop is straightforward to design rather than a level-triggered flip flop.
2. By using the Master-Slave configuration, we can also eliminate the race around condition.

5. D Flip-Flop

- **Construction**



- **Truth Table**

Clock	D	Q	Q'
↓	0	0	1
↑	0	0	1
↓	1	0	1
↑	1	1	0

Applications

1. Data Synchronizers.
2. Frequency Dividers.
3. To create delay-lines.

- **Significance**

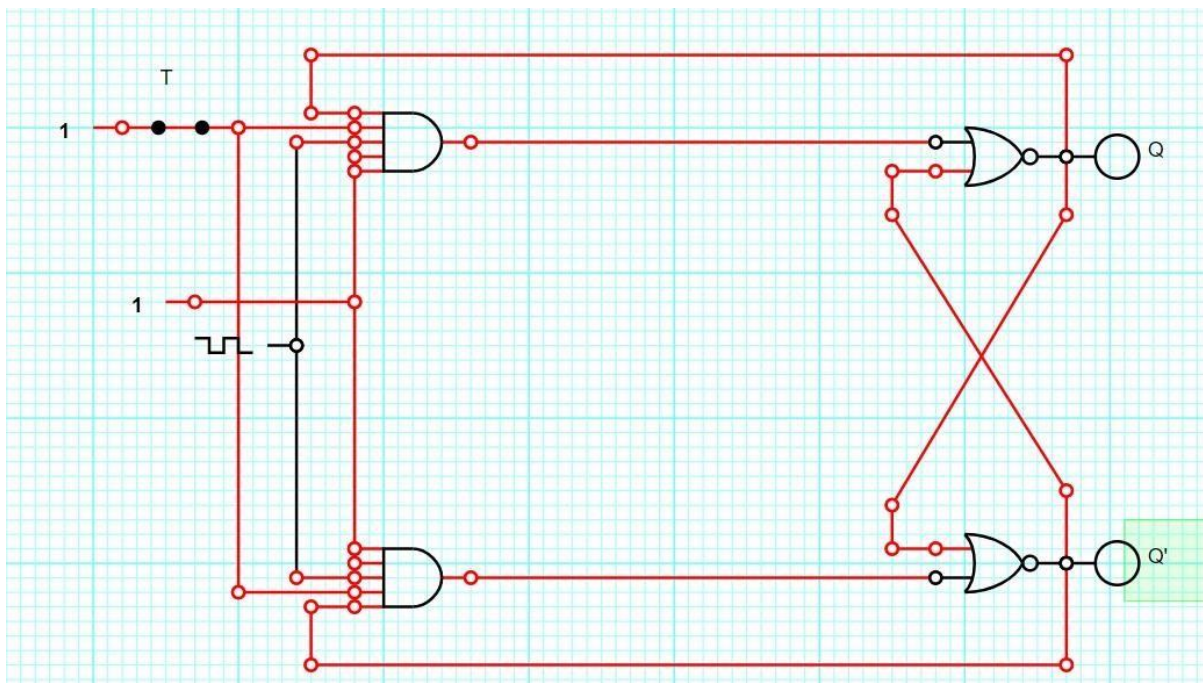
1. The advantage of D flip-flops is their simplicity and the fact that the output and input are essentially identical, except displaced in time by one clock period.

- **Limitations**

1. A D flip flop in a circuit increases the circuit's size, often to about twice the normal. Additionally, they also make the circuits more complex.

6. T Flip-Flop

- **Construction**



Truth Table

-

T	Q	Q'
0	0	0
0	1	1
1	0	1
1	1	1

- **Applications**

1. It is used in counter designs.
2. These flip flops are used for constructing binary counters.
3. They are used in frequency dividers.
4. This type of sequential circuits is also present in binary addition devices.
5. It is also used in 2-bit parallel load registers.
6. It is also used in shift registers.

- **Significance**

1. These Flip-Flops has a toggle input and a clock. When a clock is triggered, it inverts the value of Flip-Flops. They are good for counters.

- **Limitations**

1. The main disadvantage of T flip – flop is that the state of the flip – flop at an applied trigger pulse is known only when the previous state is known.