5th Sem. B.Tech/B.Tech Dual (Supplementary)
CO&A CS-505
[CSE]

SUPPLEMENTARY EXAMINATION-2012

5th Semester B.Tech / B.Tech Dual(M.Tech/MBA)

COMPUTER ORGANIZATION & ARCHITECTURE CS-505

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Q.No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) Differentiate between micro-routine and micro-instruction. [2 × 10
   (b) List the microinstructions in the *fetch cycle* in a single bus CPU organization.
   (c) Differentiate between byte addressable and word addressable.
   (d) What is the difference between *memory access time* and *memory cycle time*?
   (e) How many separate address and data lines are needed in a 8Kx16 memory?
   (f) Define speed up ratio in a pipeline. Draw the space-time diagram for a six-segment pipeline to process eight tasks.
   (g) List the function of I/O interface.
   (h) Differentiate between the *valid bit* and the *dirty bit*.
   (i) How many memory references are required for fetching and executing each of the following instructions?
   (a) ADD 50(R_1),R_2 (b) SUB (R_1)+R_2
   (j) Differentiate between *tightly coupled* and *loosely coupled* multiprocessors.

2. (a) What are addressing modes? Explain different types of addressing modes with suitable example. [4

(b) Write a program that can evaluate the following expression in single accumulator processor and stack base computer.(A*B)+(C*D). [4

3. (a) What is Cache mapping? Explain the direct mapping technique with suitable example and also explain its advantage and disadvantages. [4

(b) Why is *memory interleaving* technique used? Consider a memory of 8 words per block. If two clock cycle are required to transfer address from CPU to main memory, six clock cycle to access the first word, three clock cycles each for the consecutive words and two clock cycles for transferring the word from memory to cache. Then calculate the total clock cycle required to transfer the block with interleaving and without interleaving if number of modules are four. [4

4. (a) Explain the 3-bus architecture inside CPU with suitable example. Write the control signals for the following instructions. MUL $30(R_1),R_5$ [4

(b) Explain the working principle of micro-programmed control unit with suitable diagram. Explain how is it different from hardwired control unit. [4

5. (a) Explain the difference between Isolated I/O and memory mapped I/O. [4

(b) State and explain the Flynn's classification of computer with proper diagram. [4

25:00

6. (a) What is pipeline technique? Why is it used? Give examples of two types of pipelining in a processor. [4

A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speed up ratio of pipeline system for 100 tasks. What is the maximum speed up that can be achieved?

(b) What is a pipeline hazard? What are the different types of hazards? Explain the control /branch hazards with its remedy. [4

7. (a) What are the different data transfer schemes? Explain the working principle of DMA data transfer. [4

(b) Multiply the following using booth's multiplication algorithm. [4

(-13) x 7

8. Write short notes on ***any two***. [4 × 2

(a) Virtual memory

(b) Array Processor

(c) Associative memory

(d) Instruction set completeness.

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