HPCA/ CS-3007/ CSE &CSSE /V/2019

Autumn Mid-Semester Examination
School of Computer Engineering
KIIT University, Bhubaneswar-24

Time: 90 Mins ***Full Mark: 20***

(Answer any four including Question number 1 which is compulsory)

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1. [1 × 5 = 5]

(i) Consider a 5-Stage Pipeline with 60, 70, 90, 100 & 80 nsec cycle times & the Interface registers have a delay of 10 nsec. Calculate speedup with respect to non pipeline syste

(ii) Explain the R, I and J type MIPS instruction format with one example from each type.

(iii) We wish to execute I_1, I_2, I_3, I_4 instructions in the program order within a loop in a 5-Stage Pipeline as given below. What is the number of cycles needed to execute the following loop?

For (i = 1 to 2)

{ $I_1 : I_2 : I_3 : I_4$}

(vi) Consider a non-pipelined processor that takes 4 cycles for ALU operations and 5 cycles for branches and 4 cycles for memory operations. Assuming branch instructions account for 15% of all instructions and memory account for 25%, what is the average CPI of a non-pipelined CPU?

(v) What is structural hazard? Explain with suitable example

2. [2 X 2.5]

a. What is pipeline? Explain briefly 5-Stage Pipeline for MIPS processor.

b. What is Control Hazard? How do we deal with Control Hazard?

Consider the following instructions :-

```
        LOAD    R2, 10(R5)
        STORE   (04)R8, R2
        MUL     R3, R2, R4
        SUB     R2, R3, R1
        BNEQZ   R2, L1
        LOAD    R7, (14)R6
        END

L1:-    LOAD    R7, 21(R2)
        SUB     R4, R7,R5
        MUL     R7, R4, R5
```

If the branch instruction is taken in the above sequence of instructions, then find out the independent instruction which can be placed into delayed slot for all possible cases in order to improve the system performance.

[P.T.O]

K Prep

3. [2 X 2.5]

a. Consider the following MIPS instructions in a 5-Stage pipeline processor with IF, ID, EXE, MEM, WB stages of 1 clock cycle each.

```
LOAD   R2, (02)R3
DIV    R7, R1, R2
MUL    R1, R7, R1
STORE  R1, (04)R8
ADD    R1, R7, R2
```

For the above sequence of instructions draw time and space diagram in order to find out total number of clock cycles required to complete their execution using with and without operand forwarding?

b. Consider the following MIPS instructions

```
ADD R1, R2, R3
SUB  R3, R1, R2
ADD R4, R1, R3
MUL R1, R2, R3
SUB  R3, R5, R6
```

Find out all possible dependancies exists in the above given instructions along with their justification.

4. [2 X 2.5]

a. Consider a task where 75% of the task can be enhanced. If the above task is executed in a 2-core machine M then the speedup-enhanced is 2 times. Based on the above specification answer the following questions.

i. Find out the number of additional cores required to achieve twice the over all speedup achieved by M.

ii. Find out the additional number of cores required to achieve 4-times over all speedup achieved by M.

b. Consider a 5-Stage Pipeline and we wish to execute $I_1, I_2, I_3, \ldots I_{15}$ instructions in program order. Find out the number of clock cycles in required to complete those instructions in the following cases

Case 1: Find out number of clock cycles required to complete $I_1, I_2, I_3, \ldots I_{15}$ instructions in a 5-Stage Pipeline.

Case 2: Find out number of clock cycles required to complete $I_1, I_2, I_3, \ldots I_{15}$ instructions in a 5-Stage Pipeline, where I_4 is a unconditional Branch instruction and I_{12} is the target instruction.

5. Write short notes on any two of the following [2 X 2.5]

a. Flynn's Classification

b. Data Hazard and its Types

c. Seven dimensions of an ISA

========== BEST OF LUCK ==========

[P.T.O]

K-Prep