Semester: 4th
Subject Name:-Computer Architecture &
Code:-CS2006

SPRING MID SEMESTER EXAMINATION-2023

School of Computer Engineering
Kalinga Institute of Industrial Technology, Deemed to be University
Computer Architecture
[CS 2006]

Time: 1 1/2 Hours **Full Mark: 20**

Answer any four Questions including Q.No.1 which is Compulsory.
The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. Answer all the questions. [1 x 5]

a) What is the final value of R1 and R2 after executing the instruction "Compare R1, R2", (Initially value of R1=10, R2=20)?

Solution Scheme: R1=10, R2=20 …… (1 Mark).

b) How many memory references are required for fetching and executing the following instructions.

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INC A    // 2-WORD instruction
JMP L1   // 2-WORD instruction
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Solution Scheme: INC A FETCH=2, EXECUTE =2 TOTAL=4 (0.5 Mark)
JMP L1 FETCH=2, EXECUTE =0 TOTAL=2 (0.5 Mark)

c) Write appropriate instruction to perform the following operation: Multiply the content of register R1 by 128 without using MUL opcode. The content of R1 an unsigned integer.

Solution Scheme : LshiftL #7, R1 (1 Mark)
Or R1 +R1+R1……..128 times using branch instruction (1 Mark)

d) Give the importance of RUN and END signal.

Solution Scheme: RUN signal (0.5 Mark)
RUN=1: Counter to be incremented by 1 at the end of every clock cycle. RUN=0: counter stops counting.
END Signal (0.5 Mark)
It starts a new instruction fetch cycle by resetting the control step counter to its starting value.

e) What are the possible values of PC after performing the following Branch instruction with proper justification. (Assume instruction is 1 word, 1word = 4 bytes and byte addressable).

Memory Location	Instruction
2000	Branch>0 1000

Solution Scheme: PC=3004 if previous instruction result is >0 (0.5 Mark)
PC=2004 Otherwise (0.5 Mark)

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2. Long Answer Type Question [5 Marks]

A) How to represent the number "-20" in little and big endian style. Assuming the memory locations starts at the address 2000 and the memory is byte-addressable memory organized in 32-bit words. [2 Marks]

Solution Scheme: Step marking may be awarded.

-20= 1111 1111 1111 1111 1111 1111 1110 1100=FF FF FF EC

Little endian: (1 Mark)

EC	FF	FF	FF

Big Endian: (1 Mark)

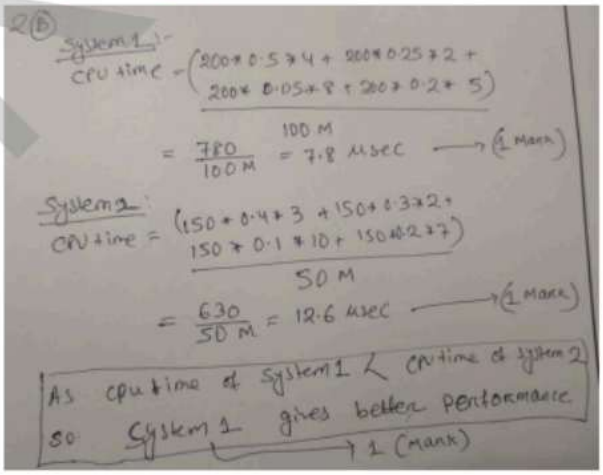
FF	FF	FF	EC

B) Which system gives better performance to execute a program. The specifications of systems are given below. [3 Marks]

System-1 runs with 100MHZ processor. Program contains 200 instructions. ALU instruction, data transfer instruction, unconditional branch instruction and conditional branch instructions are 50%, 25%, 5% and 20% of the program respectively. ALU instruction, data transfer instruction, unconditional branch instruction and conditional branch instructions take 4, 2, 8 and 5 Clock Cycles respectively.

System-2 runs with 50MHZ processor. Program contains 150 instructions. ALU instruction, data transfer instruction, unconditional branch instruction and conditional branch instructions are 40%, 30%, 10% and 20% of the program respectively. ALU instruction, data transfer instruction, unconditional branch instruction and conditional branch instructions take 3, 2, 10 and 7 Clock Cycles respectively.

Solution Scheme: Step marking may be awarded.



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3. Long Answer Type Question [5 Marks]

(A) Explain the working principle of microprogrammed control unit design with proper block diagram. Why hardwired control unit is faster than microprogrammed control unit. [2 Marks]

Solution scheme: Explain the working principle of microprogrammed control unit design with proper block diagram (1.5 Mark)

Why hardwired control unit is faster than microprogrammed control unit. (0.5 Mark)

(B) Initially the stack pointer SP contains 5000 and keeping a value 1000 in top of the stack. What are the content of PC, SP, and the top of the stack? [3 Marks]

i) After the subroutine call instruction is executed in the main program?

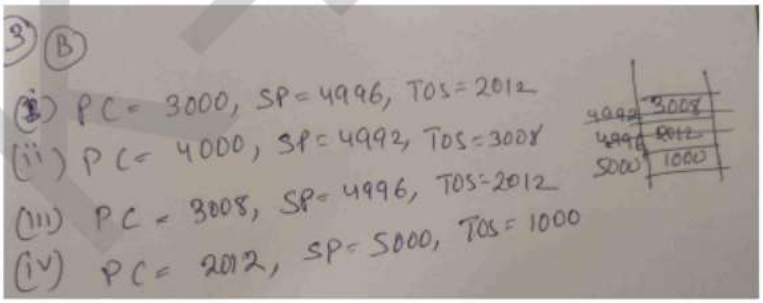
ii) After the subroutine call instruction is executed in the subroutine SUB1?

iii) After the return from SUB2 subroutine?

iv) After the return from SUB1 subroutine?

Main Routine	Subroutine-1 (SUB1)	Subroutine-2 (SUB2)
2000: ADD R1, R2	3000: AND R11, R12	4000: OR R8, R9
2004: SUB R4, R5	3004: CALL SUB2	4004: DIV R10, R12
2008: CALL SUB1	3008: RETURN	4008: RETURN
2012: MUL R3, R6		

Solution Scheme: If all 4 bits are correct then full mark(i.e.3) will be awarded otherwise step marking may be awarded.



4. Long Answer Type Question [5 Marks]

A) Write the assembly language programs for "SAFEPUSH" and "SAFEPOP". Assume stack address space ranges from 2000 to 1000 and stack grows in decreasing order (upwards). Assume instruction is 1word, 1word = 4 bytes and byte addressable.[2 Marks]

Solution Scheme: Step marking may be awarded.

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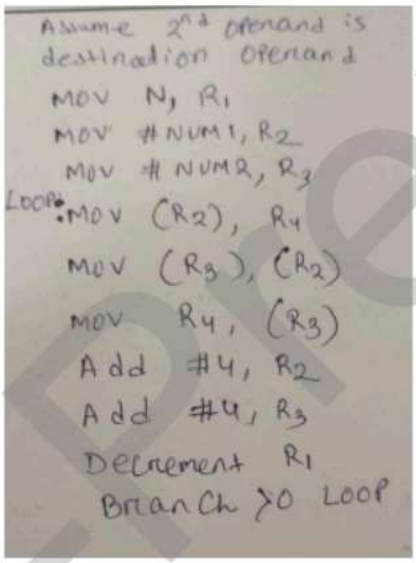
SAFEPOP (1 Mark)	SAFEPUSH (1 Mark)
Compare #2000, SP	Compare #1000, SP
Branch>0 EMPTYERROR	Branch <=0 FULLERROR
MOV (SP)+, ITEM	MOV NEWITEM, -(SP)

B) Write an assembly language program to swap two single dimensional arrays with same size. The starting address of first array is NUM1. Similarly, the starting address of second array is NUM2. The total number of integers is kept in memory locations N. Assume machine is 32 bit and byte addressable.[3 Marks]

Solution Scheme: Step marking may be awarded. This is one sample answer. Another type of sample answer can be possible like autoincrement.



5. Long Answer Type Question [5 Marks]

A) Draw the schematic diagram of three bus CPU organization. Why Constant 4 is used in three bus CPU organization?[2 Marks]

Solution Scheme: Draw the schematic diagram of three bus CPU organization. (1 Mark)

Why Constant 4 is used in three bus CPU organization? (1 Mark)

B) Write the control signals for the following instructions using single bus architecture (Assume instruction is 1 word, machine is 32 bits and byte addressable). [3 Marks]

I1: CALL SUB1 //SUB1 is a subroutine

I2: RETURN

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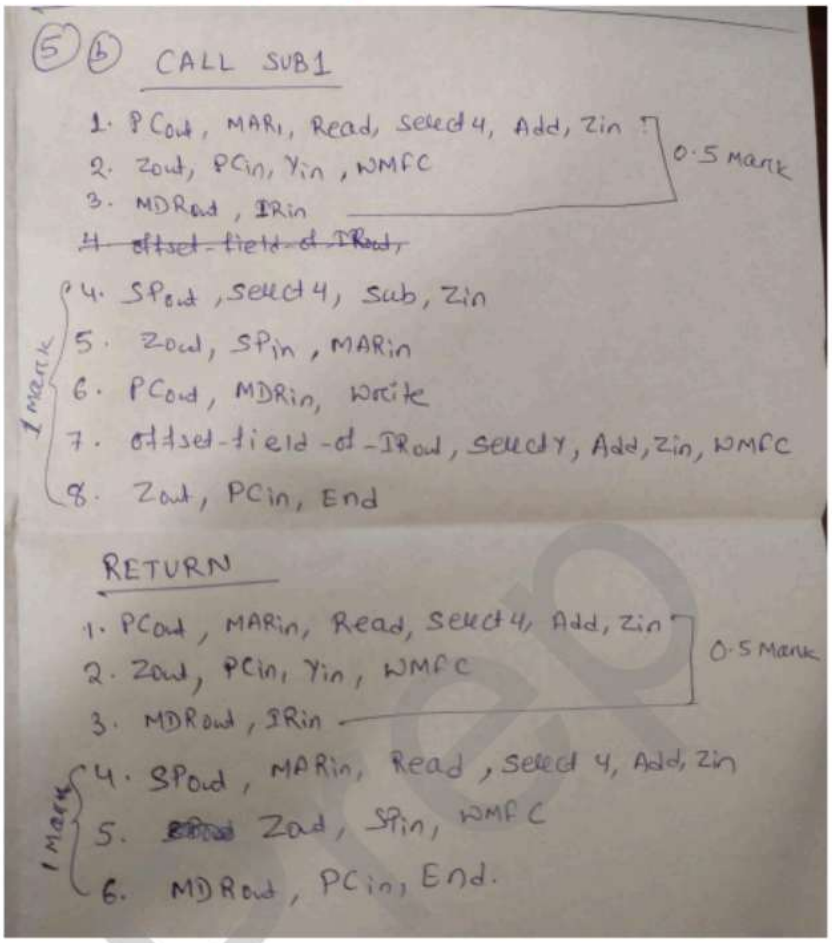
Solution Scheme: Step marking may be awarded.



*** Best of Luck ***