Semester: 3rd
Subject Name:- Comp. Arch. & Code:- CS 21
Branch (s): - IT, CSSE

AUTUMN **MID SEMESTER EXAMINATION-2024**

School of Computer Engineering
Kalinga Institute of Industrial Technology, Deemed to be University
Computer Organization and Architecture
[CS-21002]

Time: 1 1/2 Hours **Full Mark: 20**

Answer Any four questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. Answer all the questions. [1 Mark X 5]

a) Why constant 4 in MUX is present in three bus architecture?
b) Explain the compare instruction and discuss the need of compare instruction with the help of a suitable example.
c) After branch instruction execution, PC will updated to _____ ? (initial value of R3=200, R4=400 and SUB R3, R4 is equivalent to R4<- [R4]-[R3])
(i) If branch instruction is "Branch >0 1000"
(ii)Ifbranch instruction is "Branch <0 2000"

Memory Location	Instruction
1000	SUB R3, R4
1004	Branch instruction

d) The content of register R1 is 10101011. What will be the decimal value of the content of R1 after executing the following instruction? Assume the number is represented in 2's complement format and the carry bit is zero.
RotateLC #2, R1 //RotateLeft through carry.
e) Write the control signals for instruction fetch in the three bus organization by using R=A.

2. (a) Draw the schematic diagram of the architecture of three bus CPU, clearly showing each component. Explain the function of each component. [2.5 Marks]
(b)Write the sequence of control steps required for single bus CPU organization of the following instruction: (2nd Operand is the destination operand) [2.5Marks]
SUB R1, 50(R2)
ADD -(R2), R3

3. (a) Represent a number "-500" in little endian and big endian format starting at address 1000. The machine is byte addressable and each word consists of 2 bytes. [2.5Marks]

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(b) If a 10GHz computer takes 5 clock cycles for ALU instructions, 13 clock cycles for branch instructions and 3 clock cycles for data transfer instructions. Then find the total time taken by the computer to execute the program consists of 200 number of instruction and number of ALU instructions is 50% , number of branch instructions is 20% and number ofdata transfer instructions is 30% . [2.5Marks]

4.(a) How many memory references are required to fetch and execute the following instruction? Also calculate the effective address of the following instruction. (2^{nd} operand is the destination)

(i)ADD (R5),R6 (ii)ADD 1000, R1 (iii) SUB R2, 20(R1) [2.5Marks]

(b) Before the following program is executed, assume that the content of memory location 3000 is 7 and the content of register R5 is 2000. The content of each of the memory locations from 2000 to 2010 is 20. [Here, the 2^{nd} operand is the destination] [2.5Marks]

INSTRUCTION
MOV 3000, R1
L1: MOV (R5), R2
ADD R1, R2
MOV R2, (R5)+
Decrement R1
Branch≠0 L1
HALT

What will be the content in memory locations from 2000 to 2010 after the program is executed?

5. (a)Write a program to evaluate the given arithmetic expression :- X= A – (B – C * D + E) /F

i) Using a stack organized computer with zero-address operation instructions.

ii) Using RISC computer instruction format. [2.5Marks]

(b) Given the following program fragment

Main Program	First Subroutine SUB1	Second Subroutine SUB2
1000: ADD R1, R2	5000: ADD R1,R2	6000 SUB R6, R1
1004: CALL SUB1	5004: CALL SUB2	6004 XOR R1, R5
1008: MUL R4, R5	5008: RETURN	6008 RETURN

Initially the stack pointer SP contains 8000.

What are the content of PC, SP, and the top of the stack? [2.5Marks]

i) After the subroutine call instruction is executed in the main program?

ii) After the subroutine call instruction is executed in the subroutine SUB1?

iii) After the return from SUB2 subroutine?

*** Best of Luck ***