5. What is the content of x5 and x6 after execution of the following assembly code on RV32I?

Source code

```
.data
num: .zero 10
.text
la x22,num
addi x5,x0,0x380
sw x5,0(x22)
lb x6,0(x22)
```

- x5=0x0000 0380 and x6=0x0000 0080
- x5=0xFFFF F380 and x6=0xFFFF FF80
- x5= 0x0000 0380 and x6=0x0000 0380
- x5=0x0000 0380 and x6=0xFFFF FF80

6. In RV32I, Assume content of x5=0xFFFF FFFF.
a) If the Instruction executed is **xori x6, x5, -1** then what is the content of x6?
b) If the Instruction executed is **xori x0, x5, -1** then what is the content of x6?

- None of these
- a) x6=0x0000 0000
  b) x0=0x0000 0000
- a) x6=0xFFFF FFFF
  b) x0=0x0000 0000
- a) x6=0x0000 0000
  b) x0=0x0000 0000

7.
Assume, PCpresent= 0x0000 0010 and the following instructions are executed. What is the content of x11 and X12 after execution of following sequence
auipc x11, 0x0FFF6
addi x12, x11,-1

- None of these
- x11= 0x0FFF 6010 and x12= 0x0FFF 600F
- x11= 0x0FFF 6010 and x12= 0x0FFF 6009
- x11= 0x0FFF 6010 and x12= 0x0FFF 60FF

8. Choose the matching answer to indicate the stages of datapath used/active by following Instructions when they enter the datapath
a) lw x10,0(x12)
b) sw x10,4(x12)
c) add x5,x6,x7
d) beq x1,x2,label

- a) IF,ID,EX,MEM,WB
- b) IF,ID,EX,MEM
- c) IF,ID,EX,WB
- d) IF,ID,EX

- a) IF,ID,EX,MEM,WB
- b) IF,ID,EX,MEM,WB
- c) IF,ID,EX,WB
- d) IF,ID,EX,MEM

- a) IF,ID,EX,MEM
- b) IF,ID,EX,MEM
- c) IF,ID,EX,WB
- d) IF,ID,EX

- a) IF,ID,EX,MEM,WB
- b) IF,ID,EX,MEM
- c) IF,ID,EX
- d) IF,ID,EX,MEM,WB

9. In RV32I, What will be the content of x10 after execution srai x10,x10,2. Assume x10= -88 before execution.

- -44
- -11
- -22
- None of these

10.
What will the content of x10 be after the execution of the following instructions? Assume x10=0x05 before execution
addi x10,x0,0x800

- None of these
- x10=0x00000800
- x10=0x000007FF
- x10=0xFFFF F800

11.
Assume that **A is an array of 100 double-word unsigned numbers** and the **base address of the array A is in x22**. If A[20] is to be read from memory and copied into x12 then which Instruction you would use?

- ld x12,100(x22)
- lw x12,400(x22)
- ld x12,800(x22)
- ld x12,0(x22)

12. Assume x5= 0xFFFF FFFE and x6= 0x0000 0001
Will the execution of **blt x5,x6, exit** branches to label exit or not?

- Will not branch to label exit
- May or May not branch to label exit
- Will branch to label exit
- None of these

13. Branch Instructions use _____ addressing mode?

- Register Address Mode
- Base addressing Mode
- Immediate addressing Mode
- PC Relative addressing Mode

14. Which Instruction format jalr x5, 0x24(x10) belongs ?

- S Format
- J Format
- I Format
- R Format

15. What is the machine code of the sw x14, 8(x2).
The opcode and fun3 of sw instruction is 010 0011 and 010 respectively

- 0x00E12443
- 0x04E12423
- 0x00E12423
- None of these

16. In RV64 processor, What are the number of registers in the Register file?

- 32
- 128
- 64
- None of these

17. What will be the state of PCSrc when beq x0,x0, label execute?

- None of these
- PCSrc=0
- PCSrc=1
- It depends on zero=1 or zero=0

18. Assume the following sequence code is executed using 5-Stage RISC-V datapath without forwarding and hazard detaction unit. What should be the number of NOPs/Stalls to be introduced

```
lw    x4, 8(x31)
add   x3, x1, x2
sw    x3, 12(x31)
add   x5, x1, x4
```

- 1
- 0
- 2
- None of these

19. In the 5-stage pipelined RISC-V processor, the hazard Detection Unit wants to check if the Instruction in EX stage is a load Instruction. Which of the following conditions it would check?

- if (ID/EX.MemRead)
- if (EX/MEM.MemWrite)
- if (ID/EX.RegWrite)
- None of these

20. Consider the following mix of instructions

R-type	I-type (non-load)	Load	Store	Branch	Jump
20%	30%	22%	13%	12%	3%

What %age of Instructions use the RegWrite Control signal?

- 65%
- 77%
- 72%
- 100%

21. If the following sequence of instructions executes on a 5-stage pipelined RISC-V with a forwarding unit, then how many NOP/stalls are to be introduced?
lw x2,0(x10)
add x5,x6,x2

- 0
- 2
- 1
- None of these

22. In a 5-stage pipelined architecture if T_{IF} = 200ps, T_{ID} = 170ps, T_{EX} = 210ps, T_{MEM} = 200ps, and T_{WB} = 100ps then what will be Tclk ?

- Tclk = 880 ps
- Tclk = 100 ps
- Tclk = 210 ps
- Tclk = 200 ps

23. What is the state of the control signals generated by the main control unit if the sw x10,0(x21) is executed?

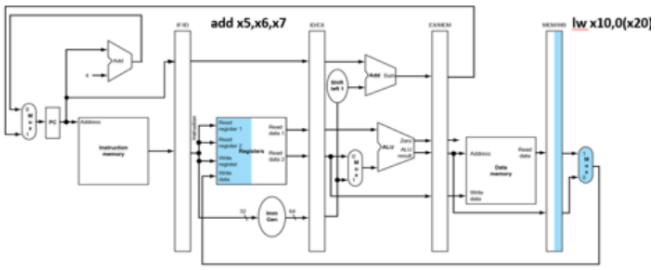
ALUop[2]	ALUSrc	MemRead	MemWrite	Branch	MemtoReg	RegWrite
00	0	0	1	0	x	0

ALUop[2]	ALUSrc	MemRead	MemWrite	Branch	MemtoReg	RegWrite
00	1	0	1	0	x	1

None of these

ALUop[2]	ALUSrc	MemRead	MemWrite	Branch	MemtoReg	RegWrite
00	1	0	1	0	x	0

24. Assume add x5,x6,x7 is in the ID stage and lw x10,0(x20) is in the WB stage. As per the given architecture the lw writes the result into _____ register?



x10

x5

None of these

Both x5 and x10