LINEAR INTEGRATED CIRCUITS

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Unit 2 Simultaneous equations with m < 1 (attenuation)

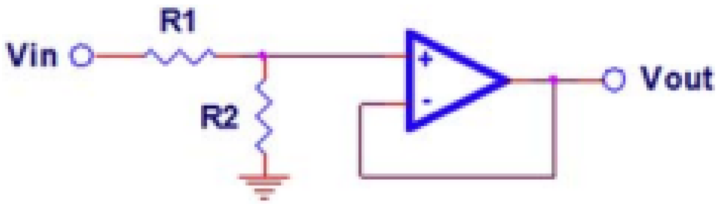
- Linear op amp transfer function is limited to equation of straight line $y = +/-mx+/-b$, where m is gain, b is offset, x is input and y is output

Table 5.1: The Gain and Offset Matrix

		b < 0	b = 0	b > 0
Noninverting	$m > 1$	Case 2 (Section 4.4.2)	Noninverting gain (Section 2.3)	Case 1 (Section 4.4.1)
	$m = 1$	Section 5.4	Noninverting buffer (Section 5.7)	
	$m < 1$		Section 5.2	Section 5.3
	$m = 0$	Negative reference or regulator (Chapter 21)	Ground	Positive reference or regulator (Chapter 20)
Inverting	$m < -1$	Section 5.7	Section 5.5	Section 5.6
	$m \geq -1$	Case 4 (Section 4.4.4)	Inverting gain (Section 2.4)	Case 3 (Section 4.4.3)

Table represents different combination of **m** and **b**

Unit 2 Non inverting attenuator with zero offset, positive offset and negative offset

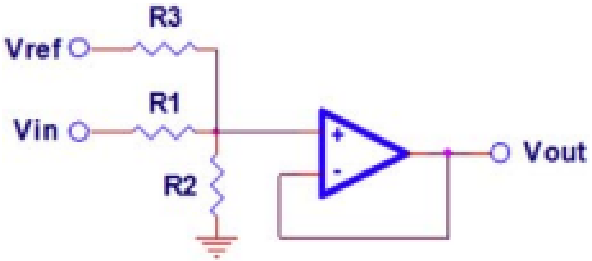


Circuit diagram

$$Vout = m \times Vin$$

$$m = \frac{R2}{R1+R2}$$ Gain

Non inverting attenuator with Zero offset



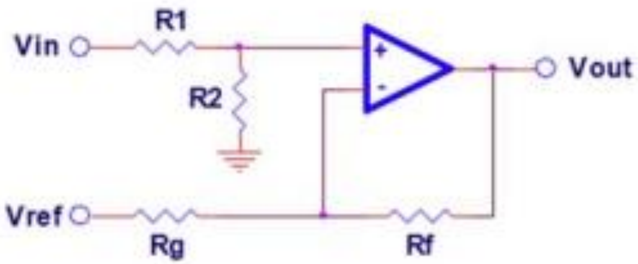
Circuit diagram

$$Vout = m \times Vin + b$$

$$m = \frac{1/R1}{1/R1 + 1/R2 + 1/R3}$$

$$b = Vref \times \frac{1/R3}{1/R1 + 1/R2 + 1/R3}$$

Non inverting attenuator with positive offset



Circuit diagram

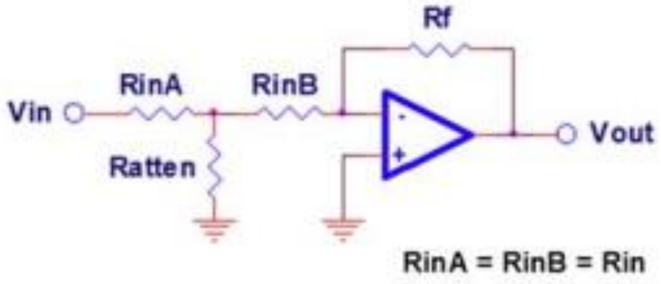
$$Vout = m \times Vin - b$$

$$m = \left(\frac{R2}{R1+R2}\right) \times \left(1 + \frac{Rf}{Rg}\right)$$

$$b = Vref \times \frac{Rf}{Rg}$$

Non inverting attenuator with negative offset

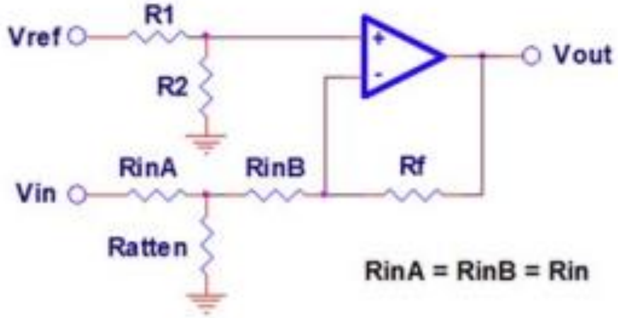
Unit 2 Inverting attenuator with zero offset, positive offset and negative offset



$$Vout = -m \times Vin$$

$$m = \frac{Rf \times Ratten}{Rin \times (Rin + 2 \times Ratten)}$$

Inverting attenuator with Zero offset

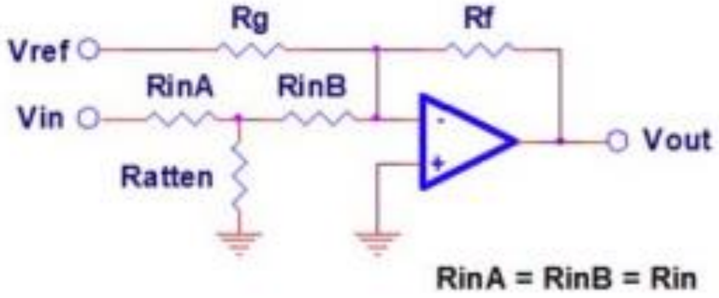


$$Vout = -m \times Vin + b$$

$$m = \frac{Rf \times Ratten}{Rin \times (Rin + 2 \times Ratten)}$$

$$b = Vref \times \left(\frac{R2}{R1 + R2}\right) \times \left(1 + \frac{Rf}{Rin + Rin \| Ratten}\right)$$

Inverting attenuator with Positive offset



$$Vout = -m \times Vin - b$$

$$m = \frac{Rf \times Ratten}{Rin \times (Rin + 2 \times Ratten)}$$

$$b = Vref \times \frac{Rf}{Rg}$$

Inverting attenuator with Negative offset

General summary points while considering non ideal scenario

- Concept of DC errors and AC errors
  - DC errors are offset voltage and input bias current, they are constant over entire frequency range
  - AC errors are CMRR, PSRR, differential gain, they can not be ignored at high frequencies
- Inaccuracies related to op amp can be minimized using negative feedback
- Stability is usually an criteria when operating frequency is high
- Internally compensated and externally compensated op amp circuits are used for better stability.

Unit 2 Development of non ideal op amp equations

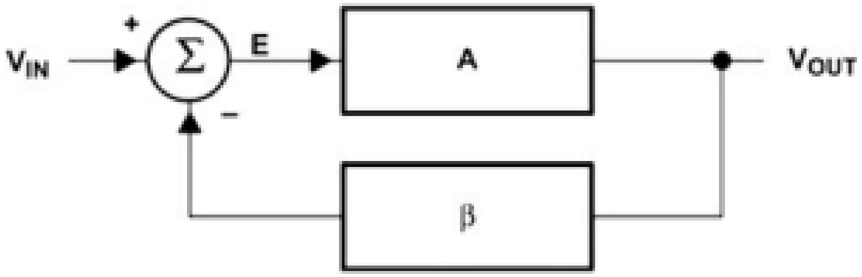


Figure 7.1
Feedback system block diagram.

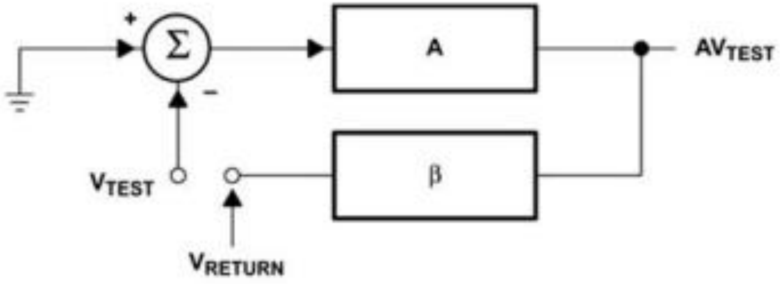


Figure 7.2
Feedback loop broken to calculate loop gain.

Transfer function,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta}$$

When loop gain is large, transfer function is,

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta}$$

Error indicator E, proportional to signal and inversely proportional to loop gain

$$E = \frac{V_{IN}}{1 + A\beta}$$

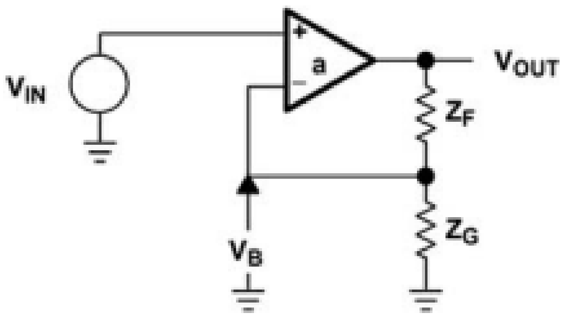


Figure 7.3
Noninverting op amp.

amplifier transfer equation.

$$V_{OUT} = a(V_{IN} \pm V_B)$$

--------- 1

V_B calculated based on resistor divider from V_{OUT}

$$V_B = \frac{V_{OUT}Z_G}{Z_F + Z_G} \quad \text{for } I_B = 0$$ --------- 2

From 1 and 2,

$$V_{OUT} = aV_{IN} - \frac{aZ_G V_{OUT}}{Z_G + Z_F}$$

After simplification,

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}}$$ ------- 3

In the form of closed loop function,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta}$$ ------- 4

By comparing 3 and 4, **loop gain** is given by,

$$A\beta = \frac{aZ_G}{Z_G + Z_F}$$

Unit 2 Development of non ideal op amp equations - Non Inverting amp

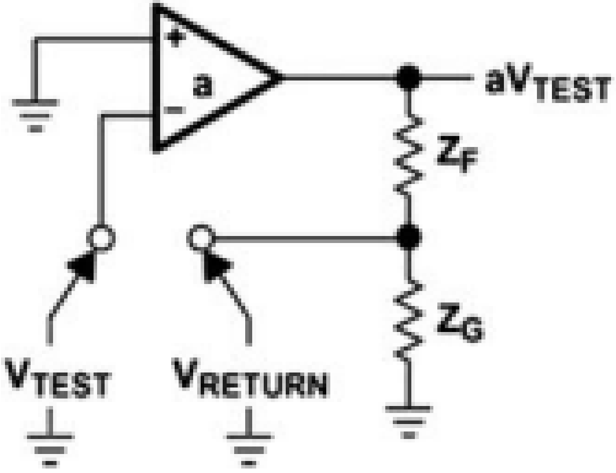


Figure 7.4
Open-loop noninverting op amp.

$$V_{RETURN} = \frac{aV_{TEST}Z_G}{Z_F + Z_G}$$

$$\frac{V_{RETURN}}{V_{TEST}} = A\beta = \frac{aZ_G}{Z_F + Z_G}$$

For measurement loop gain, break the loop, apply test signal at one end and measure voltage at the other end

Unit 2 Development of non ideal op amp equations Inverting amp

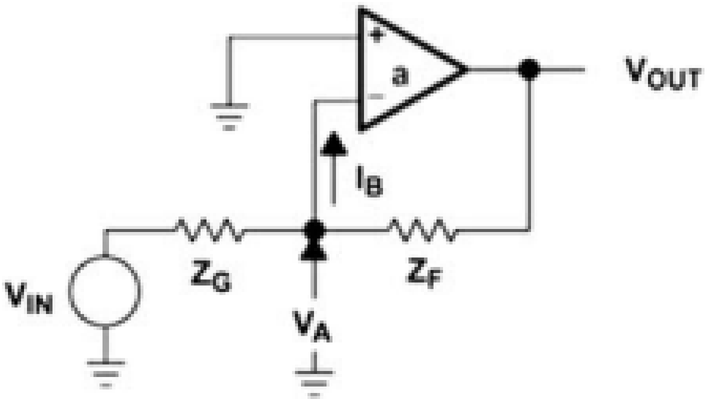


Figure 7.5
Inverting op amp.

Using superposition theorem, calculate voltage V_A

$$V_A = \frac{V_{IN}Z_F}{Z_G + Z_F} + \frac{V_{OUT}Z_G}{Z_G + Z_F} \quad \text{for } I_B = 0 \qquad \text{--------5}$$

$$V_{OUT} = -aV_A$$

Simplifying equation 5

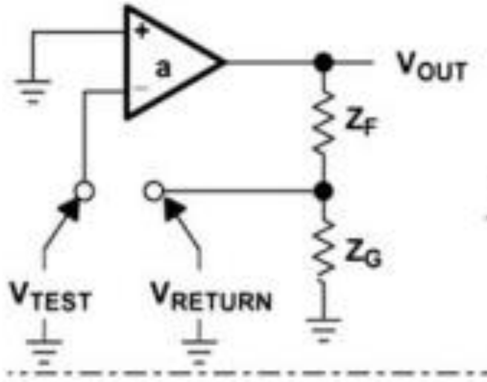
$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{-aZ_F}{Z_G + Z_F}}{1 + \dfrac{aZ_G}{Z_G + Z_F}}$$

open loop gain

loop gain

- Open loop gain is different compared to non inverting amp
- Loop gain is same compared to non inverting amp

Unit 2 Development of non ideal op amp equations - Inverting amp



$$\frac{V_{RETURN}}{V_{TEST}} = a\frac{Z_G}{Z_F + Z_G}$$

Figure 7.6
Inverting op amp: feedback loop broken for loop gain calculation.

$$\frac{V_{RETURN}}{V_{TEST}} = \frac{aZ_G}{Z_G + Z_F} = A\beta$$

Loop gain

For measurement of loop gain, break the loop, apply test signal at one end and measure voltage at the other end

Unit 2 Development of non ideal op amp equations - Differential amp

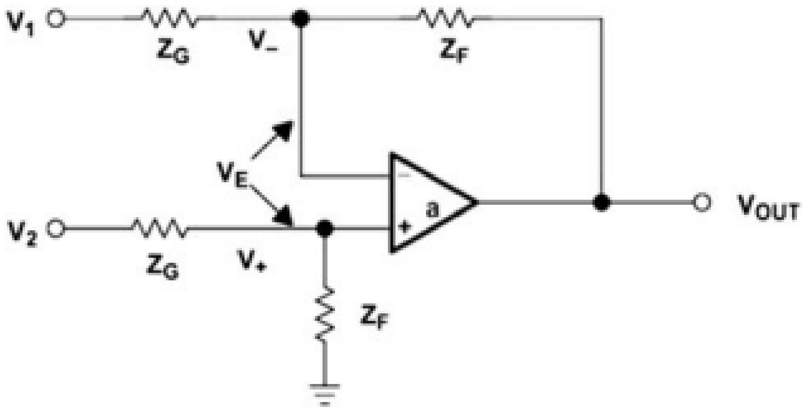


Figure 7.7
Differential amplifier circuit.

: transfer equation.

$$V_{OUT} = aV_E = \cancel{V_+ + V_-}$$

$a(V_+ + V-)$

Voltage at non inverting terminal is calculated as,

$$V_+ = V_2 \frac{Z_F}{Z_F + Z_G}$$

Voltage at inverting terminal is calculated as,

$$V_- = V_1 \frac{Z_F}{Z_F + Z_G} - V_{OUT} \frac{Z_G}{Z_F + Z_G}$$

Voltage at output, using super position theorem,

$$V_{OUT} = a\left[\frac{V_2 Z_F}{Z_F + Z_G} - \frac{V_1 Z_F}{Z_F + Z_G} - \frac{V_{OUT} Z_G}{Z_F + Z_G}\right] \quad \text{----1}$$

Unit 2 Development of non ideal op amp equations Differential amp

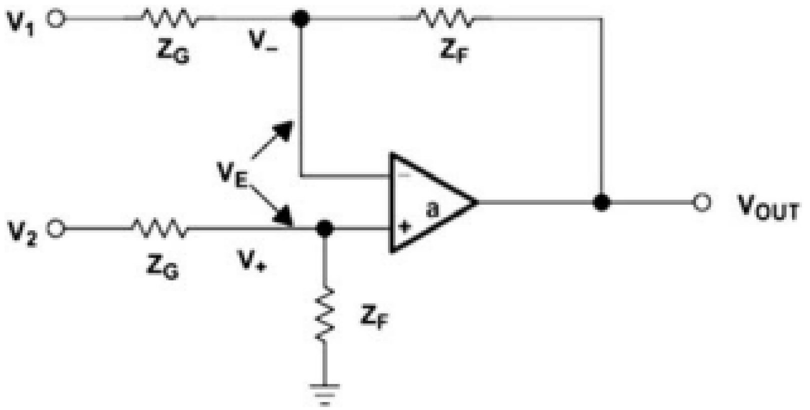


Figure 7.7
Differential amplifier circuit.

After simplifying equation 1 of previous slide,

open loop gain

loop gain

$$\frac{V_{OUT}}{V_2 - V_1} = \frac{\dfrac{aZ_F}{Z_F + Z_G}}{1 + \dfrac{aZ_G}{Z_F + Z_G}}$$

- Loop gain is same compared to non inverting amp and inverting amp

Operating Region

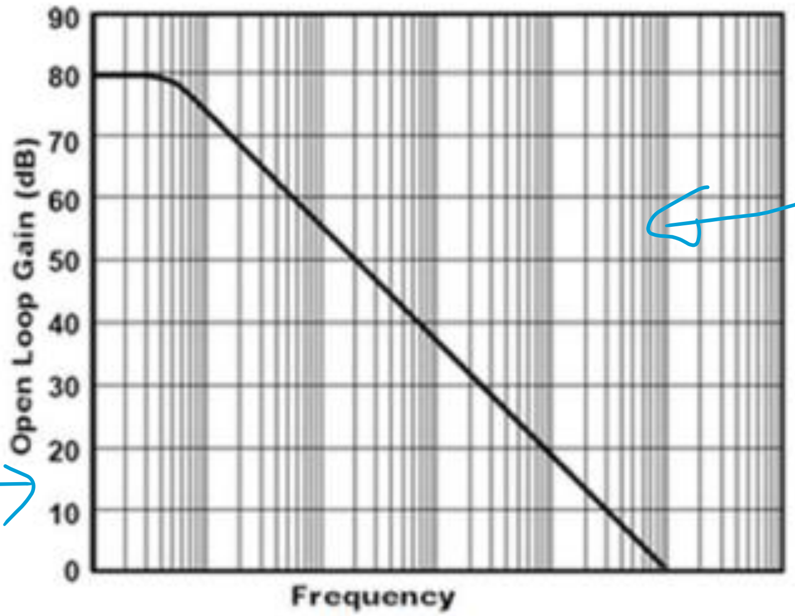


Figure 7.8
Bode response of a typical op amp.

Not an operating region

From Bode plot, clearly non operating region and operating region can be divided

When open loop gain is high

noninverting op amp:

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

when a >> $\frac{V_{OUT}}{V_{IN}} = 1 + \frac{Z_F}{Z_G}$

When open loop gain is high

inverting op amp stage:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{-aZ_F}{Z_G + Z_F}}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

when a >> $\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_G}$

Results in ideal op amp relation

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Different scenarios for changes in a, R_G and R_F

Non ideal transfer function for inverting op amp

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{-aZ_F}{Z_G + Z_F}}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

Table 7.1: Real Inverting Op Amp Stage Gains for a = 80 dB

a	R_G	R_F	Attempted	Actual	Error (%)
10,000	100,000	100,000	−1	−0.9998	−0.0200
10,000	10,000	100,000	−10	−9.9890	−0.1099
10,000	1000	100,000	−100	−99.0001	−0.9999
10,000	100	100,000	−1000	−909.0083	−9.0992
10,000	10	100,000	−10,000	−4999.7500	−50.0025
10,000	1	100,000	−100,000	−9090.8264	−90.9092
10,000	1	1.00E + 12	−1E + 12	−9999.9999	−100

Error is more for higher gains

Non ideal transfer function for non inverting op amp

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

Table 7.2: Real Noninverting Op Amp Stage Gains for a = 80 dB

a	R_G	R_F	Attempted	Actual	Error (%)
10,000	100,000	100,000	2	1.9996	−0.0200
10,000	10,000	100,000	11	10.9879	−0.1099
10,000	1000	100,000	101	99.9901	−0.9999
10,000	100	100,000	1001	909.9173	−9.0992
10,000	10	100,000	10,001	5000.2500	−50.0025
10,000	1	100,000	100,001	9090.9174	−90.9092
10,000	1	1.00E + 12	1E + 12	9999.9999	−100

In actual scenario, operating region is much lesser

operating region

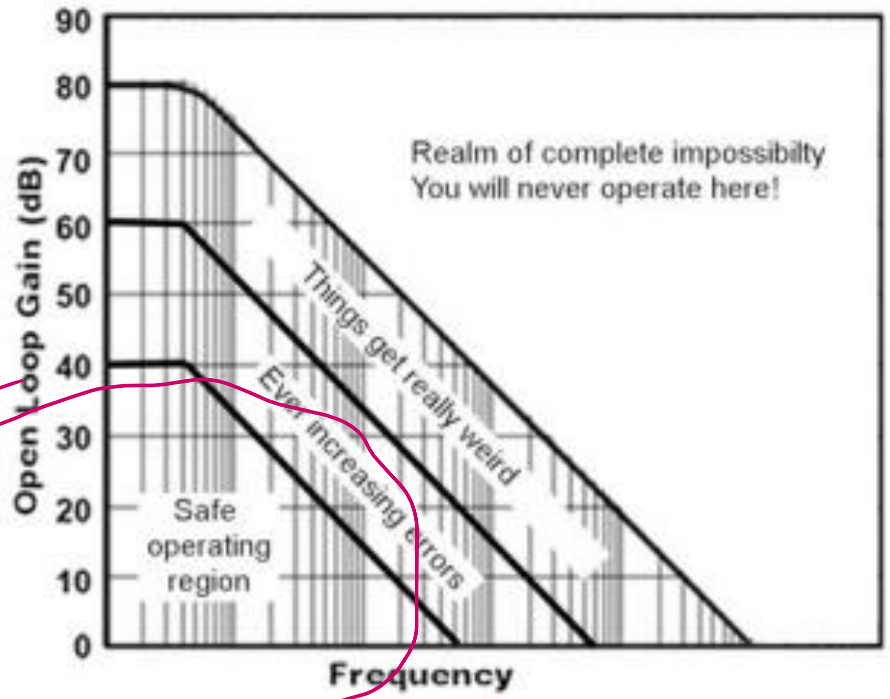
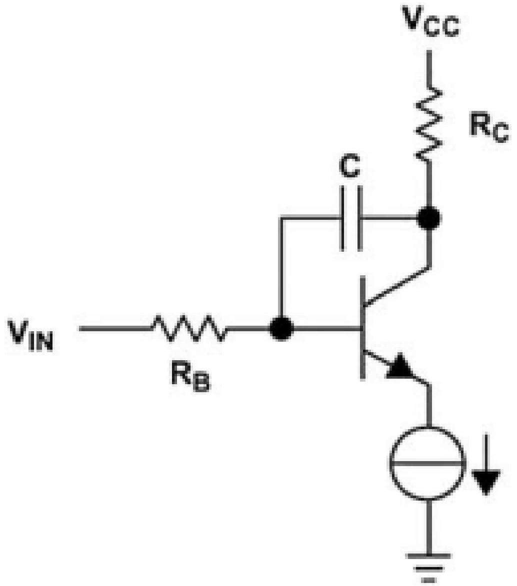


Figure 7.9
Bode response representation of safe operating region.

Background

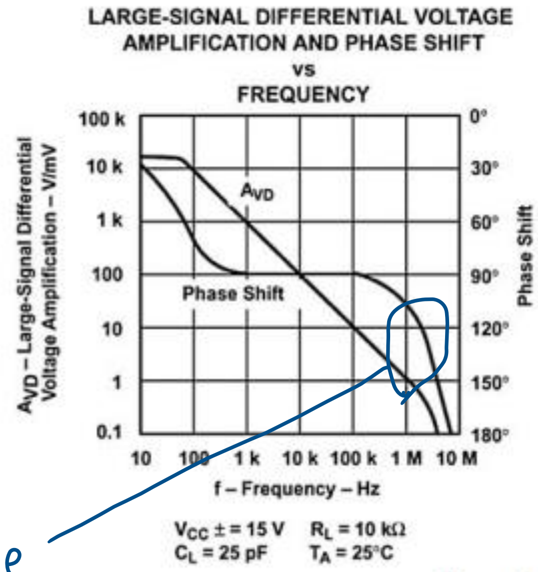
- Oscillations are considered as boundary between stability and non stability
- Poor stability circuit exhibits ringing and overshoot
- Phase margin is one measure for stability of the circuit
- Compensation provides patch between stability and performance
- Compensation network is by RC network

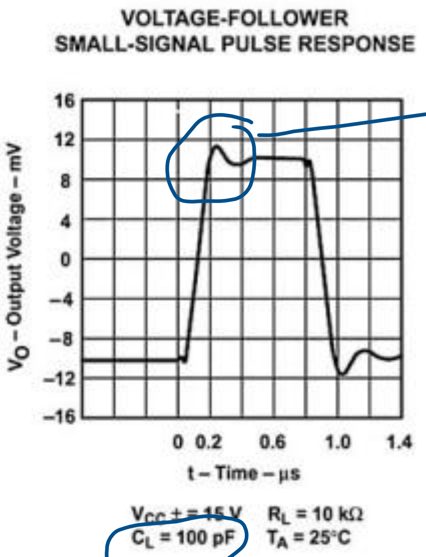
Unit 2 Voltage feedback op amp compensation - Internal compensation



A capacitor C connected between input and output for compensation, called internal compensation capacitor, it is part of IC

Phase margin 72°



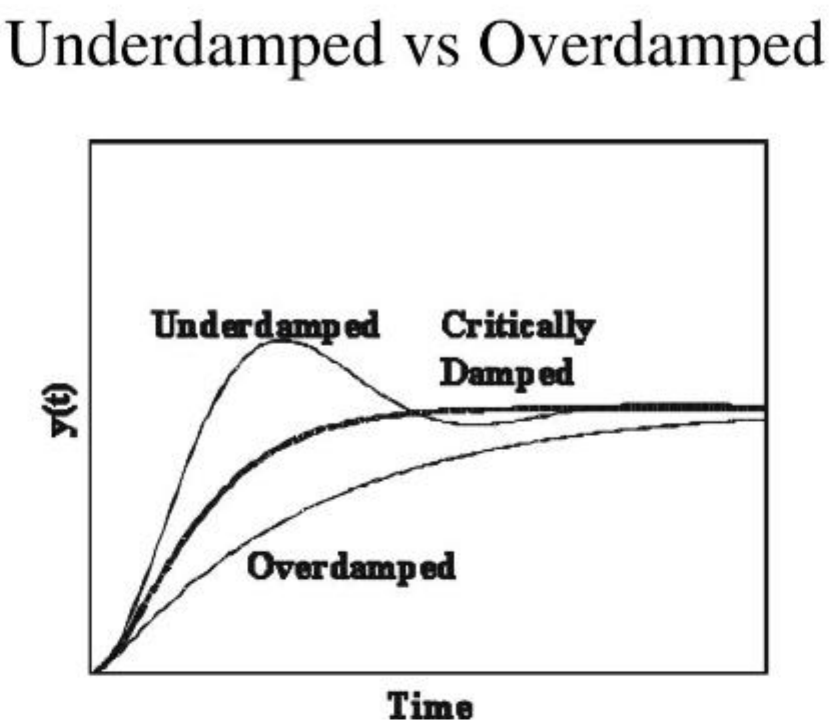


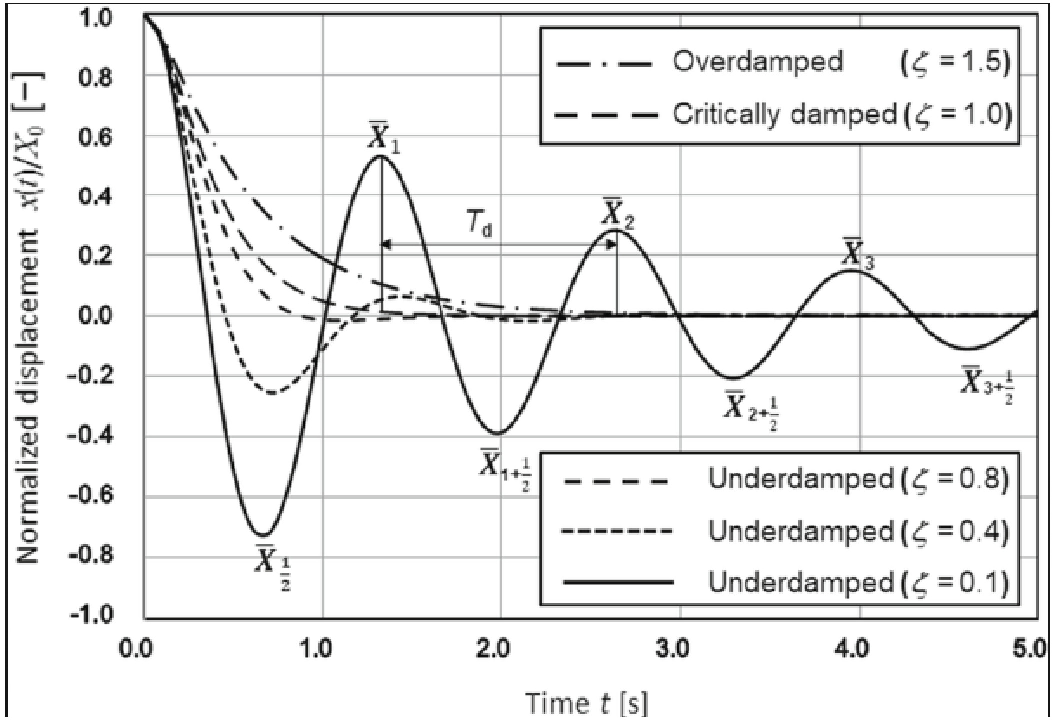
overshoot 10%

Plot of internally compensated op amp

loading capacitor changes phase margin

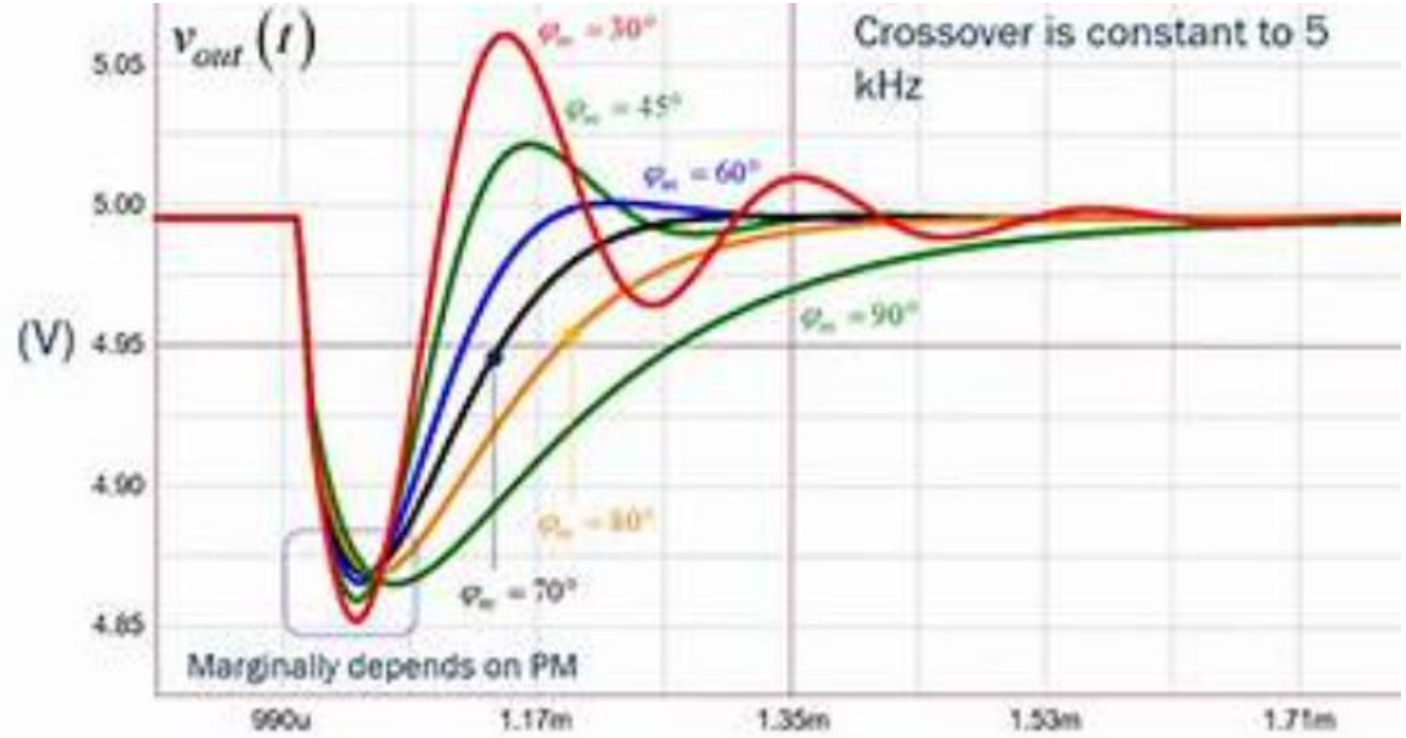
Unit 2 Voltage feedback op amp compensation - Internal compensation





Critically damped circuits are preferred over other types. They settle faster with minimum overshoot

Unit 2 Voltage feedback op amp compensation - Internal compensation

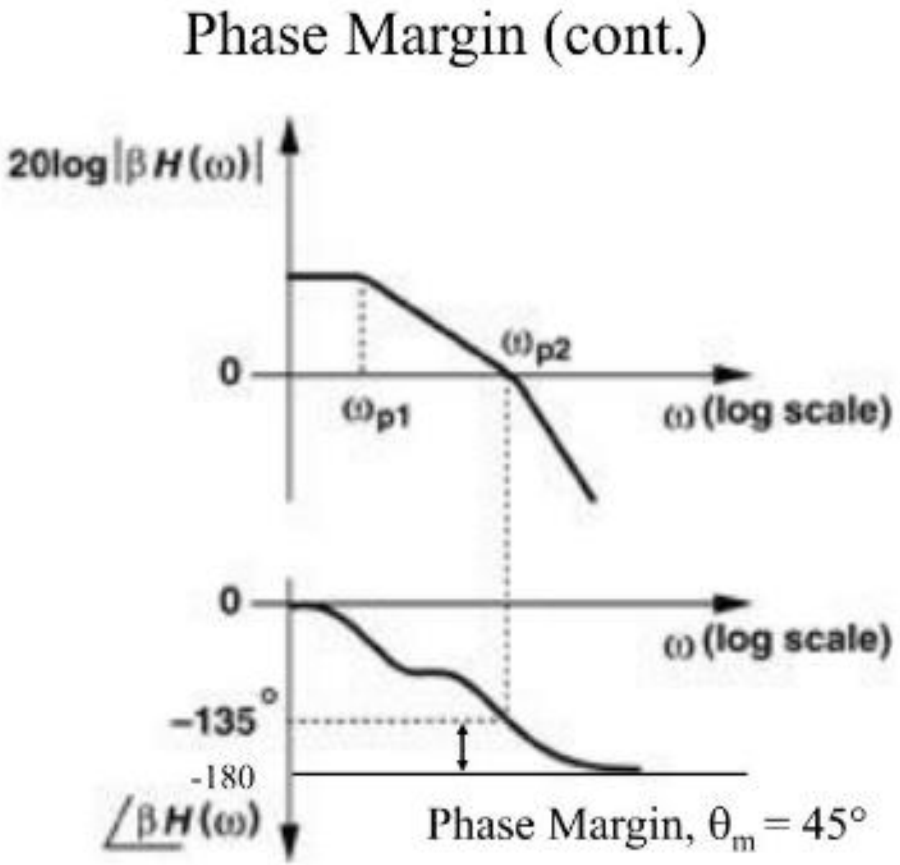


For critically damped circuits, phase margin has to be around 60 degrees

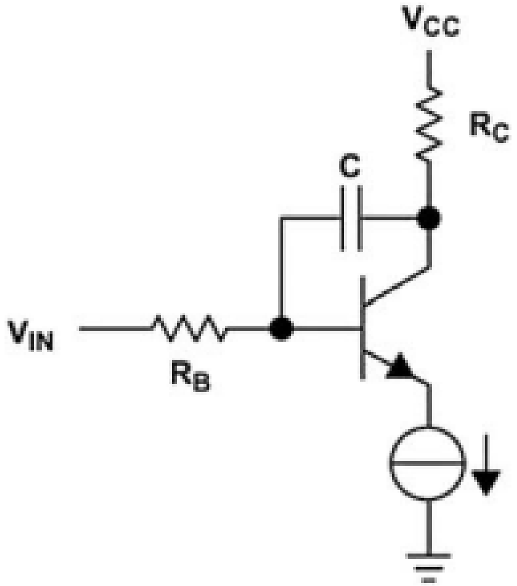
Unit 2 Voltage feedback op amp compensation - Internal compensation

Bode plot

- Decrease in gain for pole frequency
- Phase shift of -90 degrees at pole frequency
- Increase in gain for zero frequency
- Phase shift of +90 degrees at pole frequency



Unit 2 Voltage feedback op amp compensation Internal compensation



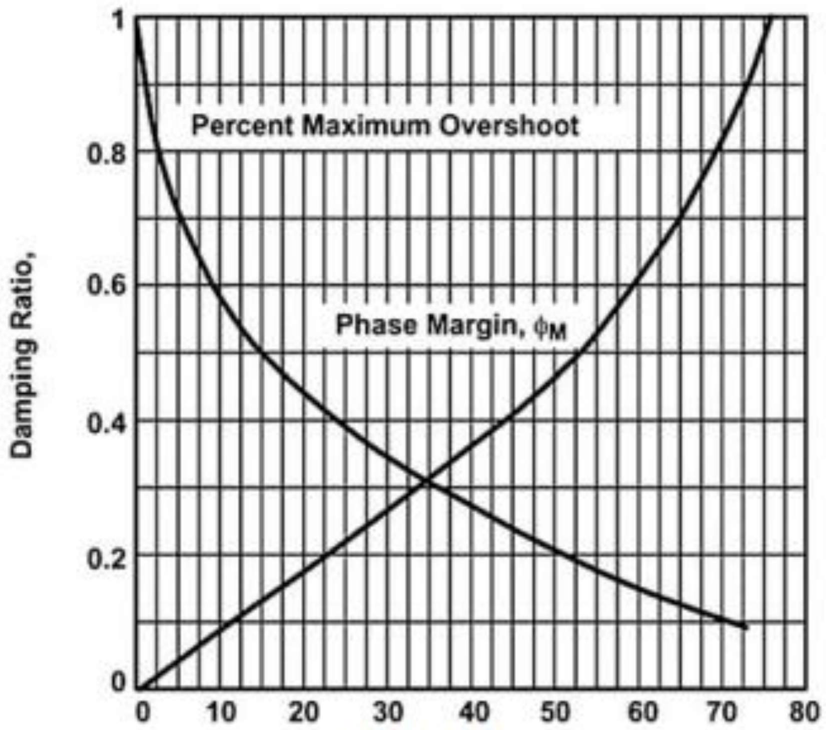


Figure 8.3

Phase margin and percent overshoot versus damping ratio.

Plot of internally compensated op amp, measure of phase margin with damping ratio and overshoot (Data sheet for TL03X)

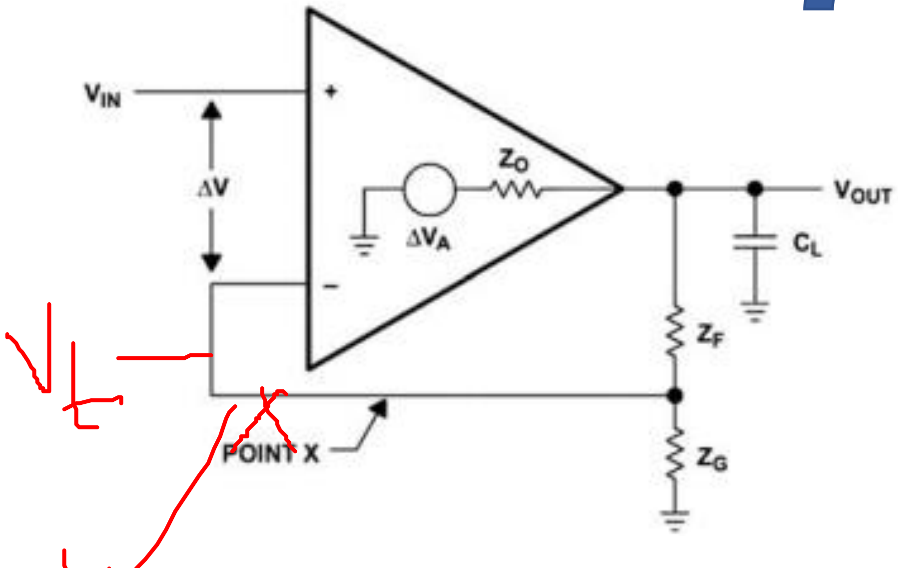
Summary points

- High frequency noise reduction by closed loop configuration
- Improve phase margin in turn improving stability
- Reduce overshoot by having better phase margin
- Compensation can be tailored to the circuit requirement

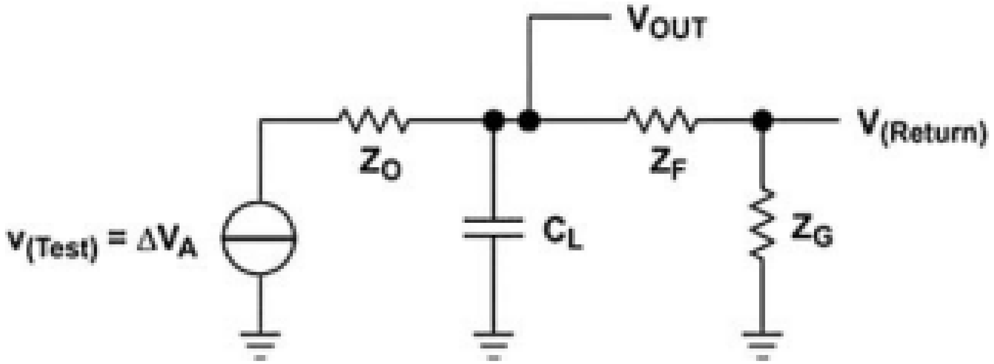
Unit 2 Dominant pole compensation

- In this type of compensation, an output capacitor is added
- Combination of output capacitor and output impedance forms dominant pole (a low frequency pole)

Circuit transformation



Loop broken for loop gain calculations



Equivalent circuit after loop break

Unit 2 Dominant pole compensation

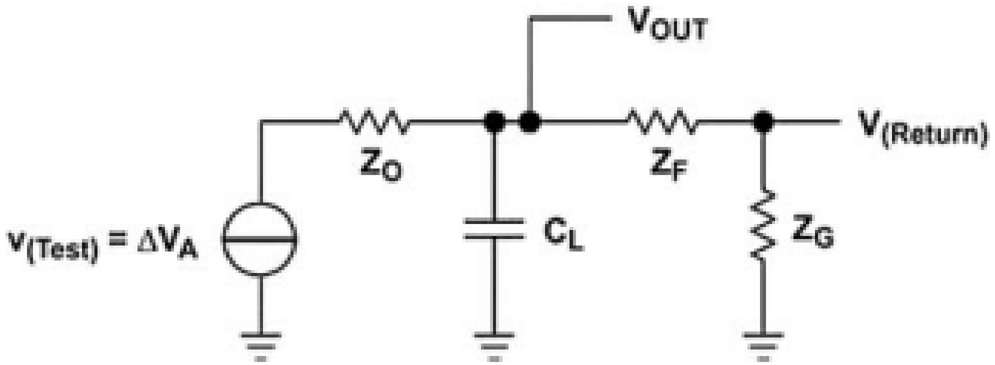


Figure 1

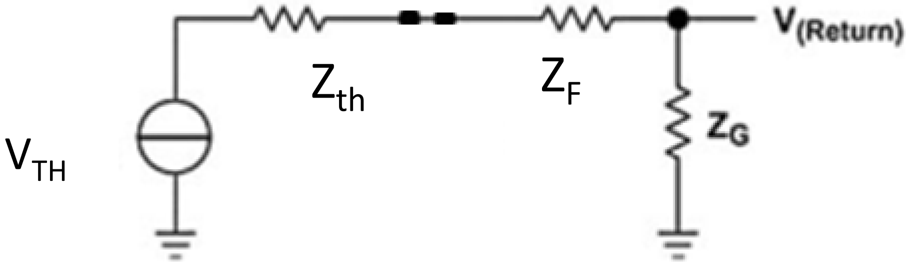


Figure 2

Apply Thevenin's theorem in Figure 1 to separate Z_o and C_L

$$V_{TH} = \frac{\Delta Va}{Z_O C_L s + 1}$$

$$Z_{TH} = \frac{Z_O}{Z_O C_L s + 1}$$

Calculate V_{return} voltage from Figure 2 using resistive divider theorem

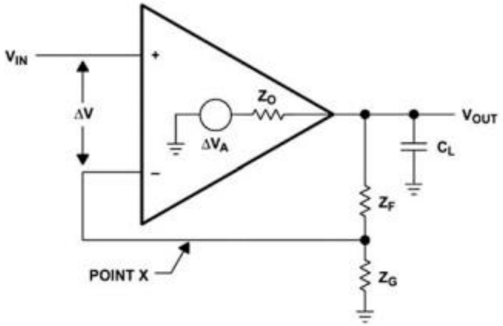
$$V_{RETURN} = \frac{V_{TH} Z_G}{Z_G + Z_F + Z_{TH}} = \frac{\Delta Va}{Z_O C_L s + 1}\left(\frac{Z_G}{Z_F + Z_G + \dfrac{Z_O}{Z_O C_L s + 1}}\right)$$

Unit 2 Dominant pole compensation

$$V_{RETURN} = \frac{V_{TH}Z_G}{Z_G + Z_F + Z_{TH}} = \frac{\Delta Va}{Z_O C_L s + 1}\left(\frac{Z_G}{Z_F + Z_G + \frac{Z_O}{Z_O C_L s + 1}}\right)$$

Here $\Delta V_a = aV_{test}$

Rearranging

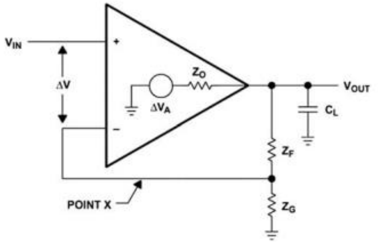


$$\frac{V_{RETURN}}{V_{TEST}} = A\beta = \frac{\frac{aZ_G}{Z_F + Z_G + Z_O}}{\frac{(Z_F + Z_G)Z_O C_L s}{Z_F + Z_G + Z_O} + 1}$$

When $(Z_F+Z_O) >> Z_O$

$$A\beta = \frac{aZ_G}{Z_F + Z_G}\left(\frac{1}{Z_O C_L s + 1}\right)$$

Unit 2 Dominant pole compensation



$$A\beta = \frac{aZ_G}{Z_F + Z_G}\left(\frac{1}{Z_O C_L s + 1}\right) \quad \text{-----1}$$

In case op-amp a second order system

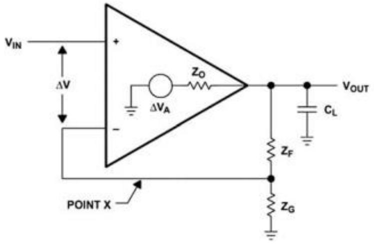
$$a = \frac{K}{(s+\tau_1)(s+\tau_2)} \quad \text{-----2}$$

From 1 and 2, Loop gain is equal to

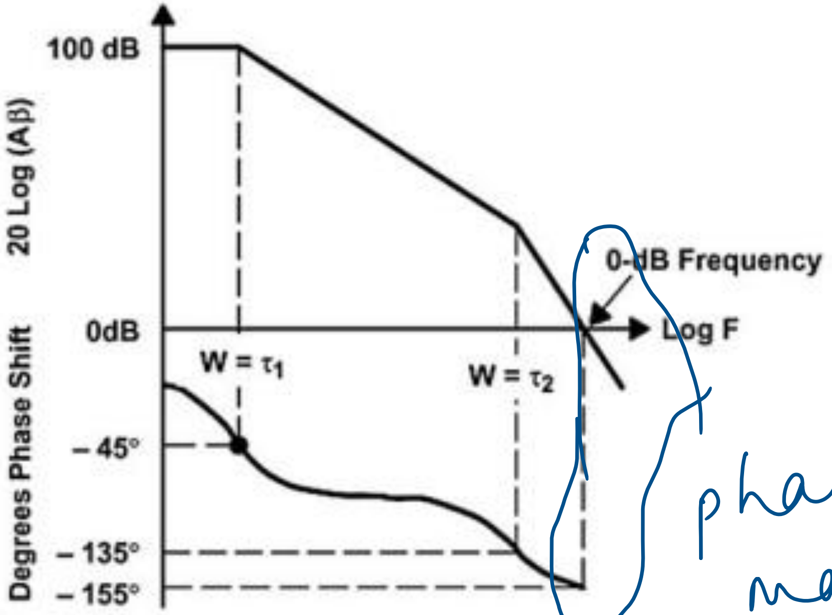
$$A\beta = \frac{K}{(s+\tau_1)(s+\tau_2)}\,\frac{Z_G}{Z_F + Z_G}\,\frac{1}{Z_O C_L s + 1}$$

It is a three pole System

Unit 2 Dominant pole compensation



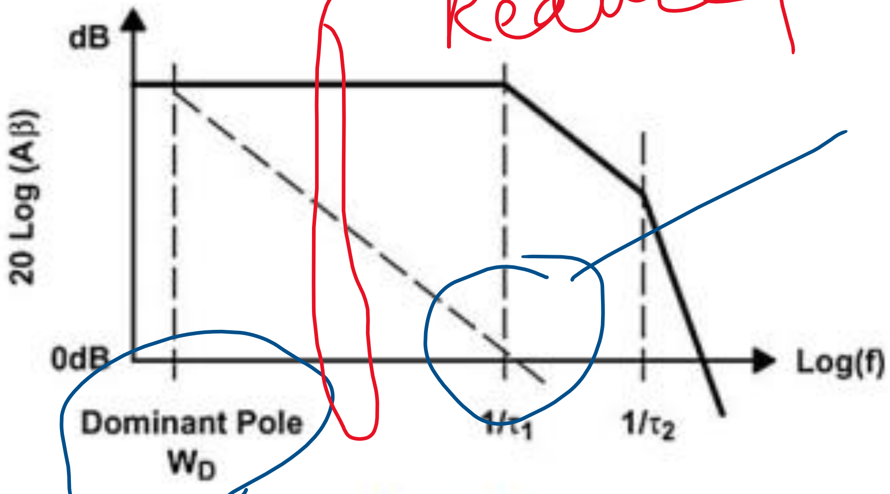
Bode plot without compensation



phase margin 25°

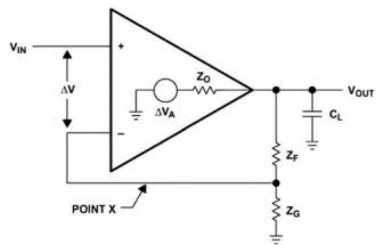
Bode plot with compensation

Gain Reduced



Phase margin around 45 degrees

Additional pole By compensation technique



Loop gain $$A\beta = \frac{aZ_G}{Z_F + Z_G}\left(\frac{1}{Z_O C_L s + 1}\right)$$

when $Z_0 << Z_F$

$$A\beta = \frac{aZ_G}{Z_G + Z_F}$$

Closed loop transfer function is given by (From slide 7)

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

when $a = \infty$

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_F + Z_G}{Z_G}$$

Which represents gain of non inverting amp in ideal conditions

Unit 2 Gain compensation

- Loop gain parameter and closed loop parameters are related

Loop gain $$A\beta = \frac{aZ_G}{Z_G + Z_F}$$

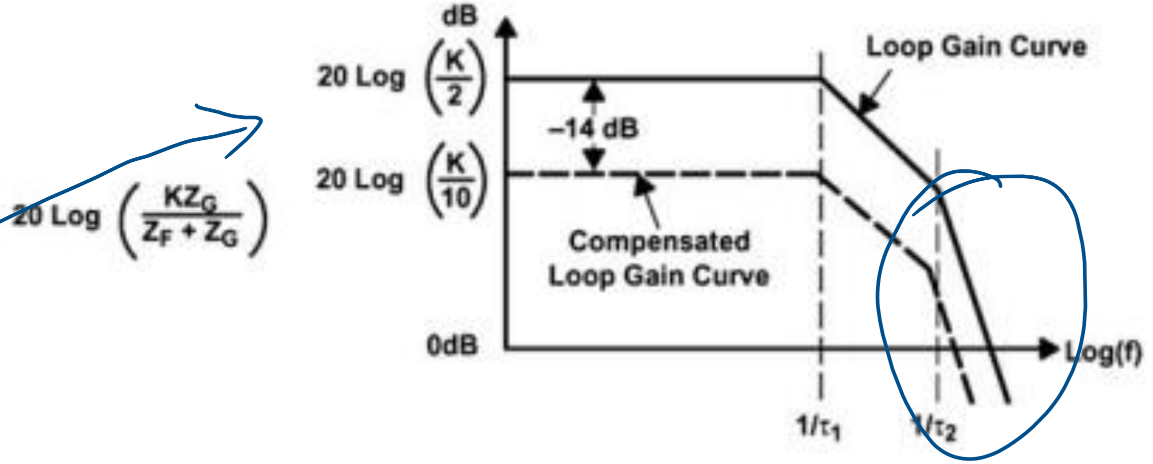
Closed Loop gain (Non ideal) $$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \dfrac{aZ_G}{Z_G + Z_F}}$$

Closed Loop gain (Ideal) $$\frac{V_{OUT}}{V_{IN}} = \frac{Z_F + Z_G}{Z_G}$$

- Example, Change non inverting amp closed loop gain from 2 to 10

- Loop gain will reduce by -14db

Gain compensation – Bode plot

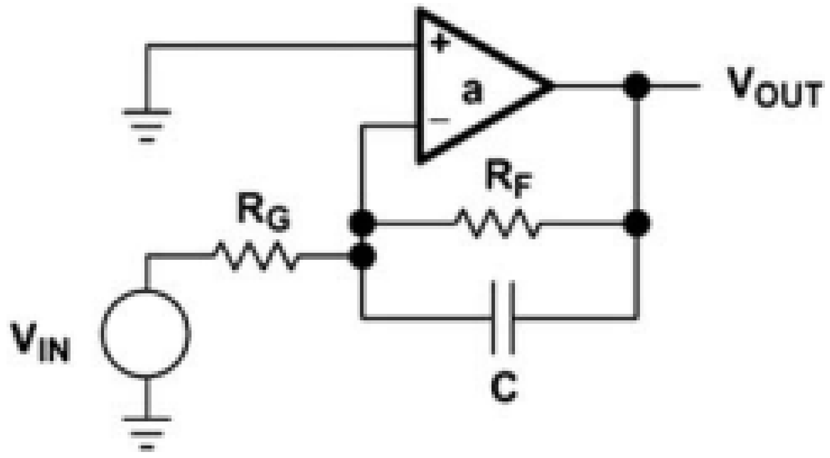


improved phase margin

Improvement observation from the Bode plot

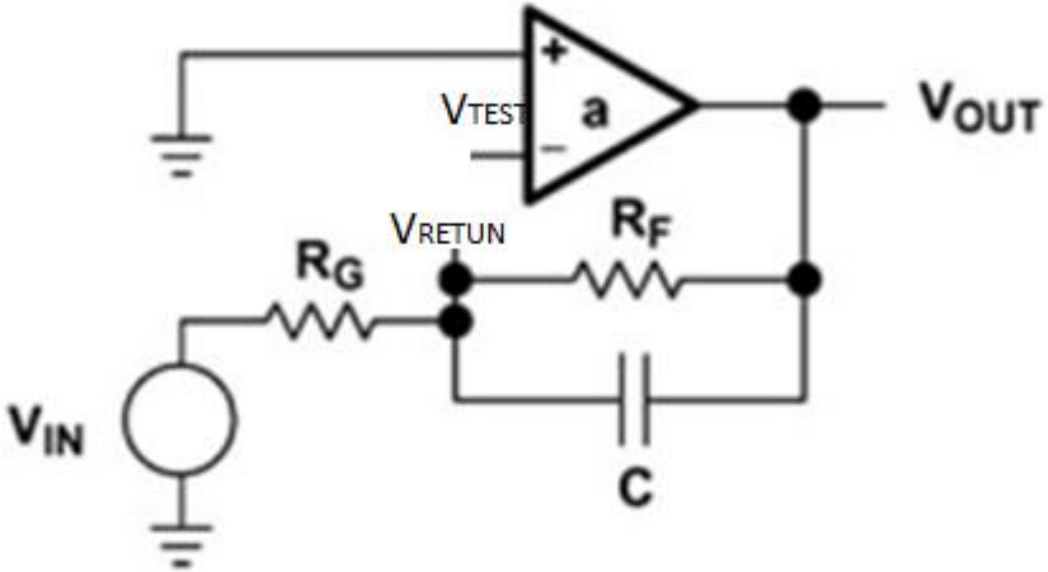
Unit 2 Lead compensation

- In this compensation, C is added across feedback resistor
- C is because of parasitic capacitance



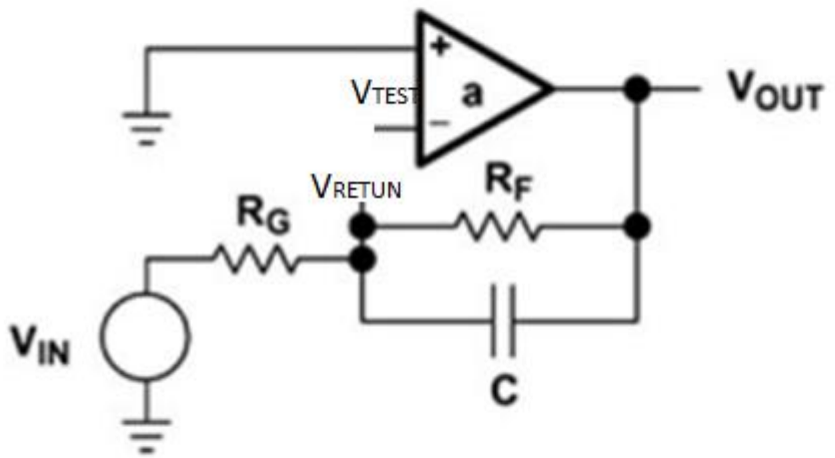
Circuit diagram

- Break the loop and apply test signal for loop gain calculation



Unit 2 Lead compensation

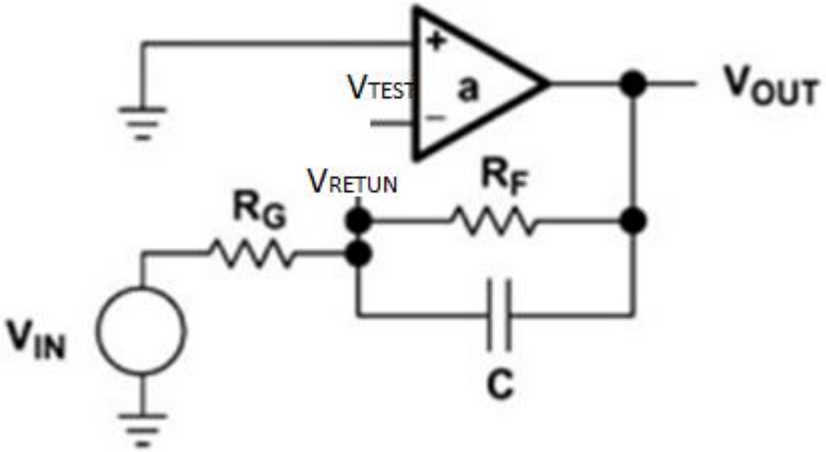
By using voltage divider theorem for the circuit shown, we can write loop gain as



$$\frac{V_{return}}{V_{test}} = \frac{a R_G (sCR_f + 1)}{R_G (sCR_f + 1) + R_F}$$

OR

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{R_F C s + 1}{R_G \| R_F C s + 1}\right)$$



Considering op amp gain as two pole system,

$$a = \frac{K}{(s+\tau_1)(s+\tau_2)}$$

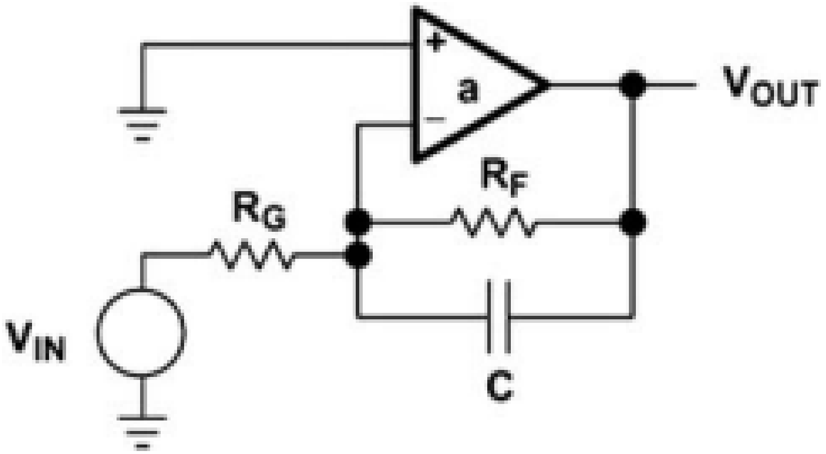
We can rewrite loop gain equation as,

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{R_F C s + 1}{R_G \| R_F C s + 1}\right)\left(\frac{K}{(s+\tau_1)(s+\tau_2)}\right)$$

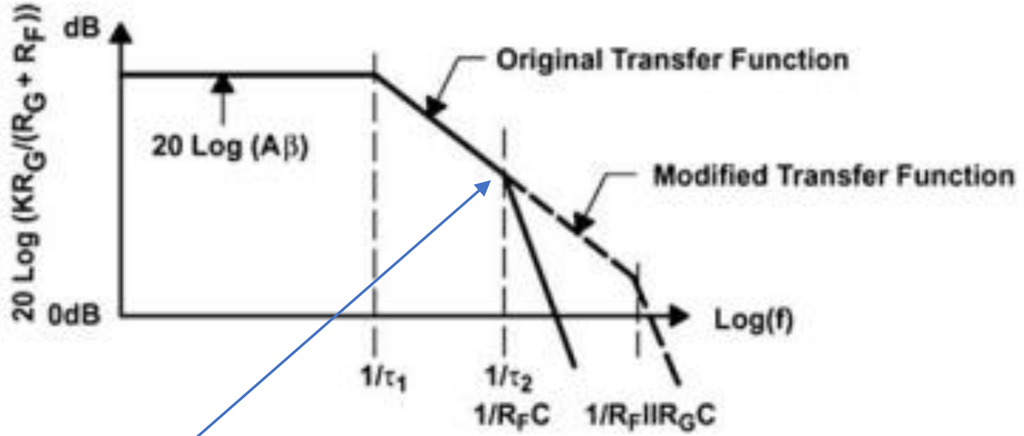
Unit 2 Lead compensation

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{R_F C s + 1}{R_G \| R_F C s + 1}\right)\left(\frac{K}{(s+\tau_1)(s+\tau_2)}\right)$$

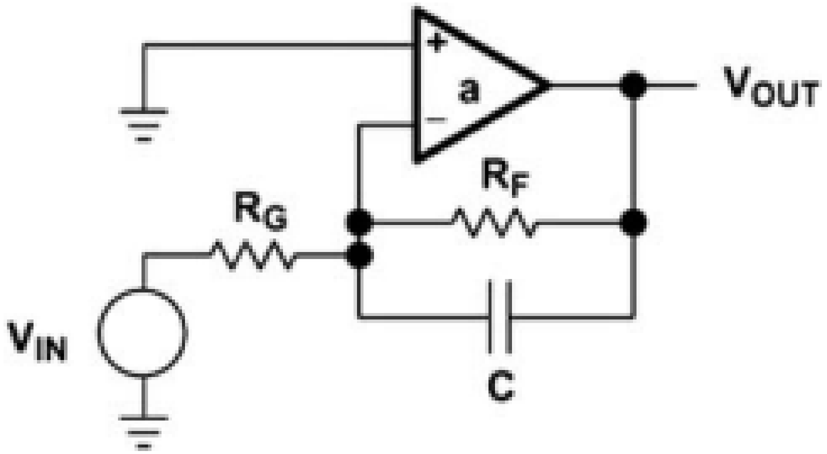
Zero introduced



Bode plot of lead compensation



- Zero placed near second pole
- R_F has to larger compared to R_G in parallel with R_F
- Improves phase margin



Transfer function of inverting amp is given by

Closed Loop gain (Non ideal)

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{-aZ_F}{Z_G+Z_F}}{1+\frac{aZ_G}{Z_G+Z_F}} \quad \text{------10}$$

$$a = \frac{K}{(s+\tau_1)(s+\tau_2)} \quad \text{----11}$$

When **a** is infinity, transfer function shown in 10 can be seen as,

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{\cancel{Z_{IN}}\ Z_G}$$

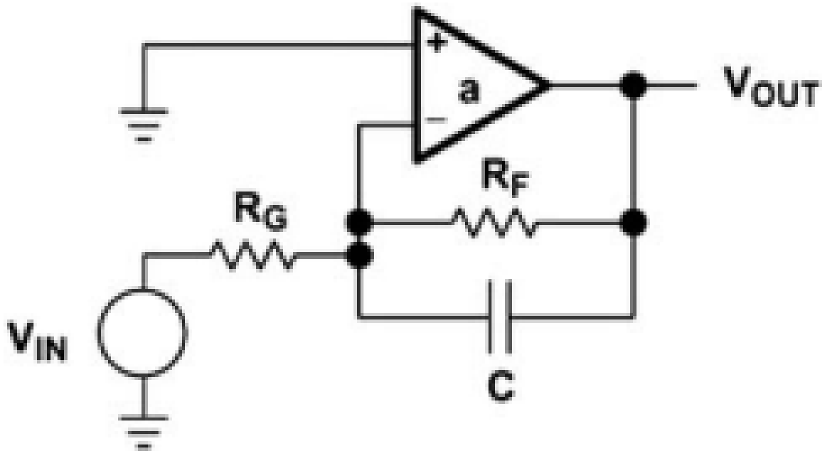
Substituting $R_F||C$ for Z_F and R_G for Z_G

Transfer function is given by

Closed Loop gain (Ideal)

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G}\left(\frac{1}{R_FCs+1}\right) \quad \text{----12}$$

Unit 3 Lead compensation



Transfer function of inverting amp is given by

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$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{-aZ_F}{Z_G + Z_F}}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \qquad \text{------10}$$

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When **a** is infinity, transfer function shown in 10 can be seen as,

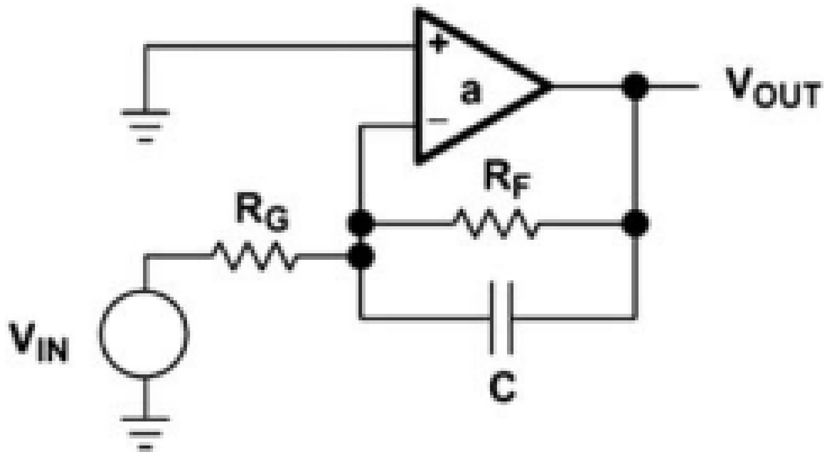
$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{\cancel{Z_{IN}}} \quad Z_G$$

Substituting $R_F || C$ for Z_F and R_G for Z_G

Transfer function is given by

Closed Loop gain (Ideal)

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G}\left(\frac{1}{R_F C s + 1}\right) \qquad \text{----12}$$



Behavior on bode plot for 10, 11,12

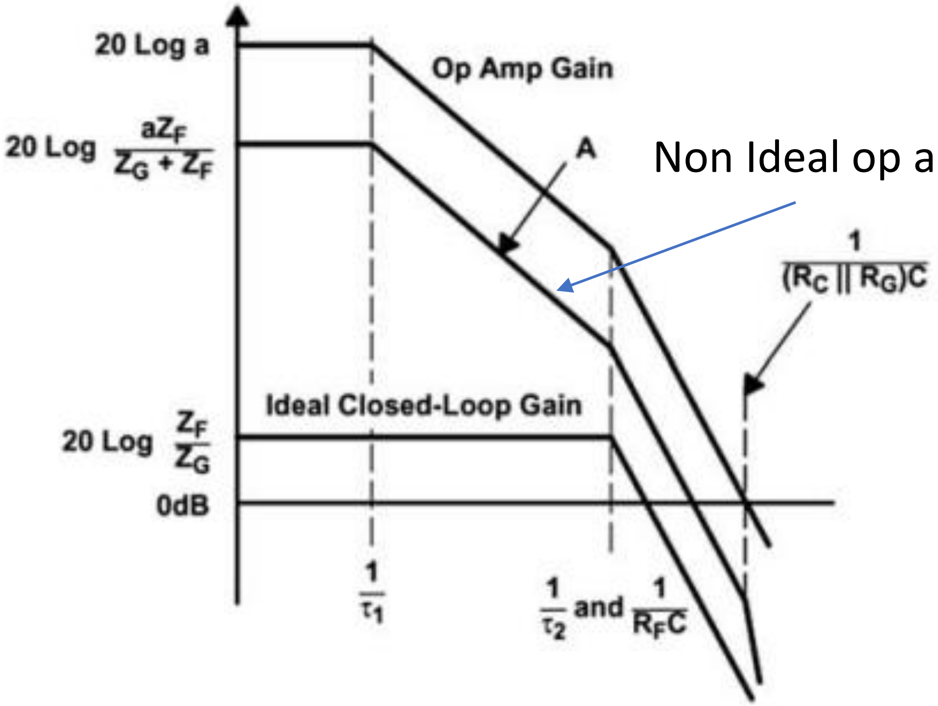
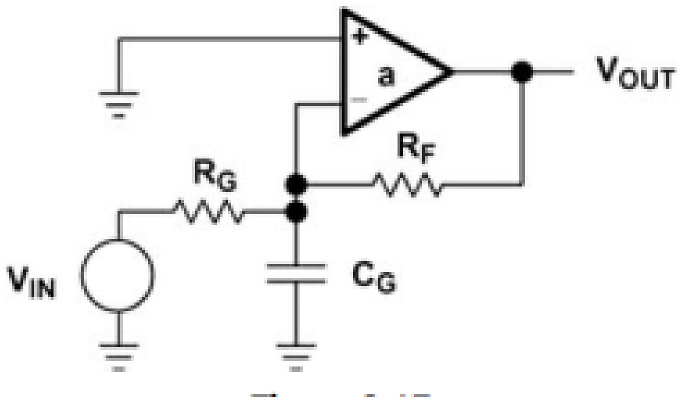


Figure 8.15
Inverting op amp with lead compensation.

Stray capacitance is added due to PCB trace
This circuit is unstable because of three poles

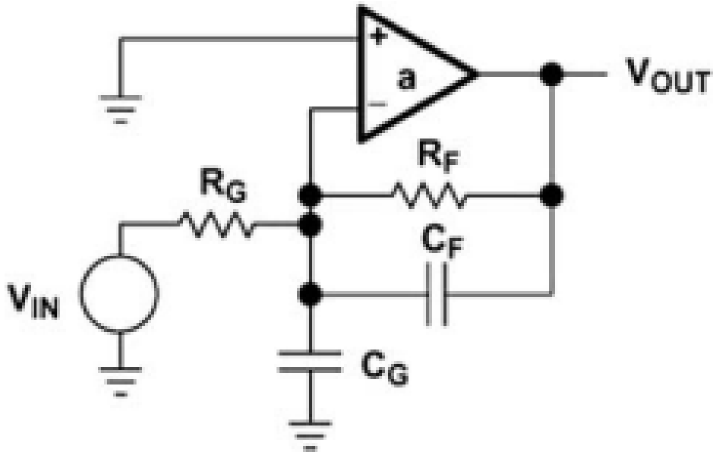


Circuit diagram

Loop gain

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{1}{R_G \| R_F C s + 1}\right)\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right)$$

Compensation capacitor is added parallel to feedback resistor



Circuit diagram

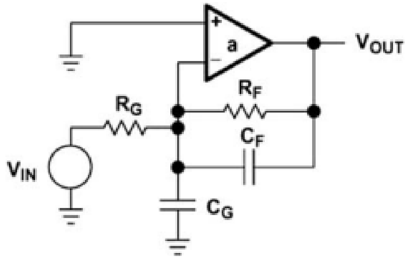
Loop gain for the circuit shown is

$$A\beta = \left[\frac{\dfrac{R_G}{R_G C_G s + 1}}{\dfrac{R_G}{R_G C_G s + 1} + \dfrac{R_F}{R_F C_F s + 1}}\right]\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right)$$

If $R_G C_G = R_F C_F$

Loop gain is $$A\beta = \left[\frac{R_G}{R_G + R_F}\right]\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right)$$

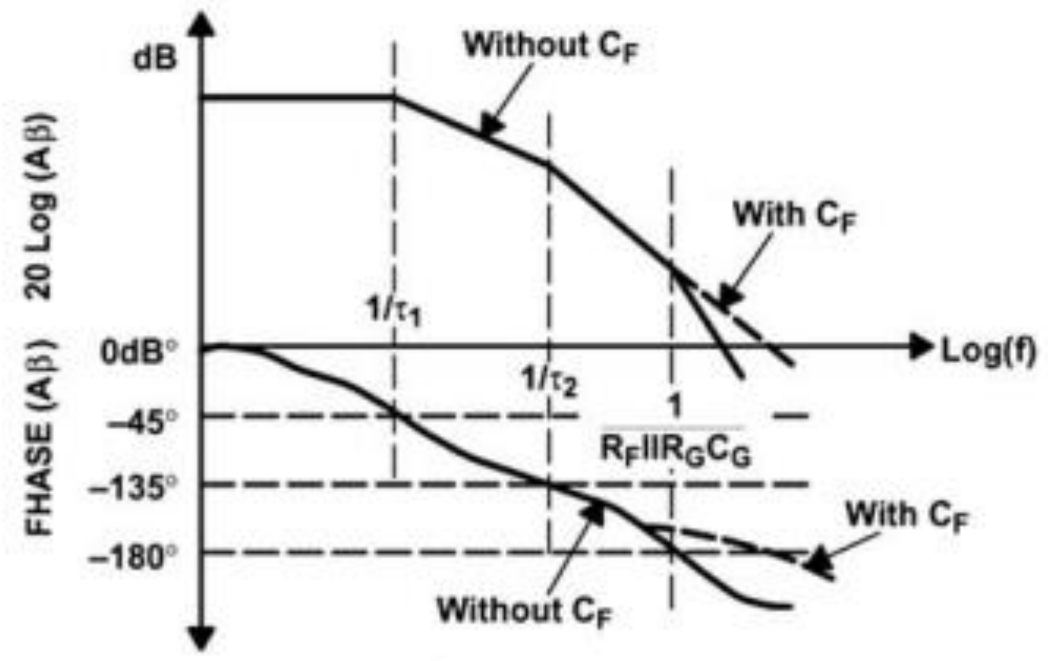
Unit 2 Compensated attenuation



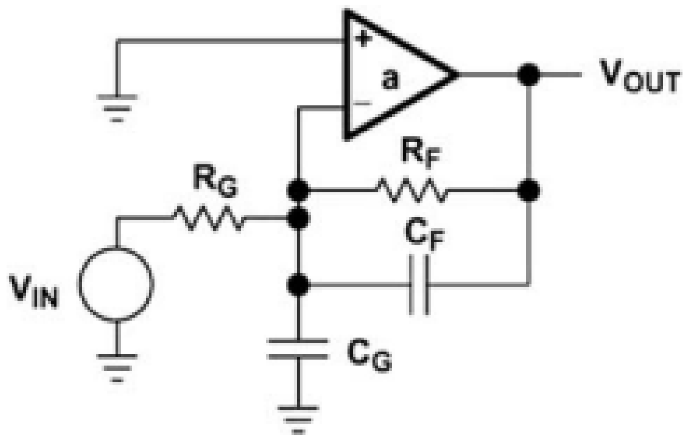
- With addition of compensation capacitor, it cancels pole and zero.
- It acts like open loop gain, a two pole system

$$A\beta = \left[\frac{\dfrac{R_G}{R_GC_Gs+1}}{\dfrac{R_G}{R_GC_Gs+1}+\dfrac{R_F}{R_FC_Fs+1}}\right]\left(\frac{K}{(\tau_1 s+1)(\tau_2 s+1)}\right)$$

Gain plot



Unit 2 Compensated attenuation



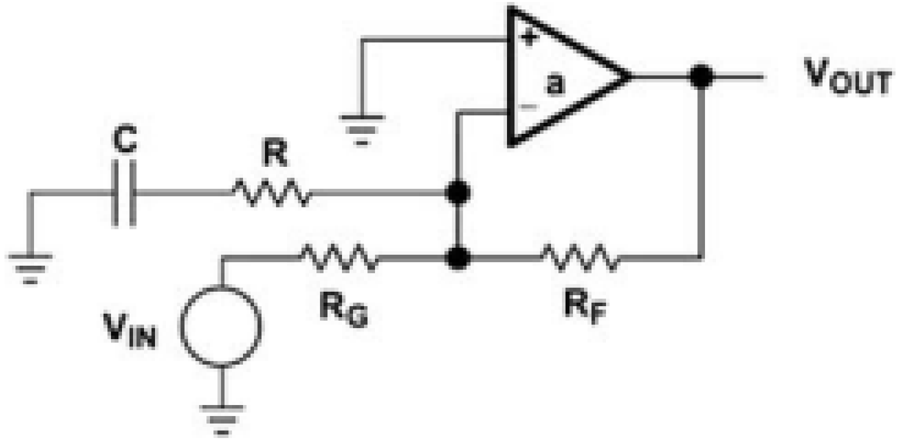
In compensated attenuation circuit, closed loop gain of inverted amp does not change. Capacitor has not effect on gain

Closed loop gain

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{R_F}{R_F C_F s + 1}}{\dfrac{R_G}{R_G C_G s + 1}}$$

When $R_F C_F = R_G C_G$ $\quad \dfrac{V_{OUT}}{V_{IN}} = -\left(\dfrac{R_F}{R_G}\right)$

- R and C used for compensation
- Compensation circuit adds Pole and Zero

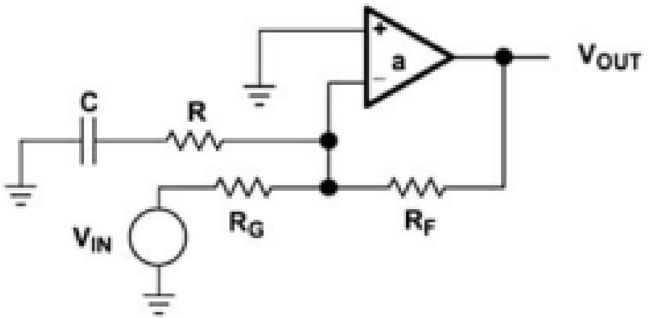


Circuit diagram

loop gain of the circuit diagram shown

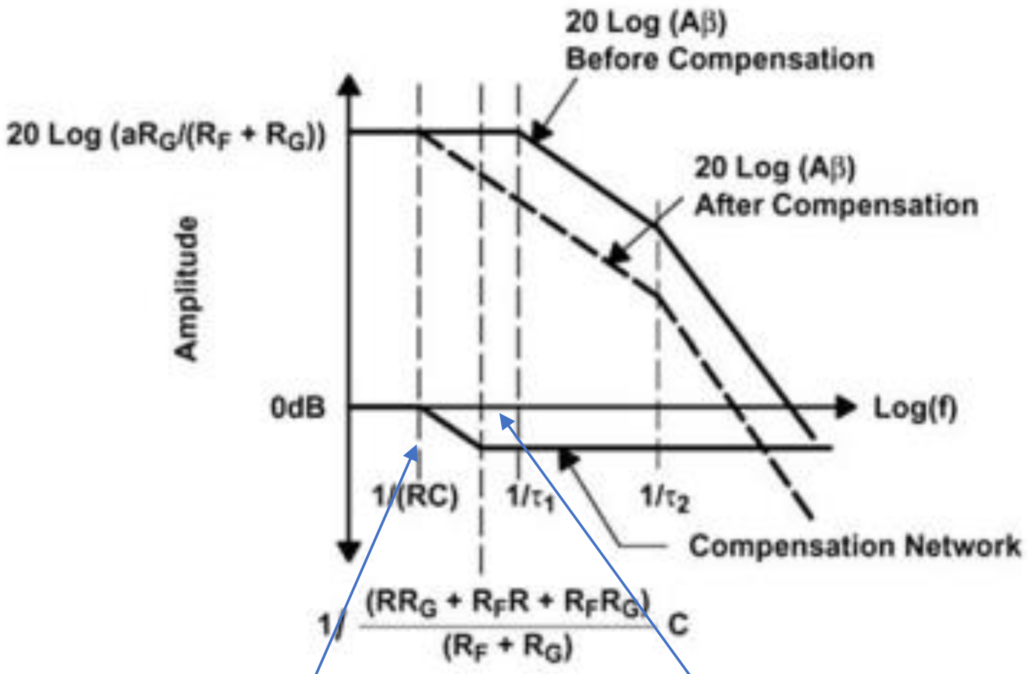
$$A\beta = \frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \frac{R_G}{R_G + R_F} \frac{RCs + 1}{\frac{(RR_G + RR_F + R_G R_F)}{(R_G + R_F)} Cs + 1}$$

Unit 2 Lead lag compensation



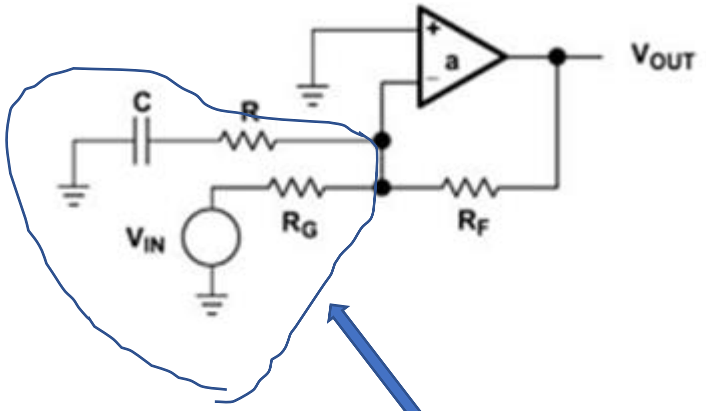
$$A\beta = \frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \frac{R_G}{R_G + R_F} \frac{RCs + 1}{\frac{(RR_G + RR_F + R_G R_F)}{(R_G + R_F)}Cs + 1}$$

Gain plot



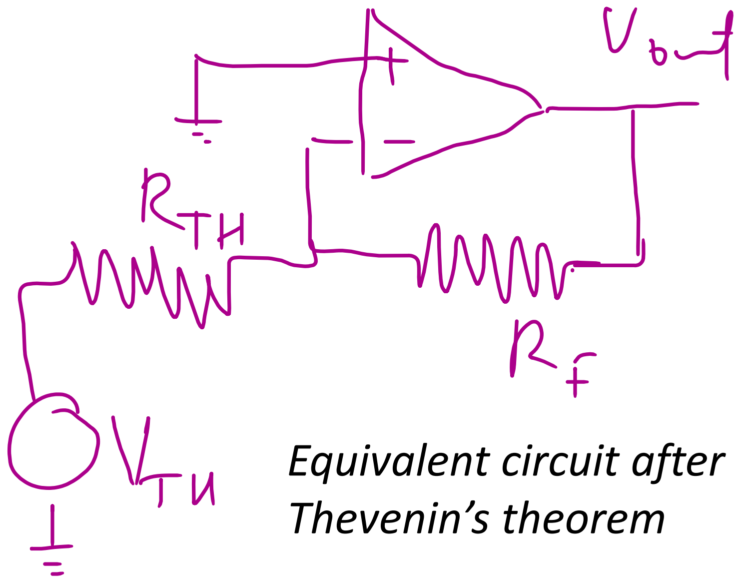
This introduces a **pole** and **zero**

Ideal closed loop gain can be calculated, use Thevenin's theorem first



Apply Thevenin's theorem here

$$V_{TH} = V_{IN} \frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}}$$



Equivalent circuit after Thevenin's theorem

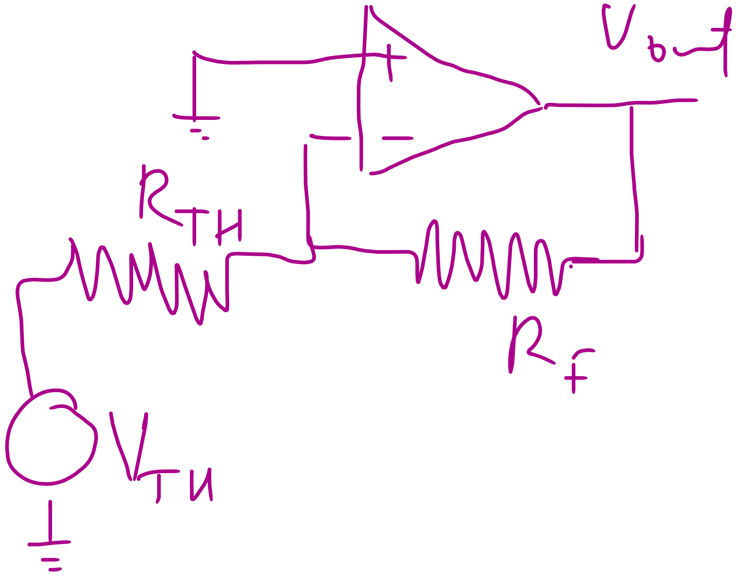
$$R_{TH} = \frac{R_G\left(R + \frac{1}{Cs}\right)}{R + R_G + \frac{1}{Cs}}$$

Unit 2 Lead lag compensation

Ideal closed loop gain calculated,
based on inverting amp configuration

$$V_{OUT} = -V_{TH}\frac{R_F}{R_{TH}}$$

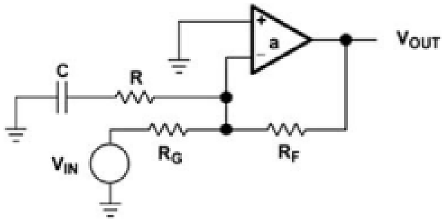
Substitute V_{TH} and R_{TH}
(refer previous slide)



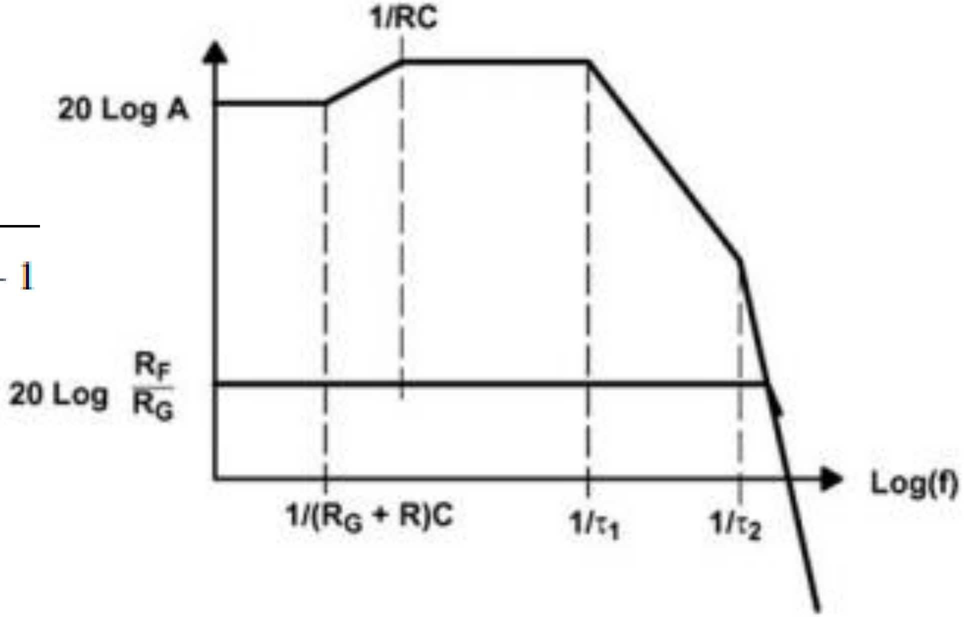
$$-\frac{V_{OUT}}{V_{IN}} = \frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}} \cdot \frac{R_F}{\frac{R_G\left(R + \frac{1}{Cs}\right)}{R + R_G + \frac{1}{Cs}}} = \frac{R_F}{R_G}$$

gain remains same

Unit 2 Lead lag compensation



Bode plot of lead lag compensation techniques for closed loop gain



Loop gain

$$A\beta = \frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \frac{R_G}{R_G + R_F} \frac{RCs + 1}{\frac{(RR_G + RR_F + R_G R_F)}{(R_G + R_F)} Cs + 1}$$

Closed Loop gain

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_F}{R_G}$$

Unit 3 Comparison of compensation schemes

Scheme	Advantages	Disadvantages
Internal compensation	No need for extra component	Under certain load capacitance, it is unstable
Dominant pole compensation	Suitable for high load capacitance	Load capacitance make op amp to ring
Gain compensation	Good in terms of stability	Gain reduces
Lead compensation	Increases bandwidth	Reduces closed loop gain
Compensated attenuator	Useful scheme when stray capacitance seen at inverting input	Needs matching two RC time constants
Lead lag compensation	Increased bandwidth	More external components

Textbook :

Op Amp for Everyone : Bruce Carter and Ron Mancini Fifth Edition 2017

THANK YOU

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