Ten Advanced Optimizations of cache Performance

- Small & Simple 1st lvl cache to Reduce Hit time & Power.

The following questions investigates the impact of small & simple

Compare the access-time of 4 set associative cache with 64 byte blocks & a single bank. What are the relative access time of 32kB & 64kB cache in comparison to a 16kB cache

$$AMAT \rightarrow 1 + MT \times MP$$

Critical word 1st & early restart to reduce the miss penalty.

the image of critical word 1st &

Consider [...]

Early Restart on L2 cache misses. Assume a 1MB L2 with 64-byte blocks & a refill path that

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2nd optimization: Way Prediction to reduce Hit time

Assume that 64kB 4 way set associative Cache has access time of 2 cycles with miss rate of 3.3% in a sys. As an alternative Cache organization you are considering a way-predicted cache modelled as a 64kB direct-mapped cache with 80% prediction accuracy. The direct-mapped has access time of 1 cycle & miss rate of 5.5%. Assume miss penalty as 10 cycles. What is the avg. mem. access time of the way-predicted cache?

Loop Unrolling
  } → Can loop overhead be minimised?
  ]   f.ther minised.

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with & without scheduling