Memory Design and Testing

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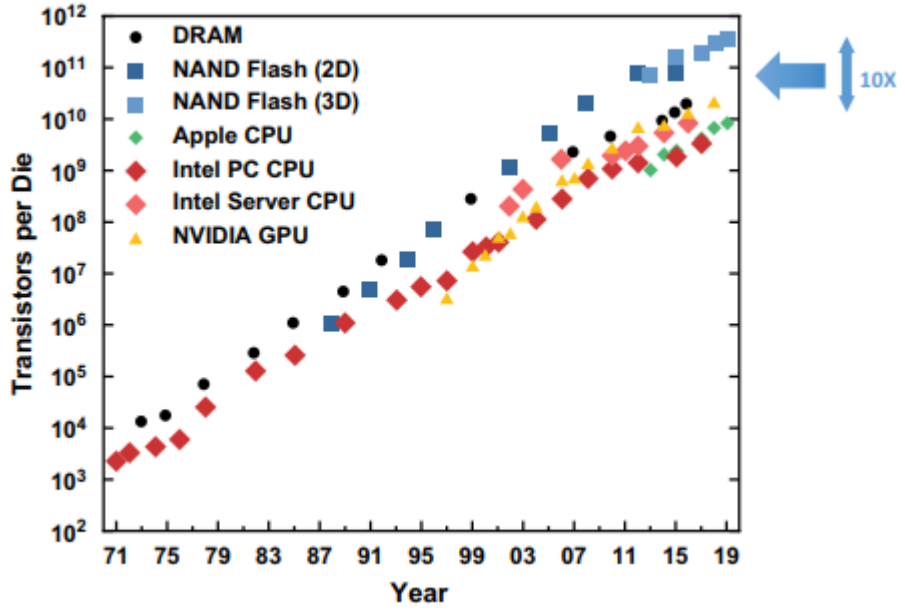
Industry Technology Trend

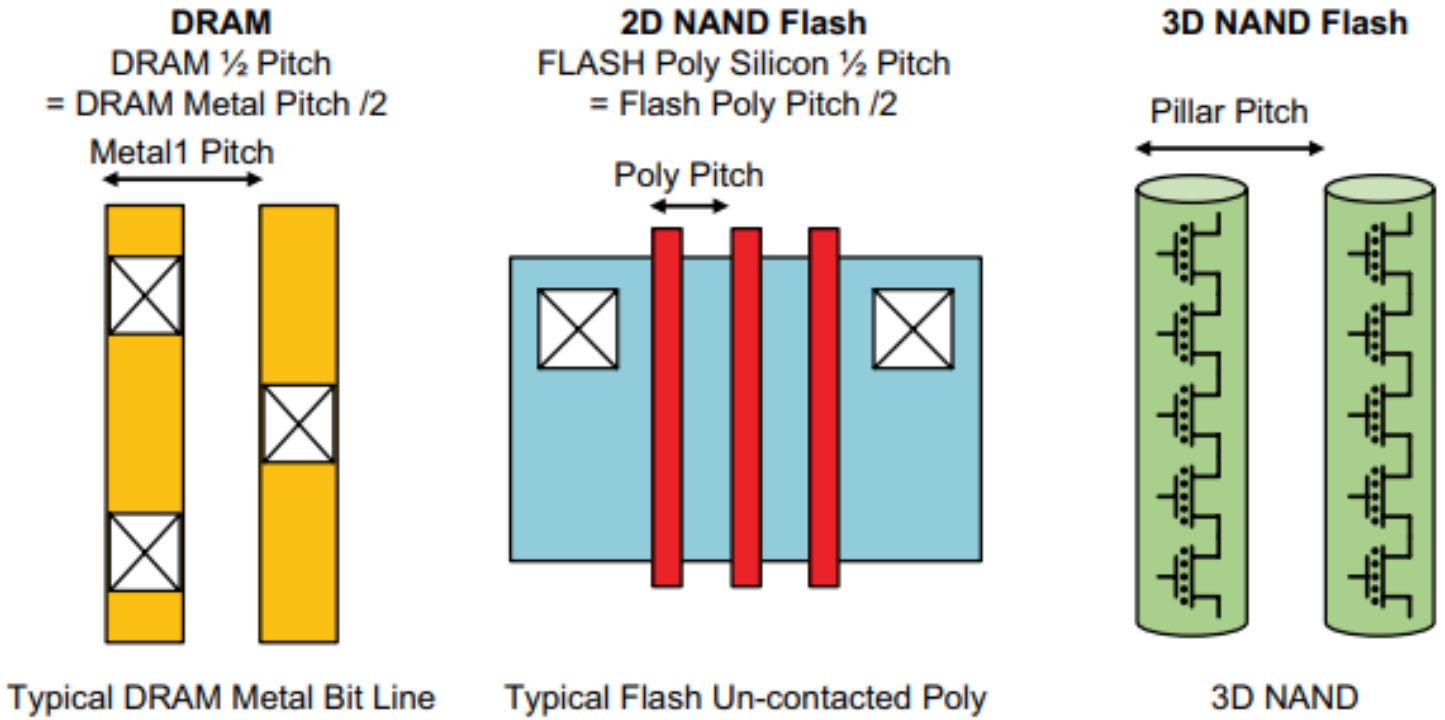
- Moore's law of semiconductor industry
- Moore's law applicable even to memory technology



- Deviation from Moore's law
  - 3D technology

Industry Technology Trend : Definition of technology node

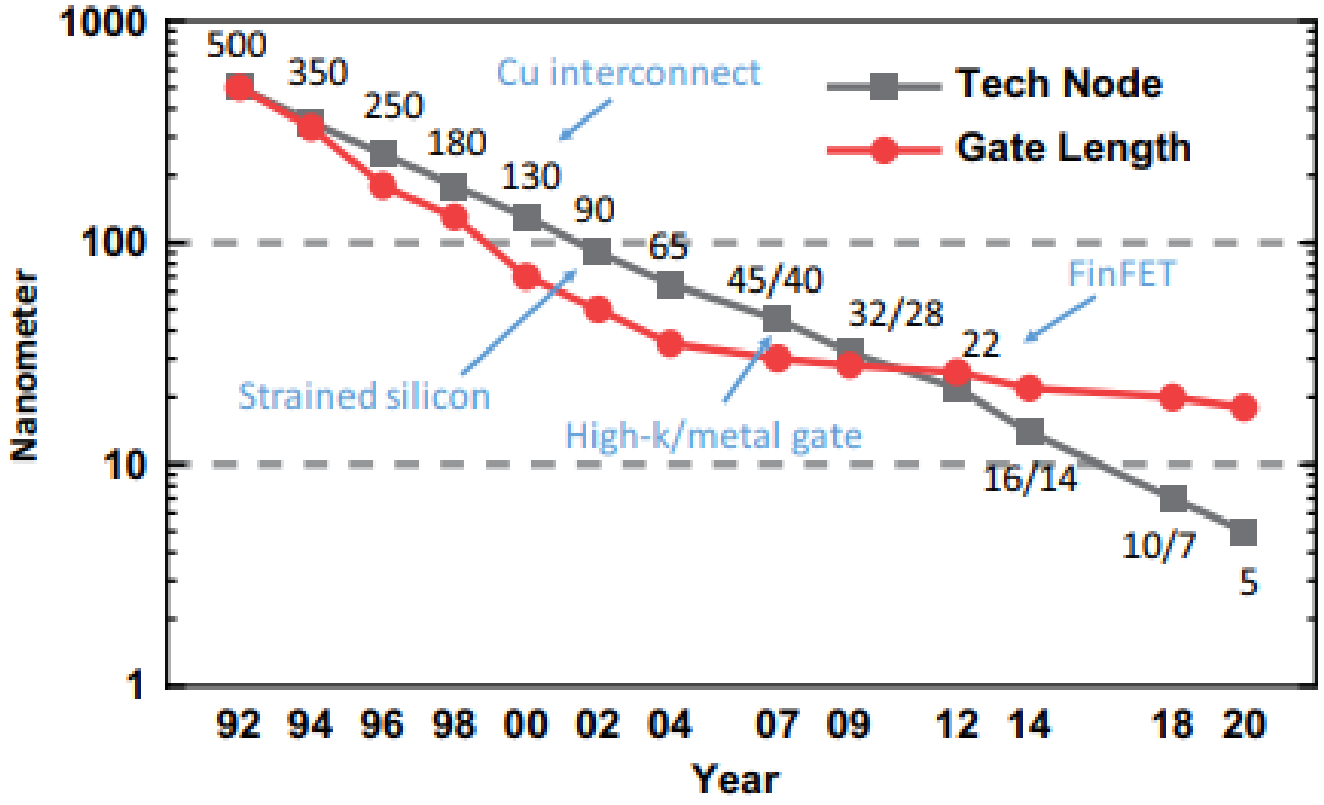
- Feature size (F) definition for memory



General lithographic feature size F=1/2 pitch

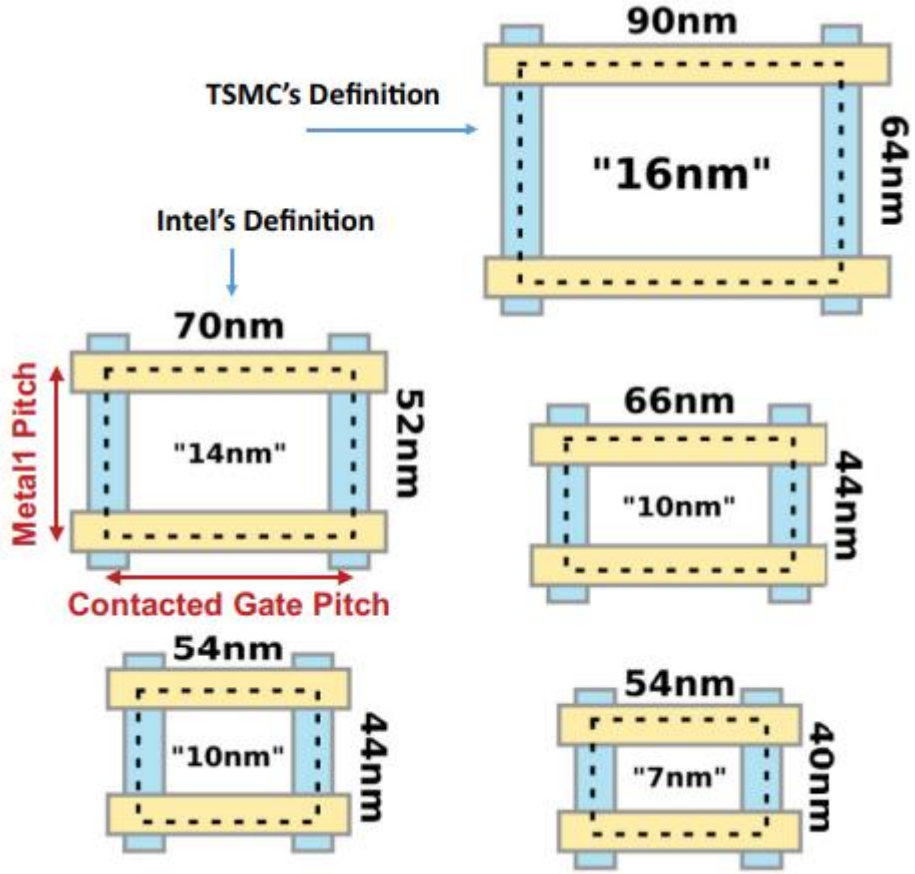
Industry Technology Trend : Definition of technology node

- In recent times, technology node does not represent minimum gate length
- Gate length in 5nm technology node is 20nm!

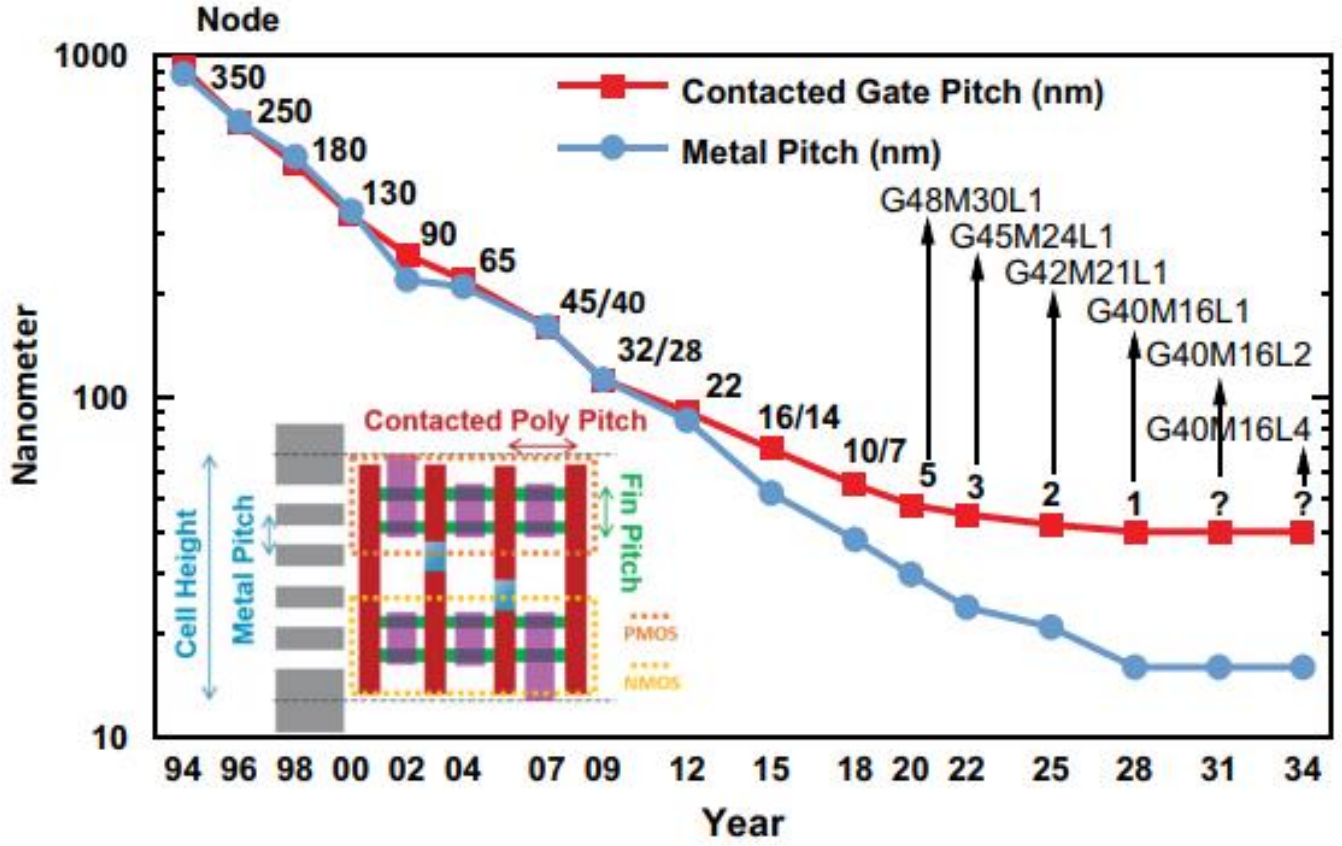


Industry Technology Trend : Definition of technology node

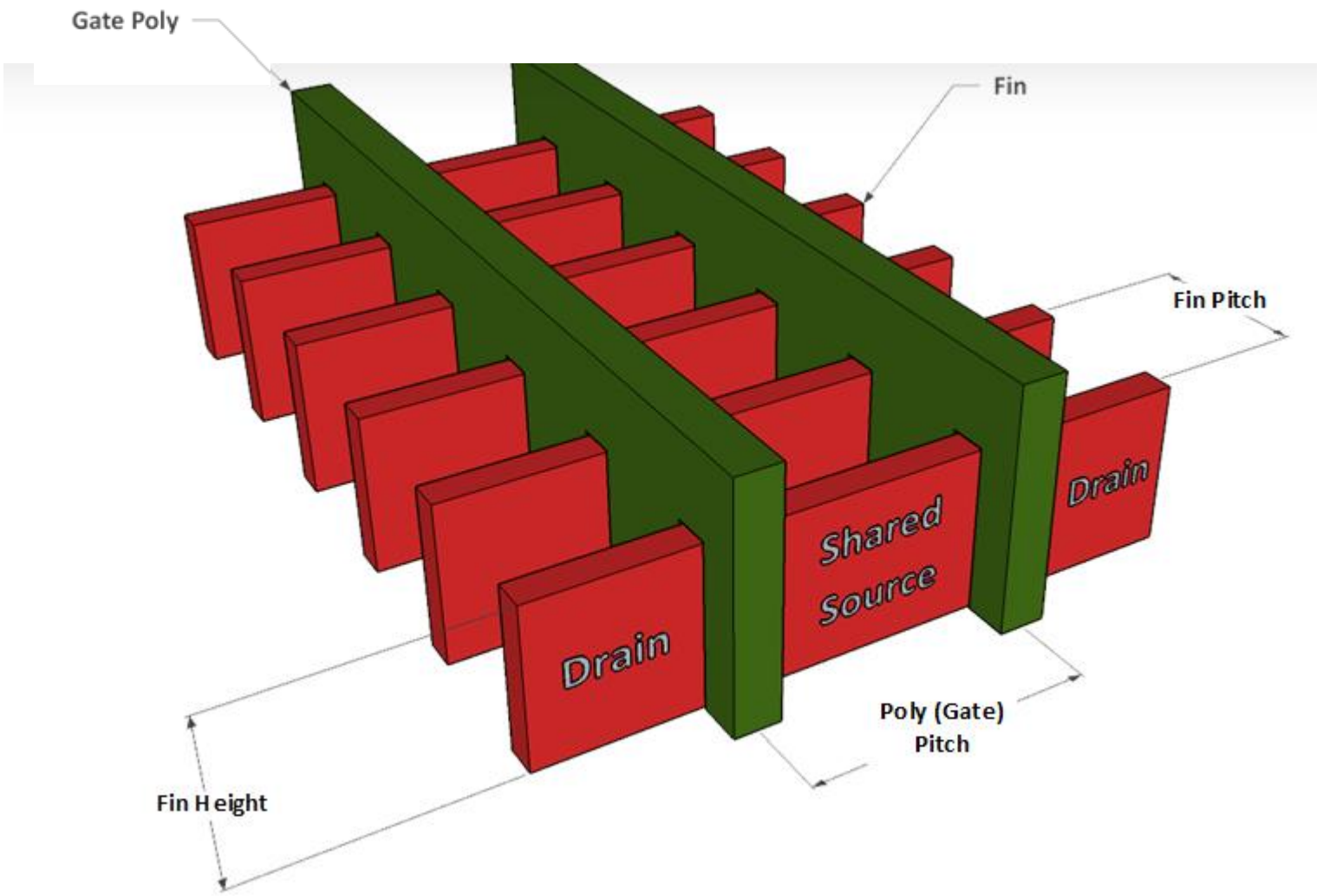
- Newer scaling parameter for logic transistor density
  - Contacted Gate Pitch and Metal Pitch
  - More suitable for FinFET technology
  - Effective area is product of contacted gate pitch and metal pitch



Industry Technology Trend : Definition of technology node



Industry Technology Trend : Definition of technology node



Industry Technology Trend : Definition of technology node

- Recent trend is reduce M1 and Fins

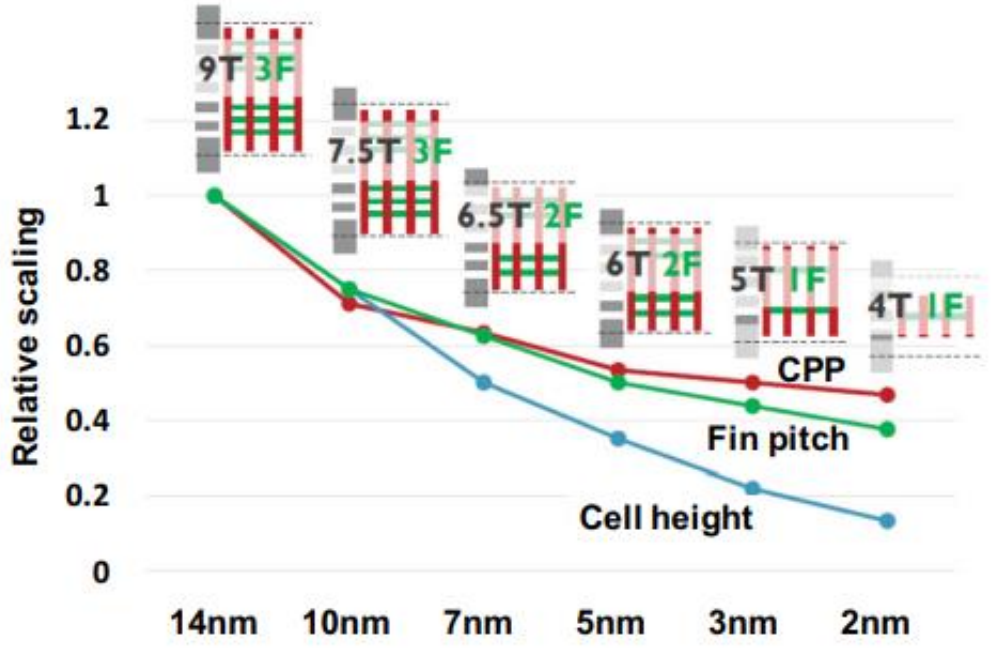
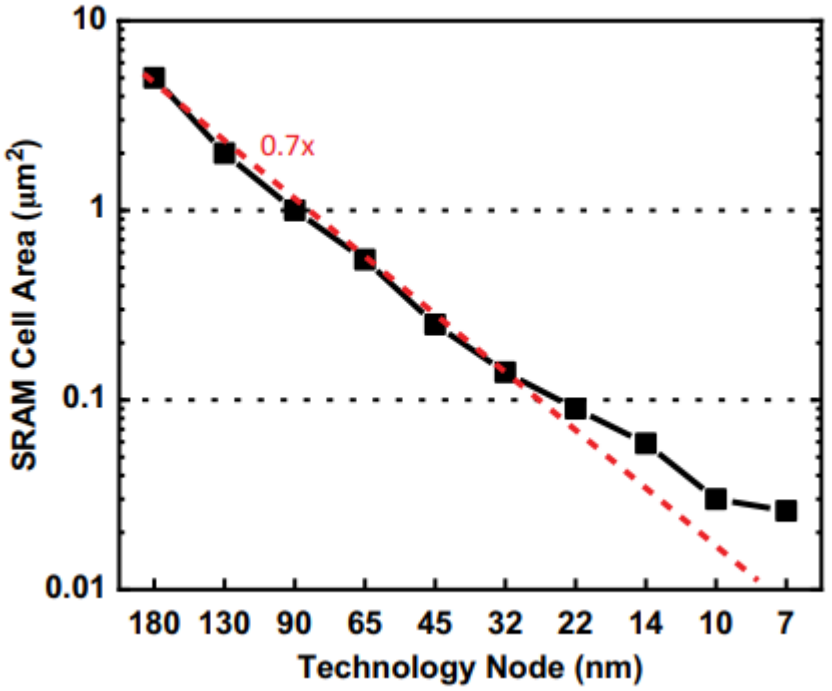


FIGURE 1.16 The scaling trend of the logic standard cell layouts in recent and projected generations. T is the number of M1 tracks and F is the number of fins.

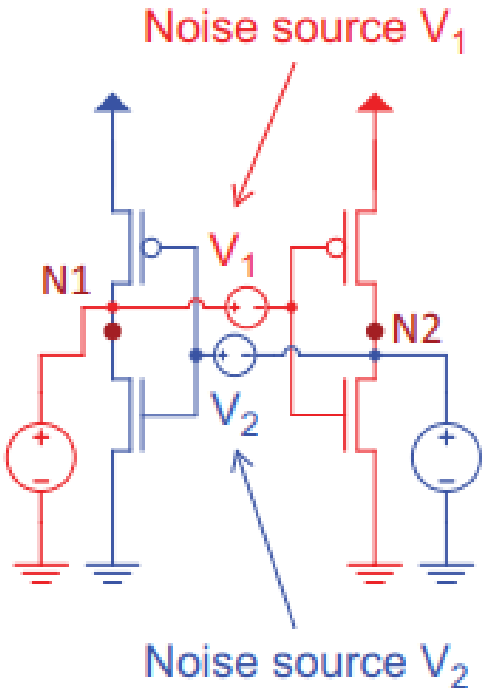
Industry Technology Trend : Definition of technology node

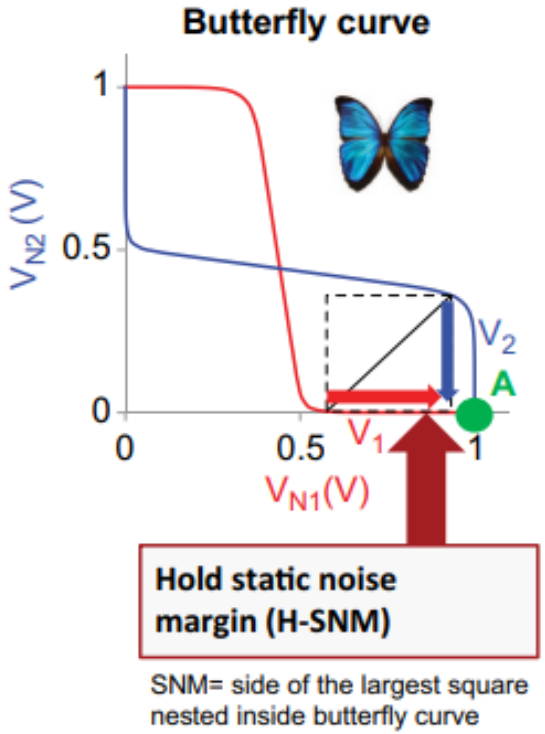
- Trends in SRAM
  - Does not CGP/M1 pitch criteria
  - Uses absolute area as measure of scaling



SRAM Stability analysis : Static Noise margin

- Static noise analysis is used to study noise distrurbances on SRAM cell
- It is classified as HSNM, RSNM, WSNM
- In HSNM, PG transistors are off, No connection to bit line and complementary bit line

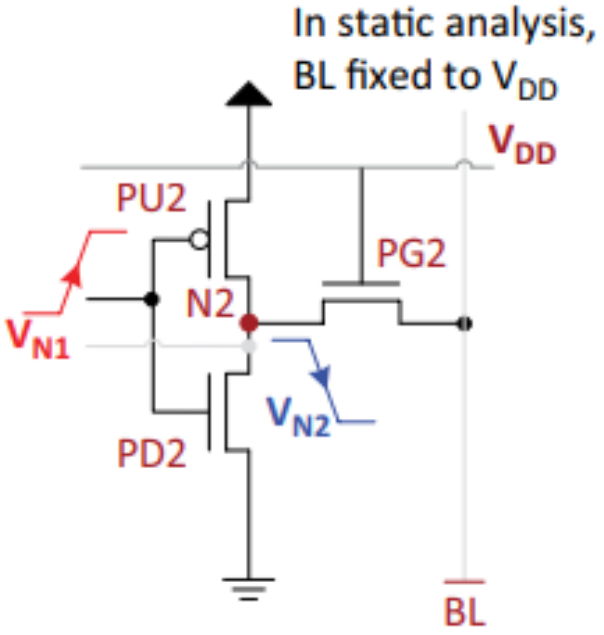


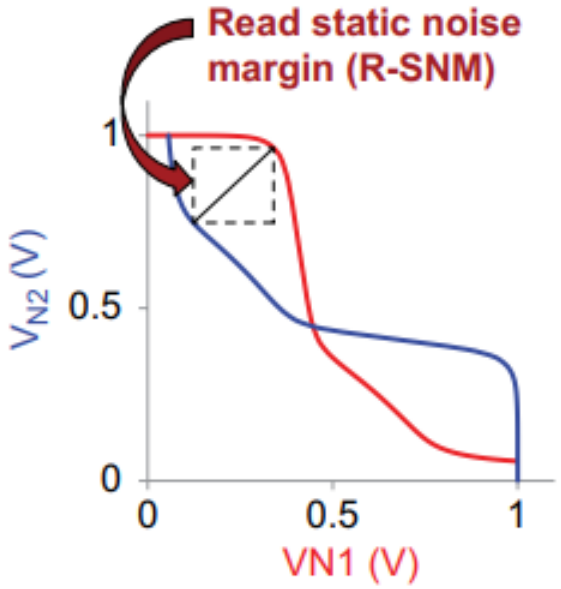


SNM= side of the largest square nested inside butterfly curve

SRAM Stability analysis : Static Noise margin

- In RSNM, PG transistors turned on, connected bit line and complementary bit line



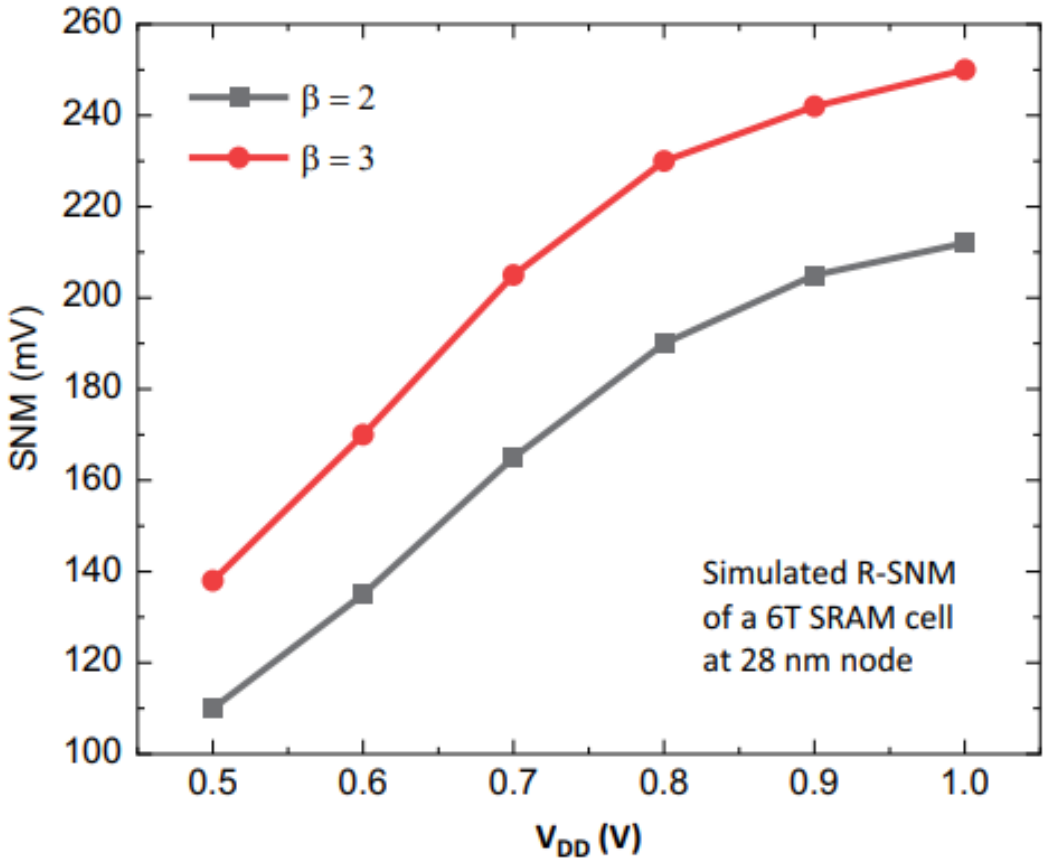


- Smaller noise margin

V_{N1} sweeps from 0 to VDD

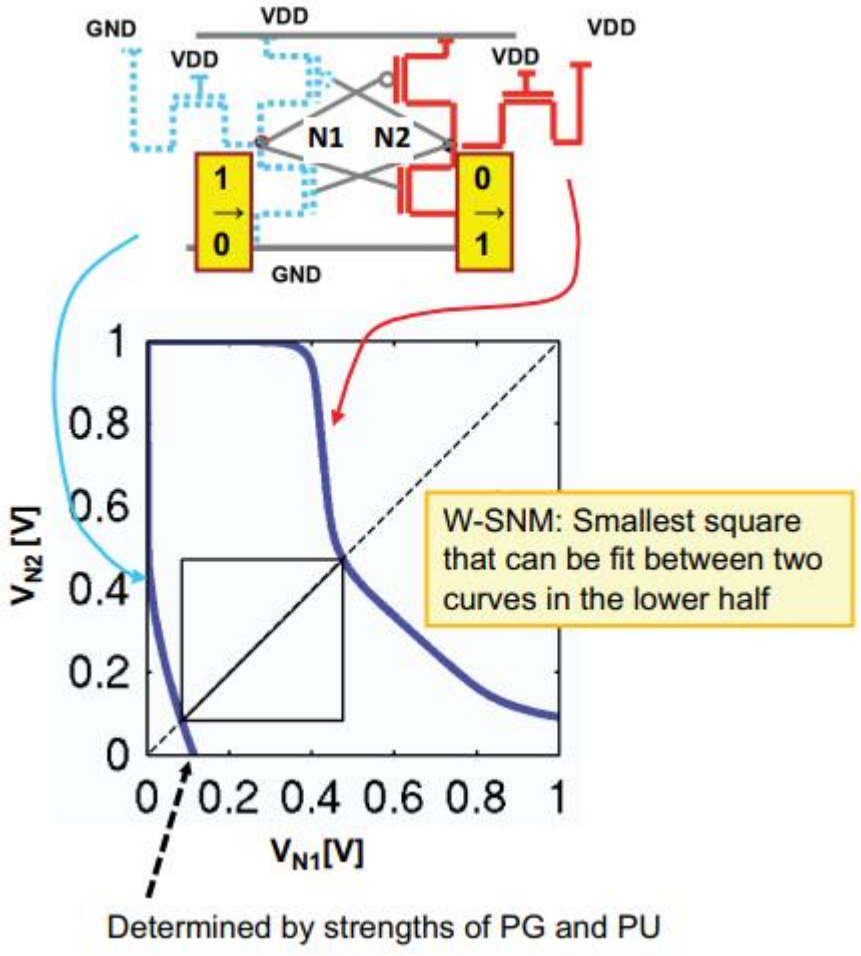
V_{N2} decreases from VDD to a low value (non-zero) that is determined by the β ratio

SRAM Stability analysis : Static Noise margin



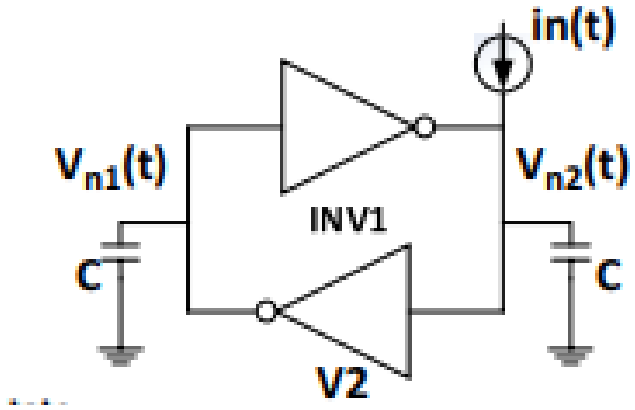
SRAM Stability analysis : Static Noise margin

- In WSNM, one bit line is connected to VDD and other to GND
- Right branch has the same condition as read operation
- Left branch, it decay from certain low value to ground



SRAM Stability analysis : Dynamic Noise margin

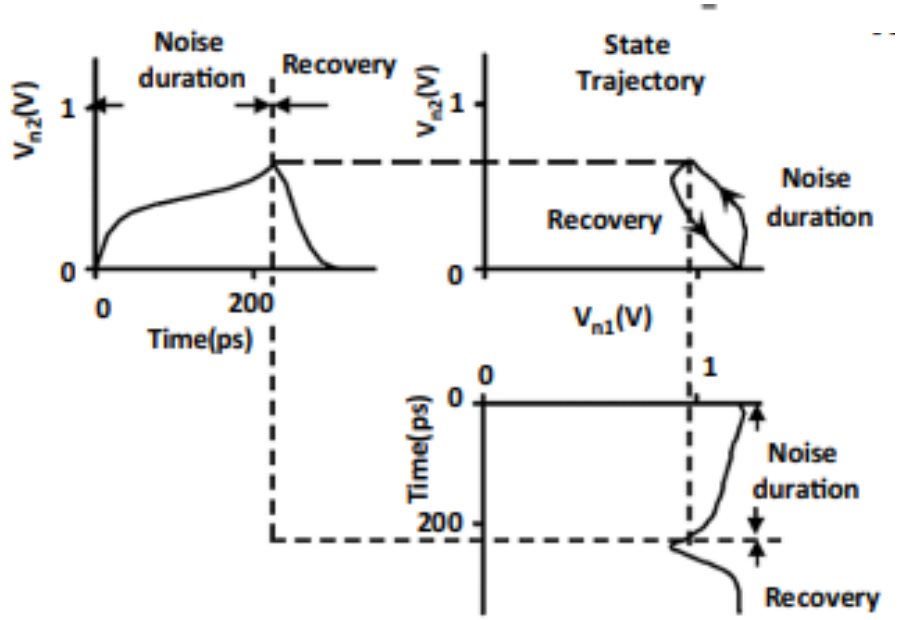
- Dynamic analysis is more practical
- A current is injected onto one of the nodes
- Based on time duration voltage is developed
- If time duration is short voltage developed does not flip the content of SRAM
- If duration is long content of SRAM may flip



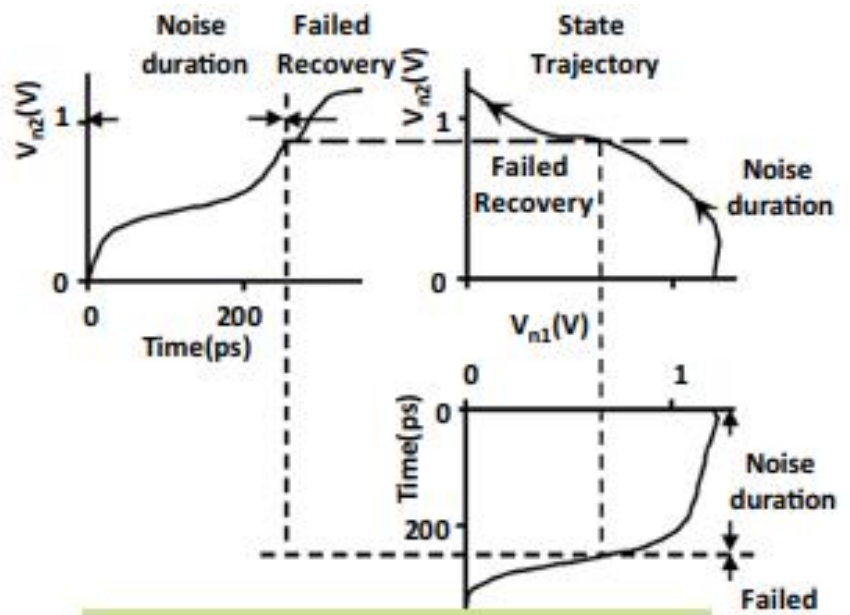
Test setup

SRAM Stability analysis : Dynamic Noise margin

- Two cases



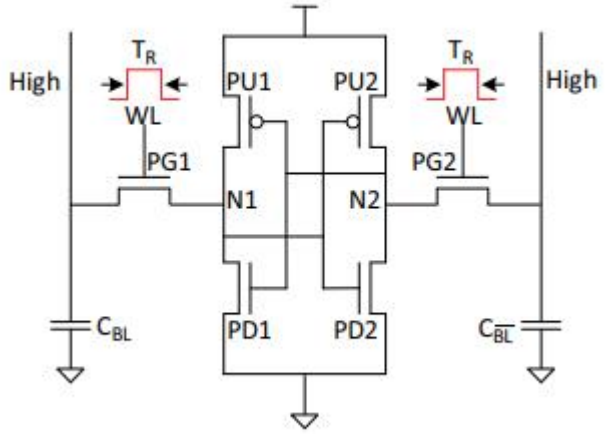
(a) Dynamic recovery if noise current is short in duration

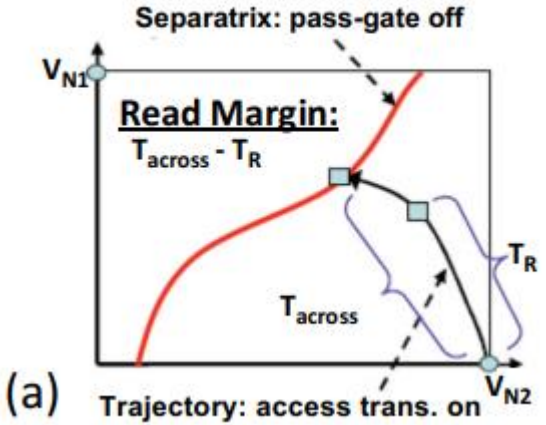


(b) State flip if noise current is long in duration

SRAM Stability analysis : Dynamic Noise margin

- Concept of separatrix, which defines boundary between stable and unstable state
- Current through pass transistor acts as current source
- A condition of $T_R < T_{across}$ should be satisfied for accidental write from read operation





SRAM Stability analysis : Dynamic Noise margin

- Concept of separatrix, which defines boundary between stable and unstable state
- Current through pass transistor acts as current source
- A condition of $T_W < T_{across}$ should be satisfied for write operation