Memory Design and Testing

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Department of Electronics and Communication Engg.

MEMORY DESIGN AND TESTING

UNIT 1 – Semiconductor Memory Technology overview

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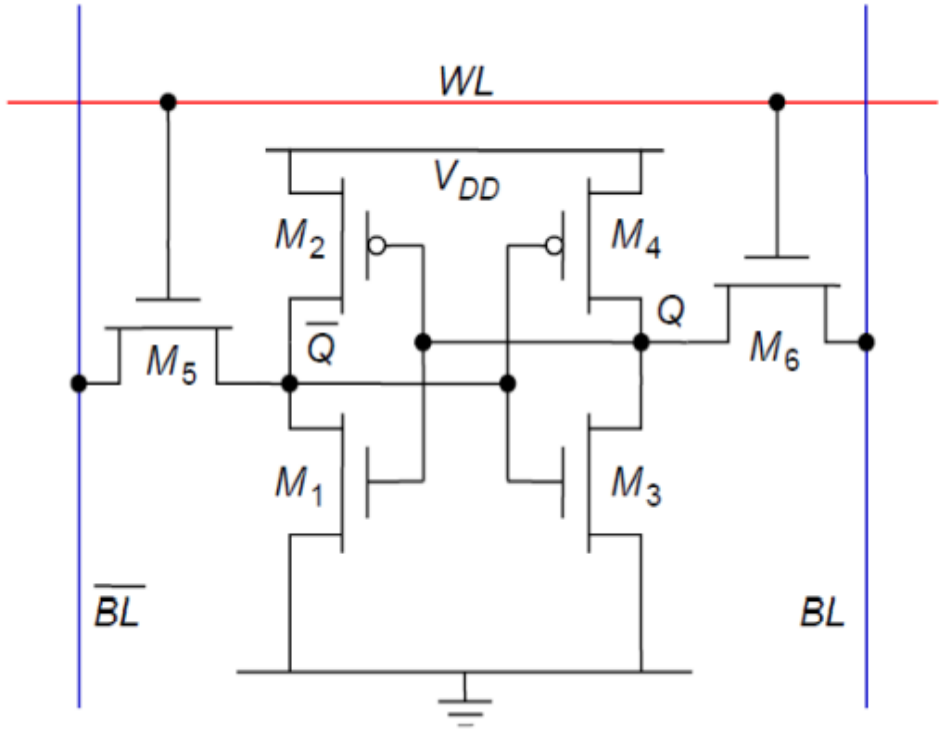
6T SRAM Cell

- Two Cross Couple CMOS Inverters are formed by using Transistor pairs M1 – M2 and M3 – M4.
- Two Bit Lines are used to transfer data and are complement to each other and form the cell.

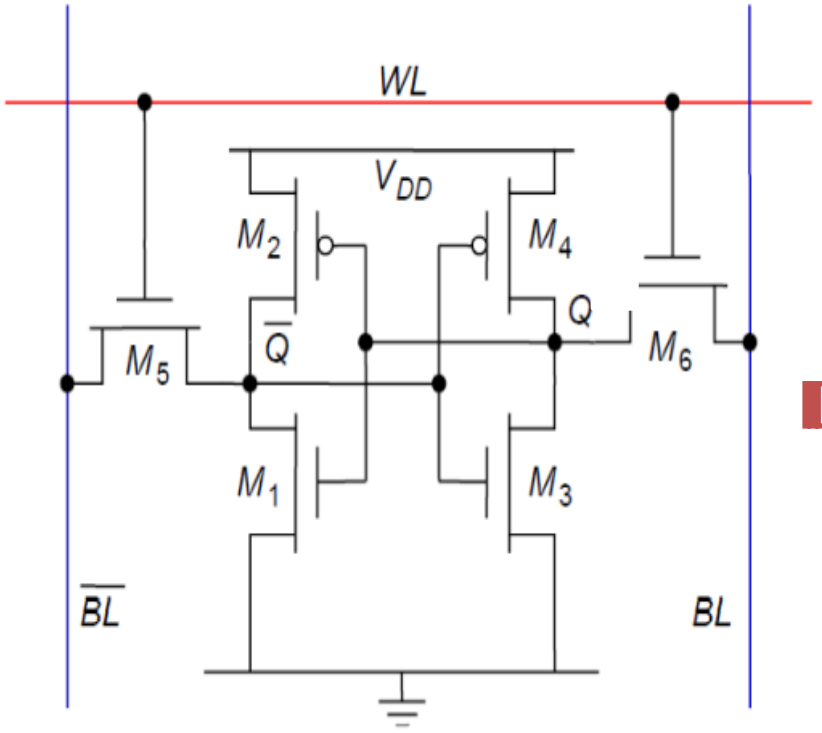


- The generic structure of the MOS static RAM cell, consisting of two cross-coupled CMOS inverters and two access transistors as shown.
- Access to the cell is enabled by the word line, WL, which controls the 2 pass transistors, M5 and M6 .
- These access MOS devices provide the provision to Write / Read the stable state stored in back to back connected Inverters.
- These Access Transistors also Isolate one Cell from another in a Memory Array
- Q indicates the data stored in the Cell.
- Bit Line (BL) and BL' are the lines through which data accessing is done.

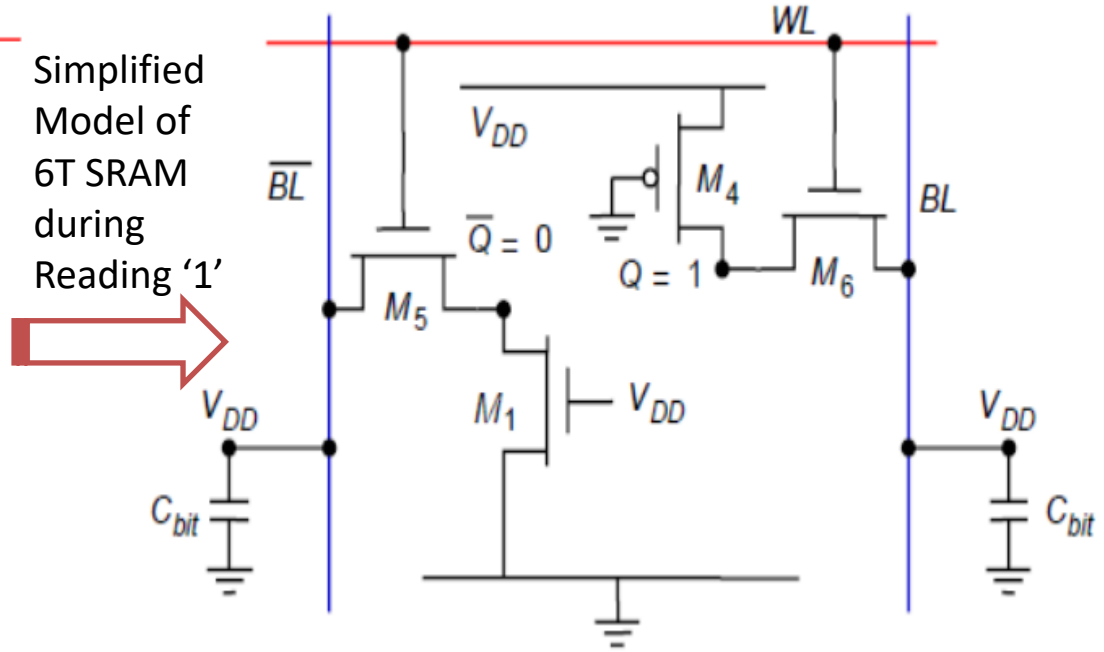
6T SRAM Cell – Read Operation

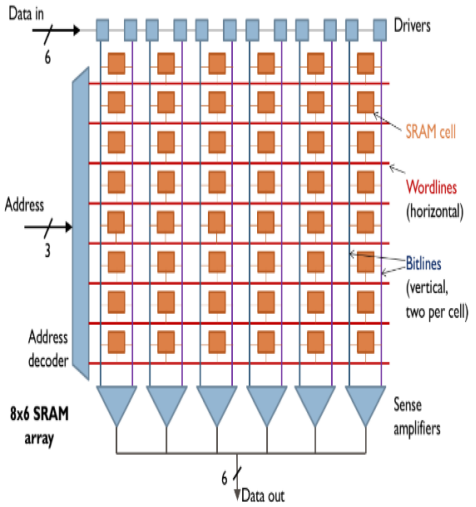
Reading Stored Q=1

Assume that a 1 is stored in Memory Cell, i.e., Q=1.



Simplified Model of 6T SRAM during Reading '1'





Cbit refers to the bit-line capacitance which is of the order of pF for large memories.

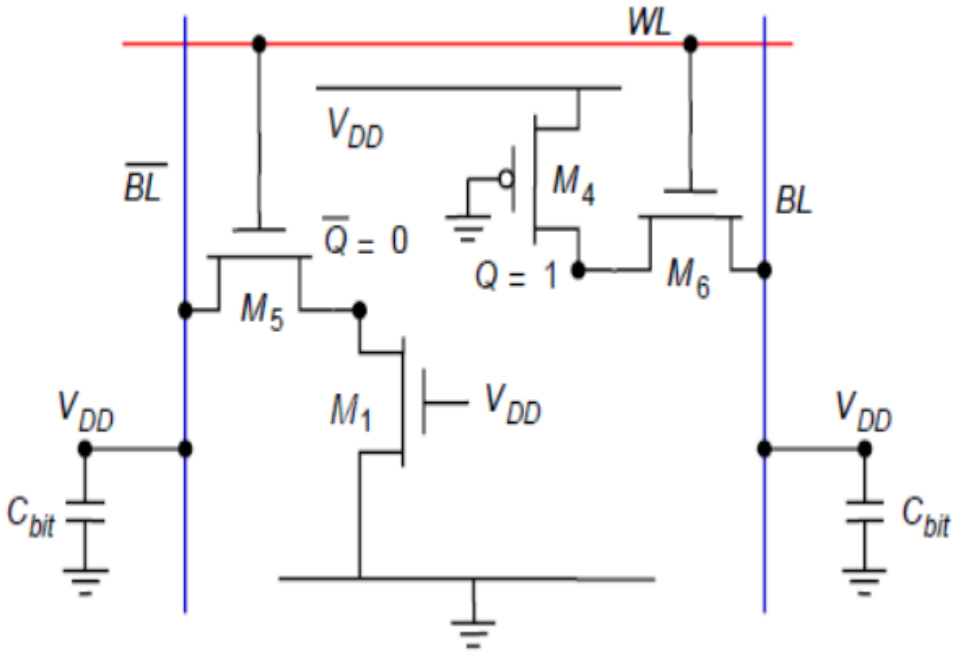
As Q=1 , M1 is ON, M2 is OFF in Inverter1 and Q'=0, M4 is ON and M6 is OFF in Inverter2

6T SRAM Cell – Read Operation

Reading Stored Q=1

Sequence of Operation

- ✓ Bit lines are pre-charged to V_{DD} =2.5V before the READ operation is initiated and then are switched OFF .
- ✓ Read cycle is started by making WL=High, enabling the tow Access Transistors M5 and M6 after initial word line delay.
- ✓ As M5-M1 are Active, BL' begins to discharge to ground potential through the series transistors M5 – M1 and BL remains at its pre-charge state.
- ✓ For a small-sized SRAM cell, W/L need to be small as much as possible. Therefor Ron of MOS is very HIGH.



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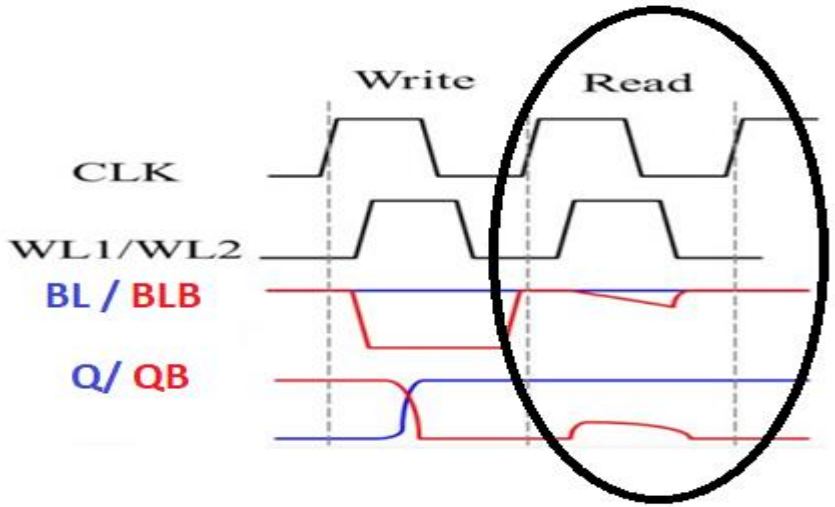
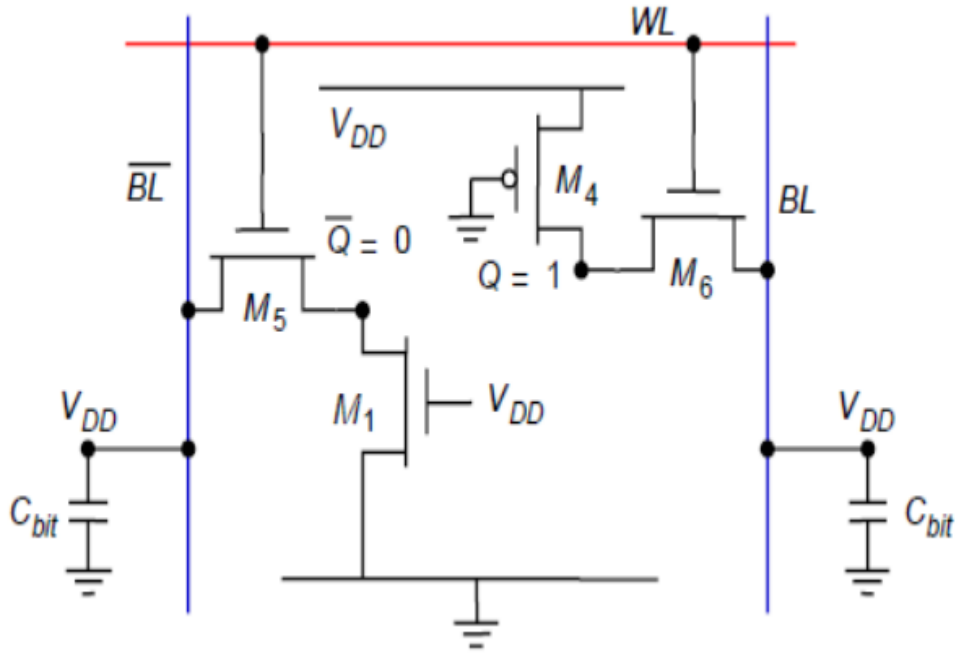
6T SRAM Cell – Read Operation

Reading Stored Q=1

Sequence of Operation

- ✓ As a result, the discharging current is less. This results in a slow discharge of LARGE bit line capacitance.
- ✓ As the difference between the 2 bit lines builds up, the sense amplifier is activated to accelerate the reading process. It quickly discharges BL' bit lines.





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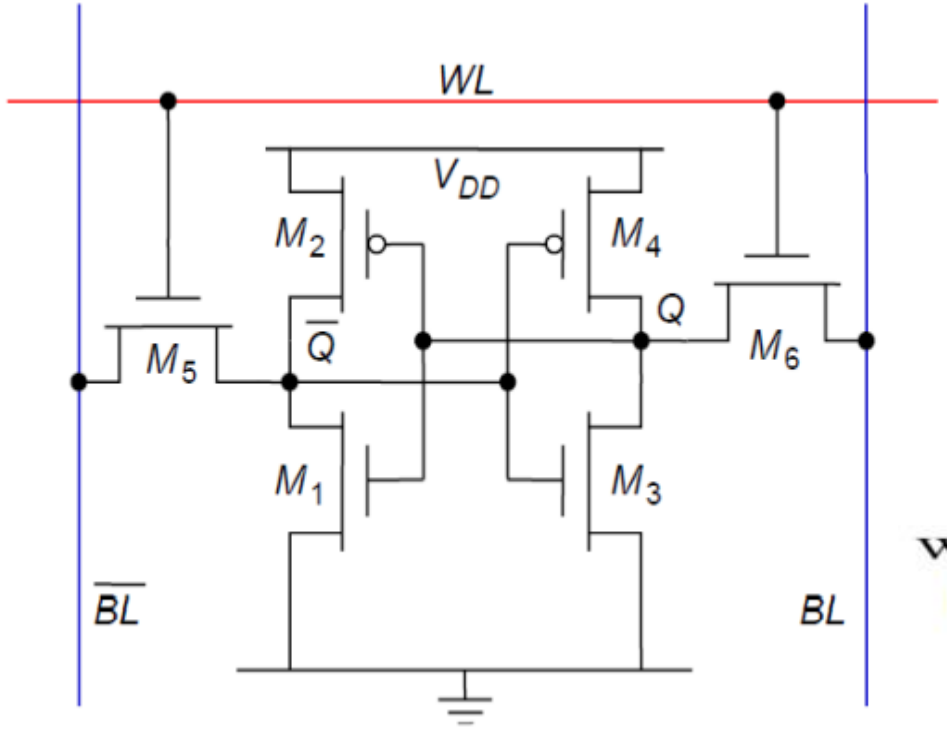
6T SRAM Cell – Design Aspects

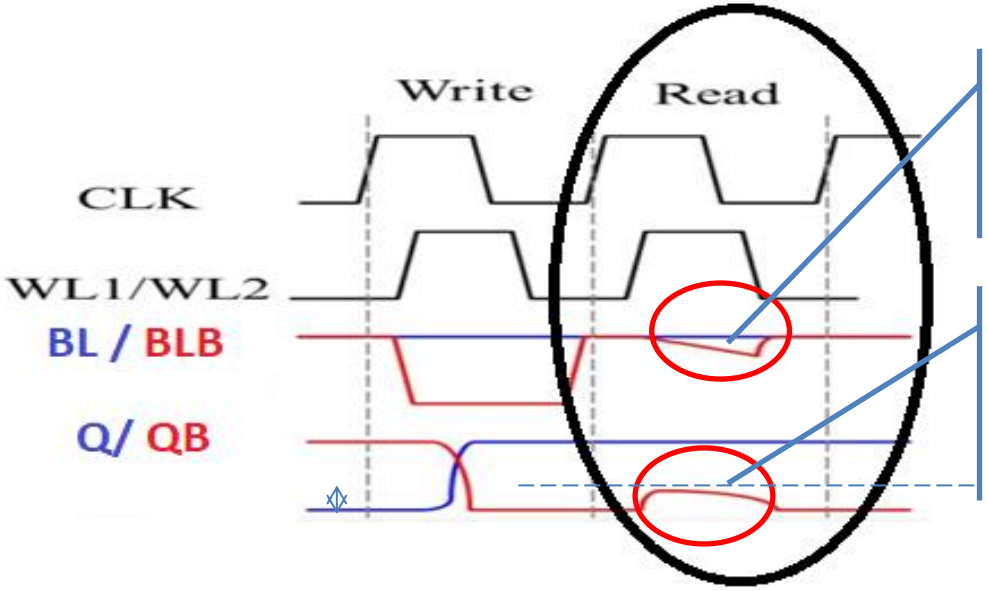
The two basic requirements which dictate the (W/L) ratios are :

(a) The **data-read operation** should **not destroy the stored information** in the SRAM Cell i.e., **Read Upset**

(b) The cell **should allow the modification** of the **stored information during the data- write phase.**



The Key design issue for the data-read operation is then to guarantee that the ***voltage*** ΔV ***does not exceed the threshold of M3***, so that the transistor M3 remains turned OFF during the read phase.



Reading'1' indicates BL' getting discharged but by ΔV

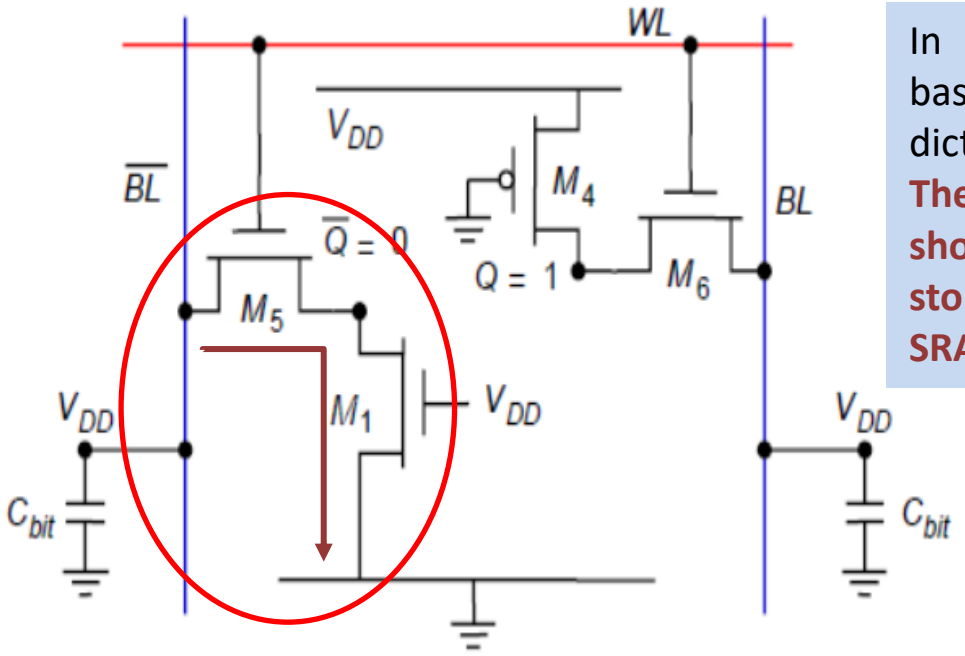
Reading'1' indicates Q' has increased which may cause Read Upset if Not less than Vtn

6T SRAM Cell – Read Operation

Reading Stored Q=1

What is Read Upset and how to address this issue ?

- ✓ Initially, upon the rise of WL, **Q' is pulled up towards the pre-charge value of BL'** as M5 is acting a pass Transistor .
- ✓ This voltage rise, ΔV at Q' **, must be low enough not to cause substantial current through M3 – M4 inverter**, which in the worst case could flip the cell. This type of malfunction is **called a read upset.**
- ✓ To prevent this, **resistance of M5 should be made larger than that of M1 to prevent ΔV from turning on M3 (Not destroying the stored data) .**
- ✓ $\left(\frac{W}{L}\right)_1 \gg \left(\frac{W}{L}\right)_5$ so that Resistance of M1 << Resistance of M5



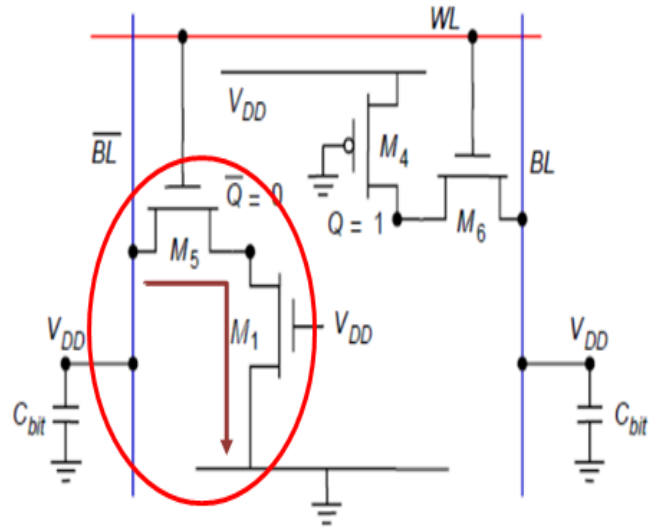
As Q=1 , M1 is ON, M2 is OFF in Inverter1 and Q'=0, M4 is ON and M6 is OFF in Inverter2

In 6T SRAM one of the basic requirement which dictate the (W/L) ratios is **The data-read operation should not destroy the stored information in the SRAM Cell.**

6T SRAM Cell – Read Operation

- **Resistance of M1 << Resistance of M5 so that ΔV at Q' does not exceed Vtn of M3.** If it exceeds it may lead to unintended change of the stored state.
- The Key design issue for the data-read operation is then to guarantee that the ***voltage*** ΔV ***does not exceed the threshold of M3***, so that the transistor M3 remains turned OFF during the read phase.
- The boundary constraints on device sizes can be determined by solving the current equation at the maximum allowed value of the voltage ripple ΔV .

$$\Delta V \leq V_{tn3} \quad \text{---------- (1)}$$



- We can assume that after the access transistors are turned on, the column voltage Vc remains approximately equal to VDD. Hence , **M5 operates in saturation while M1 operates in the linear region.**

$$\frac{k_{n\,5}}{2}(V_{DD} - \Delta V - Vtn)^2 = \frac{k_{n\,1}}{2}(2(VDD - Vtn)\Delta V - \Delta V^2) \quad \text{-------(2)}$$

$V_{GS} \geq V_{T0}$

Saturation

$V_{DS} > (V_{GS} - V_{T0})$

$I_D = \frac{Kn}{2}(V_{GS} - V_{T0})^2$

Linear

$V_{DS} \leq (V_{GS} - V_{T0})$

$I_D = \frac{Kn}{2}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2$

6T SRAM Cell – Read Operation

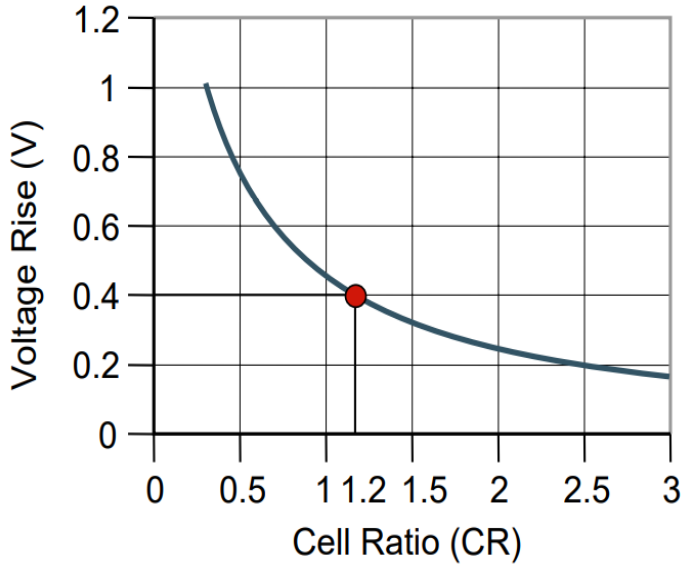
Substitute ΔV as V_{tn} in equation 2 and by simplifying the equation

$$\frac{k_{n\,5}}{k_{n\,1}'} = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_1} < \left[\frac{2(V_{DD} - 1.5Vtn)V_{tn}}{(V_{DD} - 2Vtn)^2}\right] \text{----------(3)}$$

By, Inverse of en (3) we get

and Cell Raio(CR)= $\beta = \frac{(W/L)_1}{(W/L)_5}$ ----------(4)

The variation of ΔV as a function of CR, for 250nm technology is shown below



To keep the node voltage (ΔV) from rising above the transistor's (M3) **threshold voltage (0.4V)**, **the cell ratio must be greater than 1.2.**
A **β value of 1.5 to 2.0** is typical in the industry. A β value less than 1 implies that, each time the cell is read, it is disturbed as well

To achieve the desired value of CR, W1 is increased while L1 = L5.

6T SRAM Cell – Read Operation

Substitute ΔV as V_{tn} in equation 2 and by simplifying the equation

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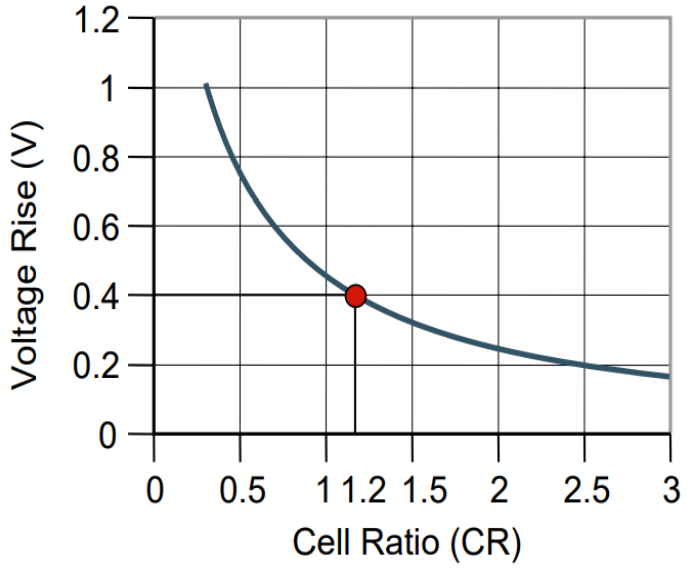

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To achieve the desired value of CR, W1 is increased while L1 = L5.

6T SRAM Cell - Read Operation

SRAM cell's stability

- An SRAM cell's stability can be described by the **"Butterfly curve"** which is obtained by **super-imposing the Voltage Transfer Curves (VTC) of the 2 Inverters of Memory Cell.**

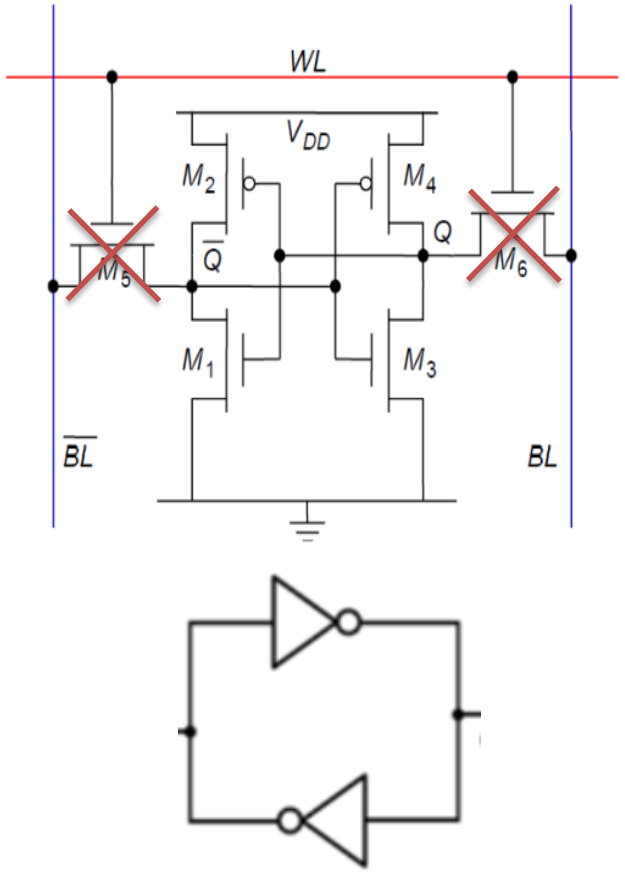
- Stability can be Analyzed by measuring **Static Noise Margin (SNM)** which we obtain by Analyzing the Memory Cell in READ state as there will be possibility Noise getting added. This Noise added may change the state.

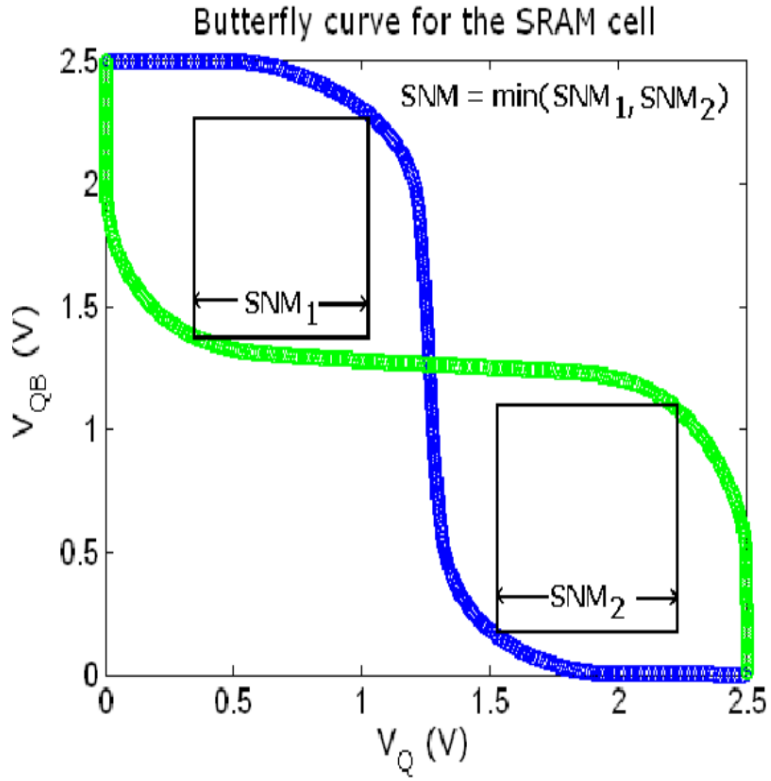
- The **Stability of the cell is given** by the size of the **Maximum square box** that can fit inside the **"Butterfly wing"**

6T SRAM Cell - SRAM cell's stability

Hold State : WL=0 and Access Transistors M5 and M6 are OFF

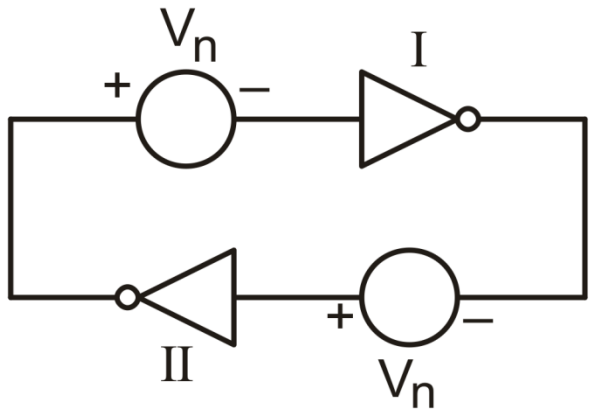
- As access Transistors are in OFF state the Cell is isolated from BL and BL', Therefore there is No possibility of state changing as there will be less chance of Noise interference.
- If we plot VTC of INV1 and INV2 and **super-imposing the VTCs we get butterfly curve.**
- As there is No Noise getting added, the **Inverters are working with a perfect VTC as shown** and gives Hold state Static Noise Margin (SNM) which is expected to be Maximum

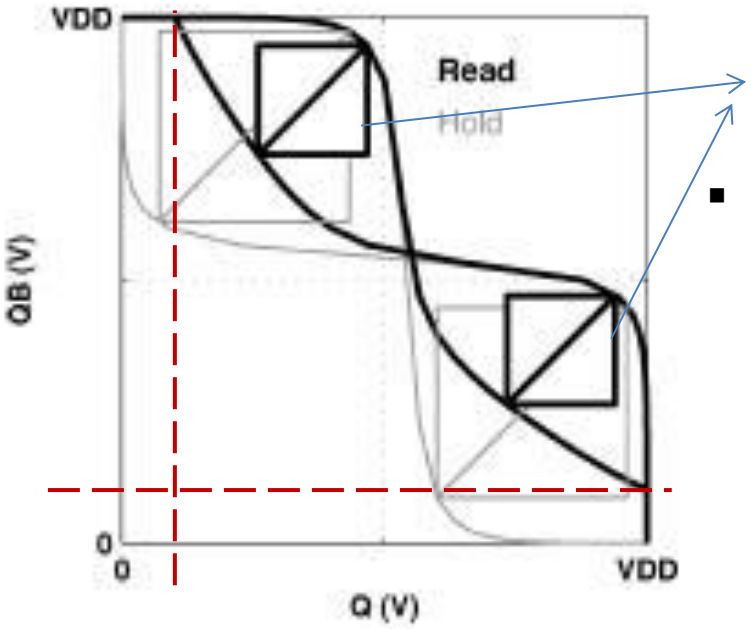




6T SRAM Cell - SRAM cell's stability

READ State : WL=1 , Access Transistors M5 and M6 are OFF and Bit lines are Pre-charged to V_{DD}



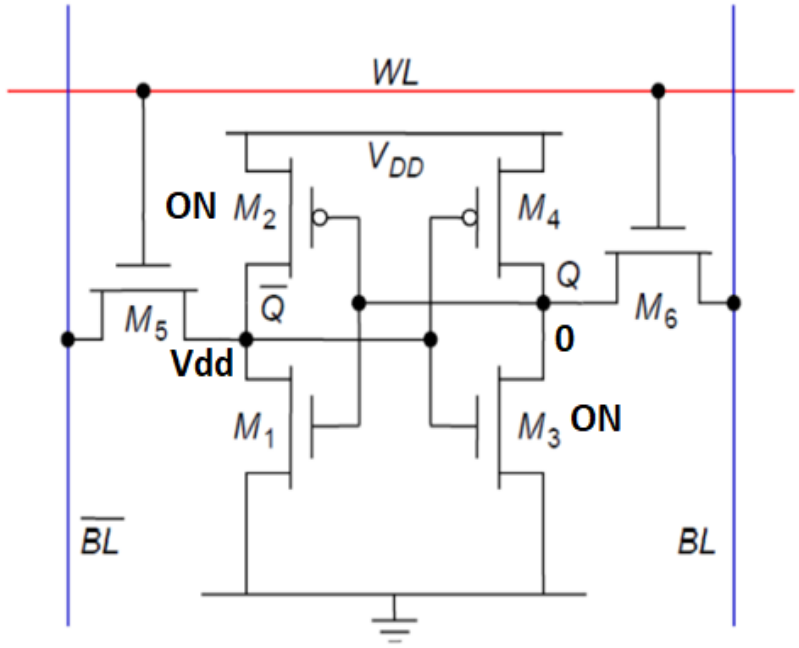


- In this figure, two squares are fit between the VTC curves. These squares are the largest possible squares that can be fit between the two inverter characteristic curves of the **SRAM cell for Read and hold state.**
- In READ, In order to find the SNM of the cell, you can measure the side lengths of both of these squares, and the smaller of the two lengths is the SNM of the SRAM cell.
- In an **ideal case** (no variations considered), **these squares should be of equal size**, and therefore only one square would need to be considered, however considering variations and transistor mismatch, these curves may not be mirror images of each other, and therefore both squares should be considered.

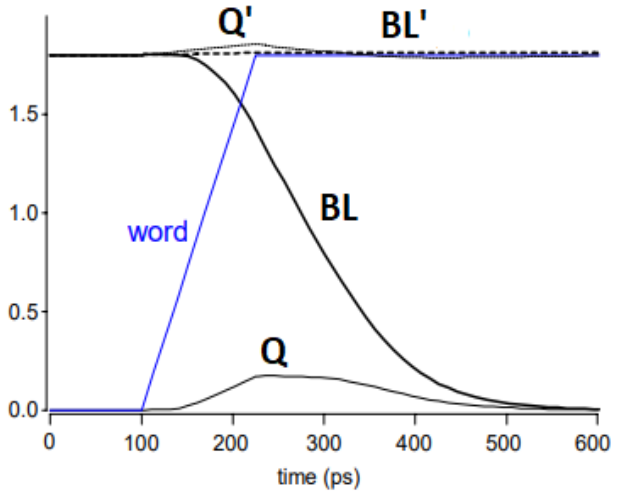
Key Points

- ✓ **The larger the box, higher the β value and hence greater the stability.**
- ✓ The curve flattens during a read operation, reducing the box size and thus implying reduced stability.

6T SRAM Cell – Read ‘0’

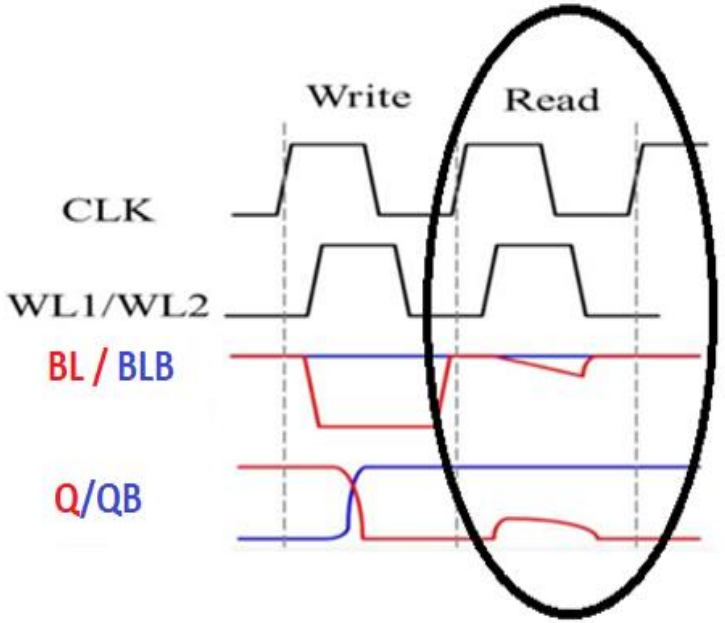


Reading '0' where in HOLD state Q=0 and Q'=1



BL discharges and BL' remains HIGH. but, Q bumps up slightly during READ operation

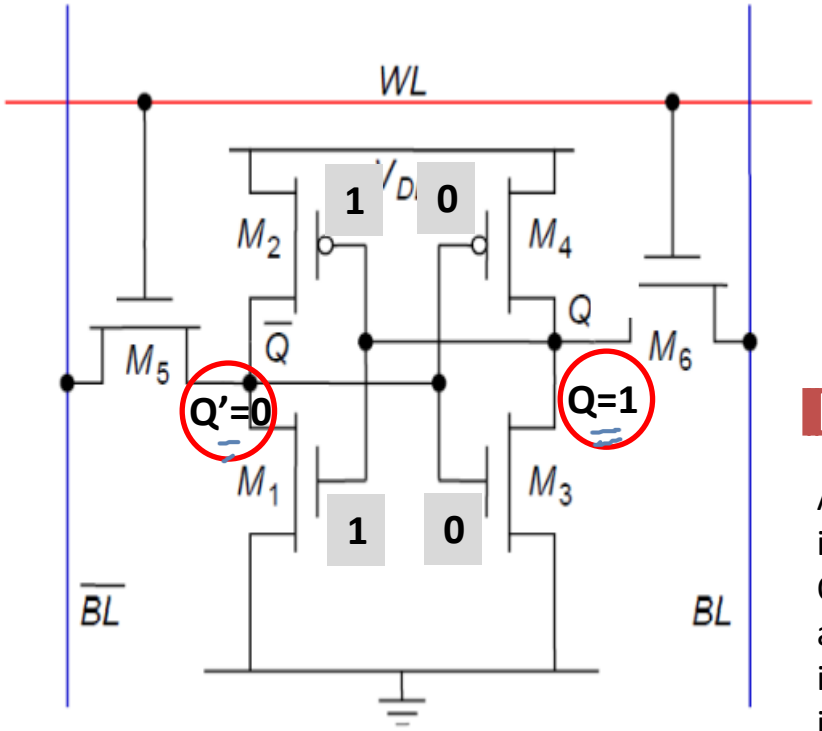
BL discharges through SA to Logic 0



6T SRAM Cell – Write Operation

Writing '0'

Assume that a '1' is current data stored in the cell, ie., Q = 1.



Simplified Model of 6T SRAM during when Stored data is '1''

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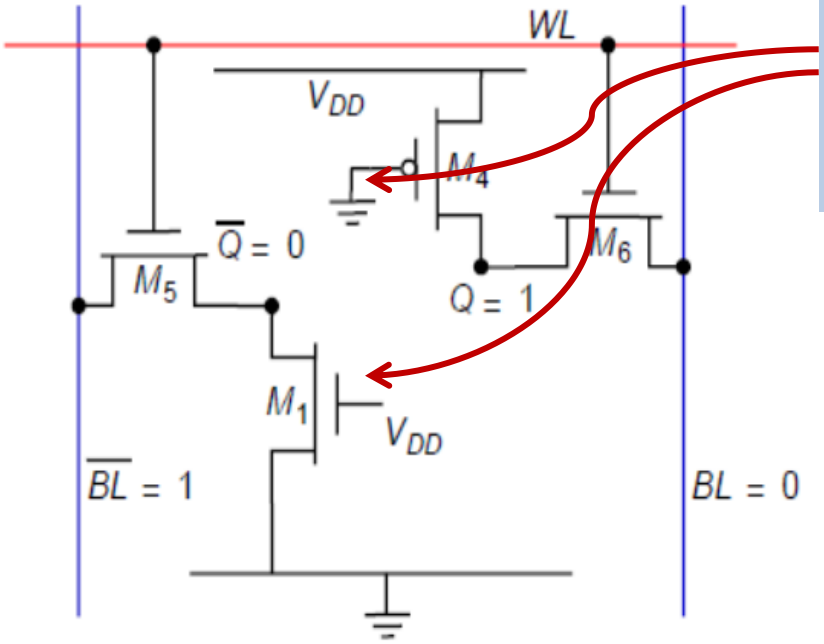

The gate of M1 and M4 stay at VDD and GND, respectively, as long as Switching has NOT commenced

A '0' is written into the cell by setting to BL' to '1' and **BL to '0'.** The simplified model of SRAM cell just before write begins is shown

6T SRAM Cell – Write Design Aspects

The two basic requirements which dictate the (W/L) ratios are :

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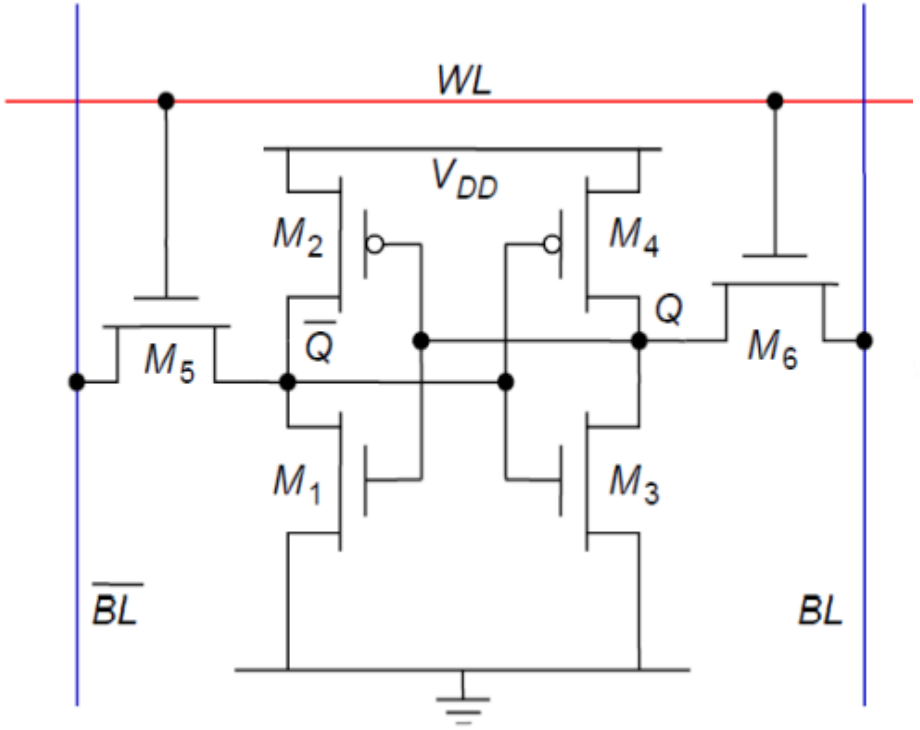

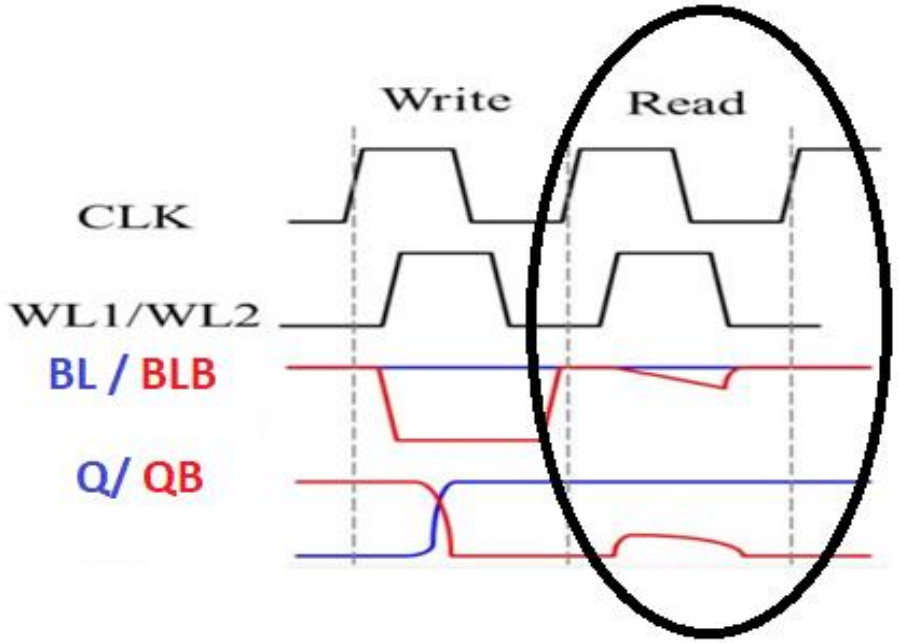

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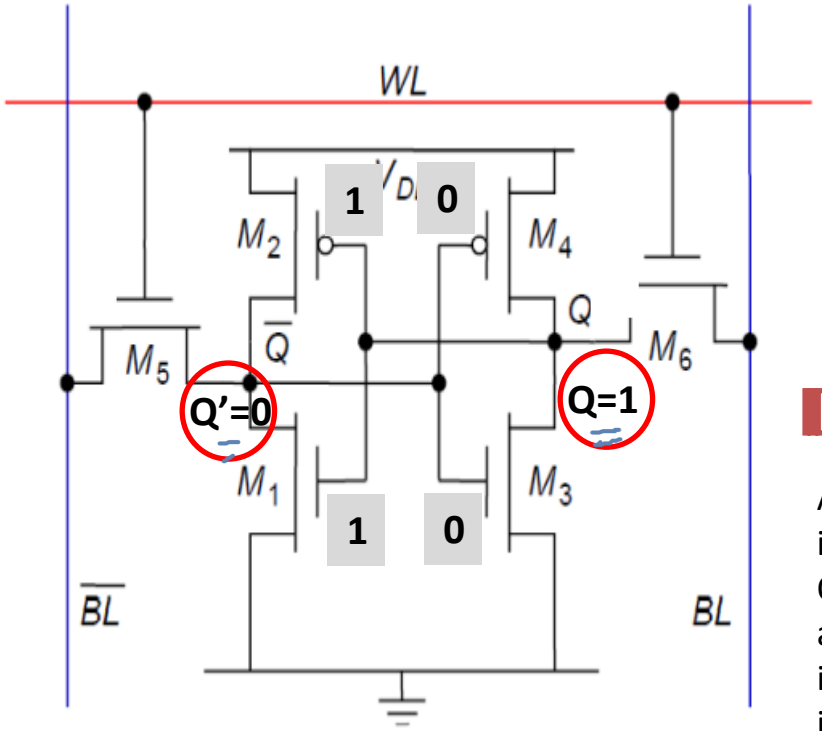

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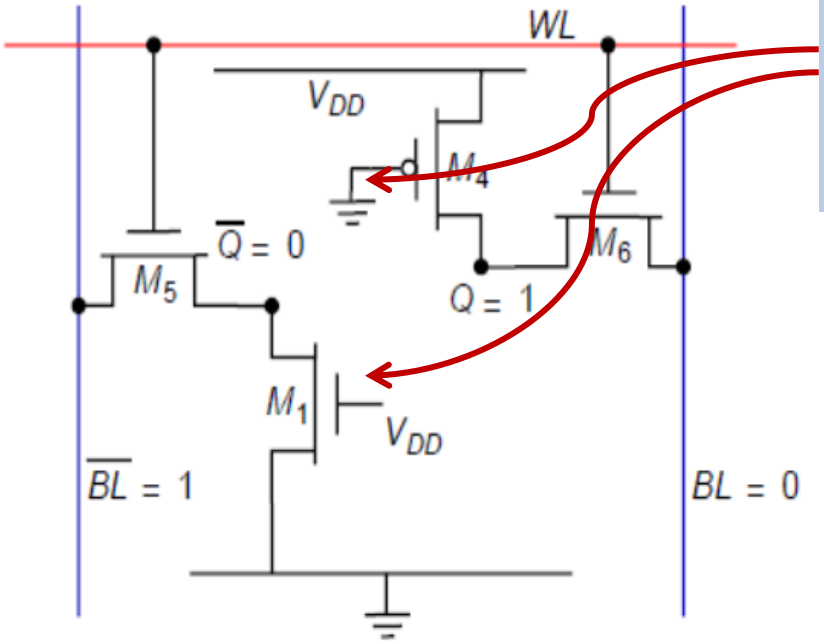

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6T SRAM Cell – Write Operation

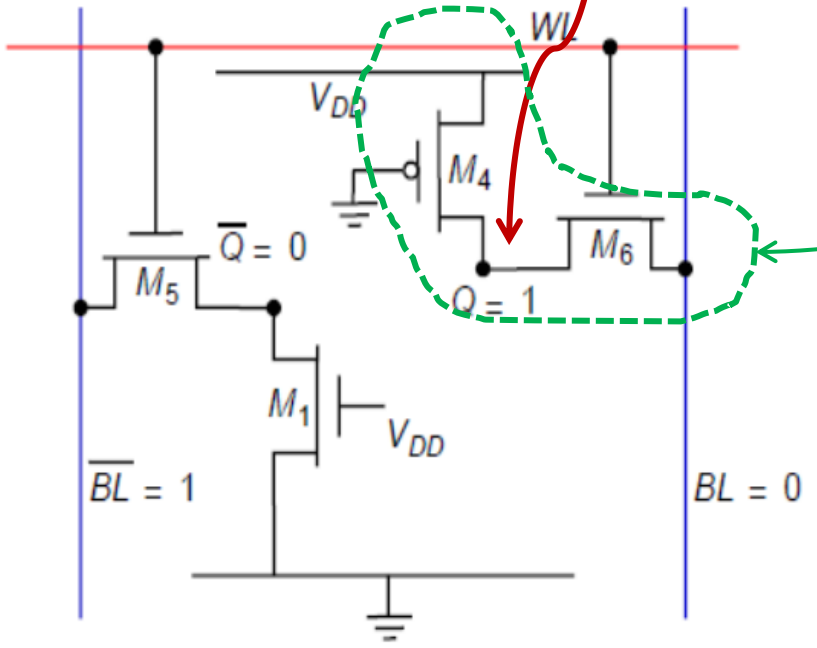
Writing '0'

Sequence of Operation

- Now lets consider writing a "0" to a cell that is storing a "1".
- The write driver makes BL=0V and BL'= VDD as '0' is written into the cell.
- Now the address decoder makes WL=1.
- Q' side of the cell cannot be pulled high enough to ensure the writing of '1' due to sizing constraint imposed by the read stability. It ensures that this voltage is kept below 0.4V.
- Hence the new value of the cell has to be written through transistor M6 . **Data '1' will be written into the cell if node Q is pulled down, below the threshold voltage of M1 to turn it OFF.**

We have to make this node voltage less than the threshold voltage of M1

Making the node voltage Q = 0V entirely depends on the design of M6 and M4 transistors



6T SRAM Cell - Write Operation

Writing '0'

Transistor M6 has to push the data '0' from BL to Q and On the other hand M4 , tries to pull-up Q to 1.

Hence for reliable writing, M6 must be stronger than M4 so that Node Voltage at Q reduces to less than Vtn, M1 to turn it OFF.

Under this condition (Q=Vtn) , the transistor **M6 operates in linear region** and **M4 operates in the saturation region**

$$\frac{k_{n\,4}}{2}(0 - VDD\ - V_{tp})^2 = \frac{k_{n\,6}}{2}(2(VDD - Vtn)V_{tn} - V_{tn}^2) \quad \text{----------(1)}$$

by simplifying the equation

$$\frac{k_{n\,4}}{k_{n\,6}} < \left[\frac{2(V_{DD} - 1.5Vtn)V_{tn}}{(V_{DD} + Vtp)^2}\right]$$

$$\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_6} < \frac{\mu_n}{\mu_p} \cdot \left[\frac{2(V_{DD} - 1.5Vtn)V_{tn}}{(V_{DD} + V_{tp})^2}\right] \text{----------(2)}$$

To summarize, the transistor M1 will be forced into cut-off mode during the write"0" operation if the above conditions are satisfied. It means M3 turns ON.

6T SRAM Cell - Write Operation

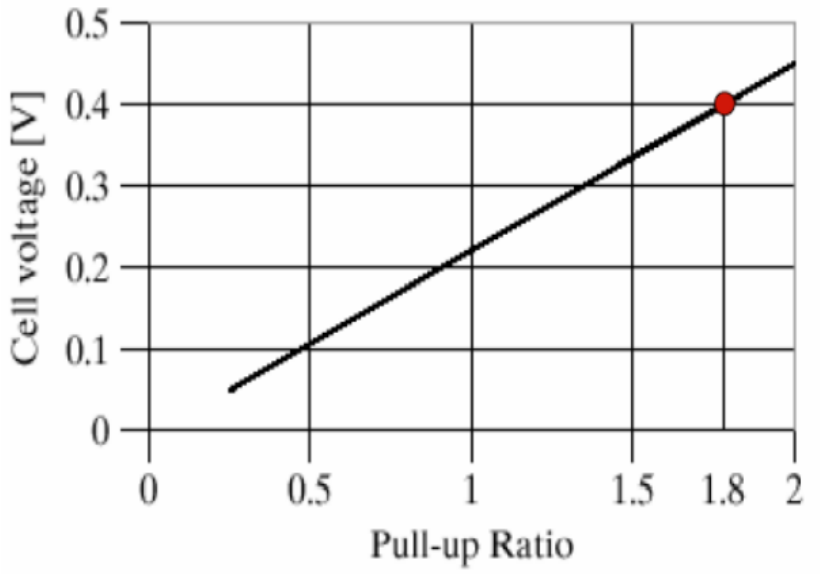
Writing '0'

Thus **the pull –up ratio PR** for write operation is given by

$$PR = \frac{(W/L)_4}{(W/L)_6} \quad \text{----------(3)}$$

The dependence of Voltage at node Q, V_Q , on PR for a 0.25 um process is shown below

To pull – down node Q below the threshold voltage, 0.4V, of M1 , PR should be less than 1.8. Therefore, the transistor sizing for efficient read and write operations: Pull – down transistors M1 , M3 – strongest, Pull-up transistors M2 , M4 – weakest, Transfer transistors - Medium



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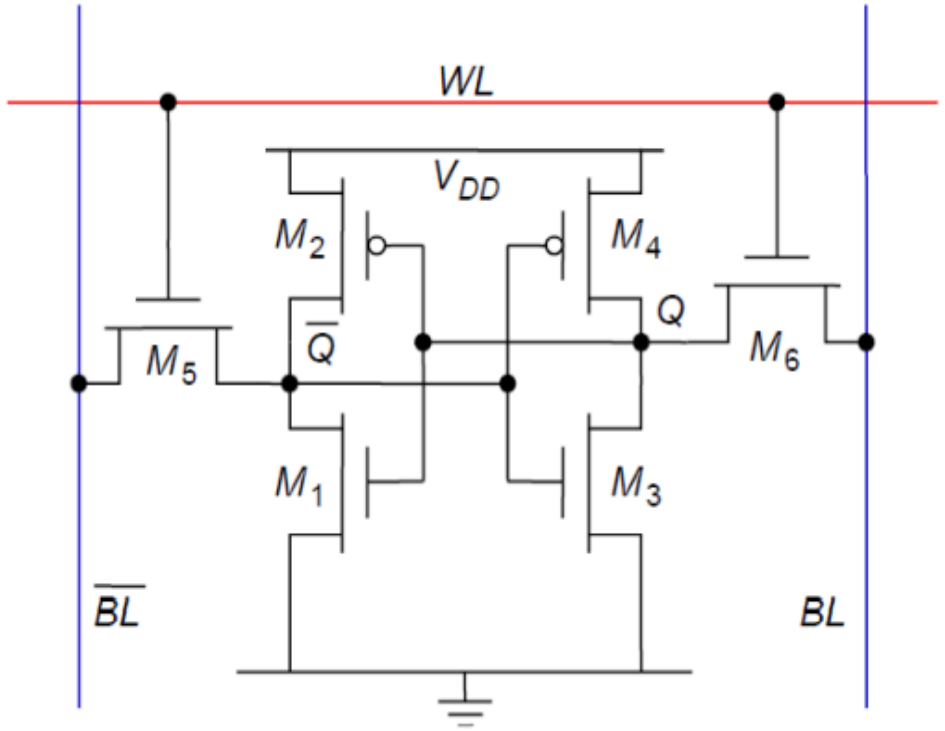

Advantages

- 6T SRAM, while simple and reliable
- Most popular due to the **lowest static power dissipation** among the various circuit configurations and compatibility with current logic process.
- Providing both polarities improves the noise margins during read and write operations
- Superior switching speed.

Disadvantages

- Consumes a substantial area because of Number of Transistors used and Placing the 2 PMOS transistors in the N-well significantly contributes to the area.

THANK YOU

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