Semiconductor Memory Design and Testing QUESTION BANK

UNIT-1

1) Explain how Read Upset is addressed in SRAM Read operation with necessary diagram and condition.
2) Explain the Transistor sizing to be maintained so that the SRAM cell allows modification of the stored information.
3) What is the Significance of Butterfly curve? Explain it with Hold and Read state butterfly curves. Comment why stability is HIGH in hold state.
4) Explain the working of 6T SRAM and also draw the layout/ stick diagram for the
5) same.
6) Write a comparison between 4T, 6T and 7T SRAM Cells.
7) Why sense amplifier need to be isolated from bit lines? Explain the function of bit switch Isolation circuit.
8) What is metastable state of cross coupled Inverters? Explain how cross coupled Inverters work as Sense amplifier in SRAM.
9) Explain how Sense Amplifier Signal is being developed and latched with a neat waveform.
10) What is the function of pre-charge circuit? Explain the significance of equalizer transistor in 3 transistor pre-charge circuit.
11) Explain the working of 3 bit Static Decoder using NOR and what are the challenges of Decoder using NOR.
12) Explain the Hierarchical Decoders and it's advantage over decoder using NOR. Also write it's drawbacks.
13) Calculate Number of Transistors required to design 8:256 Decoder using
    a. Single stage NAND Decoder
    b. NAND gate Decoder using pre-decoder
14) Explain dynamic , 2 to 4 NAND and NOR decoder.