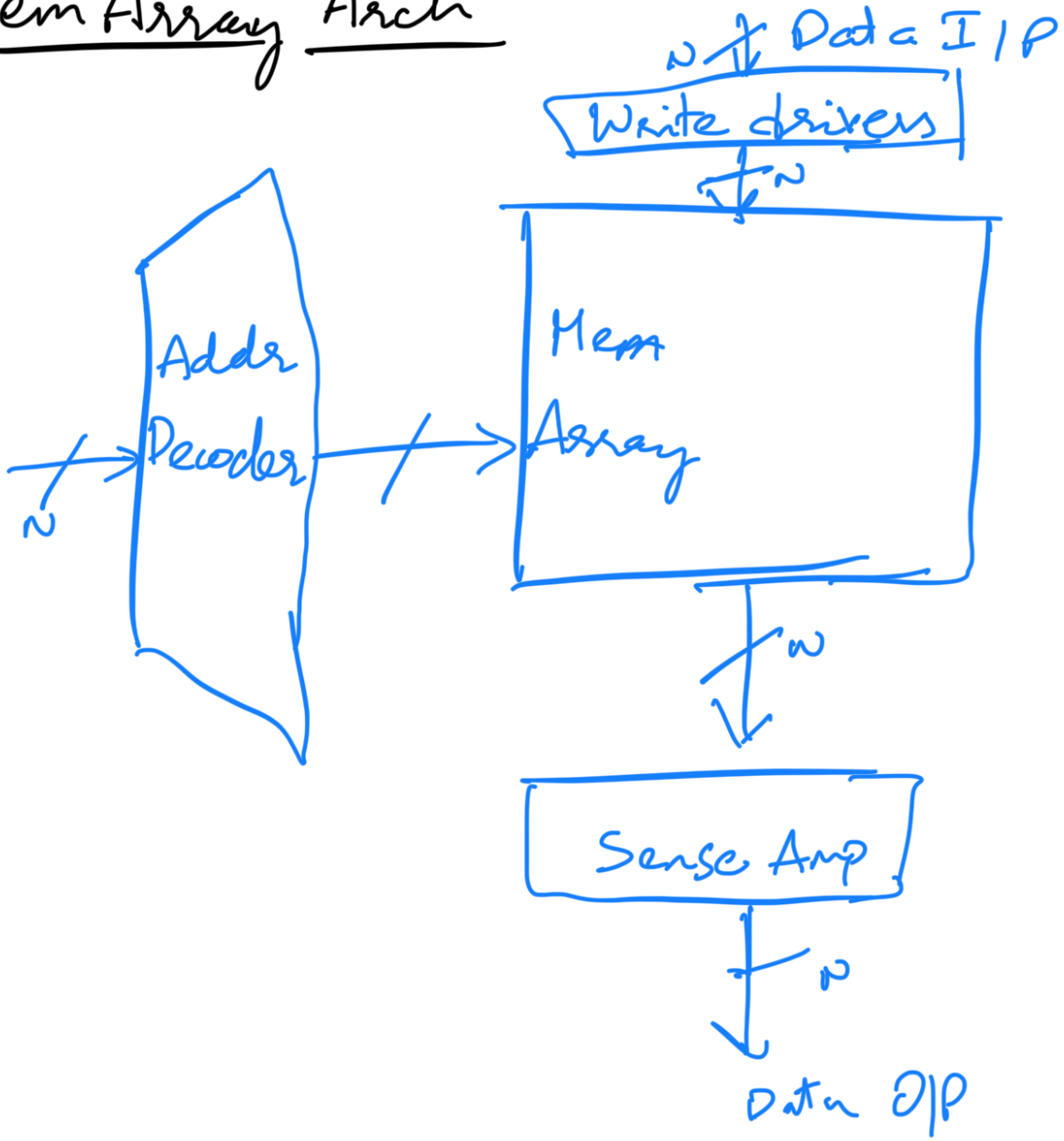
# Mem design

## Mem Array Arch




---

## Mem Org

N × M mem block

↑ ↑ ——— M # of bits

N # of words

} N words of M bit size

∴

→ need N selection lines to addr all locations
↳ driven from CPU

issue : For Large mem array as

**Select lines # = # of Mem locations**

Eg 1Mb mem would need $2^{20}$ # of select lines

Soln

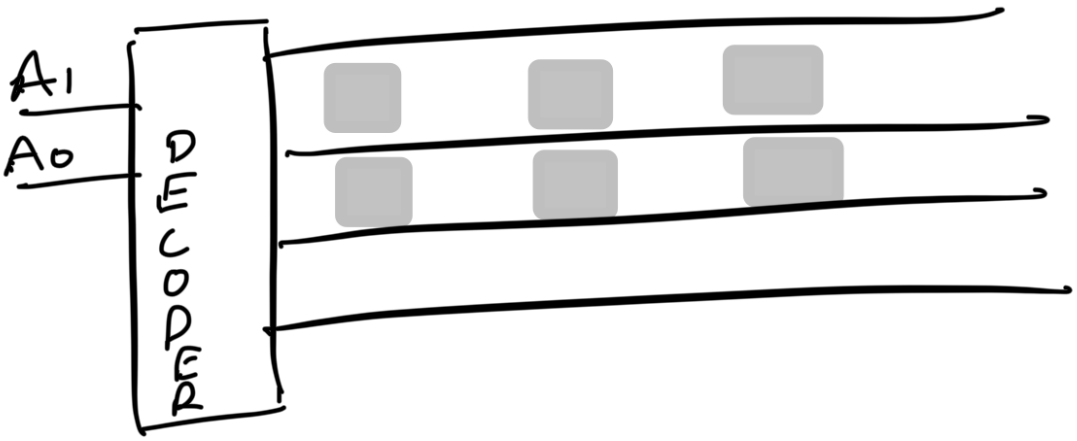
Decoder

↳ Addr decoder to reduce the # of select lines driven from CPU

∴ 1Mb mem needs $\log_2(2^{20}) = 20$

---

1K × M mem




F → Feature size

↳ Tech node

Min area to represent 1 bit = $150F^2$ where F stands for feature size which is nothing but the tech node

Eg ⇒ min size is

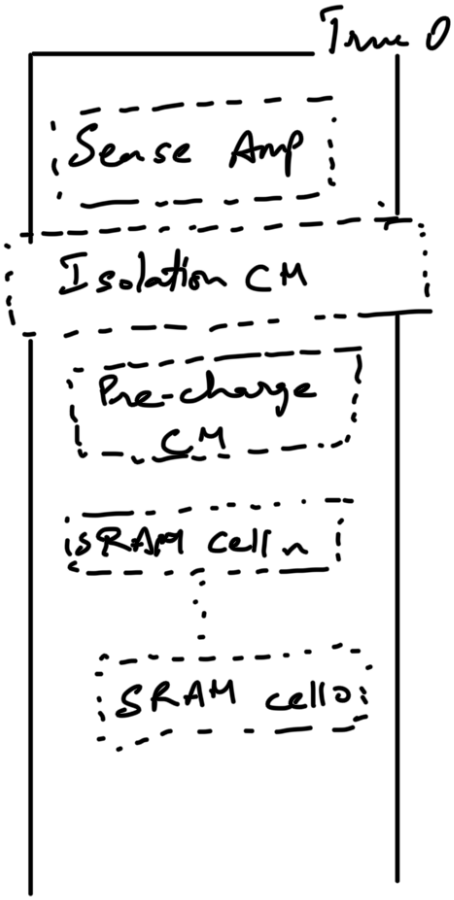
$150 \times (90 \times 90) = 12,15,000 \times 10^{-18}$

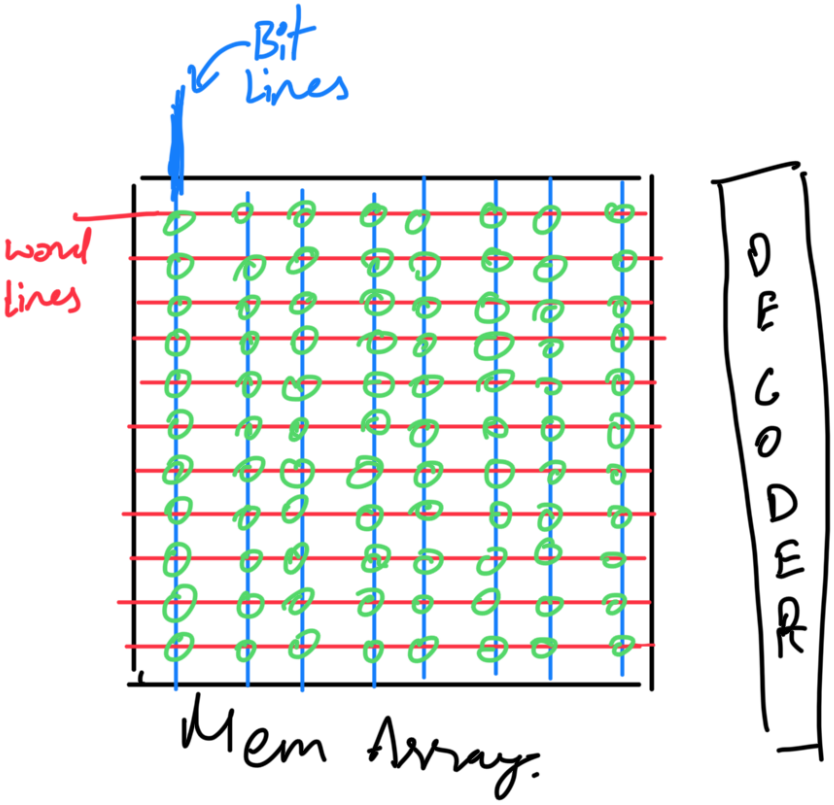
↑ nano

---

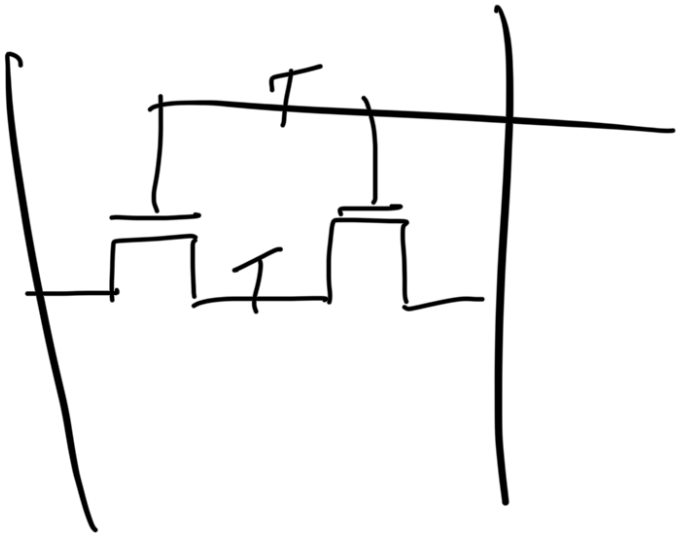
# FLASH

Read data path Cross sec. & the Peripheral circuitry



Pre-charge ckt using 2 PMOS devices.



Sense Amplifiers

Sense Amplifiers

Selected based on: - Voltage requirements
- mem arch