Memory Design and Testing

Mahesh Awati/Dr Shashidhar
Department of Electronics and Communication Engg.

MEMORY DESIGN AND TESTING

UNIT 1 – Semiconductor Memory Technology overview

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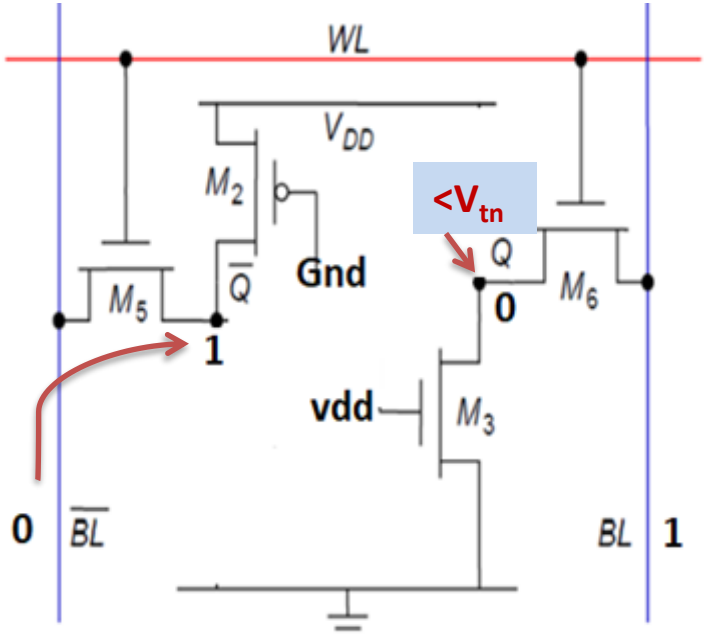
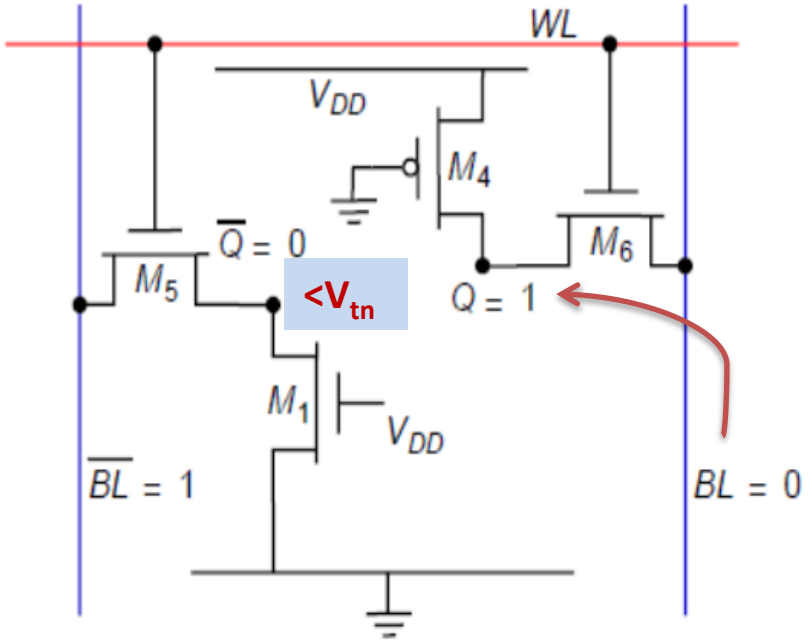
Write Driver Circuit

- The circuit that writes the data into the cells is called a write driver.
- Writing of data into the cell is **accomplished by writing '0' into either True or complemented side** of the cell and the Cell latch causes the opposite side to go to '1' state.



Writing '0' into **Complemented side** to Write '1'



Writing '0' into **TRUE side** to write '0'

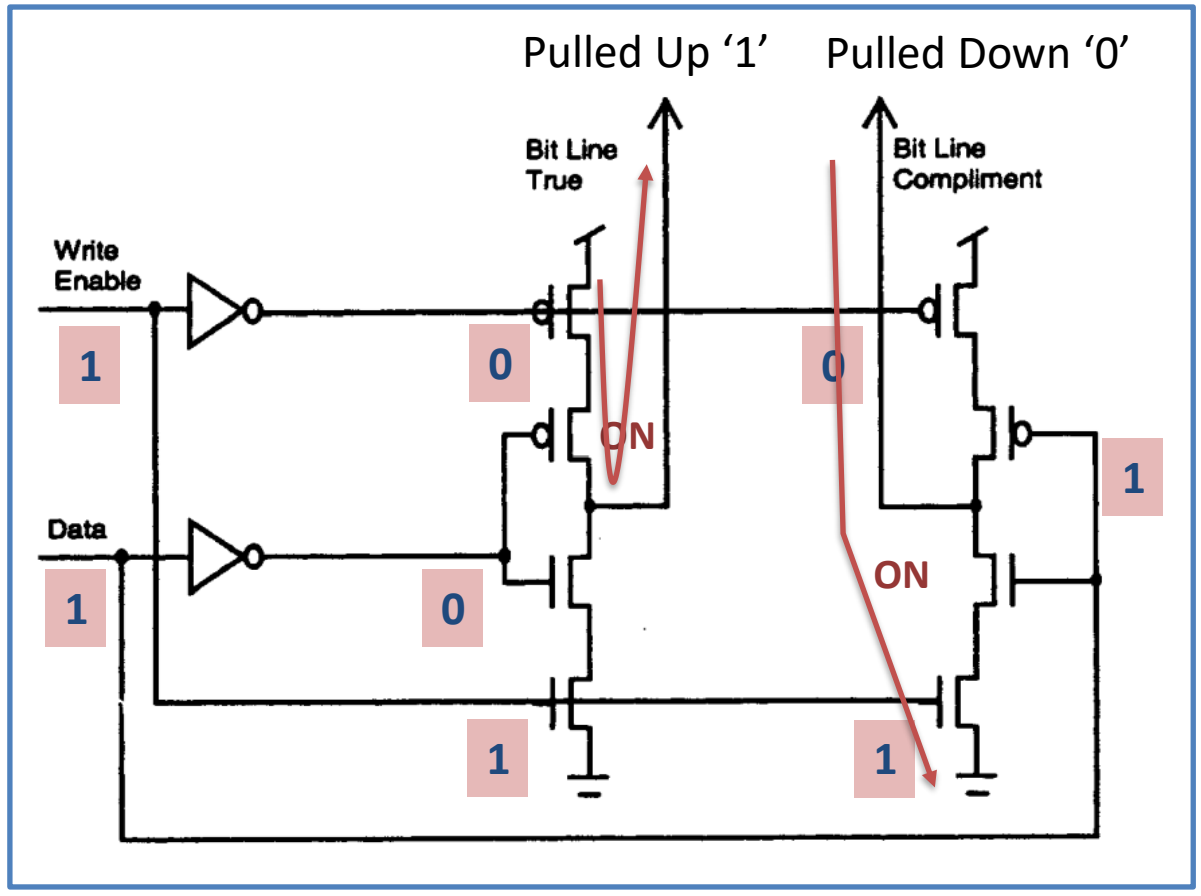
Reason: The **cells have transfer devices that are NFETs.** Thus the transfer devices drive a strong "0 but do not drive a "1" very effectively.

It can be viewed that a cell passes only a "0' and never a "1".

Since the transfer device passes only a "0", **the write head need only drive a "0"**

Write Driver Circuit

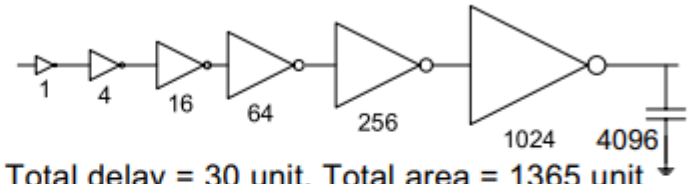
Writing of data into the cell is **accomplished by writing '0' into either True or complemented side** of the cell.



- The four vertical devices in series are often referred to **as a gated inverter.**
- When write enable (WE) is asserted high the write driver circuit drives the appropriate data values onto the bit line true and complement lines.
- Since the primary objective is to **drive a "0". the NFETs and PFETs may be similarly sized,** rather than the typical (2:1) ratio for PFETs to NFETs which is used for symmetry.

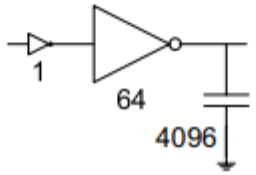
Write Driver Circuit

- Latency optimized



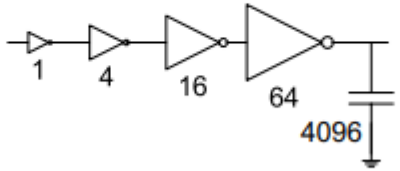
Total delay = 30 unit, Total area = 1365 unit

- Area optimized



Total delay = 130 unit, Total area = 65 unit

- Balanced design

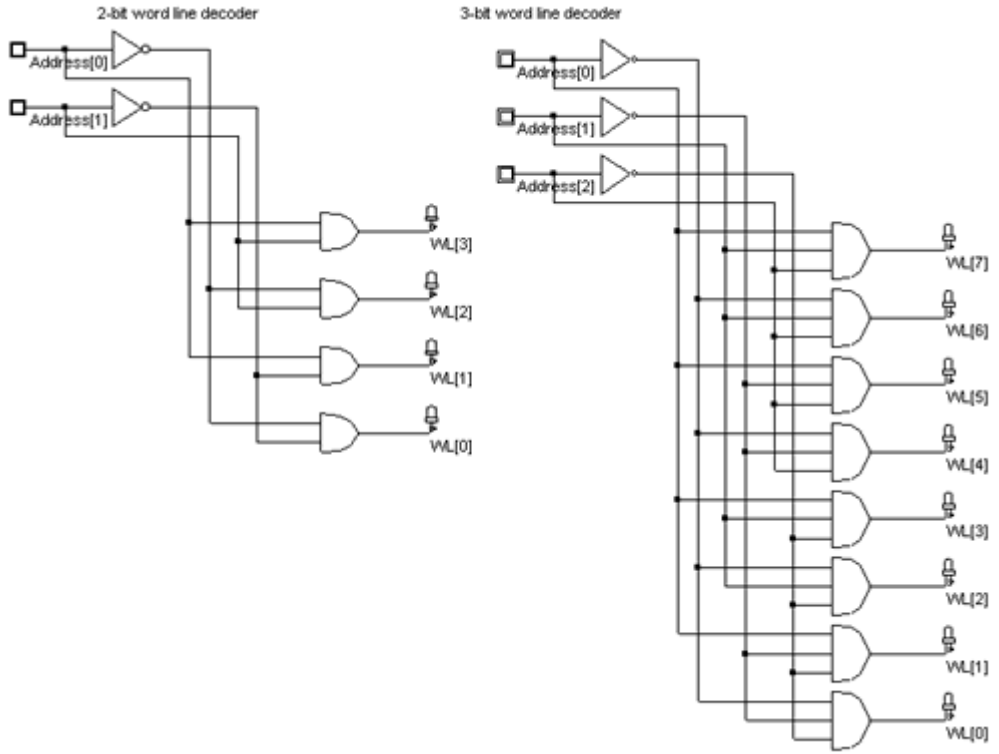


Total delay = 80 unit, Total area = 85 unit

- Lumped capacitance assumed to be 4096 units
- Optimization could be in terms of latency and area

Address Decoder

- Address Decoder are used to decode the Address of Memory Location to be accessed.
- Based on Memory size, there might be only Row Decoders or Both Row and Column Decoders. Smaller size memories will have only Row Decoders.
- Classification of Address Decoders
  1) Static Decoders
     a) Row Decoders
     b) Column Decoders
  2) Dynamic Decoders
     a) Row Decoders
     b) Column Decoders

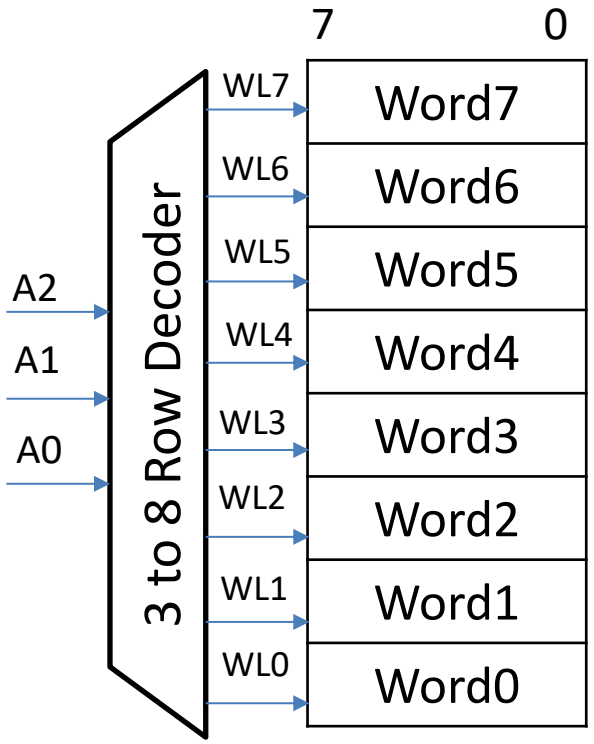


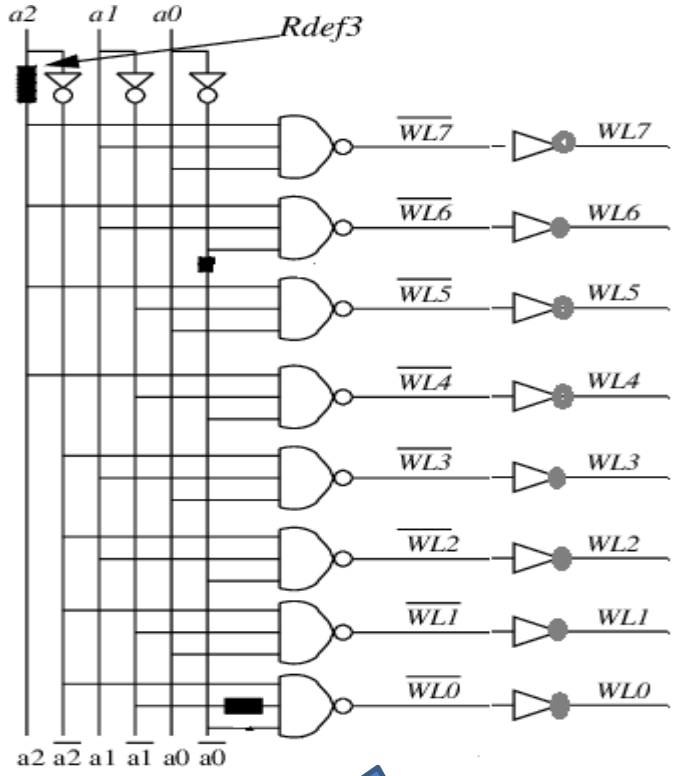
Address Decoder – Static Row Decoders

A 3 bit Address Decoder (Row)

Let us say, A Memory Size of 8 words of 8 bit Size to be addressed.

A2	A1	A0	WL
0	0	0	WL0
0	0	1	WL1
0	1	0	WL2
0	1	1	WL3
1	0	0	WL4
1	0	1	WL5
1	1	0	WL6
1	1	1	WL7

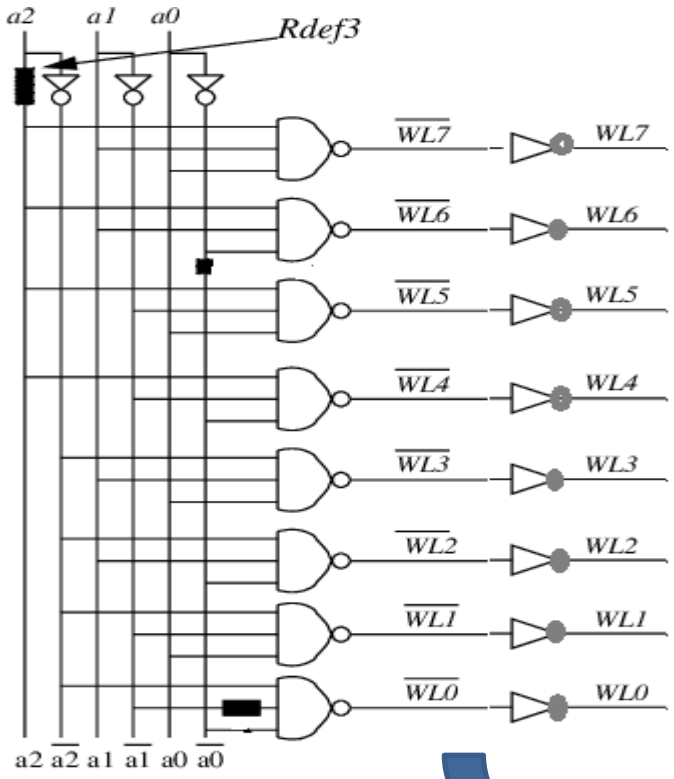




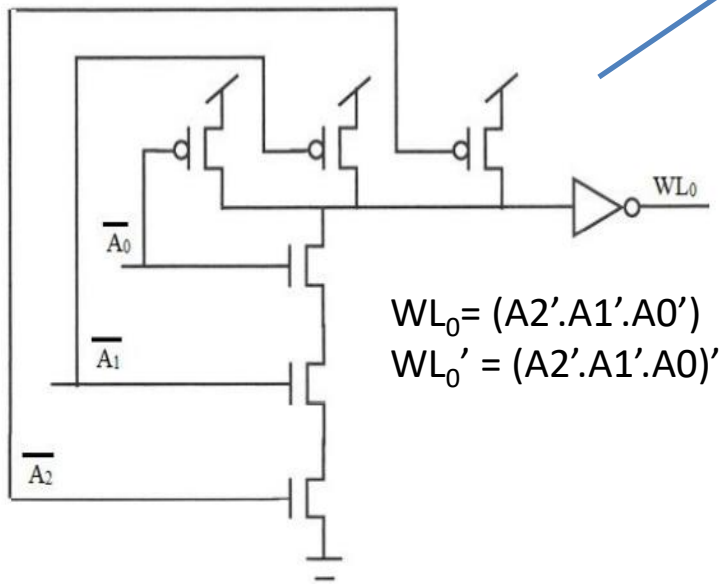
Address Decoder Static Row Decoders

A 3 bit Address Decoder (Row)

Let us say, A Memory Size of 8 words of 8 bit Size to be addressed.



Two Stage Implementation Using a 3 input NAND and INV



$WL_0 = (A2'.A1'.A0')$

$WL_0' = (A2'.A1'.A0)'$

8 such logics will give a 3 to 8 Row Decoders

This logic can also be Implemented using NOR gate
We have
$WL_0 = (A2'.A1'.A0')$
which can be written as
$WL_0 = (A2+A1+A0)'$

Single Stage Implementation using NOR gate reduces the Number of MOS devices required as No Inverter required.

Address Decoder -Static Row Decoders

Hierarchical Decoders

- Now, Splitting of Complex Logic gates into two or more logic Layers makes it Faster and Economical.
- This decomposition of CMOS Decoder makes them fast and area efficient. In this, Decoder is split in to Two Layers as
  - ✓ Pre-Decoder and
  - ✓ Final Decoder

Address Decoder -Static Row Decoders

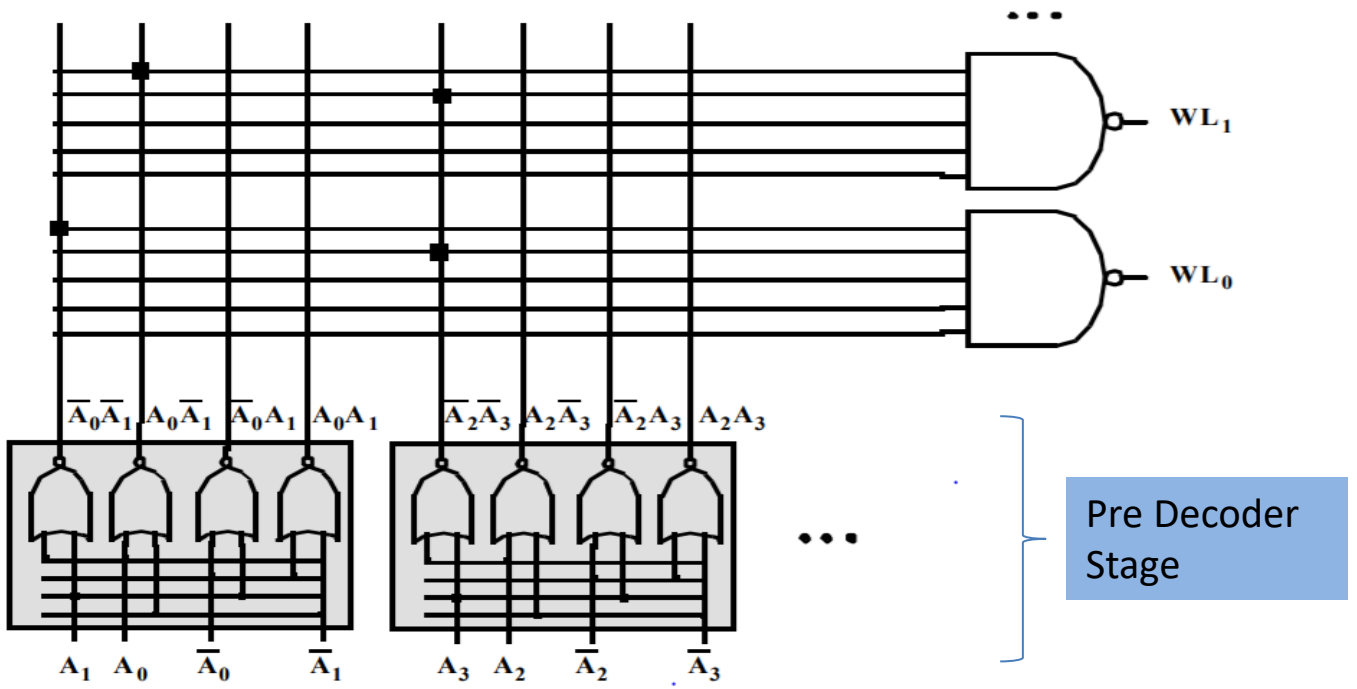
Hierarchical Decoders

- Let us consider 8:256 Decoder to be Implemented. The expression for Implementation of WL_0 using regrouping is as below

$$WL_0 = \overline{A_0.A_1.A_2.A_3.A_4.A_5.A_6.A_7}$$

$$= \overline{(A_0 + A_1)(A_2 + A_3)(A_4 + A_5)(A_6 + A_7)}$$

- We can see that Address in Stage 1 is partitioned into section of two bits that are decoded in advance.
- The resulting signals are combined using 4 input NAND gates to produce corresponding WL signals.



Address Decoder -Static Row Decoders

Advantages Hierarchical Decoders

1) Reduces Number of Transistors required.
2) As the Number of Inputs to NAND gates is Halved (4), the propagation Delay is reduced approximately by factor of 4.
   Gates with Fan IN greater than 4 should be avoided in order to reduce the propagation delay.
1) Adding a Select Signal each of the Predecoders (NOR gate) makes it possible to disable the decoder when Memory block is not selected. This results into Power Saving

Address Decoder -Static Row Decoders

Advantages Hierarchical Decoders

1) Reduces Number of Transistors required.

Calculate Number of Transistors required to design 8:256 Decoder using

a) Single stage NAND Decoder

b) NAND gate Decoder using predecoder

Write a comment based on Number of Transistors used

Total Number of Rows to be decoded is 256, (WL_{255} to WL_0)

a) Single stage NAND Decoder

In this,

Total Number of Transistors Required is = 256, 8 INPUT CMOS NAND gate

= 256 x 16 = 4096

a) NAND gate Decoder using predecoder

In this,

Total Number of Transistors Required is

= 256, 4 INPUT CMOS NAND in Final stage + 4 Sets of 4 , 2INPUT NAND

= (256 x 8) + (4 X 4 X 4) = 2112

Comment: The NAND using predecoder requires 52% Transistors of Single stage Decoders

Address Decoder -Static Row Decoders

Drawback Hierarchical Decoders

Still these designs require 4 input NAND gate are require to drive the large capacitive word lines.
The best Driver which can be used for driving large capacitive loads is an Inverter.
Therefore output NAND should be buffered.
To drive Large Capacitive load Multi stage of logics should be used. Therefore eqn

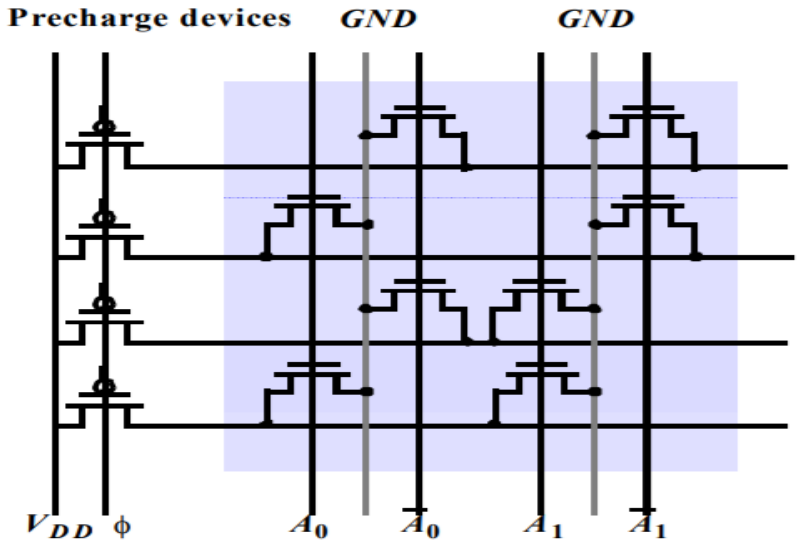
$$WL_0 = \overline{\overline{A_0}.\overline{A_1}.\overline{A_2}.\overline{A_3}.\overline{A_4}.\overline{A_5}.\overline{A_6}.\overline{A_7}}$$

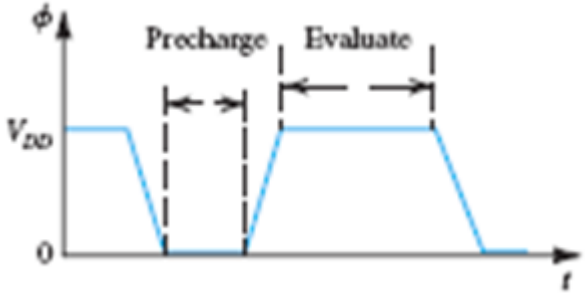
Can be broken into additional levels of logic, each of which consists of 2 input NANDs, 2 input NORs or Inverters

Address Decoder -Dynamic Decoders

Dynamic 2 to 4 NOR Decoder

- Dynamic Logic 2 input NOR gate is used in this topology.
- When Clock Ø=0; The outputs are in Pre-charged state (WL3-WL0) are HIGH.
- When Clock Ø=1; the circuit is Evaluation state where in the o/p depends on address lines A1,A0



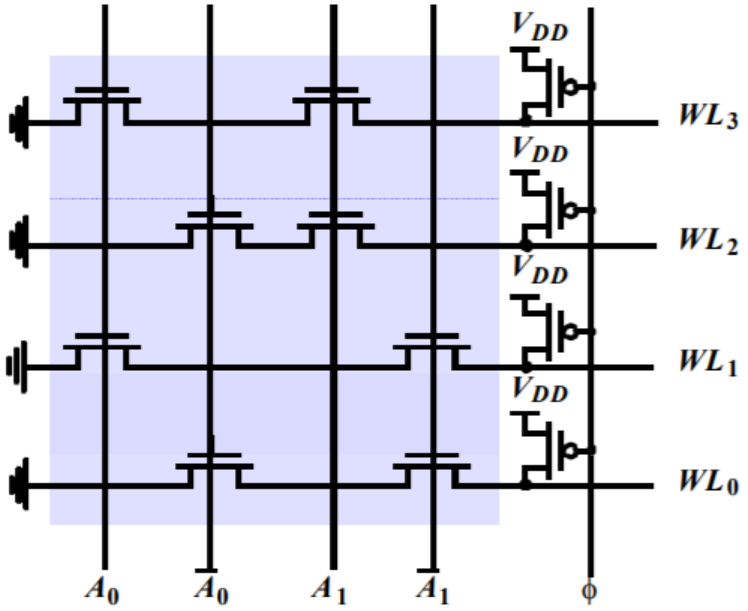


Ø	A1	A0	WL3	WL2	WL1	WL0	State
0	X	X	1	1	1	1	Pre-charged State
1	0	0	0	0	0	1	Evaluate State (WL0 is Selected)
1	0	1	0	0	1	0	Evaluate State (WL1 is Selected)
1	1	0	0	1	0	0	Evaluate State (WL2 is Selected)
1	1	1	1	0	0	0	Evaluate State (WL3 is Selected)

Address Decoder -Dynamic Decoders

Dynamic 2 to 4 NAND Decoder : It gives Active Low output.

- Dynamic Logic 2 input NAND gate is used in this topology.
- When Clock Ø=0; The outputs are in Pre-charged state (WL3-WL0) are HIGH.
- When Clock Ø=1; the circuit is Evaluation state where in the o/p depends on address lines A1,A0.
- In this, All the outputs of the Array are HIGH by default except the Selected row based on A1A0.

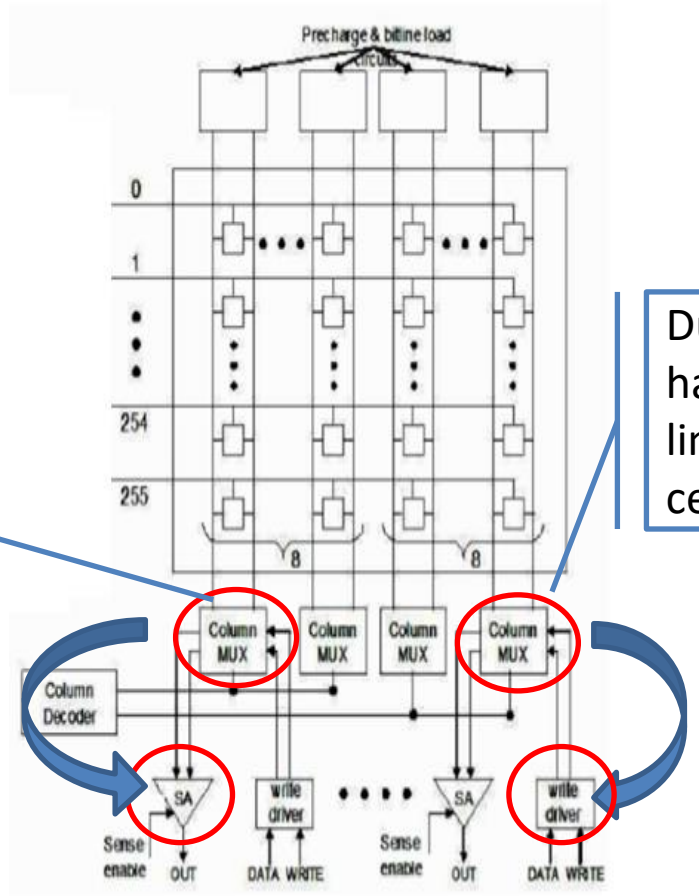


Ø	A1	A0	WL3	WL2	WL1	WL0	State
0	X	X	1	1	1	1	Pre-charged State
1	0	0	1	1	1	0	Evaluate State (WL0 is Selected)
1	0	1	1	1	0	1	Evaluate State (WL1 is Selected)
1	1	0	1	0	1	1	Evaluate State (WL2 is Selected)
1	1	1	0	1	1	1	Evaluate State (WL3 is Selected)

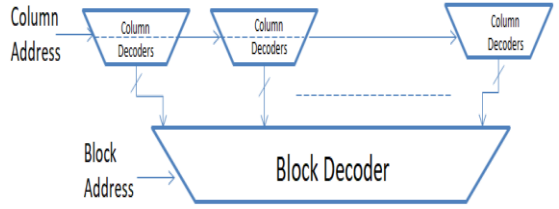
Column and Block Decoder

- Column Decoders should match with bit line pitch of the Memory Array.
- Column and block Decoder does the function of 2^k Input Multiplexer, **where k is size of the address word.**
- **For Read-Write Operations** these Multiplexers may be shared or separate.

During Read operation they have to provide the discharge path from pre-charged bit lines to sense Amplifiers (SA)

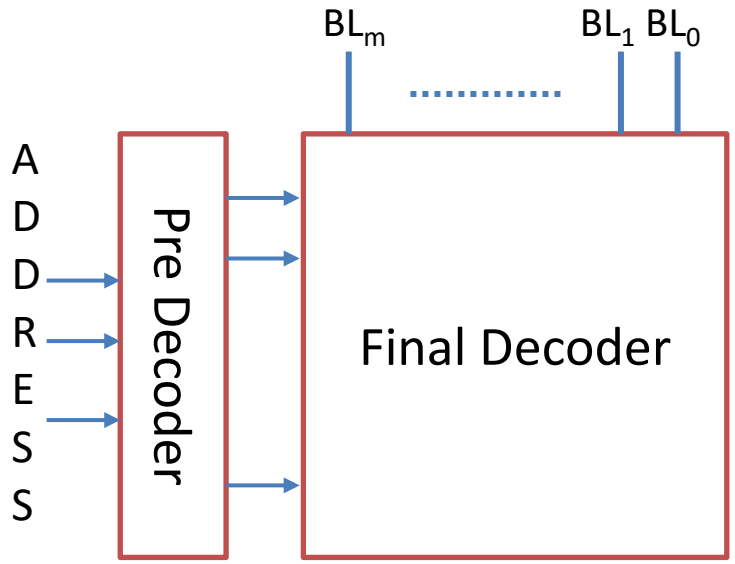


During Write operation they have to be able to drive the bit line low to write 0 in memory cell.

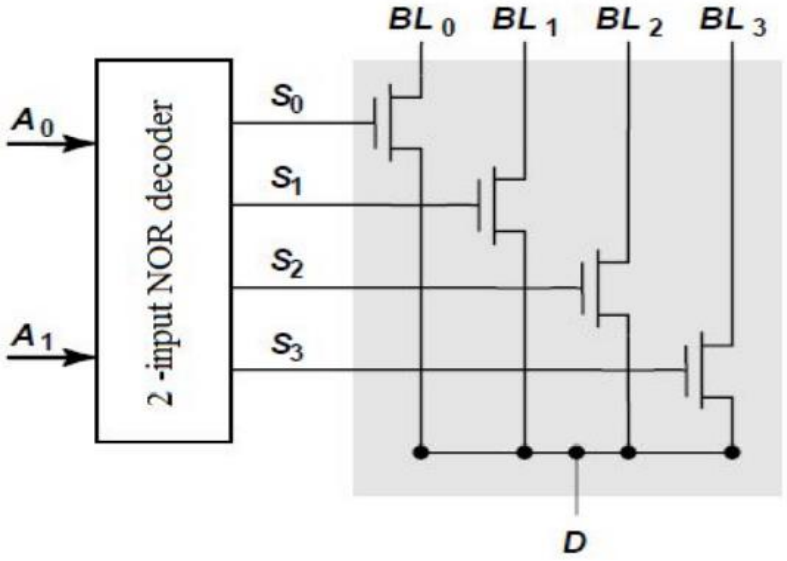


Column and Block Decoder

Column Decoder using NOR predecoder



1) MUX using NMOS Pass Transistor



2) MUX using CMOS Transmission Gate can also be used.

A1	A0	S3	S2	S1	S0	Out put D
0	0	0	0	0	1	BL0
0	1	0	0	1	0	BL1
1	0	0	1	0	0	BL2
1	1	1	0	0	0	BL3

- The Control Signal for the pass Transistors is generated by using k to 2^k predecoder.
- A 4:1 Column Decoder using nmos logic is as shown in the circuit.
- The speed of this approach is HIGH as Single pass Transistors in present in each path, which introduces minimal resistance in path.
- These use large number of Transistor i.e.,

Predecoder+ Final Decoder
= (k+1) x 2^k + 2^k

Column and Block Decoder

Column Decoder using NOR predecoder

Calculate the Number of Transistor required for Column decoder using pass transistor logic for k=2

Soln:

Number of Transistors required(T) = **Predecoder + Final Decoder**

= **(K+1) x 2^k + 2^k**

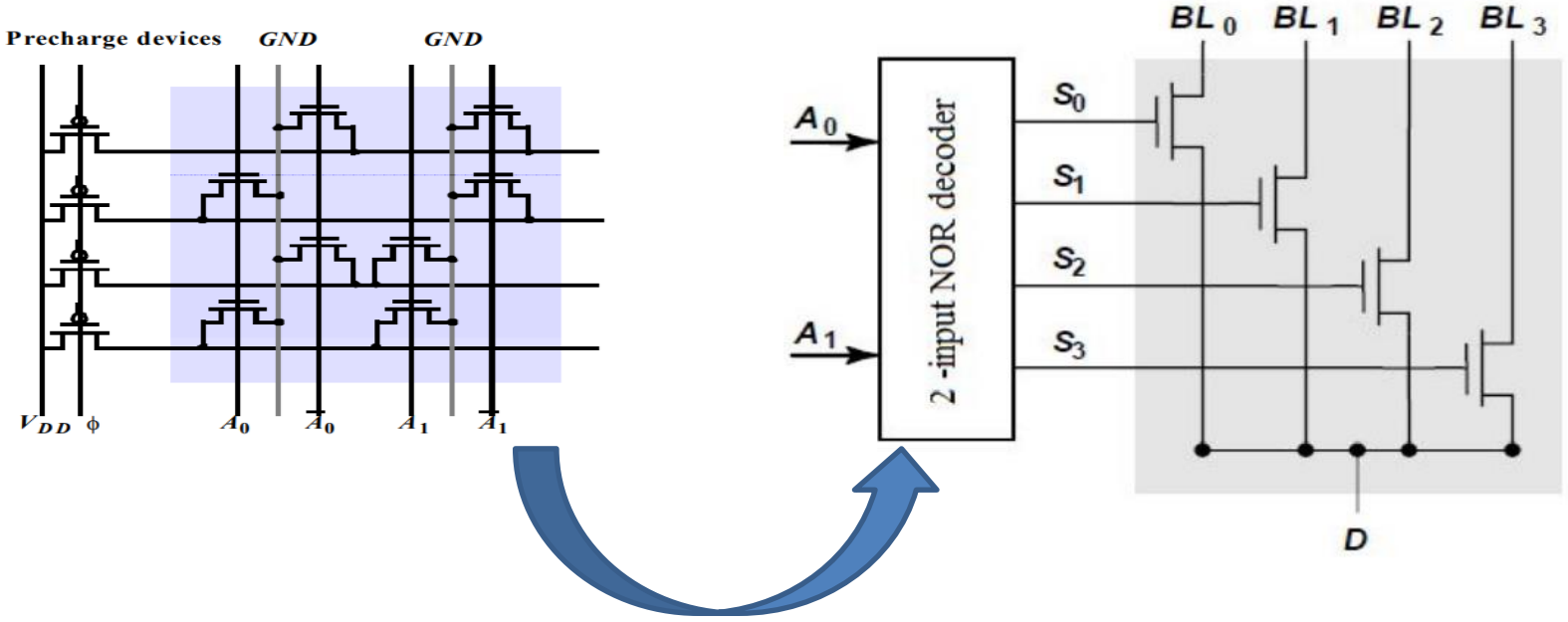
= **(2+1) x 2^2 + 2^2 =12 + 4 = 16**

If 1024:1 Column Decoder is required, then k=10

No of Transistors

= (10+1) x 2^{10} + 2^{10}

= **12,288**



Column and Block Decoder

Tree based Column Decoder

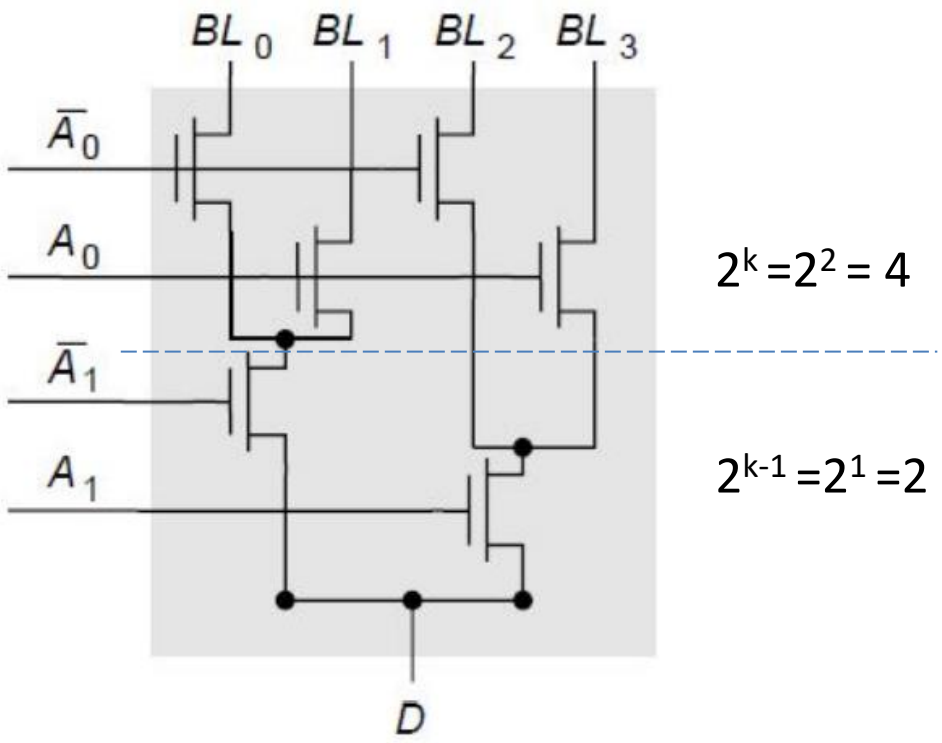
- It uses a binary reduction scheme.
- No need of predecoder
- No of Transistors required

  $2^k + 2^{k-1} + 2^{k-2} + \ldots\ldots\ldots 2^2 + 2^1 = 2x\,(2^k - 1)$

If 1024:1 (then k=10)Column Decoder is designed using Tree Decoder, then Number of Transistors required,

No of Transistors $= 2x\,(2^k - 1)$

$= 2x(2^{10}-1) =$ **2046**



$2^k = 2^2 = 4$

$2^{k-1} = 2^1 = 2$

Number of Transistors is reduced by a factor 6!

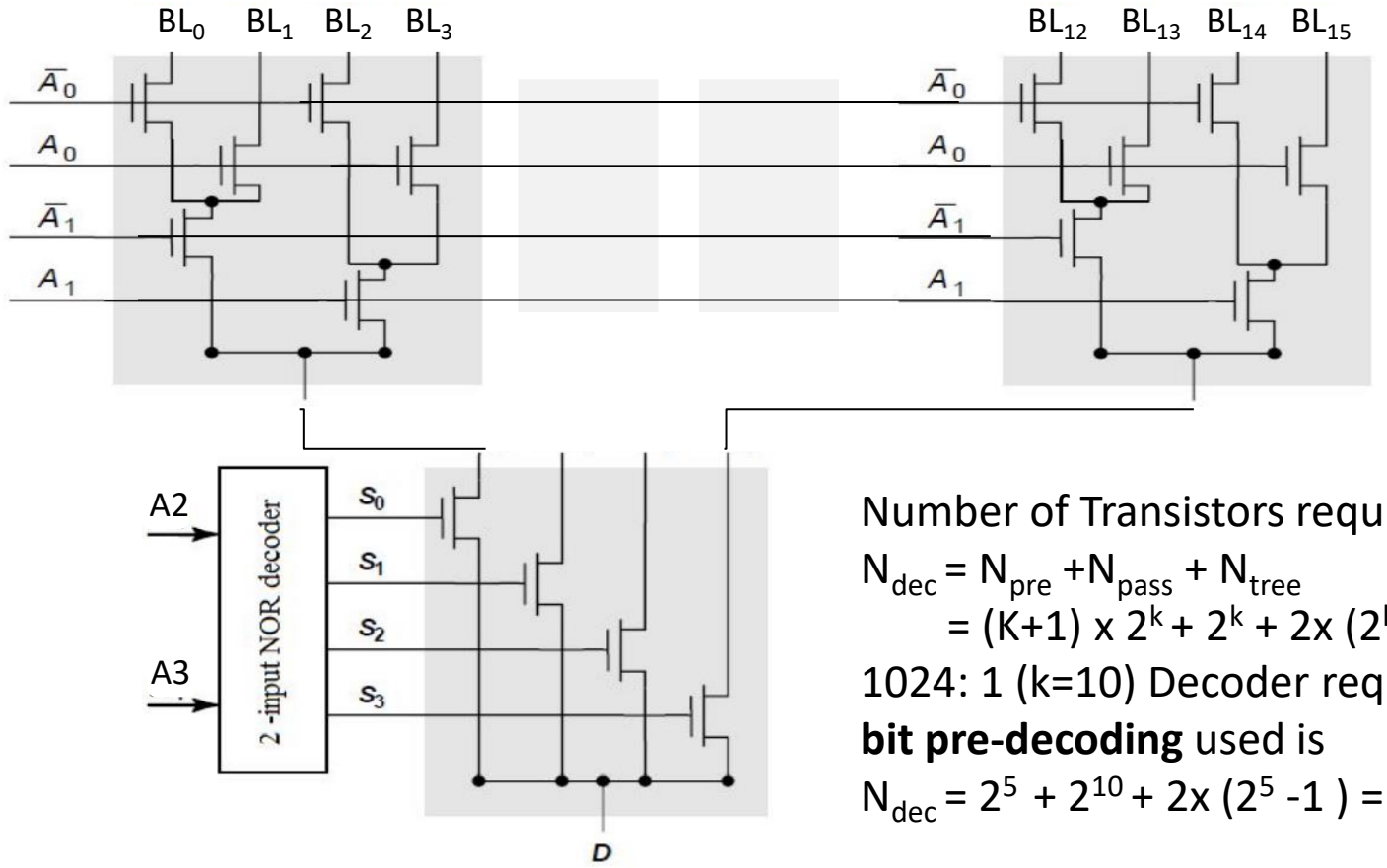
Drawback : A chain of k series connected pass Transistors is inserted in the signal path. It makes the tree approach slow which can be addressed by using buffers or progressive sizing.

Column and Block Decoder

Hybrid Column Decoders

In this, both predecoder and Tree decoder is combined to use the advantages of both approaches.

Let us see how a 4:16 Hybrid Decoder can be implemented,



Number of Transistors required

$N_{dec} = N_{pre} + N_{pass} + N_{tree}$

$= (K+1) \times 2^k + 2^k + 2x (2^k - 1)$

1024: 1 (k=10) Decoder requires if **5 bit pre-decoding** used is

$N_{dec} = 2^5 + 2^{10} + 2x (2^5 - 1) = 1278$?

Fraction of the address word is predecoded (MSB bits) and the remaining bits are tree decoded.

Ex: 4:16 , 2 bits are pre-decoded and 2 remaining bits are Tree decoded.

THANK YOU

Mahesh Awati/Dr Shashidhar
Department of Electronics and Communication

stantry@pes.edu

+91 9845695028