Memory Design and Testing

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MEMORY DESIGN AND TESTING

UNIT 3 – Non Volatile Memory and Memory Faults

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Outline

Non Volatile Memory

- ROM: Cell structure – NAND and NOR Arrays
- ROM:
  - Floating gate EPROM Cell,
  - EEPROM Cell- FLOTOX Technology,
  - EEPROM Architecture
- Flash Memory:
  - Cell operation,
  - NOR and NAND Flash
- New Memory Cells:
  - FeRAM,
  - STT RAM and
  - MRAM

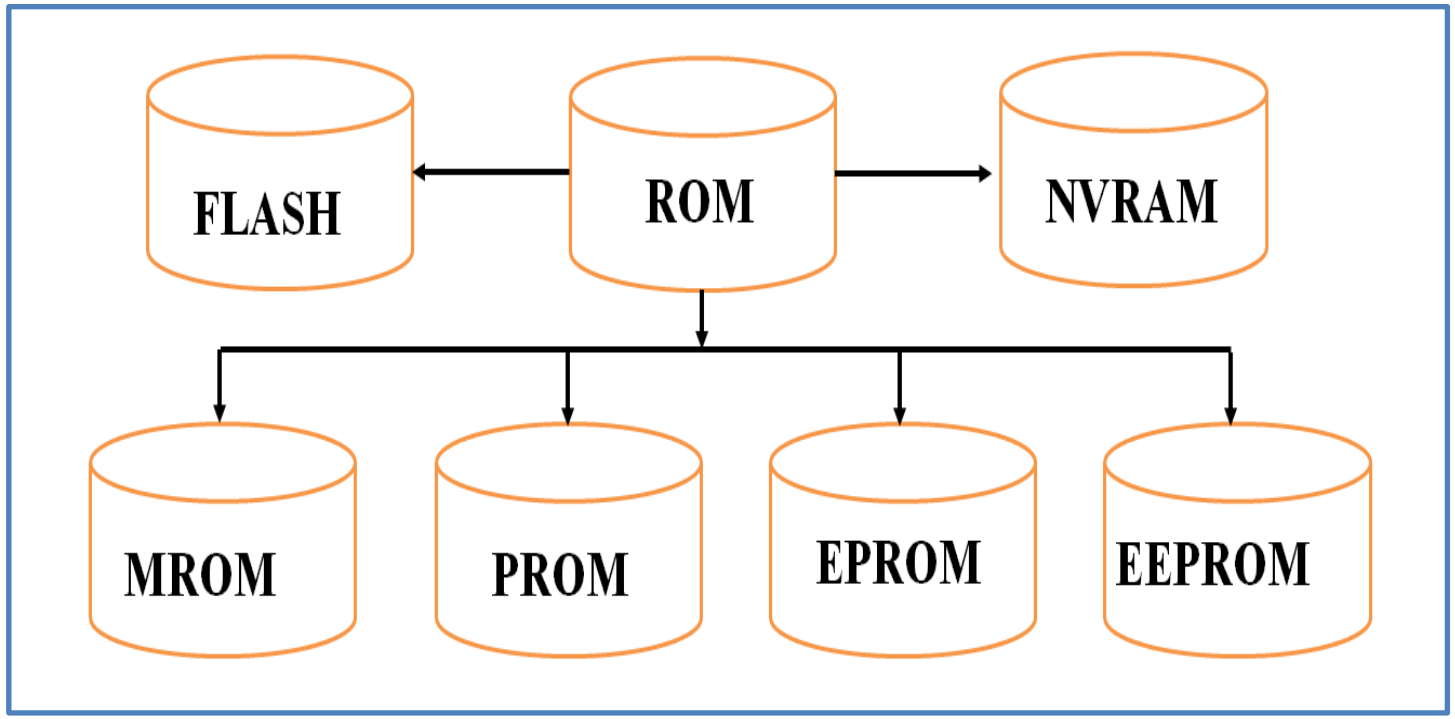
Non Volatile Memory
Introduction to ROM

- In number of large applications – The program for processor with fixed applications, once developed and debugged,
  - need only reading and
  - it should be retained even after power is removed from the chip - Non Volatile in nature

- As the contents of ROM Cell is permanently fixed simplifies the design.
  - The cell should be designed so that ‘0’ or ‘1’ is presented to the bit-line upon activation of it’s word-line.

Non Volatile Memory
Introduction to ROM

Different types of ROM



Non Volatile Memory
Introduction to ROM

Masked ROM (MROM)

- Masked ROM are hardwired devices that contain preprogrammed set of data/instruction.
- One Time Programmable device.
- Device is factory programmed by masking and metallization at the time of production itself according to data provided by end user.
- MROM need to be used
  - Once design is proven and the firmware requirements are tested and frozen, then the binary data corresponding to it can be given to MROM fabricators.

Advantages:

Low cost for High volume production. Per bit, mask ROM is more compact than any other kind of semiconductor memory. Size defends on firmware size.

Drawback:

Inability to modify the device –that is not possible to alter the bit information.

Non Volatile Memory
Introduction to ROM

One Time Programmable (OTP ROM)

- It is One Time Programmable device is not programmed by manufacturer. **End user is responsible for programming.**
- This memory has nichrome / polysilicon wires arranged in matrix.
- These **wires can be functionally viewed as fuse.** These **fuses are blown selectively according to bit patterns** by PROM programmer.
    - If fuse is not blown/burnt – logic 1 : It is default state and
    - if fuse is blown/burnt – logic 0

Use: Commercial Embedded system once prototype is finalized.

Drawback: Not reprogrammable. Therefore NOT useful and worth for development purpose as development phase involves continuous changes in firmware before finalizing. Use of **OTP at development stage is not economical.**

Non Volatile Memory
Introduction to ROM

EPROM

- These are re-programmable devices. These **use gate of MOS** devices to store the data.
- The crystal quartz window exposed to UV rays for fixed interval of time erases the stored information.
- **Drawback:** Every time memory unit need to removed from circuit board and put in UV erased for fixed time(20 to 30 min). It is tedious and time consuming.

Electrically EPROM (EEPROM)

- Information stored in EEPROM can be erased by using electrical signals at the register / byte level
- **Advantage:** Erased and reprogrammed in the circuit itself.
- **Drawback :** Capacity is limited (kilo bytes)

Non Volatile Memory
Introduction to ROM

FLASH

- These are **High capacity re-programmable devices arranged in matrix** form as pages.
- Stores information in array of floating gate of MOS.
- Erasing of memory can be done at page level without affecting other pages.
- Each page need to be erased before re-programming.
- Erasable capacity is 1000 cycles

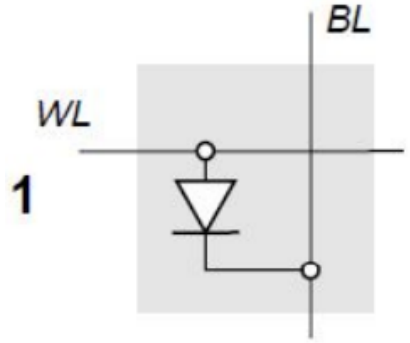
NVRAM

- Non Volatile RAM with battery back up.
- It uses static RAM cells with battery packed in single package.

Non Volatile Memory
Introduction to ROM

Diode based ROM

Data stored is '0'



Data stored is '1'

Data stored '0':

- No physical connection exists between wordline (WL) and bitline (BL), It means that the value on BL is low (0), independent of WL.

Data stored '1':

- For Data '1', when WL goes High (V_{WL}), the diode is enabled and the value on BL equals $V_{WL} - V_{D(on)}$.
- Thus the presence or absence of a diode between WL and BL differentiates between ROM cells storing a '1' or '0'

Disadvantage:

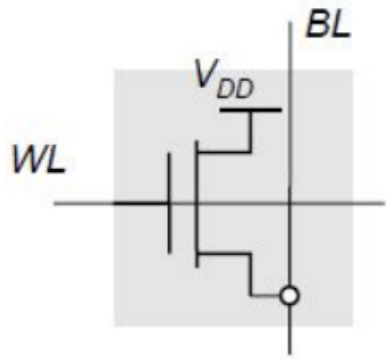
It **does not isolate the WL from the BL**. The current required to charge the BL capacitance, which can be quite large for large memories has to be provided through the WL and its drivers. Hence only used for small memories

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
Introduction to ROM

MOS based ROM 1

Data stored is '0'



Data stored is '1'

Data stored '0':

- No physical connection exists between wordline (WL) and bitline (BL), It means that the value on BL is low (0), independent of WL.

Data stored '1':

- For Data '1', when WL goes High (V_{DD}), the Nmos turns ON and BL becomes HIGH (V_{DD}–V_{tn}).
- The **output driving current is provided by the MOS rather than the WL** i.e., The WL driver is only responsible for charging and discharging the WL capacitance.

Disadvantage:

The improved Isolation comes at the penalty of more complex cell and large area.

The Large area is

i) primarily because of the **extra supply contact** for each cell.

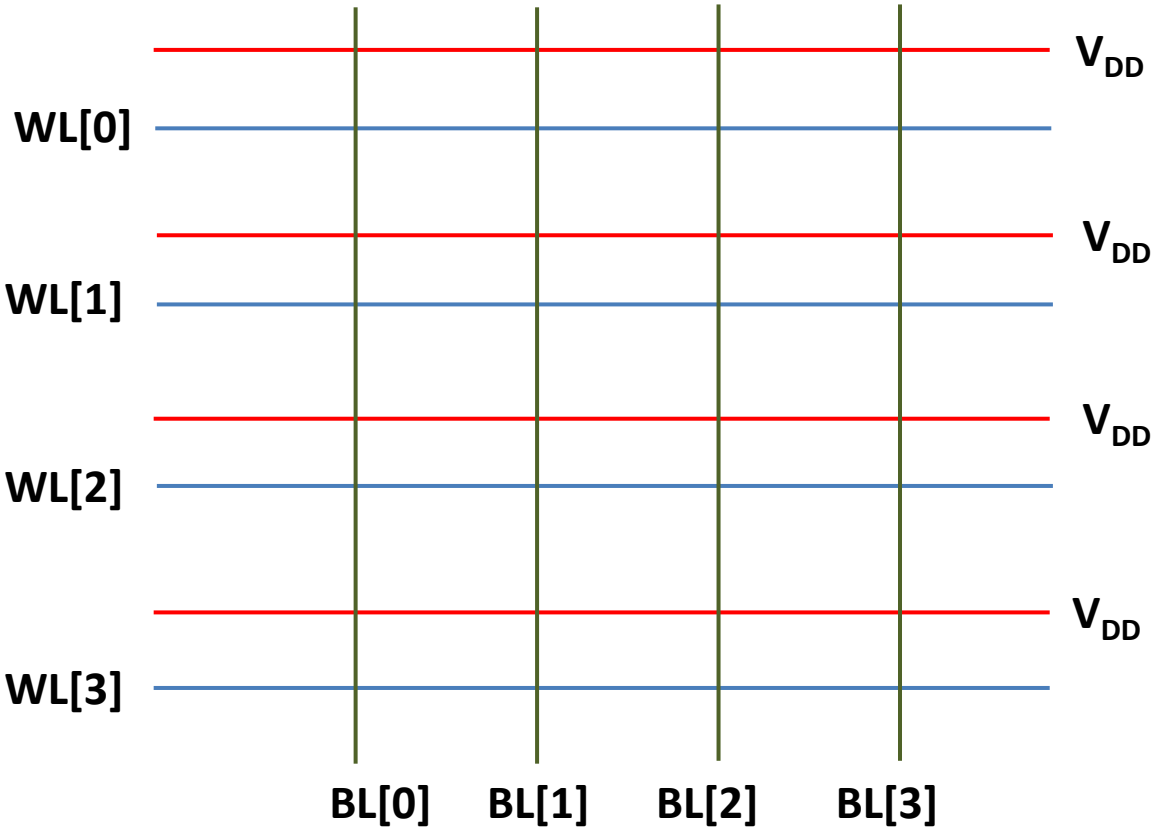
ii) **The V_{DD} rail for each row**

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM

4x4 OR ROM Array using MOS based Cell

- Presence of MOS is data ‘1’ and absence is Data ‘0’.

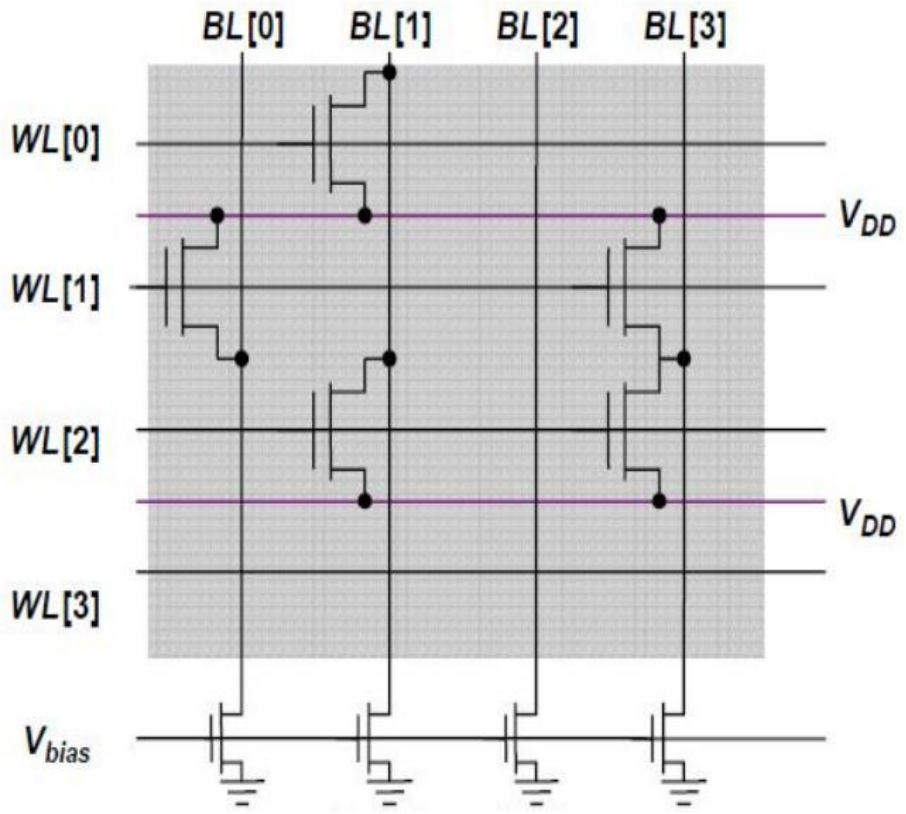


BL[0]	BL[1]	BL[2]	BL[3]
0	1	0	0
1	0	0	1
0	1	0	1
0	0	0	0

If all WLs are 0, then BL =0. **If one of the WLs containing a transistor = 1, BL = 1**. Hence this is referred to as OR ROM cell array

Non Volatile Memory
MASKED ROM

4x4 OR ROM Array using MOS based Cell



- Presence of MOS is data '1' and absence is Data '0'.

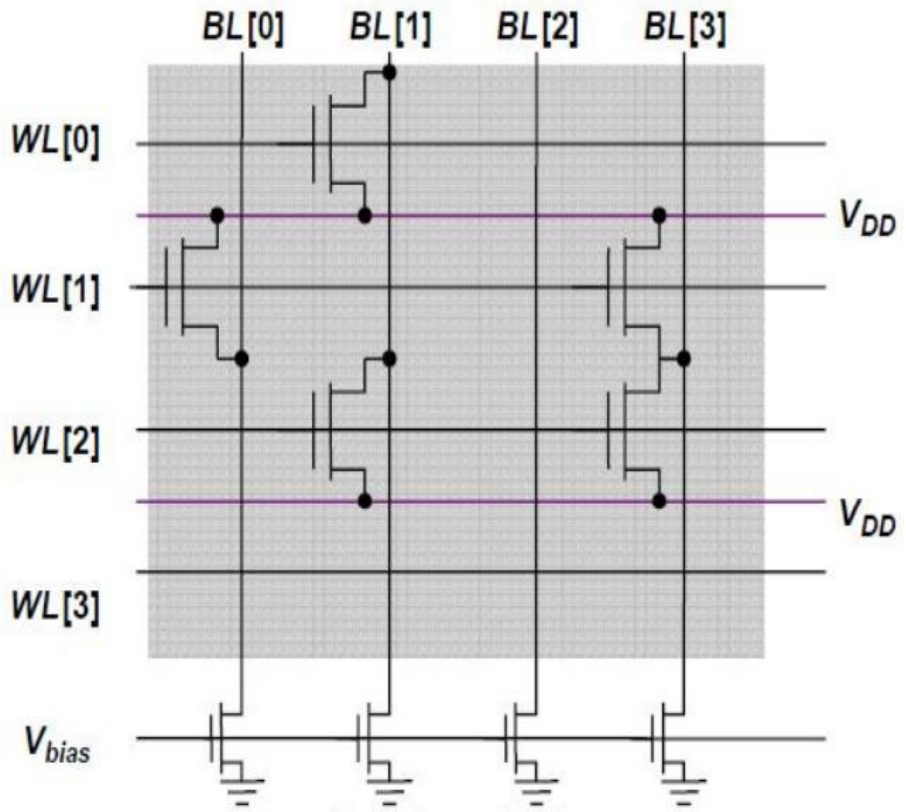
WL[0]	WL[1]	WL[2]	WL[3]	BL[0]	BL[1]	BL[2]	BL[3]
0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	1	0	1
1	0	0	0	0	0	0	0

The overhead of the supply lines is reduced **by sharing them between neighboring cells.**

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM

4x4 OR ROM Array using MOS based Cell



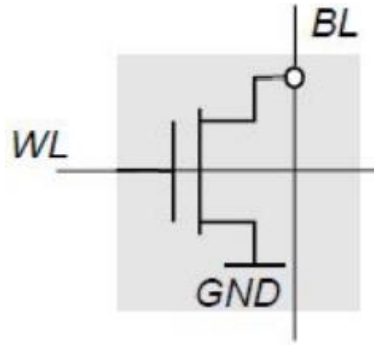
- A BL goes high if any one of the WLs containing a transistor goes high.
- If all WLs are low, BL = low. Hence this is referred to as OR ROM cell array.
- For proper operation, the **memory transistor** must be **stronger** than the **pull-down transistor**. When a WL goes high, the single transistor must be capable of pulling the BL high.
- **Disadvantage:**
  i. Larger area due to the **extra supply contact** provided in each cell.

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM

MOS based ROM 2

Data stored is '1'



Data stored is '0'

Data stored '1':

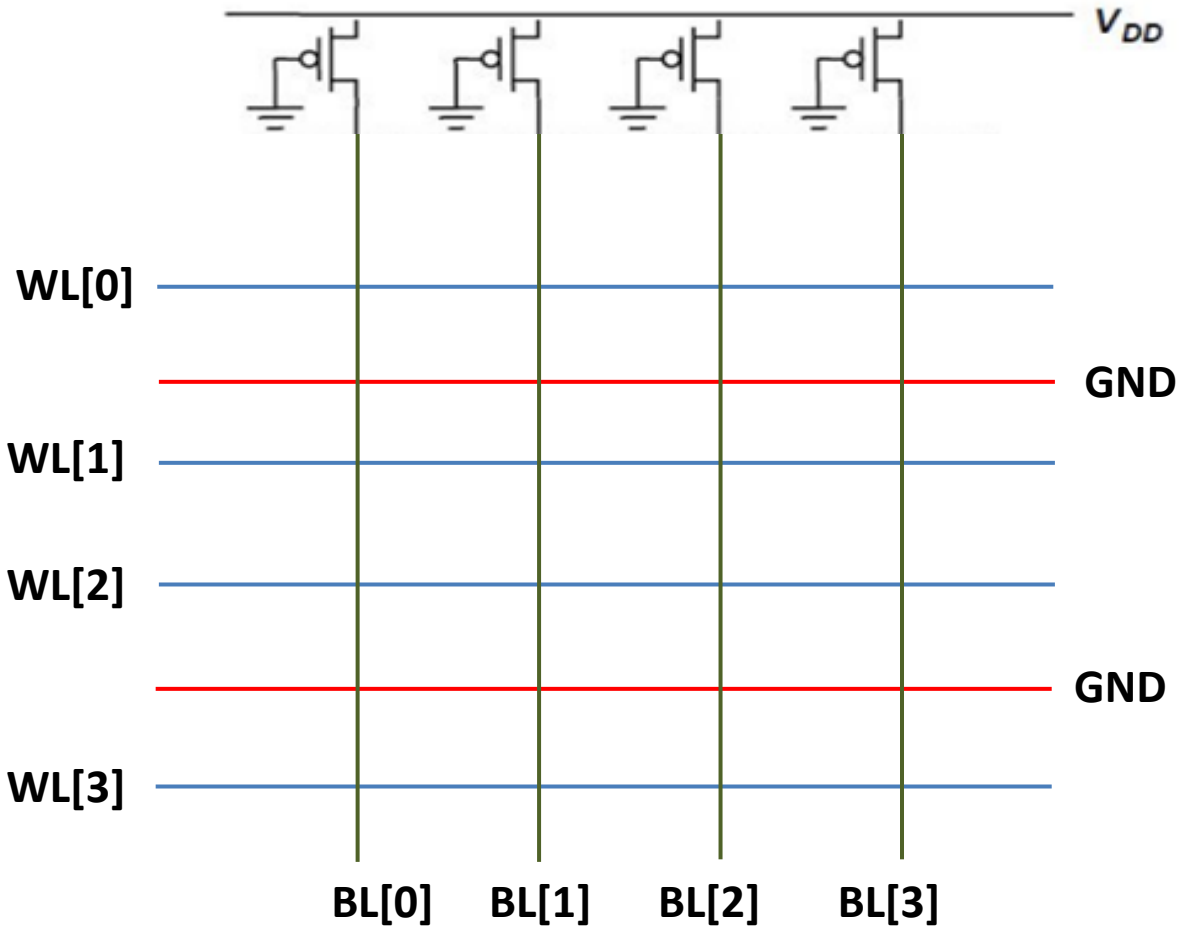
- No physical connection exists between wordline (WL) and bitline (BL), It means that the value on BL is HIGH (1), independent of WL.
- Absence of a transistor implies data stored is '1'.

Data stored '0':

- For Data '0', when WL goes High (V_{DD}), the NMOS turns ON and BL becomes LOW.
- Presence of a transistor between WL and BL causes BL to be pulled to ground when WL goes high, implying stored data of '0'

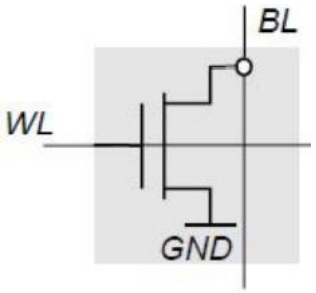
Non Volatile Memory
MASKED ROM

4x4 NOR ROM Array using MOS based Cell



- **Presence of MOS is data '0'** and absence is Data '1'.

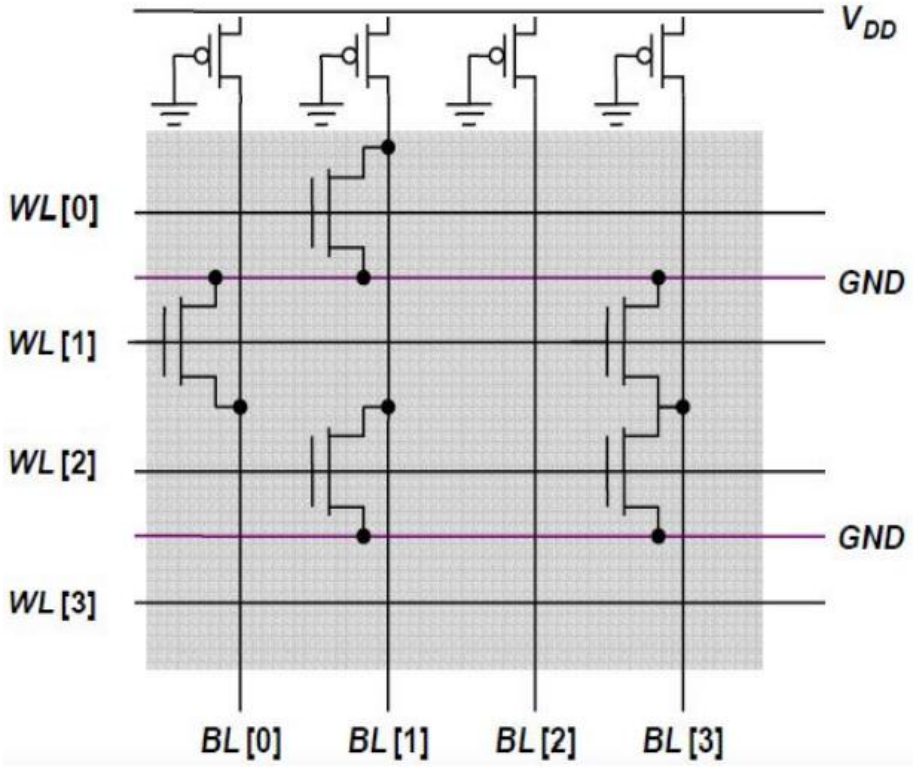
BL[0]	BL[1]	BL[2]	BL[3]
1	0	1	1
0	1	1	0
1	0	1	0
1	1	1	1



- If all WLs are 0, then BL =1. **If one of the WLs containing a transistor = 1, BL = 0**. Hence this is referred to as NOR ROM cell array

Non Volatile Memory
MASKED ROM

4x4 NOR ROM Array using MOS based Cell



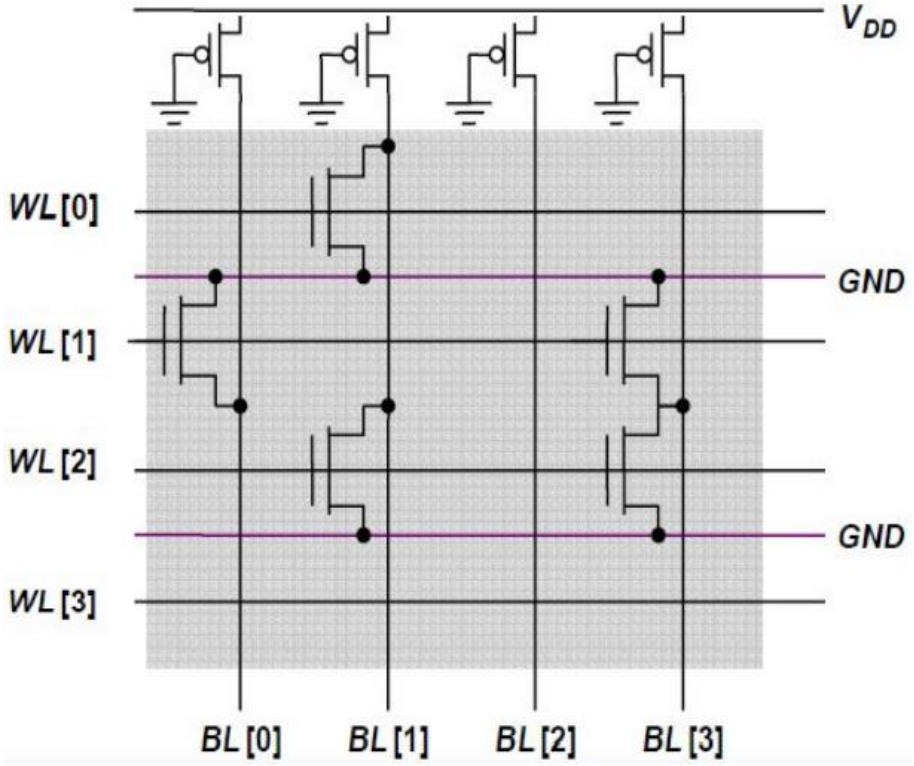
- Presence of MOS is data '0' and absence is Data '1'.

WL[0]	WL[1]	WL[2]	WL[3]	BL[0]	BL[1]	BL[2]	BL[3]
0	0	0	1	1	0	1	1
0	0	1	0	0	1	1	0
0	1	0	0	1	0	1	0
1	0	0	0	1	1	1	1

- If all WLs are 0, then BL =1. **If one of the WLs containing a transistor = 1, BL = 0**. Hence this is referred to as NOR ROM cell array

Non Volatile Memory
MASKED ROM

4x4 NOR ROM Array using MOS based Cell



- The NOR ROM array is a **Pseudo – NMOS NOR gate.**
- Under normal operating conditions, only one of the WL goes high and at most, one of the pull-down devices is turned ON. **Hence the NMOS is stronger than the PMOS pull-up, ie., its W/L is large.**

Disadvantages:

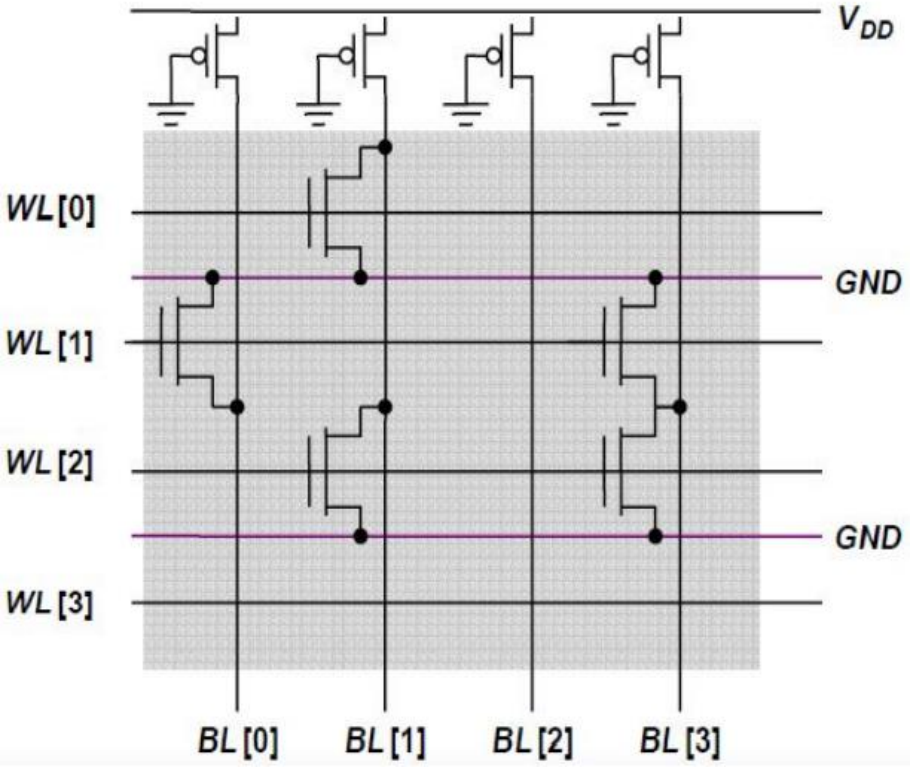
i. NMOS W/L is large will increases the cell size as well as the bit-line capacitance.

ii. Also, since the **pull-up device is sized smaller, its resistance is larger.** This increases the **RC time constant** for low – to – high transition on the BL

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM

4x4 NOR ROM Array using MOS based Cell



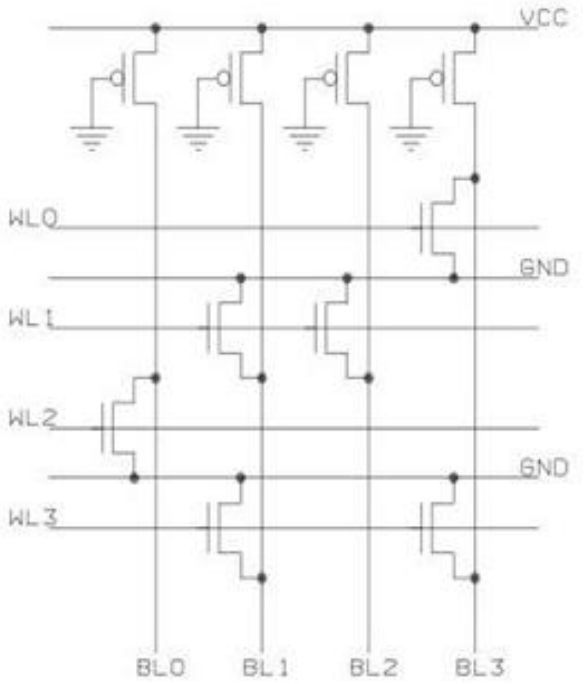
How to reduce RC time constant ?

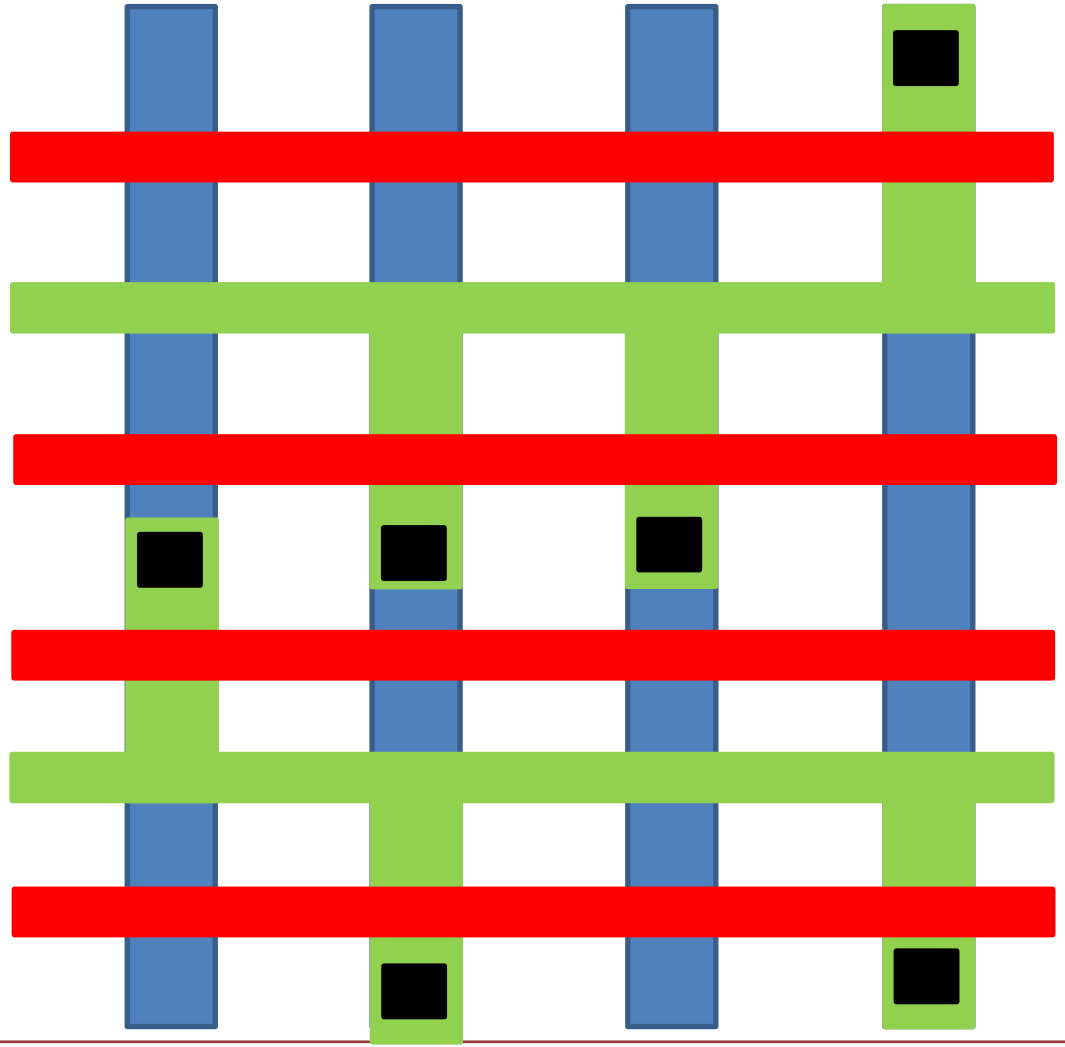
- The low – to – high transition can be improved by **widening the pull-up device** and hence **reducing its resistance**.
- This makes the **pull-up device stronger**, thereby making it difficult for the NMOS transistor to pull BL to ground. **Hence V_{OL} is high, ie., 1 - 1.5V for VDD = 2.5V.**
- Full swing can be restored by using a sense amplifier.
- At the same time, the **noise margin is reduced which is tolerable** within the memory core where the noise conditions and signal interference can be carefully controlled.

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM - LAYOUT

Active Layer





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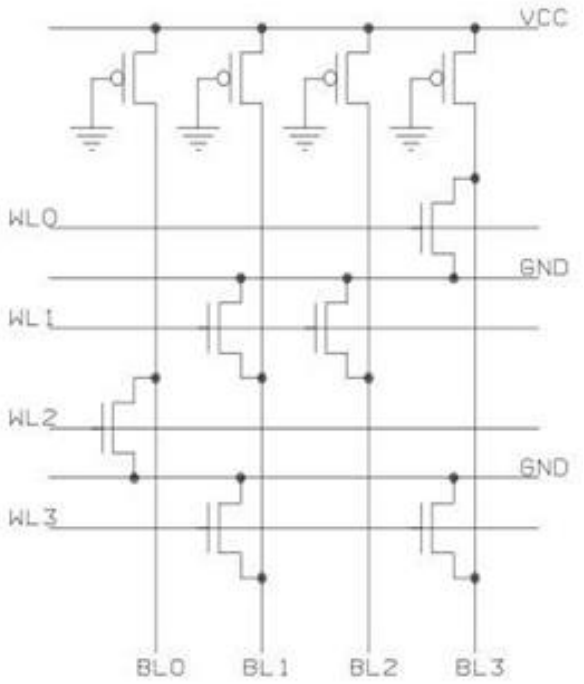
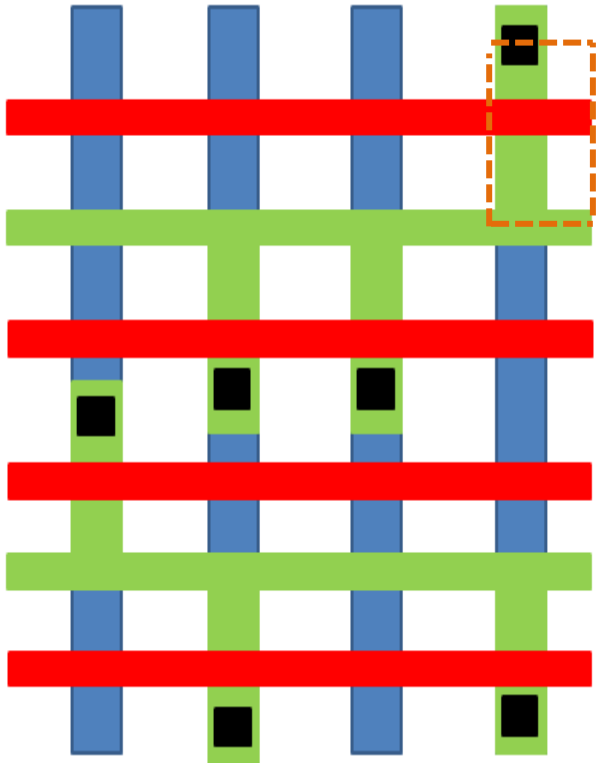
Non Volatile Memory
MASKED ROM - LAYOUT

4x4 NOR ROM Array using MOS based Cell



Active Layer



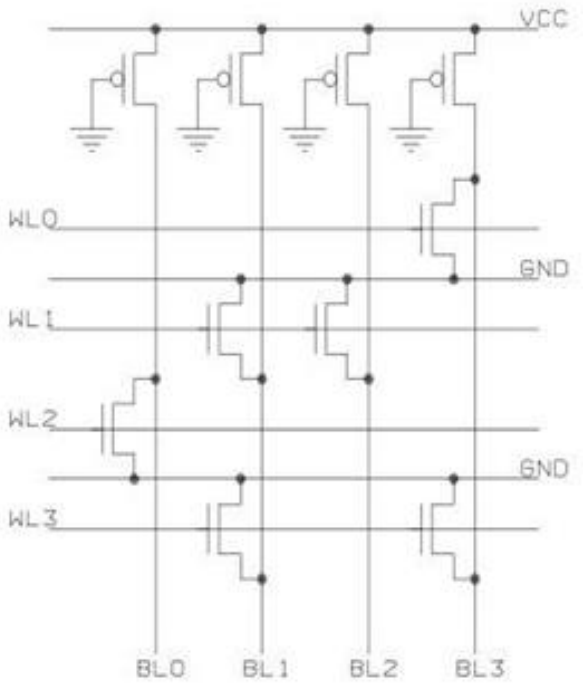
- Arrays are constructed by repeating the same cell in both horizontal and vertical direction, Mirroring of odd cells around horizontal axis in order to share the ground wire.
- In the layout shown, **The memory is written by selectively adding transistors when needed.**
- This is accomplished **with the aid of only diffusion layer.**

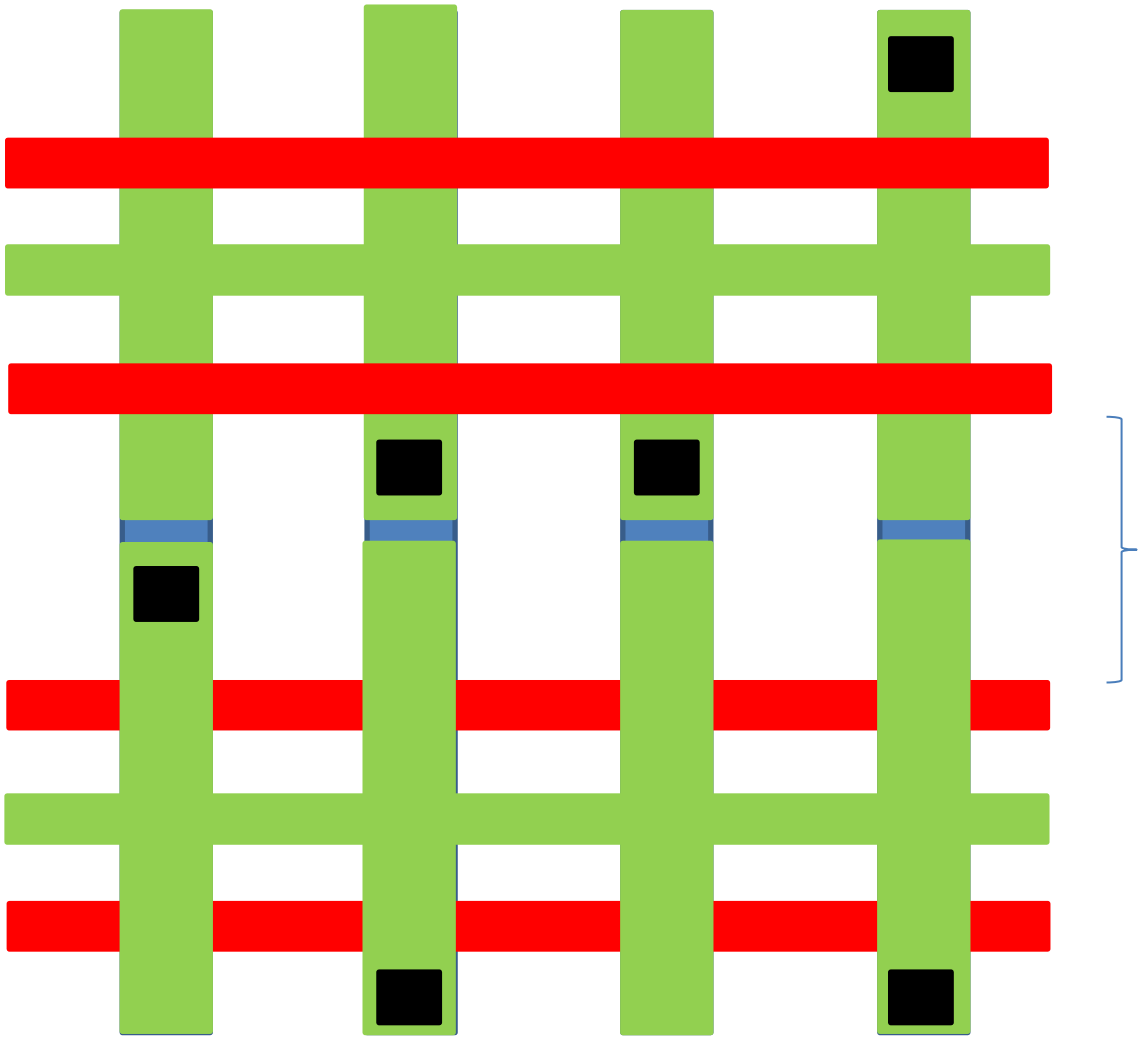
Basic Cell: (9.5X7)λ for 0.25um technology

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM - LAYOUT

Contact Layer

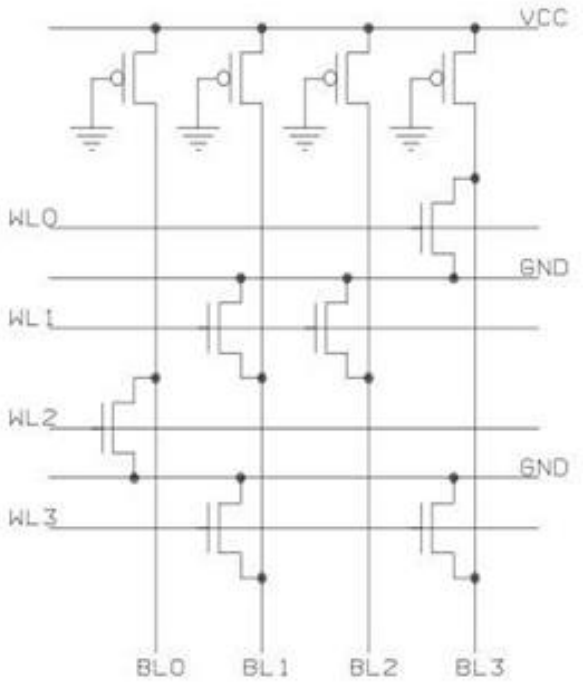




Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

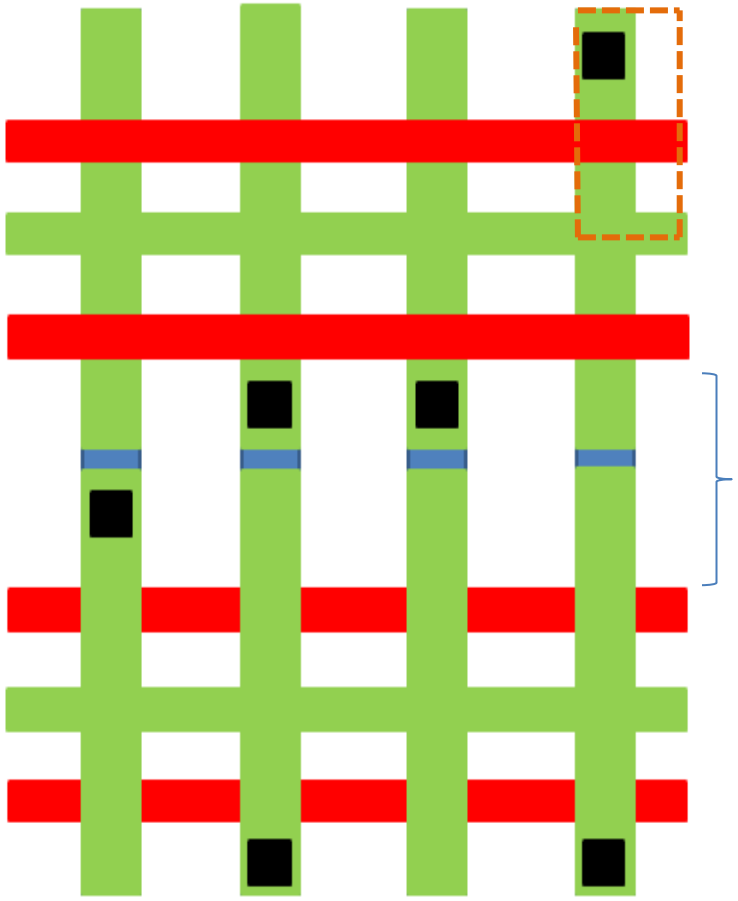
Non Volatile Memory
MASKED ROM - LAYOUT

4x4 NOR ROM Array using MOS based Cell



Basic Cell: (11X7)λ for 0.25um tehnologu

Contact Layer



- In this approach Memory is programmed by selective addition of Metal to diffusion contact.
- The presence of a Contact to bit line creates a '0' cell and absence creates '1' cell
- **Advantage:** Only one mask layer, the contact is used to program the memory

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM - LAYOUT

Comparison of the Active and Contact Implementation

Active Implementation:

- It uses 15% lesser area compared with the Contact Implementation i.e., Active Implementation uses lesser area each cell in comparison with cell of Contact Implementation.
- Ex:9.5x7 lambda and 11x7 lambda

Contact Implementation:

- In this, the **Contact Layer is a later step** in the manufacturing process. Therefore wafers can be prefabricated up to CONTACT mask and stockpiled.
- Therefore **remaining fabrication step can be executed quickly** once a specific program is defined. This reduces the turn around time between order and delivery.

In both, diffusion is used for GND line, which is generally not preferred in layout design because of the voltage drop across diffusion. The metal bypass with regularly spaced straps keeps the voltage drop within strict bound

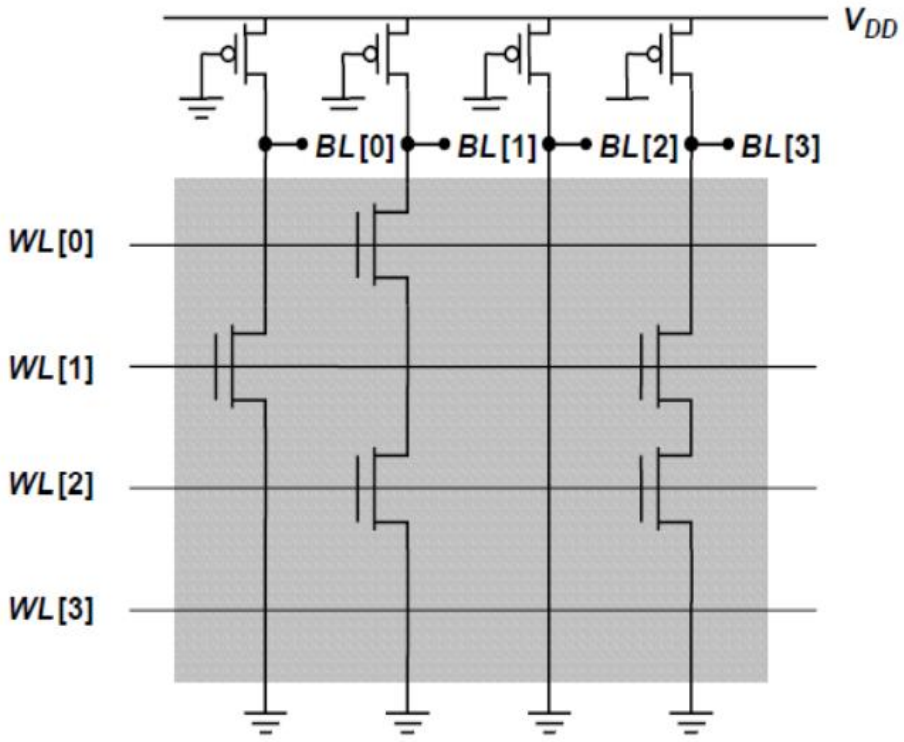
In multilayer process, programming is increasingly done in one of the Via masks. Any of these implementations can be used and the choice depends on size/performance versus turn around tie.

Drawback of NOR based ROM Layout
Large part of cell is devoted to the bit lines contact and ground connection.

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM

4x4 NAND ROM Array using MOS based Cell



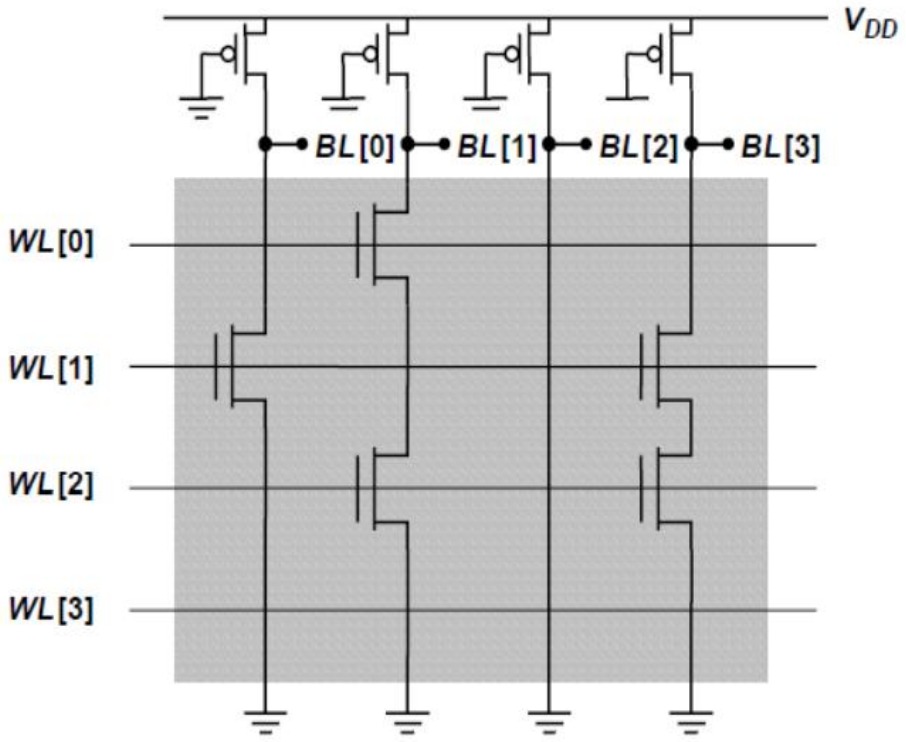
- **WLs are operated in reverse logic** mode to make the memory function. By default all WLs are **high i.e., nmos in the row are ON and** All BLs are grounded.
- When a WL is made low, the NMOS transistor is turned OFF and the BL is pulled high
- Presence of MOS is data '1' and absence is Data '0'.

WL[0]	WL[1]	WL[2]	WL[3]	BL[0]	BL[1]	BL[2]	BL[3]
0	1	1	1	0	1	0	0
1	0	1	1	1	0	0	1
1	1	0	1	0	1	0	1
1	1	1	0	0	0	0	0

- All transistors in the pull-down chain must be ON to produce a low

Non Volatile Memory
MASKED ROM

Comparison of NAND ROM with NOR ROM



Advantage over NOR ROM:

- Basic cell consists of only the transistor and no connection to any supply voltage. This reduces the cell size substantially.
- In NOR ROM, large area is devoted to GND lines and bit line contacts which can be avoided in a NAND ROM.

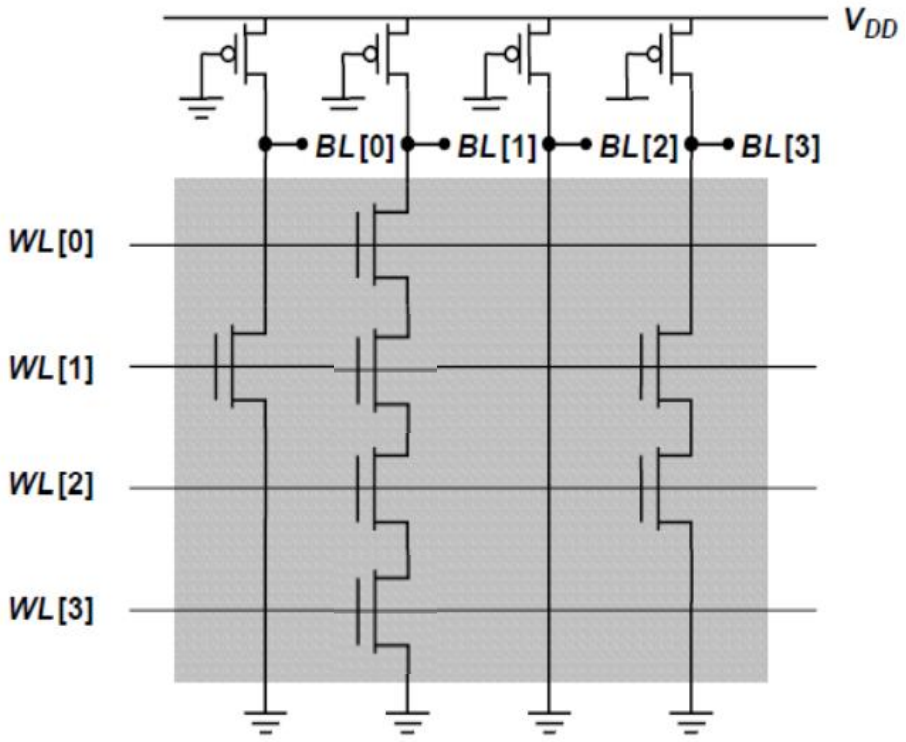
Disadvantage:

- The value of V_{OL} is a function of both the size of the memory as well as the programming.
- **A series of NMOS transistors** are involved in pulling down the bit line whereas a single PMOS transistor is involved in pulling it up

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM

Comparison of NAND ROM with NOR ROM



Disadvantage:

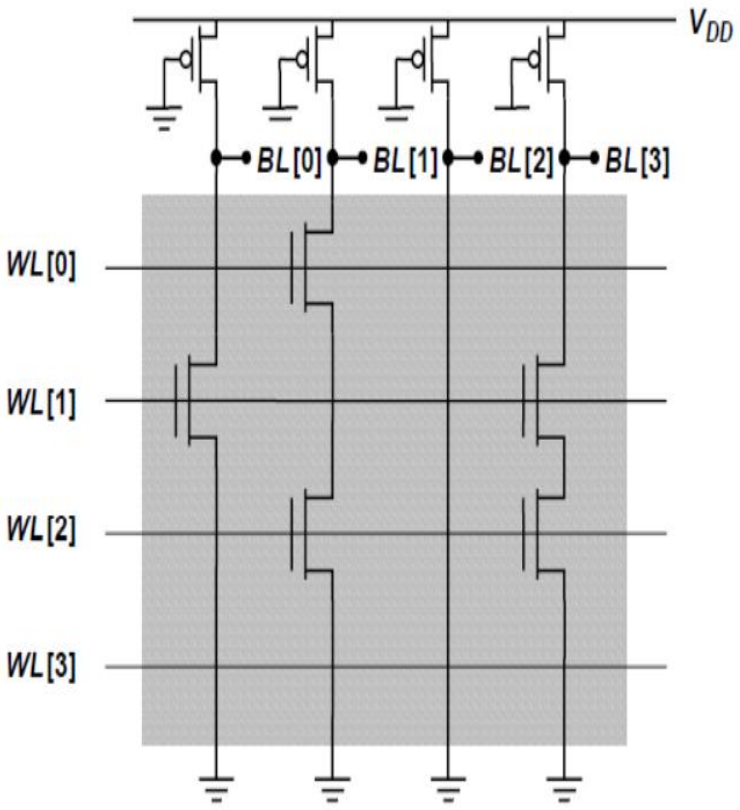
- Worst case scenario occurs when all bits in a column are set to 1 which means for a N x M memory, N transistors are connected in series.
- Assume N transistors in series can be replaced by a single transistor with length N times longer.
- Then (W/L)p can be determined as follows:

  For an 8 x 8 array, if the aspect ratio of a single NMOS transistor is 3/2, then the aspect ratio of the equivalent single NMOS transistor = 3/16 = 0.1875.

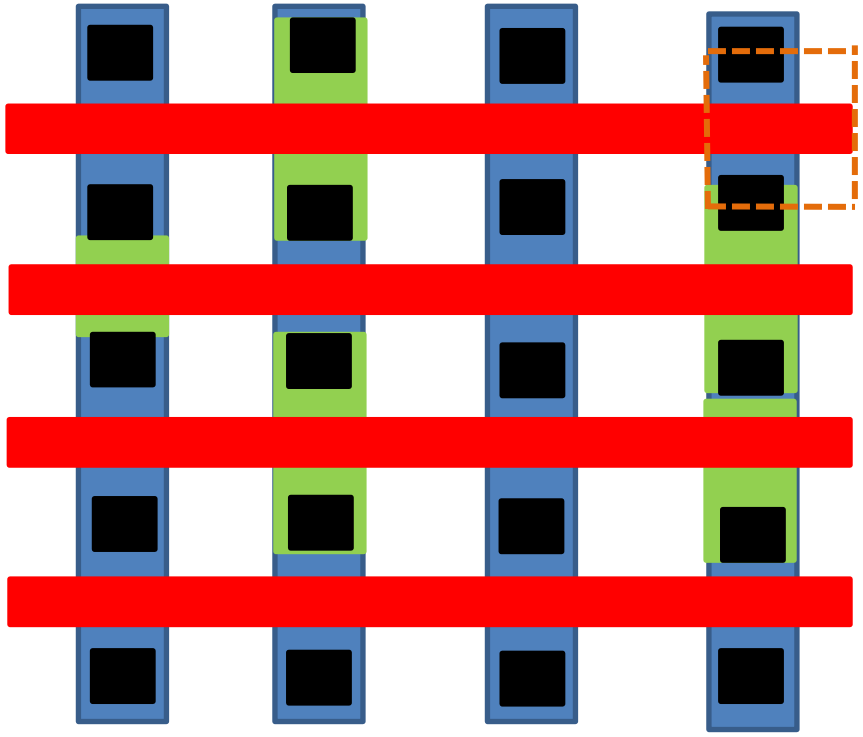
  (W/L)p = 2.5 (W/L)n = 0.47
- For 512 x 512 array, (W/L)p = 0.007

Non Volatile Memory
MASKED ROM LAYOUT

Contact Layer



Basic Cell: (8X7)λ for .25um technology



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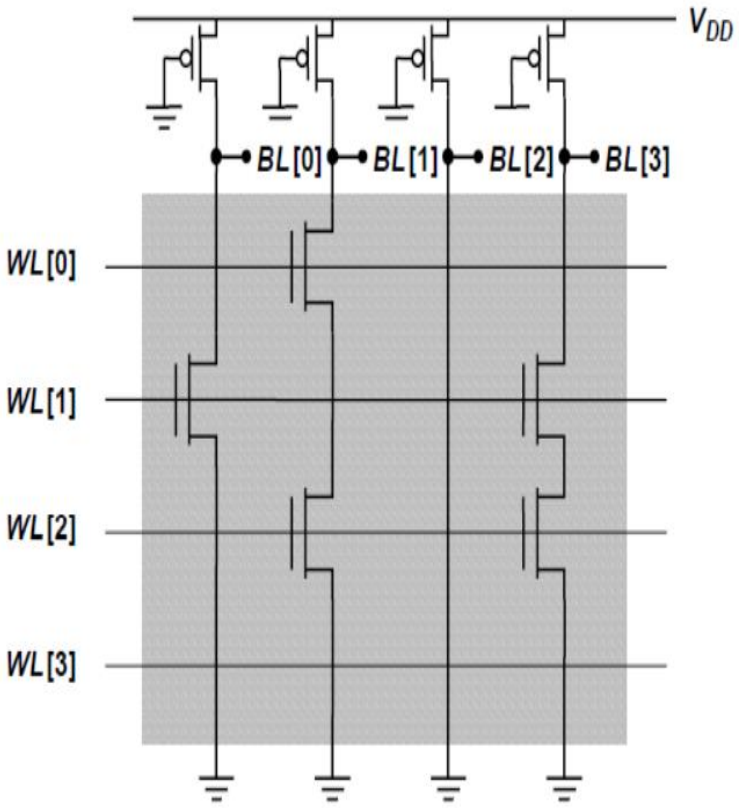
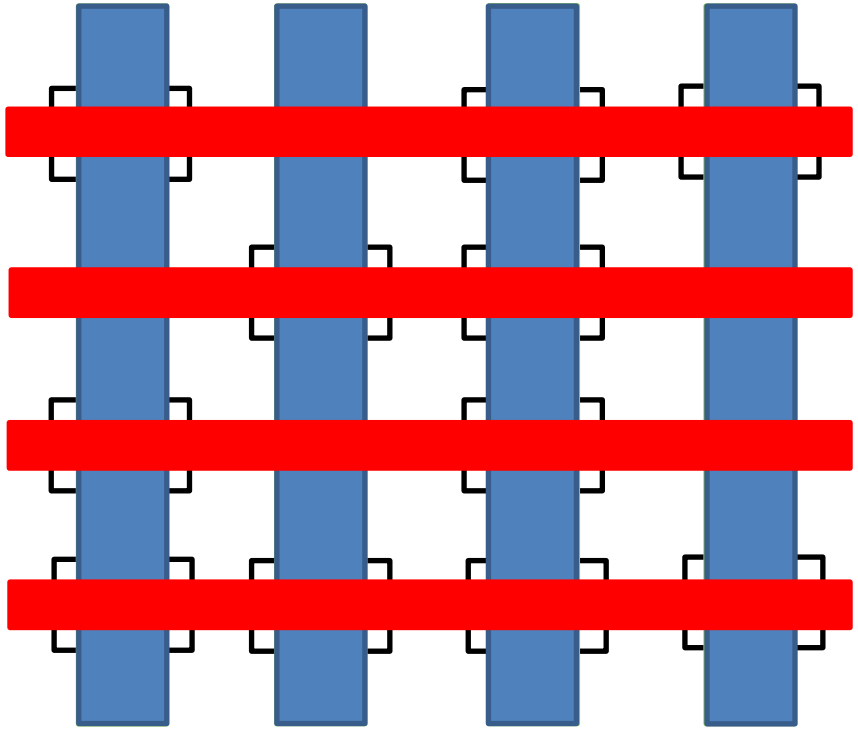
Non Volatile Memory
MASKED ROM LAYOUT

Contact Layer



Basic Cell: (5X7)λ for .25um technology



Threshold Altering Implant

- Implant in gate region means Depletion type NMOS. Channel exist without WL being made HIGH.
- Implant Not existing means it is on when WL=1 and OFF when WL=0

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
MASKED ROM LAYOUT

Area Comparision

NOR-Active Layer	NOR-Contact	NAND-Metal1	NAND-Threshold
(9.5X7)λ	(11X7)λ	(8X7)λ	(5X7)λ

MASKED ROM

Comparison of NAND ROM with NOR ROM

Disadvantage:

- Thus the pull-up transistor should be very long or if Ln = Lp = 2, then Wp = 0.94 as against Wn = 3 for 8 x 8 array and Wp = 0.14 for 512 x 512 array.
- In other words, NMOS transistors are made stronger than the single PMOS transistor. On the other hand, in a NOR ROM, since at most 1 transistor can be ON at a time along a bit line, the value of VOL is neither a function of the array size nor of the programming.
- For this reason, NAND ROMS are rarely used for arrays with more than 8 or 16 rows

Non Volatile Memory
MASKED ROM

Comparison of NAND ROM with NOR ROM

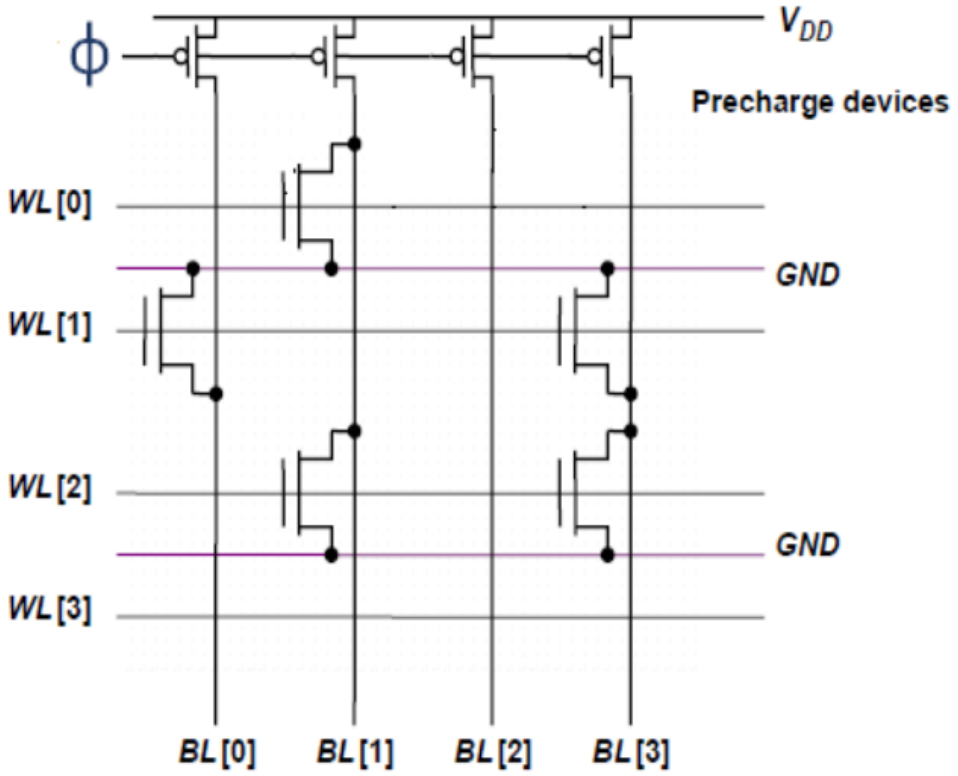
Common disadvantages:

1. Ratioed logic: VOL is determined by the ratio of pull-up and pull-down devices which can result in unacceptable transistor ratios.
2. 2. Static power consumption: A static current path exists between the supply rails when the output is low. This results in severe power dissipation problems.

To overcome these 2 issues, pre-charged logic can be used which eliminates both the issues while keeping the same cell complexity

Non Volatile Memory
MASKED ROM

Pre-charged 4 x 4 NOR ROM array



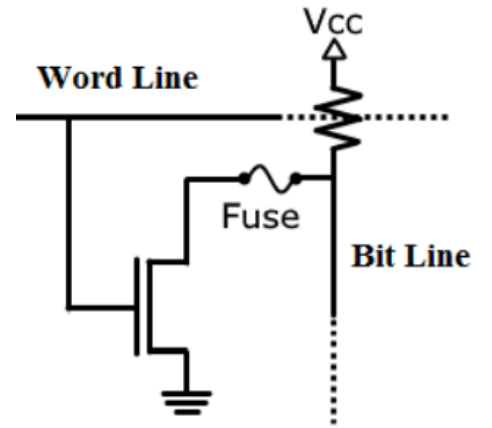
- The dynamic architecture enables independent control of pull-up and pull-down timings.
- The PMOS transistor can be made as large as necessary to reduce its resistance and hence reduce the low – to – high transition delay.
- Virtually, all large memories currently designed, use dynamic pre-charging

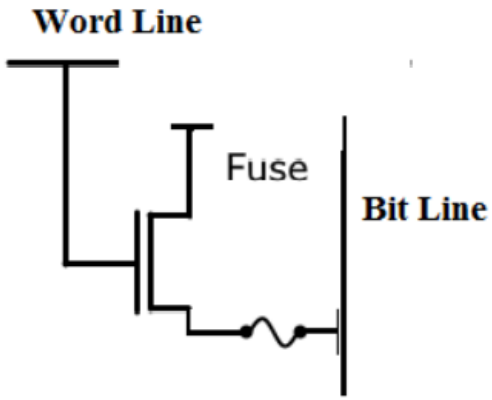
Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
PROGRAMMABLE ROM

PROM

PROM structure allows the customer to program the memory one time.





- These are called a "WRITE ONCE" device as they can be programmed only once.
- Accomplished by **introducing fuses, implemented in polysilicon** or nichrome or other conductors, in the memory cell.
- During the programming phase, **some of these fuses are blown by applying a high current.**

Advantage: Customer programmable.
Disadvantage: A single error in programming process or application makes the device unusable

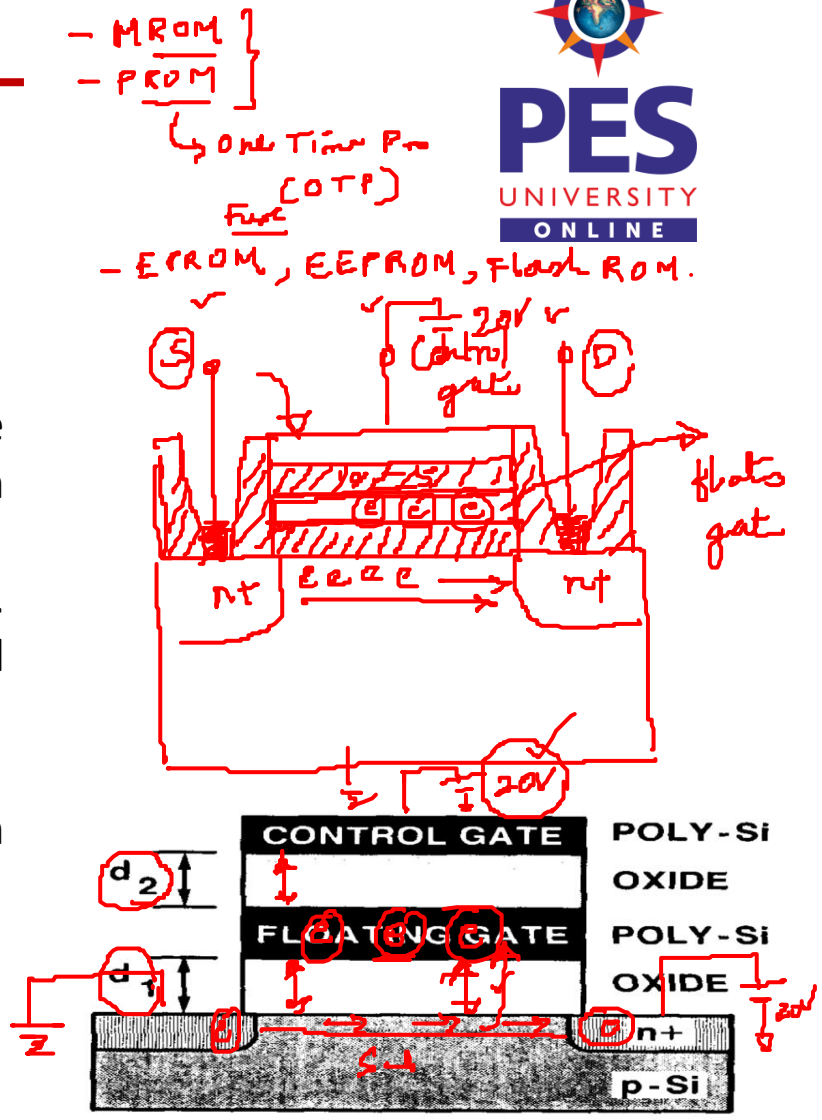
Non Volatile Memory
EPROM

Erasable Programmable ROM (EPROM)

EPROM uses Floating Gate Avalanche Injection MOS (FAMOS)

Basic Features:

- It has two gate
  - **Control gate : One on the TOP** – Which is accessible electrically where gate voltage can be applied i.e., Similar to conventional gate terminals in MOS devices.
  - **Floating gate** – Extra polysilicon inserted between gate and the channel. This does not have any electrical connection i.e., Can not be accessed electrically.
    - The Insertion of floating gate doubles the thickness of oxide (2tox).
    - The doubling of thickness of oxides , decreases Cox and ,this intern Increase threshold voltage as Vtn is inversely proportion to Cox.

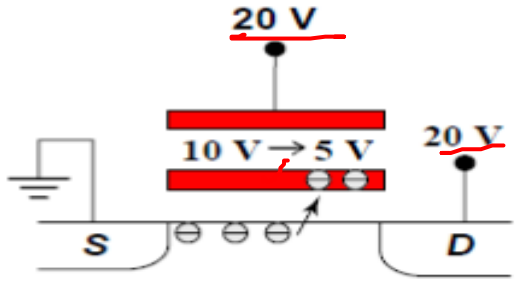


Non Volatile Memory
EPROM

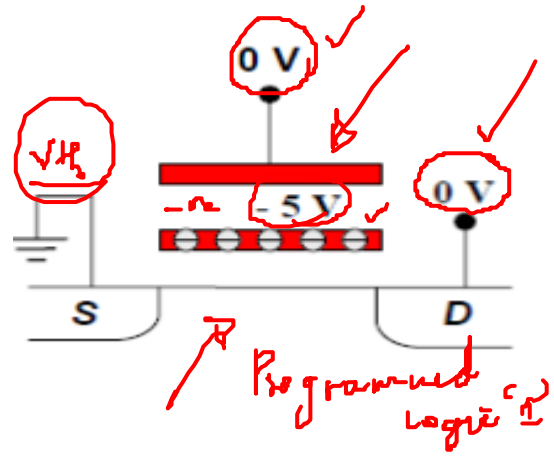
Erasable Programmable ROM (EPROM)

Working: **Programming the device implies writing a '1' into the cell**

- Let Control gate and Drain are raised to a high voltage > 12V i.e., VGS=20V and VDS=20.
- Large drain current flows through the device in its normal conduction mode.
- High-field in the drain – substrate depletion region causes avalanche breakdown of the **drain – substrate junction resulting in additional flow of current**
- High field accelerates the electrons to a high velocity. Hence termed as **"hot – electrons"**. These "Hot-electrons" gain sufficient energy, The energy acquired will be such that they break the down the SiO2 barrier between Floating gate and Substrate
- Small fraction of the electrons travelling from Source to drain will jump into the floating gate region as the and get implanted into Floating gate and get trapped once VGS and VDS is made as zero.



Hot-carrier injection

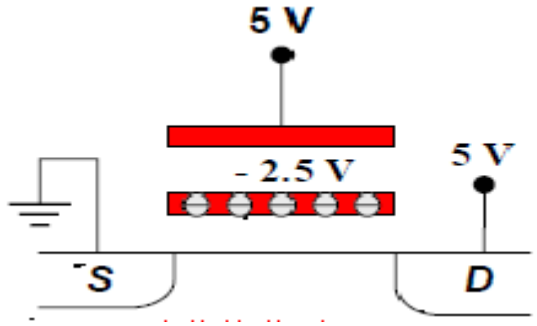


Non Volatile Memory
EPROM

Erasable Programmable ROM (EPROM)

Working: **Programming the device implies writing a '1' into the cell**

- This intern results –ve voltage on floating gate, this interns tries to pull the holes in the channel region rather than electrons which means threshold voltage is increased.
- Therefore, If the channel with –ve charges has to be formed then large gate potential has to applied so that it overcomes the –ve potential at floating gate and then tries to attract the electrons to form channel.
- It means transistor does not turn ON by applying Normal voltage at the Gate terminal



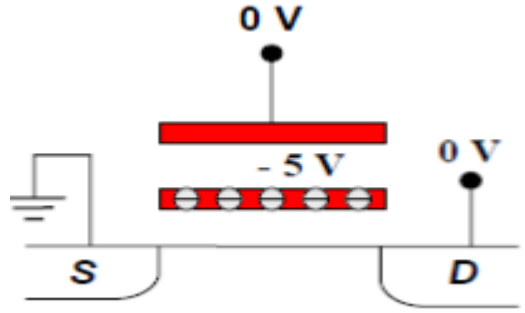
Reading Stored Data: During a Read operation, when a signal of 5V is applied to the control gate, no channel is formed. The transistor remains OFF and the bit line remains pre-charged reading a logic '1'.

Non Volatile Memory
EPROM

Erasable Programmable ROM (EPROM)

Non – volatile

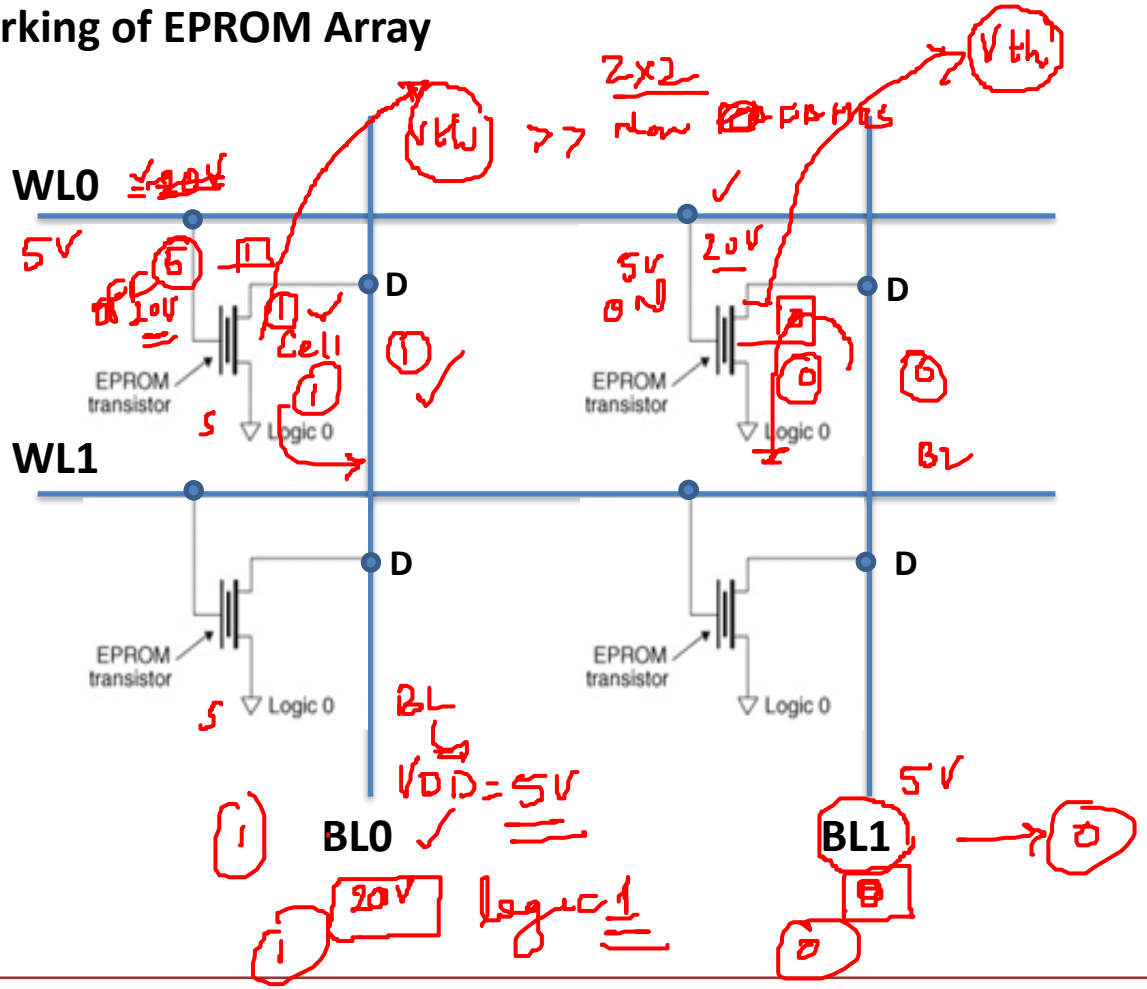
Since the floating gate is surrounded by SiO2, which is an excellent insulator, the trapped charge can be stored for many years, even when the supply voltage is removed, creating a non – volatile storing mechanism

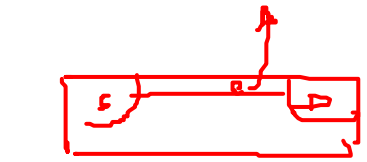


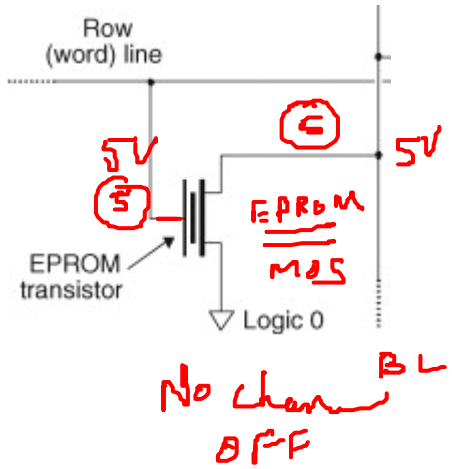
Non Volatile Memory
EPROM

Erasable Programmable ROM (EPROM)

Working of EPROM Array





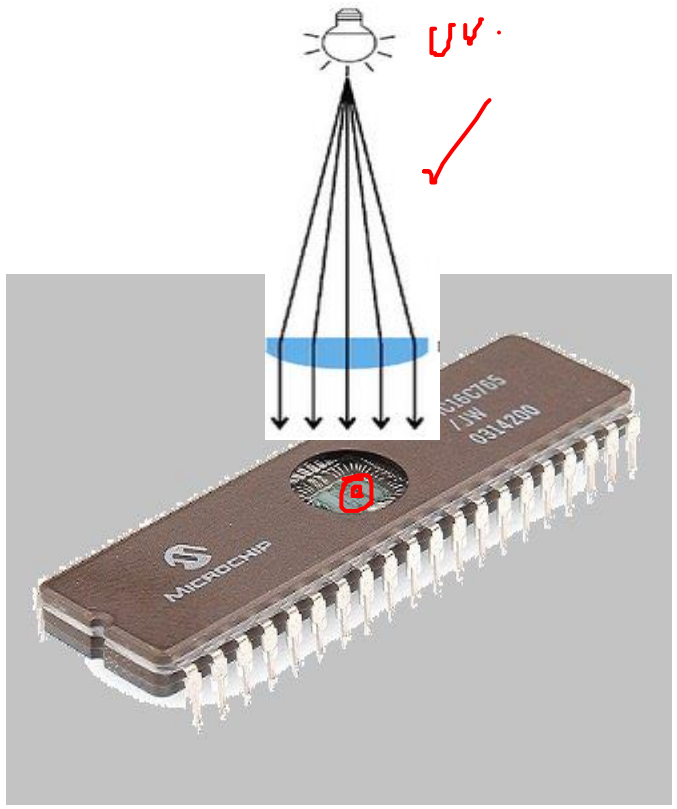


Reading Stored Data: During a Read operation, when a signal of 5V is applied to the control gate, no channel is formed. The transistor remains OFF and the bit line remains pre-charged reading a logic '1'.

Non Volatile Memory
EPROM

Erasable Programmable ROM (EPROM)

Working: Erasing the EPROM



By applying UV rays, **the Implanted electrons will attain High energy and get exited and they will overcome SiO2 barrier and move back into substrate or Control gate region**. This means reduced threshold voltage which means information is erased and ready for programming.

Part of CHIP can not be erased , the entire Memory CHIP has to be erased and reprogram whole memory

PROM - OTP

Non Volatile Memory
EPROM

Erasable Programmable ROM (EPROM)

Disadvantages

- Erasure procedure has to occur **"off-system".** The memory has to be removed from the board and placed in a EPROM programmer.
- **Entire chip** has to be erased and programmed.
- Erasure **procedure is slow** and can take several minutes depending on the intensity of UV light.
- Limited endurance: **Number of Erase/Program cycles is limited to 1000.**
- **Reliability is less since the device threshold varies** with repeated programming.
- **Packaging required a transparent window** for UV light to pass through.
- **Programming causes a large current flow,** as high as 0.5mA, which results in **high power dissipation.**

Advantages:

- Extremely simple cell and dense making it possible to fabricate large memories at a low cost.
- Can be used in applications that do not require regular programming.

Due to programming cost and reliability issues, EPROMs have been replaced by Flash memories.

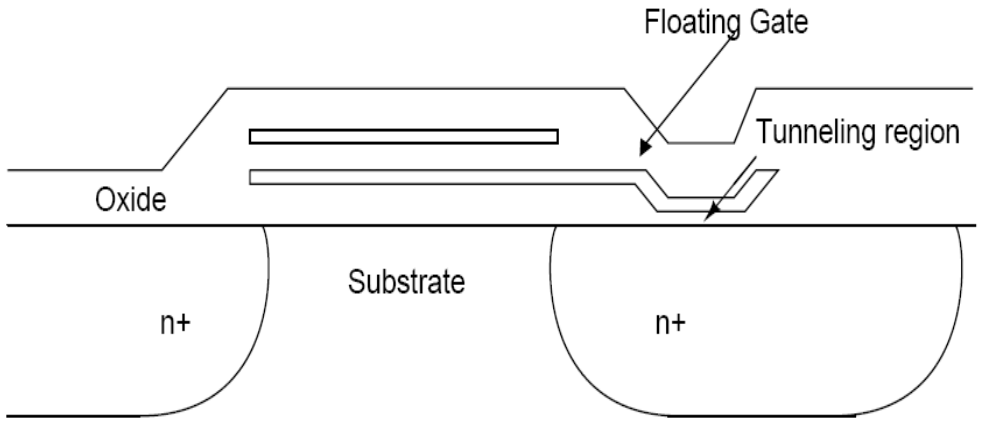
Non Volatile Memory
EEPROM

Electrically Erasable Programmable ROM (EEPROM)

Floating Gate Tunneling Oxide MOS (FLOTOX)

It uses another mechanism to inject or remove charges from the floating gate and the mechanism is called tunneling.

A portion of electric separation of the floating gate from the channel and the drain is reduced in thickness to 10nm or less which is comparatively lesser than thickness of 100nm in all other region.



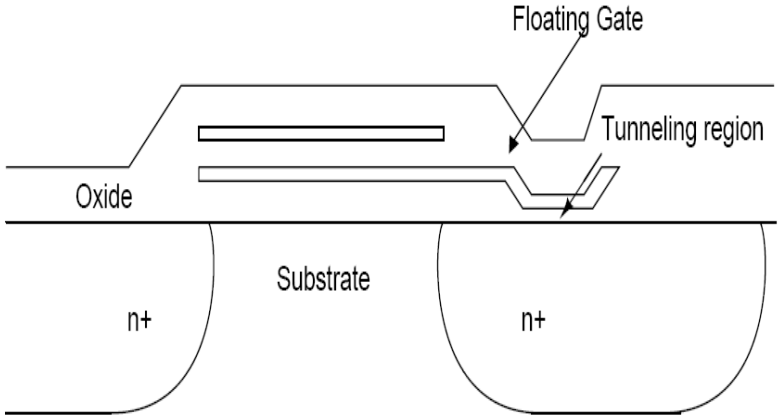
Non Volatile Memory
EEPROM

Electrically Erasable Programmable ROM (EEPROM)

Floating Gate Tunneling Oxide MOS (FLOTOX)

Operation:

- Gate is given a high positive voltage while the source and drain are grounded.
- A **fraction of the applied voltage is developed on the floating gate through capacitive coupling**
- **The electrons in the conduction band of the n+ drain, tunnel through the oxide to reach the floating gate. i.e., No need of channel or current flow, because think oxide layer the electrons in the conduction band of n+ will tunnel into floating gate**
- **The charge build-up on the floating gate reduces the electric field on the gate which decreases the electron flow.** Thus the charge build-up on the floating gate is self limiting
- The negative floating gate increases the threshold voltage of the device, **thus making the device harder to turn ON**.



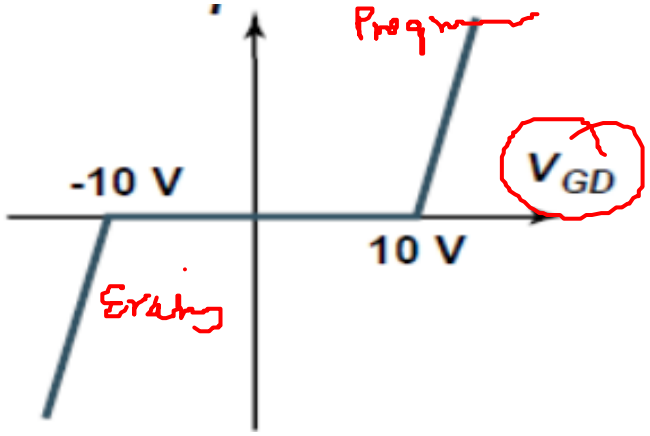
Non Volatile Memory
EEPROM

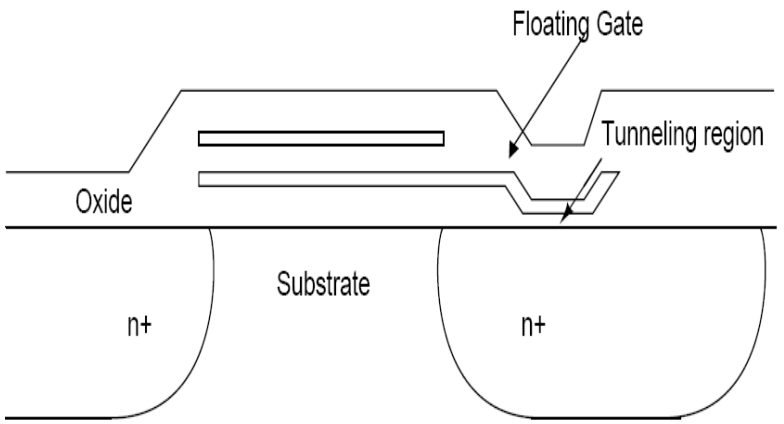
Electrically Erasable Programmable ROM (EEPROM)

Floating Gate Tunneling Oxide MOS (FLOTOX)

Operation: Erasing

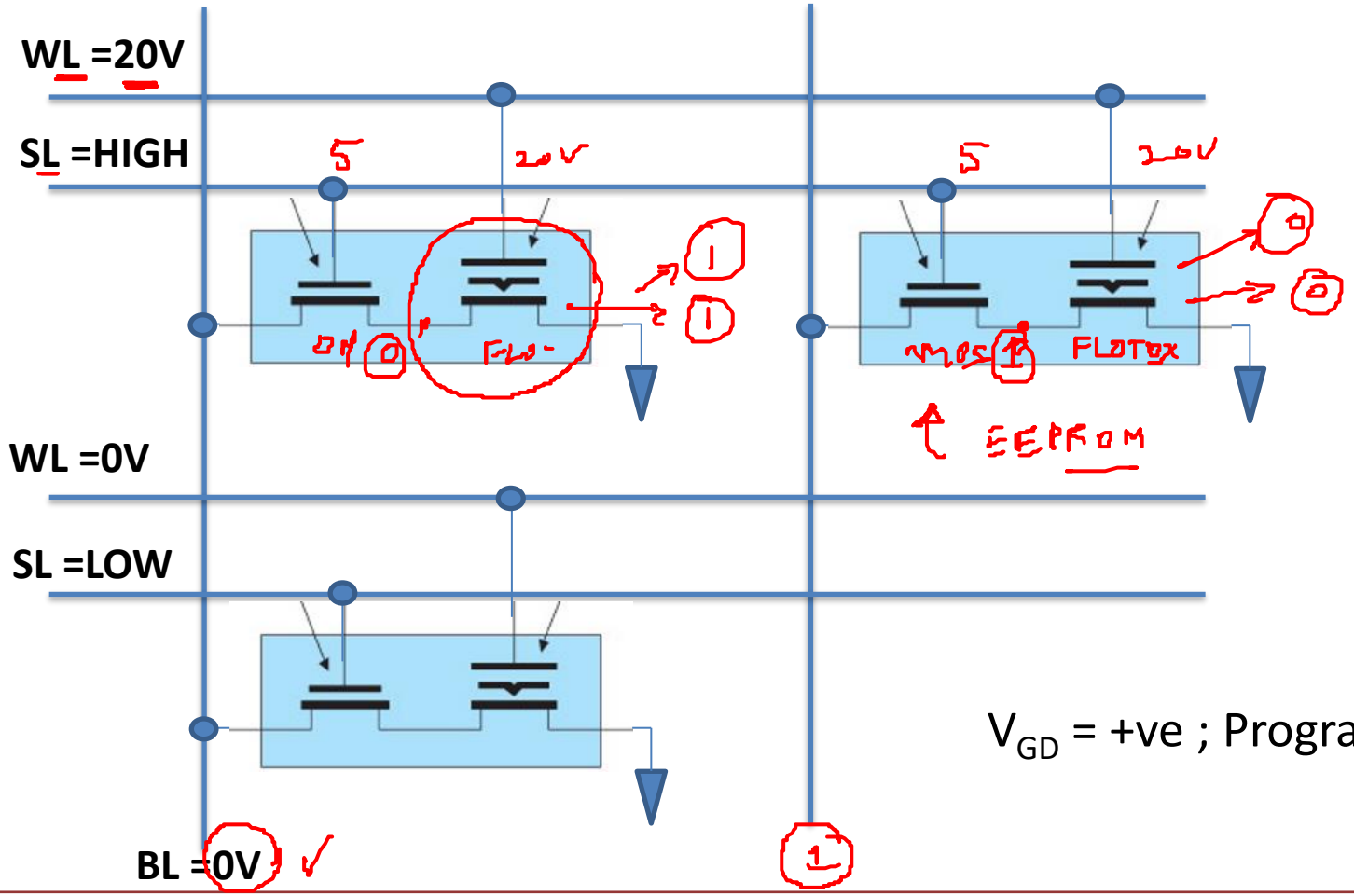
- Control gate is grounded. Source is left floating. High positive voltage is applied to the drain (VDG=+VE).
- The electrons tunnel from the floating gate back to the drain.
- Erasing is achieved by reversing the voltage applied during the writing process

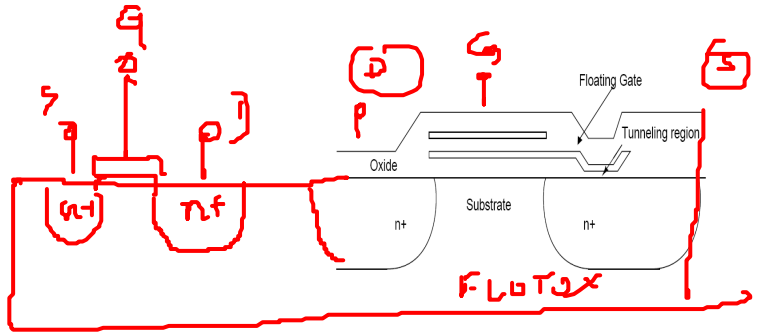


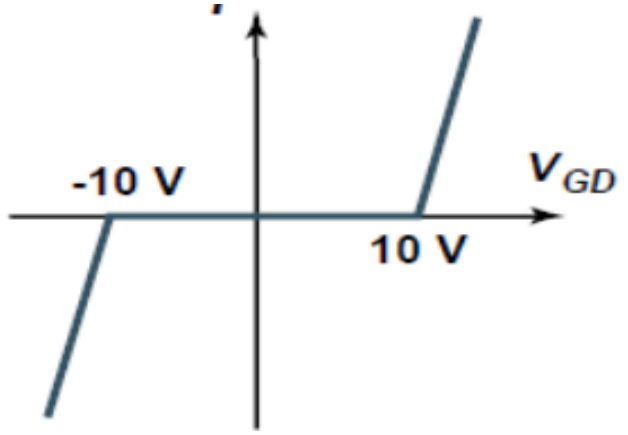


Non Volatile Memory
EEPROM

EEPROM Cell Operation : Programming (Write)







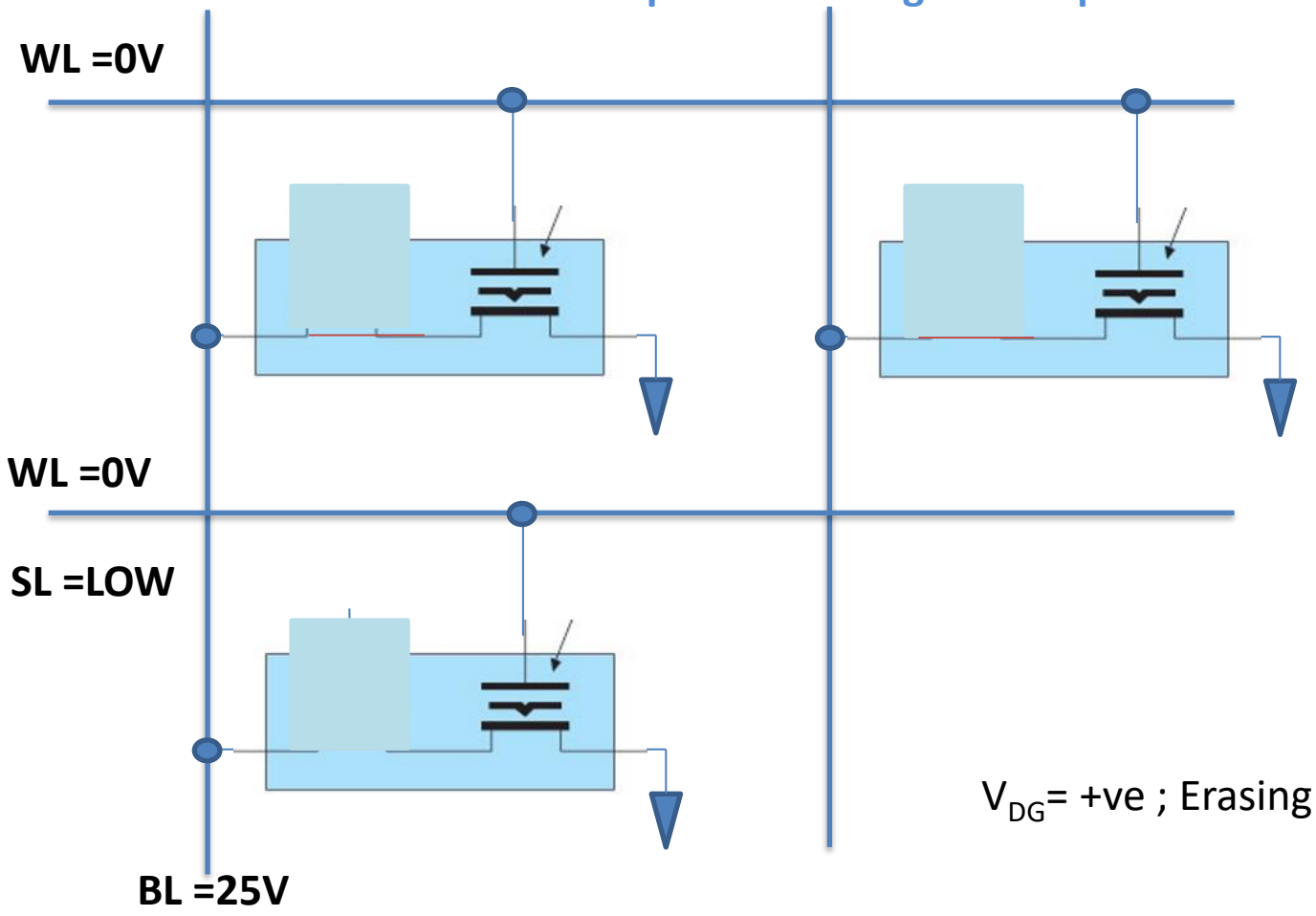
V_{GD} = +ve ; Programming

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
EEPROM

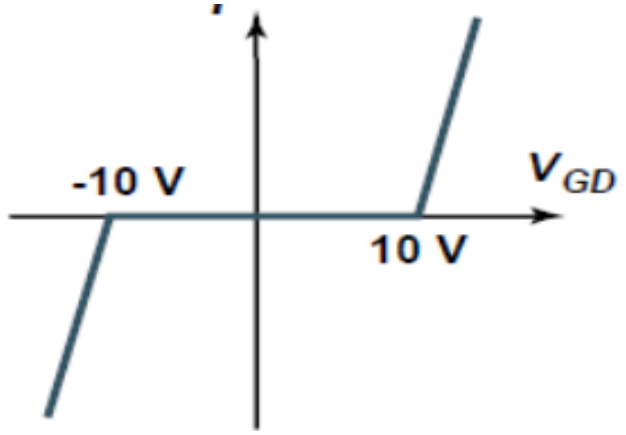
EEPROM Array and Significance of Access MOS and Erase Operation

What if Access Transistors were NOT present during Erase Operation?



V_{DG}= +ve ; Erasing

- Select Lines – decides the Row being accessed
- Word Line- Used to Control the EEPROM for Programming, Erasing and Reading Mode



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Non Volatile Memory
EEPROM

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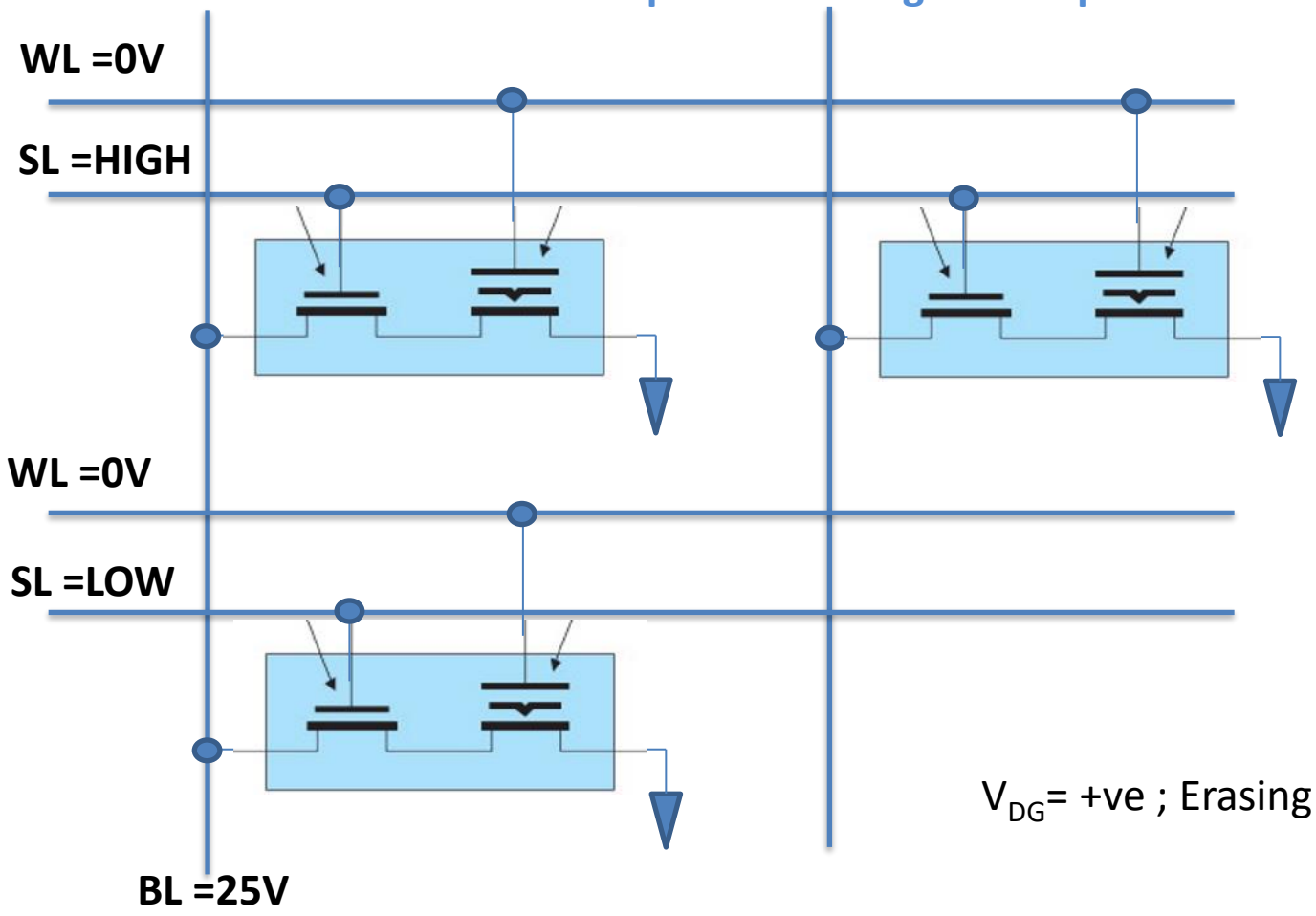

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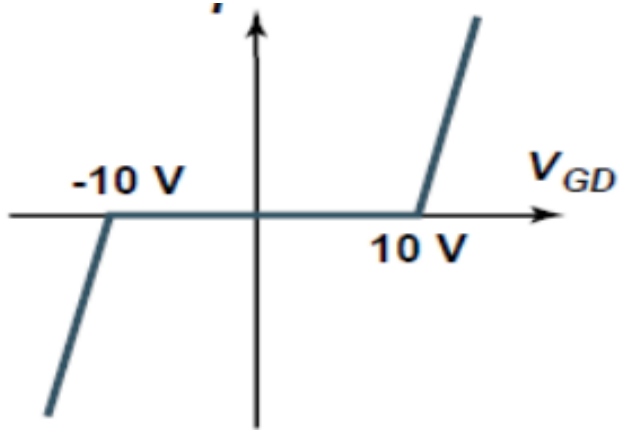
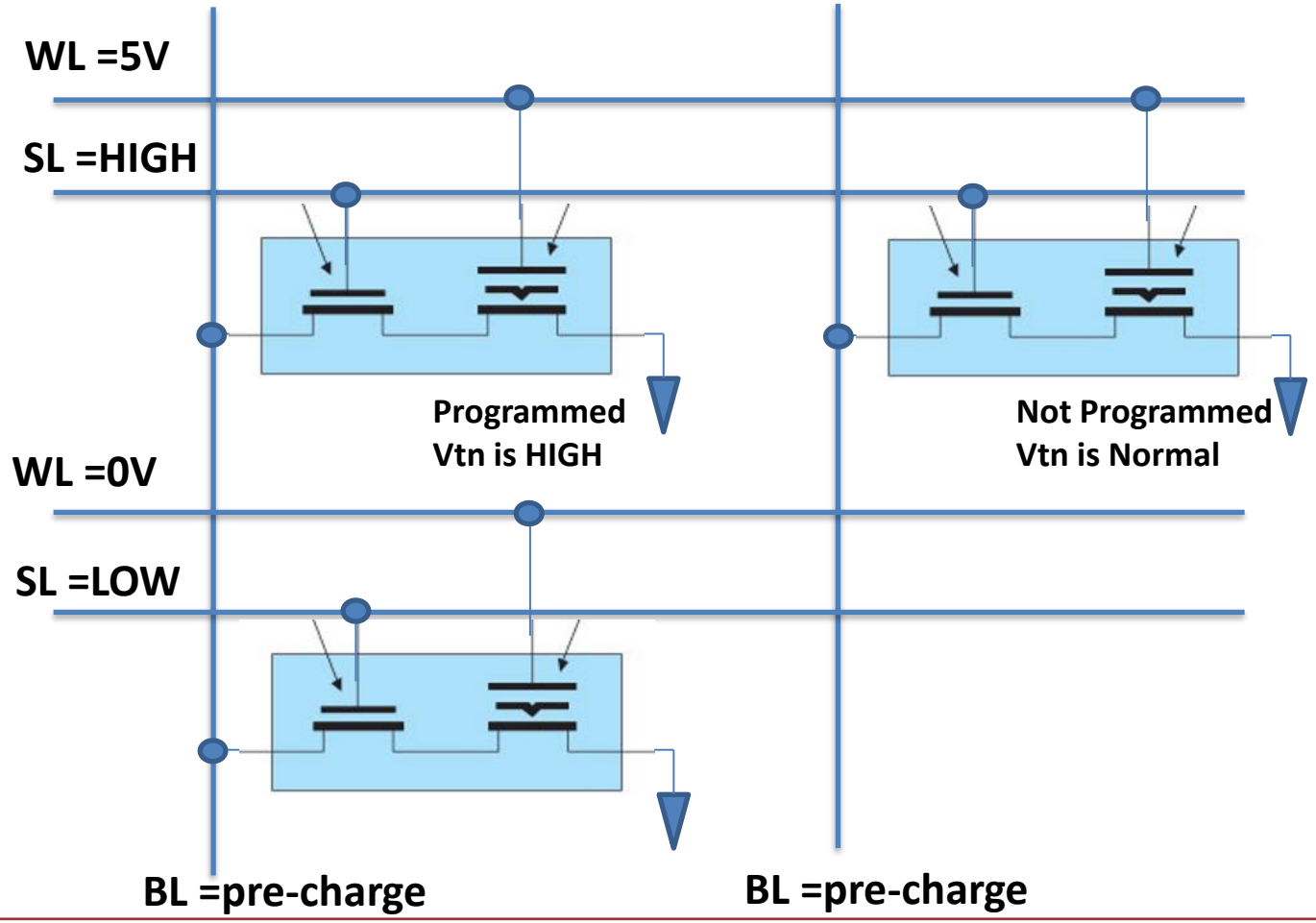


Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
EEPROM

EEPROM Cell Operation : Read Operation

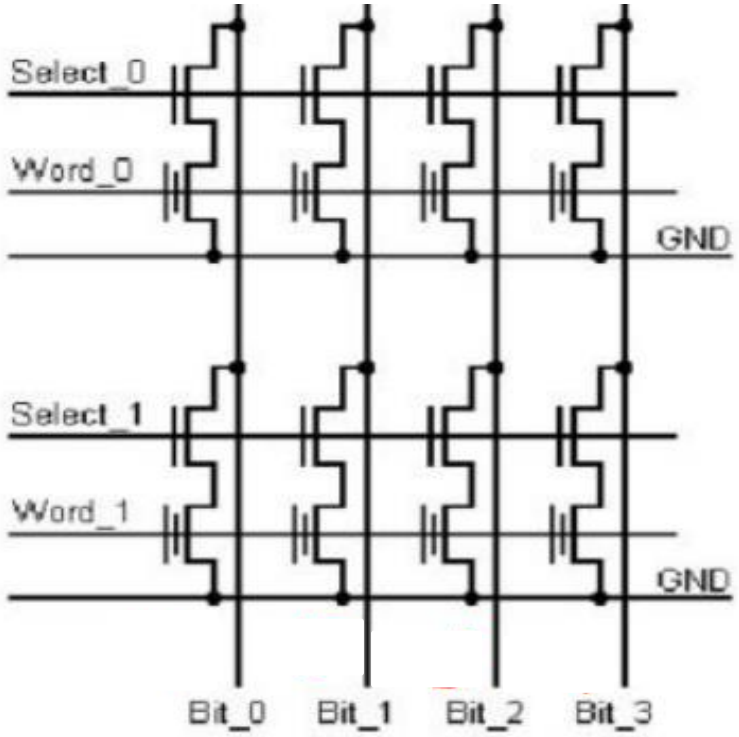


- During a Read operation, both WL and SL go high turning ON the access transistor.
  - **If the storage transistor is programmed,** it does not turn ON as threshold voltage is HIGH. BL remains at its pre-charged value, implying a '1' stored in the cell.
  - **If the storage MOS is unprogrammed then threshold voltage will be small and storage transistor will turn ON,** discharging BL to ground, implying a '0' stored in the cell

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
EEPROM

A 2X4 EEPROM Array



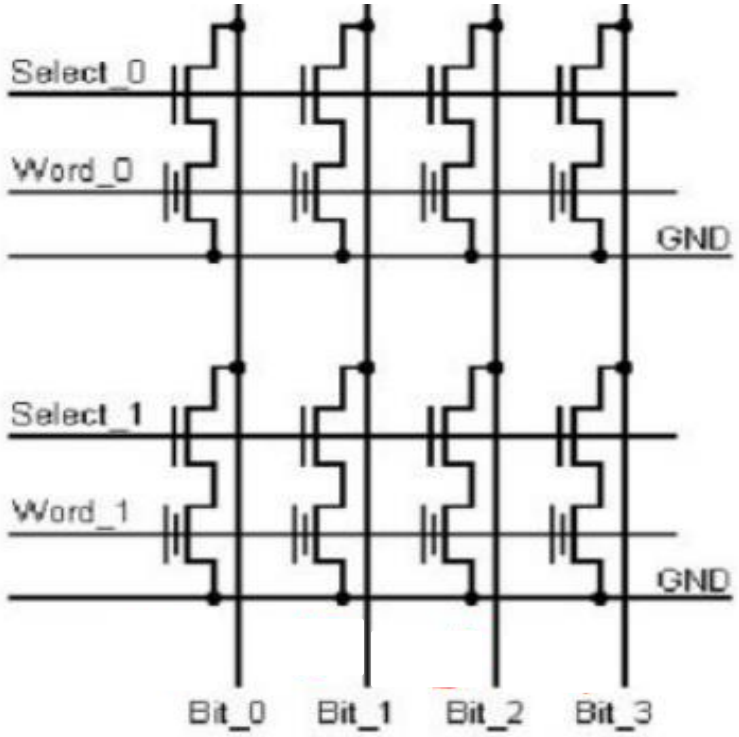
To erase Cell 1:
SL0 = 1, WL0 = 0, SL1 = 0, WL1 = 0 BL0 = 0, BL1 = 1 (High Voltage), BL2 = 0, BL3 = 0

The high – voltage on BL1 is felt at the drain of Cell 1 transistor which causes the electrons on the floating gate to move towards the drain thus erasing the transistor. In the absence of the access transistor, the cell 5 transistor would also be erased

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
EEPROM

A 2X4 EEPROM Array



To program Cell 1 transistor:
SL0 = 1, WL0 = 1, SL1 = 0, WL1 = 0 BL0 = 1, BL1 = 0 (High Voltage), BL2 = 1, BL3 = 1 (VGD1=HIGH)

The drain voltage for Cell 1 transistor is low whereas its gate voltage is high. Hence the electrons tunnel from the drain to the floating gate and Cell 1 transistor is programmed. For the other transistors in Columns 0, 2, 3, **the high drain voltage prevents the tunneling of free electrons and hence those transistors are not programmed.**

Non Volatile Memory
EEPROM

Disadvantages of EEPROM:

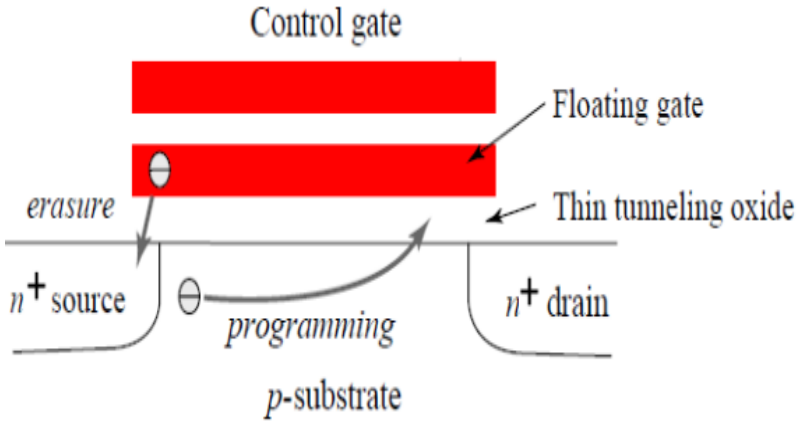
1. Larger than EPROM since there are 2 transistors in a cell.
2. FLOTOX device is larger than FAMOS device due to the extra area of the tunneling oxide. Hence lesser density and higher cost.
3. Fabrication of a very thin oxide is challenging and costly step.
4. Repeated programming causes a drift in the threshold voltage due to permanently trapped charges in SiO_2 . This leads to malfunction or the inability to reprogram the device.

Advantage: Higher endurance. Supports upto 105 erase/write cycles

Non Volatile Memory
FLASH MEMORY

Flash EEPROM is the one in which

- **Programming** is done using **Avalanche Hot – electron injection method (as in EPROM).**
- **Erasing** is performed using the Tunneling which is known as Fowler – Nordheim Tunneling method (as in EEPROM).
- Devices where in the contents of **the entire array or large blocks can be erased simultaneously.** Due to **their bulk erase characteristics, they do not have the access transistor** in each cell. Therefor the density of cells will be more in comparision with EEPROM where access MOS were required to erae selected bit.
- Flash memories use ETOX transistors as storage devices. It resembles a FAMOS cell, except that a very thin tunneling gate oxide is used.

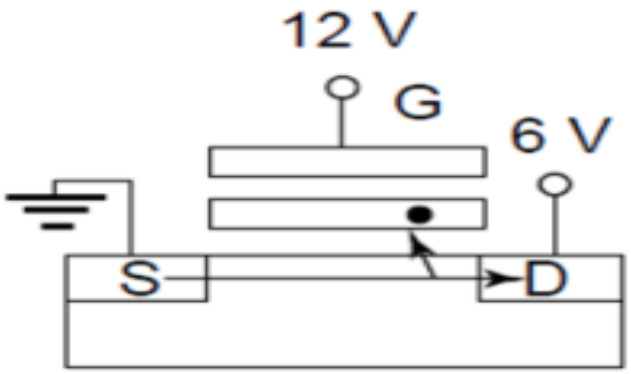


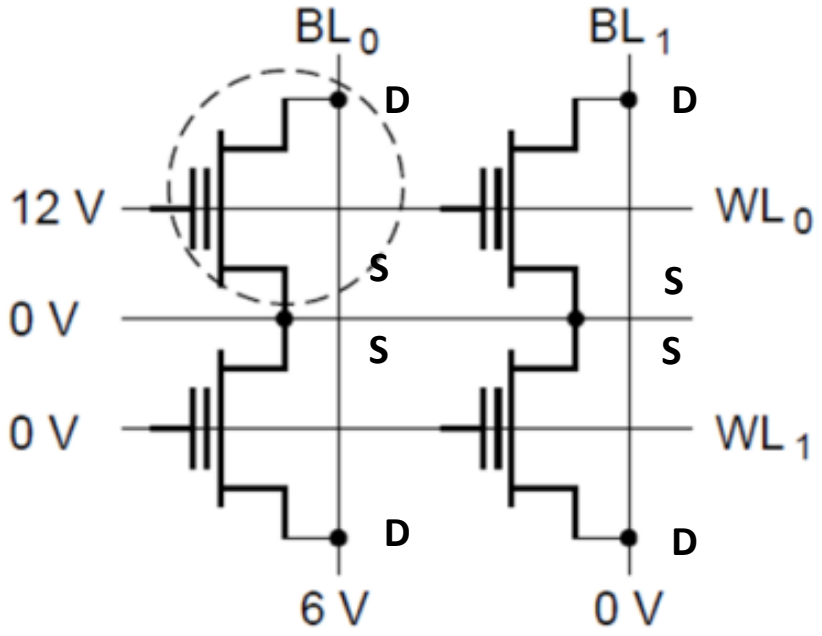
Non Volatile Memory
FLASH MEMORY

Types of Flash Memory

1. NOR Flash Memory

Case (a) : Programming (Write operation): Hot electron injection method





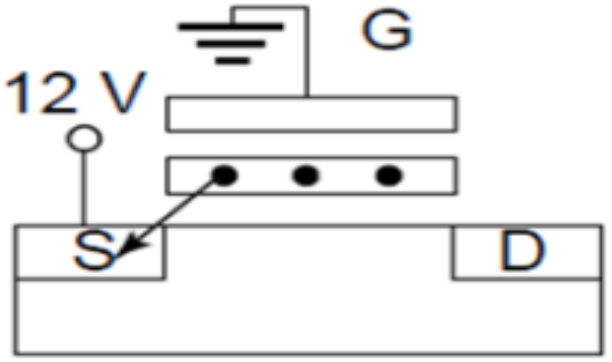
- Both drain (BL) and gate (WL) are at high voltage and Source is grounded.
- Only 1 cell (encircled) is programmed. Its threshold voltage is increased above the normal WL voltage

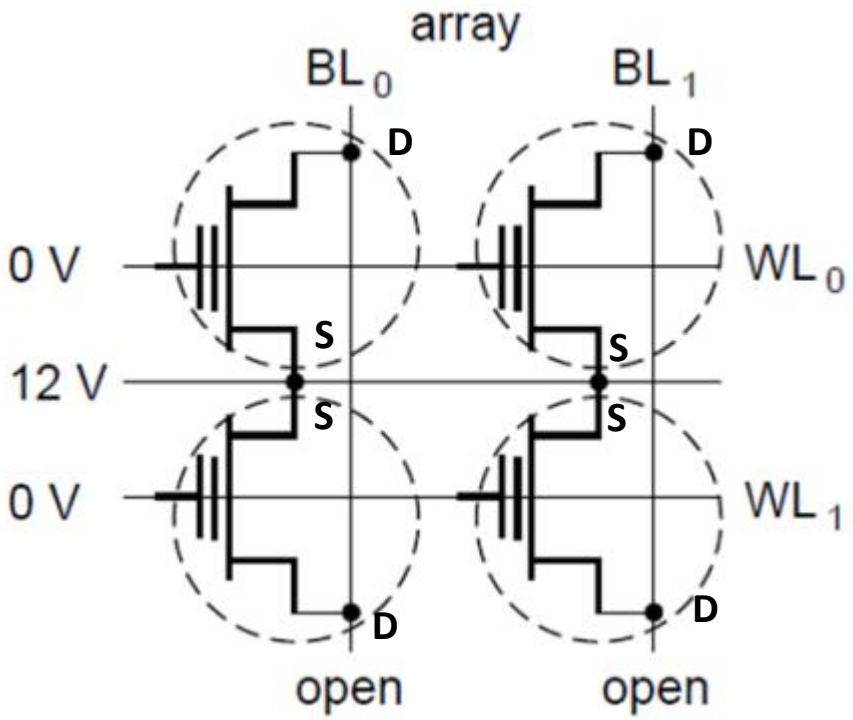
Non Volatile Memory
FLASH MEMORY

Types of Flash Memory

1. NOR Flash Memory

Case (b) : Erase operation





- Source side erase – Drain is floating, Source is connected to high potential and Gate is grounded. All cells are erased simultaneously.

Types of Flash Memory

1. NOR Flash Memory

Case (b) : Erase operation

The different initial values of the cell **threshold voltages as well as the variations in the oxide thickness may cause variations in the threshold voltages at the end of the erase operation**.

Therefore, the following steps are followed to avoid variations in the threshold

i. Before applying the erase pulse, **all cells in the array are programmed so that all thresholds start at approximately the same value.**
ii. An erase pulse of controlled width is applied.
iii. Subsequently, the whole array is read to ensure that all cells have been erased
iv. If not, another erase pulse is applied, followed by a read cycle. The algorithm is applied until all cells have threshold voltages that are below the required level. Typical erasing times are between 100 ms to 1s.

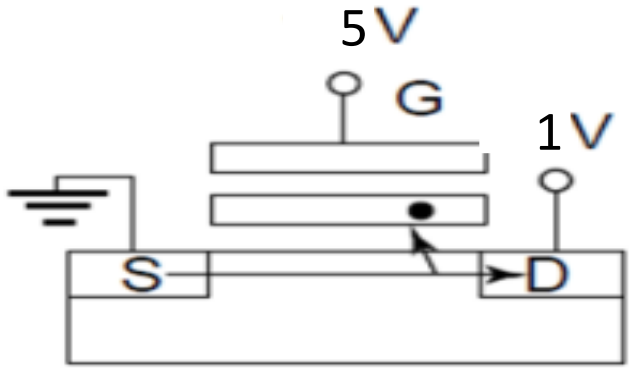
Non Volatile Memory
FLASH MEMORY

Types of Flash Memory

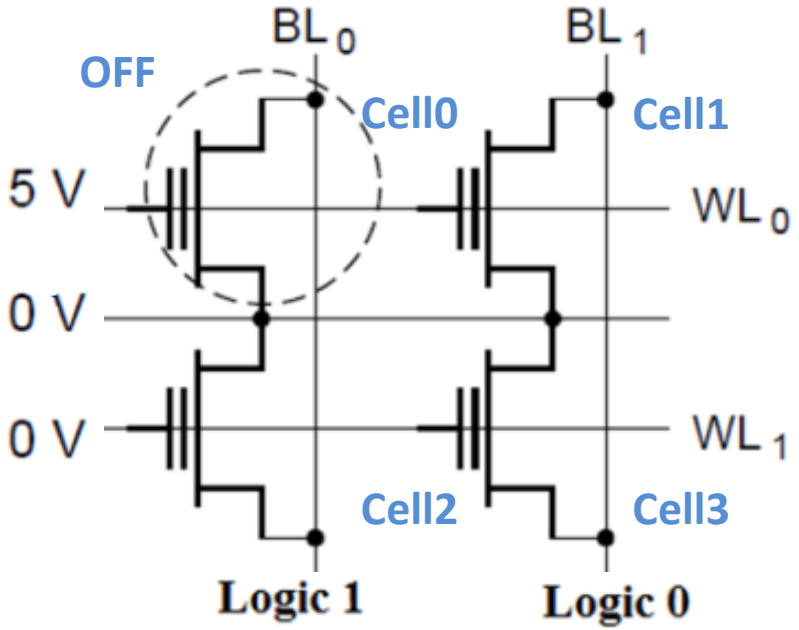
1. NOR Flash Memory

Case (c) : Read operation

Source is grounded and WL – 5V. Cell 0 is programmed and does not discharge BL0 which reads ‘1’ Cell 1 is not programmed. Hence BL discharges and reads logic ‘0’



Initially BLs are pre-charged

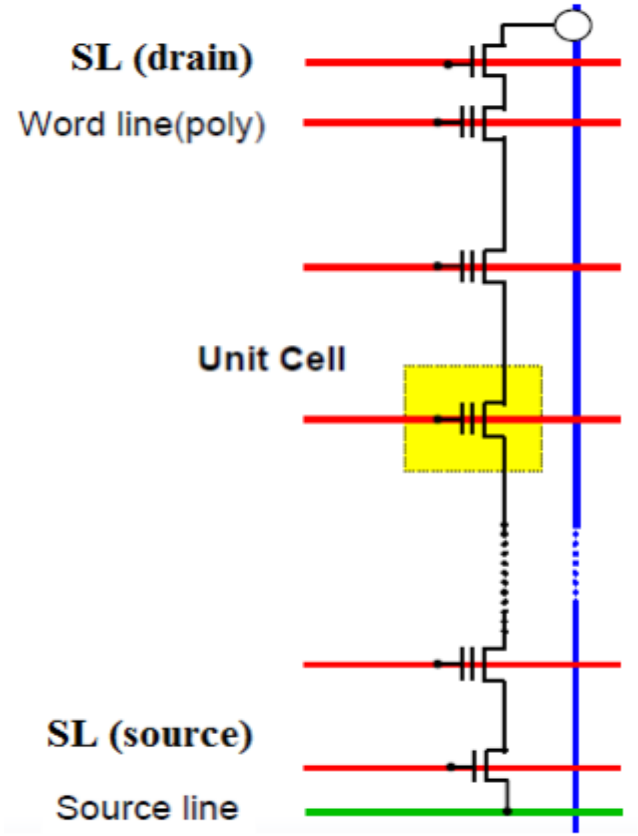


- ✓ **Cell0** is **Programmed** which means threshold voltage is HIGH and VGS=5 will not turn ON Cell0 (Cell0 is remains in OFF state) and No path for BL to discharge, Therefore BL0 remains in pre-charged state (logic1)
- ✓ Cell1, Cell2 and Cell3 are **Not Programmed** and threshold voltage is LOW(Normal) and VGS=5 will turn ON the Cell. In these Cell1 will turn ON providing discharging path for BL1

Non Volatile Memory
FLASH MEMORY

Types of Flash Memory

1. NAND Flash Memory : For both Programming and Erasing it uses EEPROM approch



Operation: Erasing

- Control gate is grounded. Source is connected to High positive voltage (Source tunneling) is applied to the drain (VSG=+VE).
- The electrons tunnel from the floating gate back to the Source.

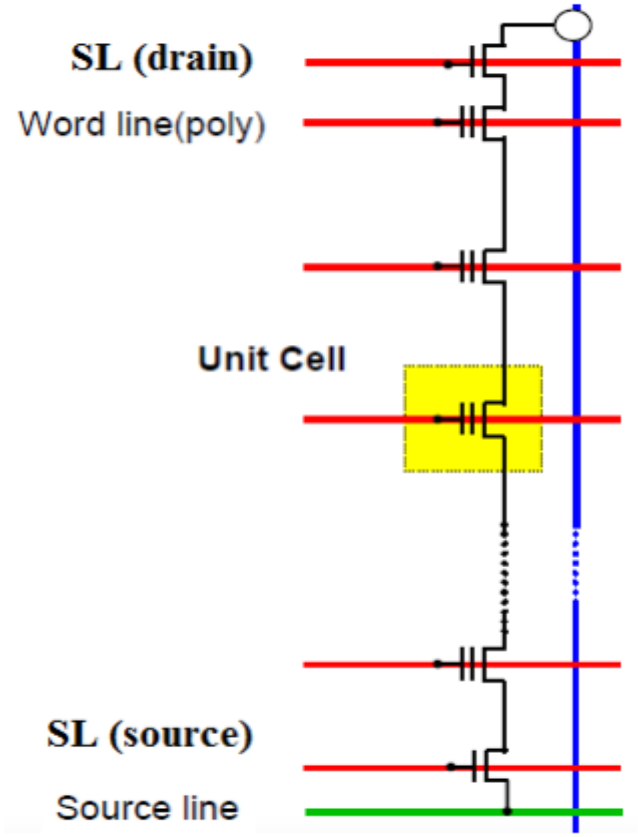
Operation: Programming

- Control gate is given HIGH Voltage and Drain Grounded (VGD=+VE).
- The electrons tunnel into the floating gate from drain.

Non Volatile Memory
FLASH MEMORY

Types of Flash Memory

1. NAND Flash Memory : For both Programming and Erasing it uses EEPROM approch



Programming:

- All WLs – 5V
- WL for the cell/s to be programmed – 20V
- SL (source) - Low, turning OFF the source select FET
  SL (drain) – High to connect the cell structure to Bit line.

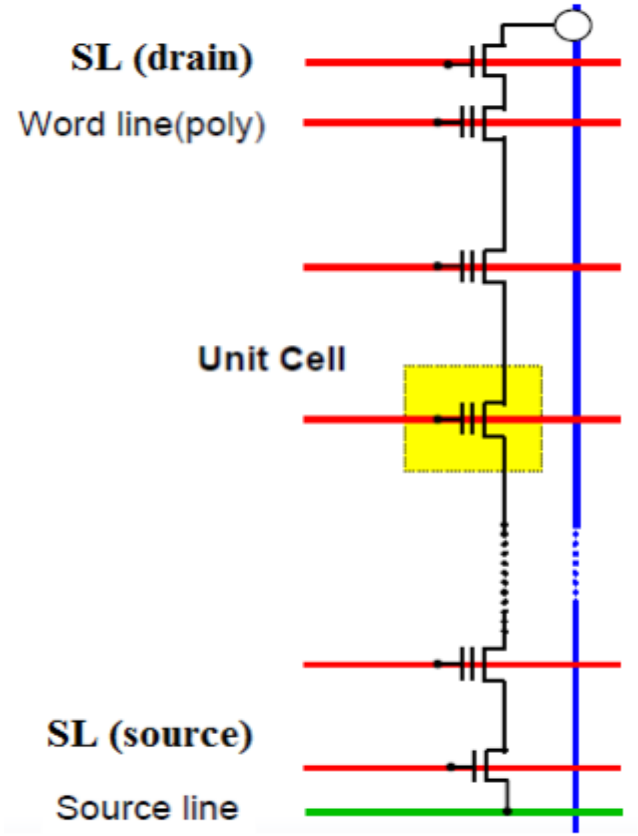
✓ If BL is grounded, (VGD=+ve) transistor is programmed.

✓ If BL is set to high voltage, then tunneling does not happen and transistor is not programmed

Non Volatile Memory
FLASH MEMORY

Types of Flash Memory

1. NAND Flash Memory : For both Programming and Erasing it uses EEPROM approch



Erase:

- Before erasing, all cells of a block are programmed to increase their threshold voltage.
- Then WL (Control gate) = 0
- SL (source) - High Source Line – 20V, which causes all substrates to get a high potential . Electrons tunnel from the floating gate to the channel (substrate) – Channel erase technique
- SL (drain) – Low, Bit line is disconnected

Advantages of NAND Flash

i. The size of the NAND flash cell is 60% smaller than the NOR Flash cell since there is no separate contact for each cell as well as no additional ground lines between rows. Hence they are denser than NOR Flash. They range in density from 1Gb to 16Gb whereas the density of NOR Flash ranges from 64Mb to 2Gb.

ii. Fast program and erase operations when compared to NOR Flash.

iii. NAND Flash is best suited for sequential data applications such as audio and video storage.

Non Volatile Memory
FLASH MEMORY

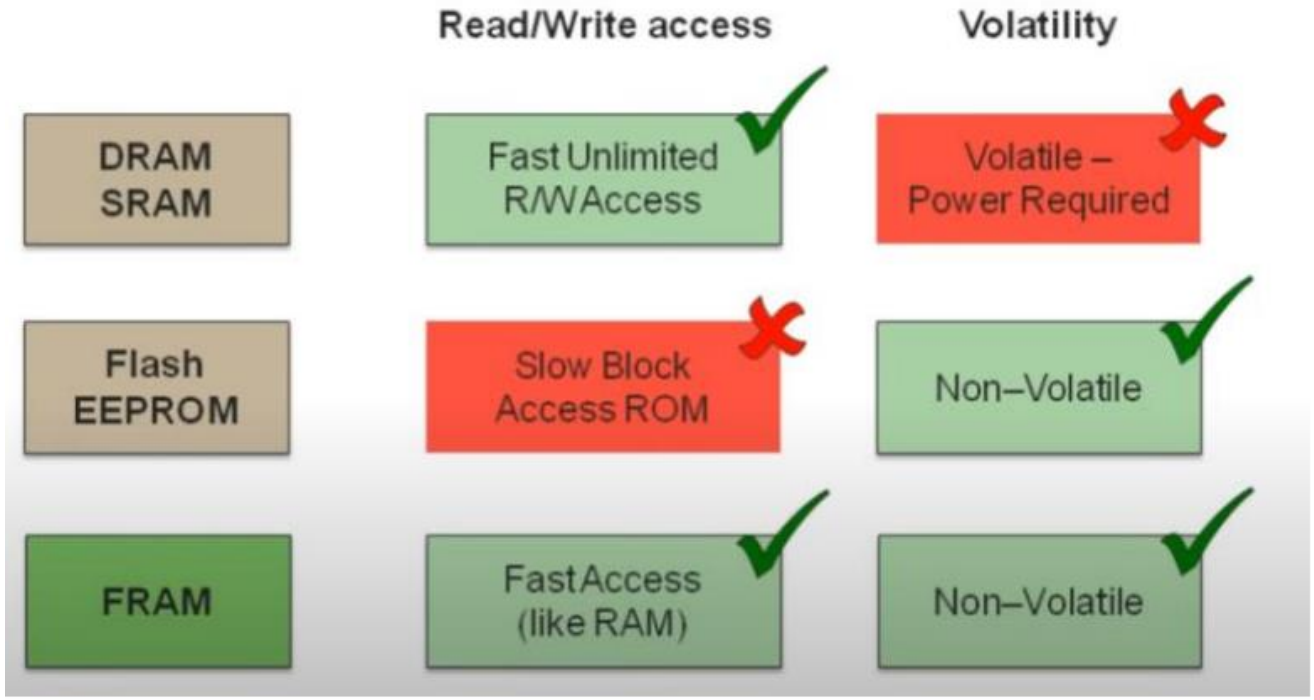
Advantages of NOR Flash

i. Faster Read operation when compared to NAND Flash
ii. NOR Flash is suited for Random Access applications such as program code storage whereas Random access of data is much slower in NAND Flash.

General Comparison:

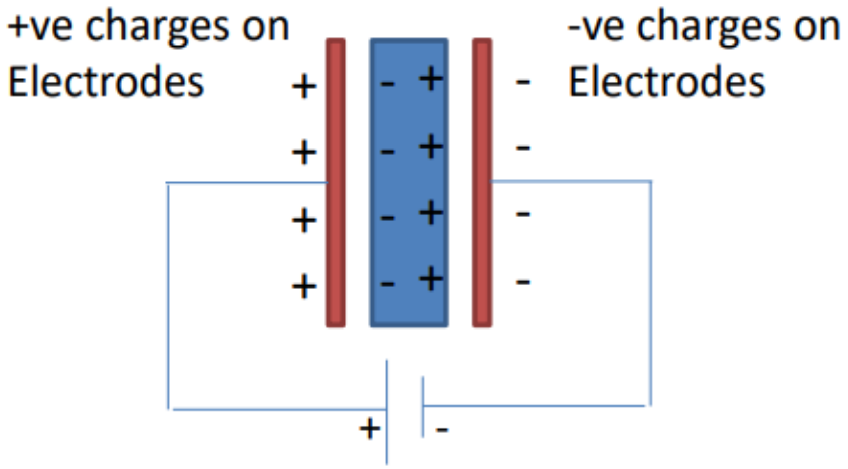
i. NOR flash uses Hot – electron injection for programming and Fowler – Nordheim tunneling for erasing whereas NAND flash uses Fowler – Nordheim tunneling for both operations.
ii. Endurance of Flash is 105 erase/write cycles. Comparison between NOR Flash and NAND Flash

Non Volatile Memory
FeRAM

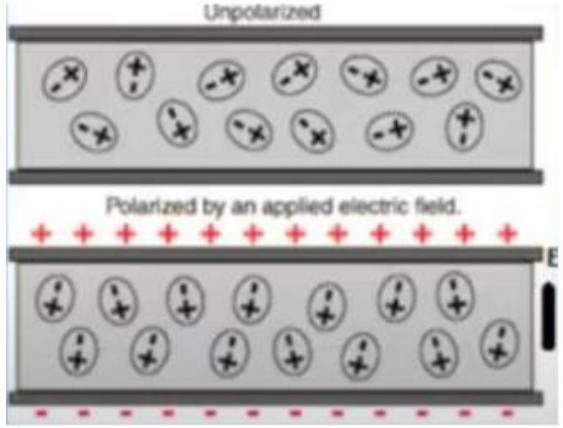


Non Volatile Memory
FeRAM

What is Polarisation ?



Opposite polarity of charges are built in dielectric material on two sides of dielectric material and is know as **polarisation**



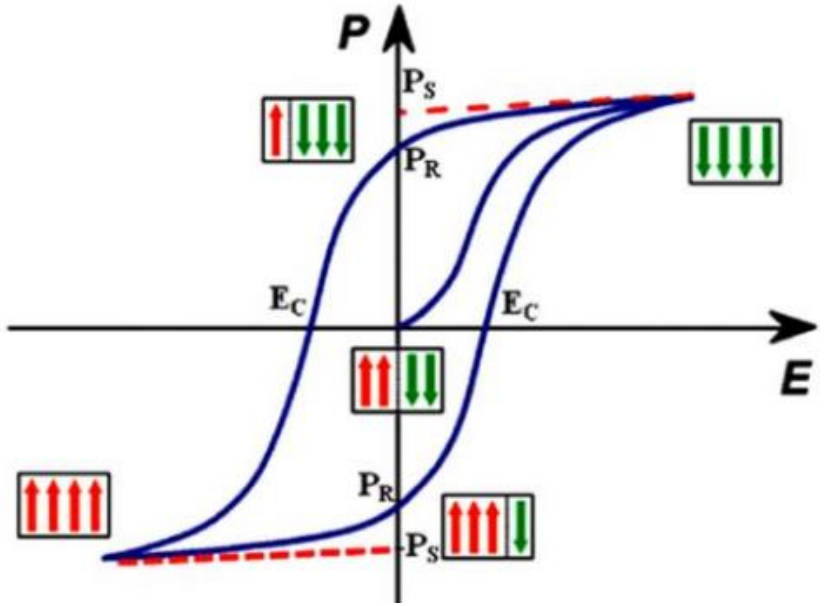
A dielectric Material gets polarised linearly with supply of potential at electrodes and then depolarised once potential at electrodes removed

A Ferro Electric Material gets polarised with supply of potential at electrodes and remains in polarised state in the absence of electric field i.e., Exhibits spontaneous polarisation – even in absence of electric field

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
FeRAM

- Materials in which the induced polarization is proportional to the electric field are called linear dielectrics. The dielectric material SiO2 is a Linear dielectric material.
- Ferroelectric materials have a non-linear relationship between the applied electric field and the polarization. It follows a hysteresis loop

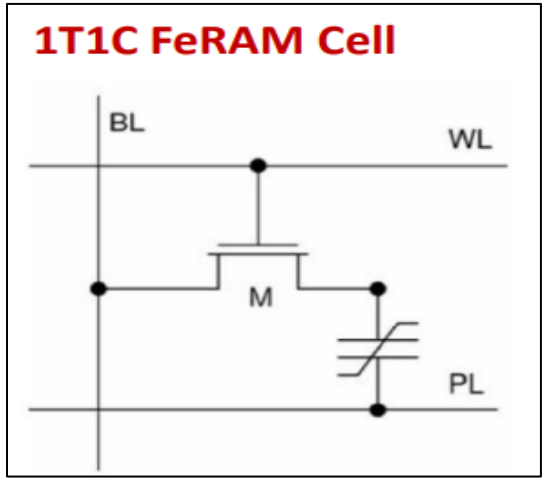


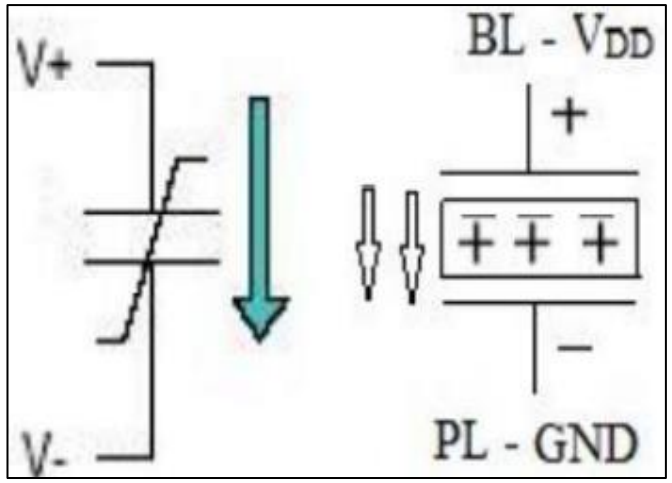
- When an external voltage is applied, the material is either polarized to a '1' state or '0' state. When the voltage is removed, residual polarization remains in the material (+Pr or –Pr) which is called spontaneous polarization.
- The dielectric constant of a ferroelectric material is much higher than that of a linear dielectric due to the effects of semi-permanent electric dipoles formed within the crystal structure

Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory
FeRAM

FeRAM cell is similar to DRAM Cell structure where it uses a Capacitor with dielectric material which has spontaneous polarization property i.e., Ferro electric material as dielectric between two plates of capacitors



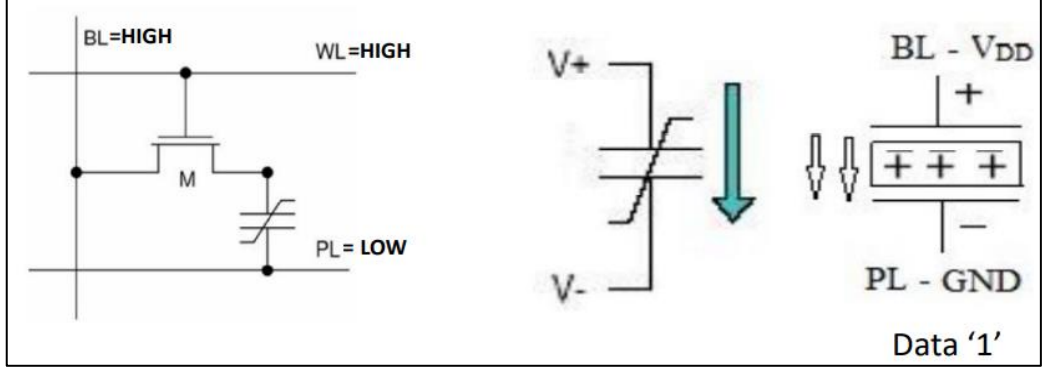


Write: Accomplished by applying a field across the ferroelectric layer by charging the plates on either side of it, forcing the dipoles inside into the “up” or “down” orientation, thereby storing a ‘1’ or ‘0’. BL=HIGH, WL=HIGH, and PL=0 ; M turns ON and One plate of the Ferroelectric capacitor will have +ve potential and the other side will have –ve potential

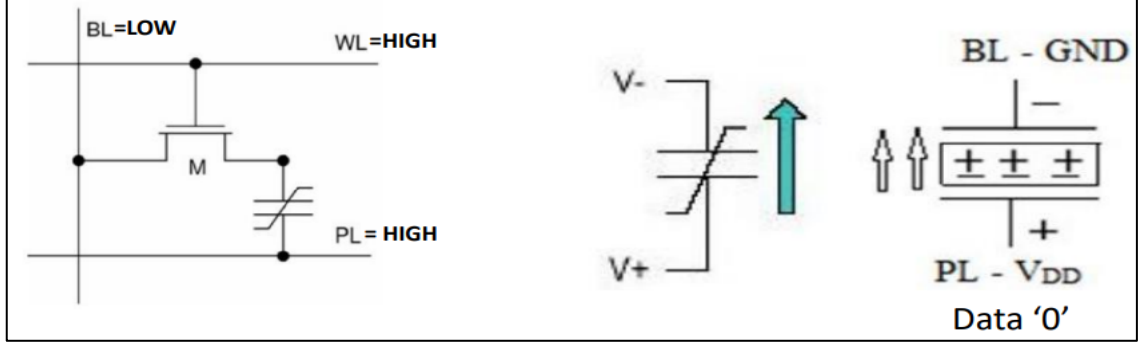
Non Volatile Memory
FeRAM

1T1C FeRAM Cell Write: Accomplished by applying a field across the ferroelectric layer by charging the plates on either side of it, forcing the dipoles inside into the “up” or “down” orientation, thereby storing a ‘0’ or ‘1’.

Write’1’: WL=HIGH, PL=LOW and BL=HIGH; M turns ON



Write’0’: WL=HIGH, PL=HIGH and BL=0; M turns ON



Reference :“Digital Integrated Circuits–A Design Perspective”, Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory

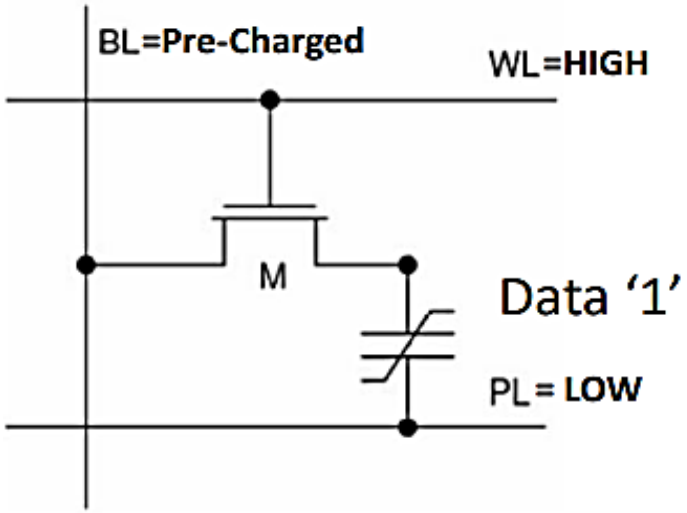
FeRAM

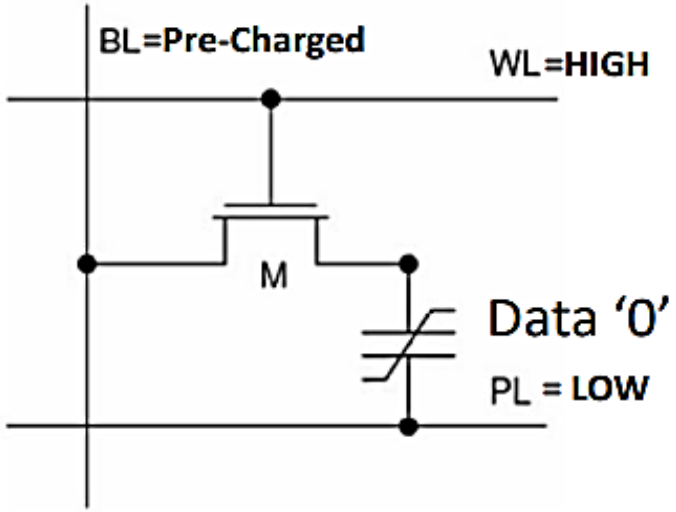
1T1C FeRAM Cell

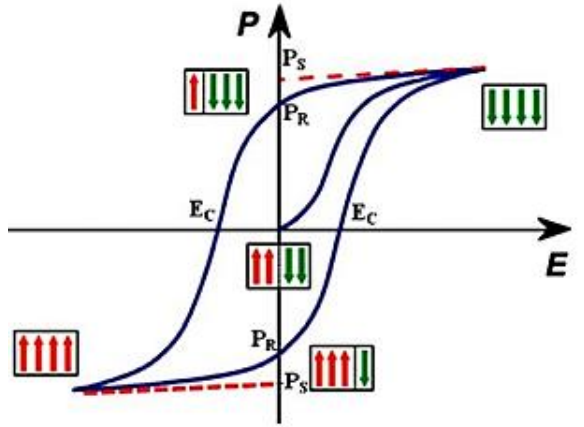
Read: WL – High, PL – GND and BL – pre-charged (High)

a) If a cell holds a '1', nothing happens on the output line.

b) If the cell holds a '0', reorientation of the dipoles occurs in the atoms which causes a brief pulse of current in the output, discharging BL slightly. This indicates a '0' in the cell. Destructive 'read' operation since the cell is overwritten. Hence requires rewriting the cell after each read







Reference :"Digital Integrated Circuits–A Design Perspective", Jan, M. Rabaey, Chandrakasan Anantha, and Nikolic Borivoje, Pearson, 2nd Edition., 2003.

Non Volatile Memory

FeRAM

Limitations:

- Endurance is limited by hysteresis fatigue which demonstrates itself with a flattened hysteresis loop and reduced residual polarization. Current commercial FeRAMs have a fatigue limit of 1012 operations.
- Can develop an imprint where the hysteresis loop shifts vertically to give preference for one data type over another.
- Polarization data can decrease over time causing a slow loss of the cell's data.
- Cannot be scaled down since materials tend to stop being ferroelectric when they are too small. Less dense

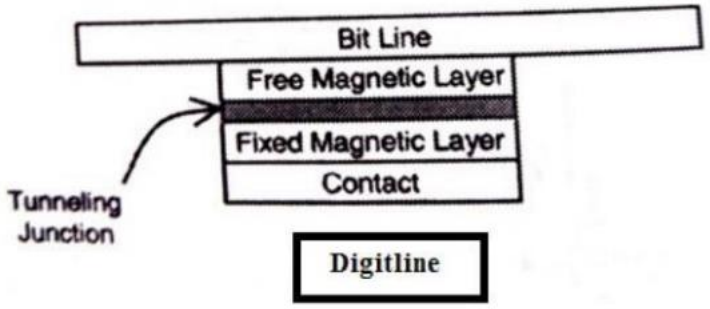
Advantages

- Does not require periodic refresh like DRAM. Refresh is required only after a read operation
- Power is consumed only when reading or writing. Hence less power than DRAM
- Most 1T1C FeRAMs have a folded bit-line architecture which keeps noise low

Non Volatile Memory

Magneto-resistive RAM - MRAM

- A metal is said to be magneto resistive if it shows a slight change in its electrical resistance when placed in a magnetic field.
- The change in resistance enables data storage.
- Core of each MRAM cell is a thin material with reversible magnetic polarity known as Magnetic Tunnel Junction or MTJ.
- This material is sandwiched between a fixed magnetic polarity material and a variable magnetic polarity material

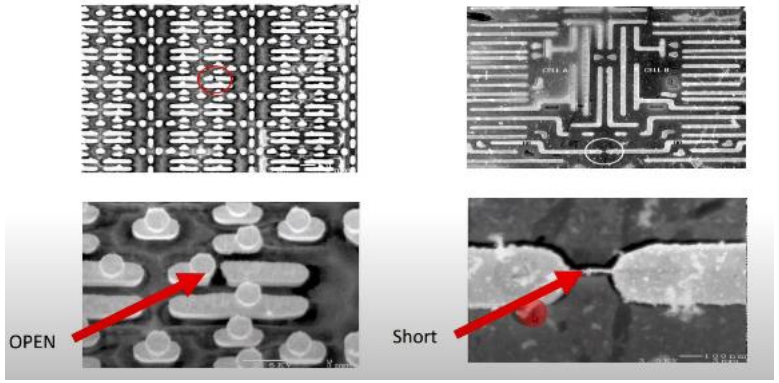


Outline

Memory Faults:

- General Fault Modeling,
- Read Disturb Fault Model,
- Pre-charge Faults,
- False Write Through,
- Data Retention Faults,
- Decoder Faults;

type	area	speed	retention	application	test method
SRAM	largest 6T	fastest <1ns	as long as power	embedded SRAM cache, registers	BIST
DRAM	medium 1T+1C	medium ~10ns	< sec.	embedded DRAM	BIST/ ATE
				on-board memory	ATE
Flash	smallest 1T	slowest ~100µs	years	SSD, USB drive	ATE



Memory Testing
Introduction

Testing:

The purpose of testing is to **detect manufacturing defects**. It may be

1) **the testing of stand-alone memories**, **through-the-pins testing,** or
2) by self-testing

Characterization:

Characterization is defined as examining the margins of a design and performing design verification.

- Characterization looks at **marginality for the voltage, temperature, timing, and any other environmental conditions**. This is done to verify that the design is, in fact, a good design.
- When a chip design is first **fabricated it should be characterized to ensure that the design functions and that it is robust.**

Memory Testing
Introduction

- In the testing of logic and Flip flop, there are regular references to **fault coverage**. This fault coverage is with respect to a given set of fault models.
  - ✓ The most common of these is the **stuck-at fault** model. The coverage defined is considered to be sufficient for that generation of chips.
- In memory technology ,
  - ✓ **The Capacity quadruples every 3 years** which leads to decrease in memory price per bit
  - ✓ **High storage capacity is obtained by raise in density, which implies decrease in size of circuit** (capacitor with same capacity using lesser area are designed) used to store a bit
  - ✓ Further **for faster access of memory** – Various techniques like Fast Page, SDRAM, DDRAM.
- In memories, **in addition to Stuck at Fault , other fault models must be considered**. Anyone who approaches memory testing with the view that **considers the stuck-at fault model as sufficient, regardless of the coverage percentage, is exceedingly foolish.**
- The stuck-at fault model is not the only way by which memories can fail. Most memories may not fail to the stuck-at fault model and yet numerous faults can still exist and need to be culled out.
- The objective in testing is to discard all defective memories that will fail in the field, not just eliminate those of a certain fault model.

Memory Testing

General Memory Fault Modeling.

Memory fault models.

There are four classic memory fault models.

1. Stuck-At Fault (SAF) Model
2. Transition Fault Model (TF) Model
3. Coupling Fault Model (CF) Model
4. Neighborhood Pattern Sensitive Fault (NPSF) Model.

Memory Testing

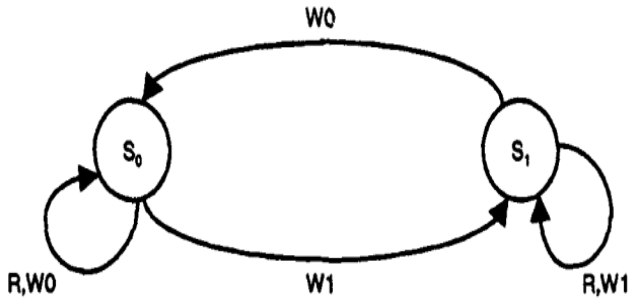
General Memory Fault Modelling.

1. Stuck-At Fault (SAF) Model

Markov diagram of memory Cell

- S0 – Memory Cell at State 0
- S1 – Memory Cell at State 0
- R – Reading ‘0’/’1’
- W0 – Writing binary ‘0’, W1 – binary ‘1’

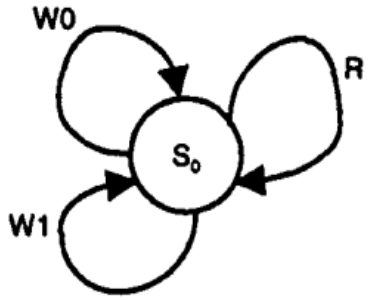
A good memory cell.



NOTATION: <*S*/*F*>: a fault in a cell [van de Goor 91]

- *S* is value or operation activating fault , $S \in \{0, 1, \uparrow, \downarrow, \updownarrow, \forall\}$
  - $\uparrow$ is rising; $\downarrow$ is falling; $\updownarrow$ is either $\uparrow$ or $\downarrow$; $\forall$ means any condition
- *F* is faulty value of cell , $F \in \{0,1, \updownarrow\}$
  - $\updownarrow$ is complement

A memory cell Stuck at ‘0’.



A memory cell Stuck at ‘1’.

Memory Testing

General Memory Fault Modelling.

2. Transition Fault Model (TF) Model

- In looks like a stuck-at fault but in this case the memory cell will retain either state. However once it is written to one state it cannot transition back.
- Thus, when the memory is powered up the cell may be in either a "0" or a "1" state. **It can only be written in one direction**

- S0 – Memory Cell at State 0
- S1 – Memory Cell at State 0
- R – Reading ‘0’/’1’
- W0 – Writing binary ‘0’
- W1 – binary ‘1’

- In the diagram, It can be seen that it is possible to transition this cell from a "0" state to a "1" state but it cannot transition back.

General Memory Fault Modelling.

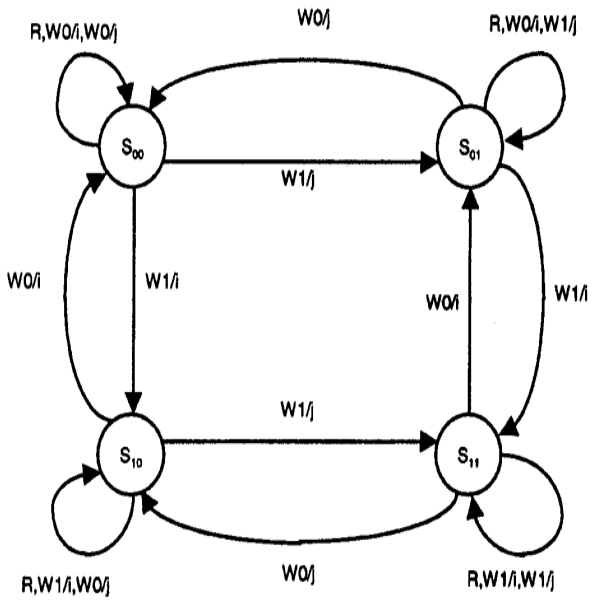
3. Coupling Fault Model (CF) Model

- Let us consider simple case of coupling of two neighbor cell.

- The coupling may cause it to go to an erroneous state or cause it to falsely transition.
- **Markov diagram** of a pair of defect free pair of cells.
- The cell states and operations are represented by their "i" and ‘j'' subscripts.
- Therefore, there am four possible states, in which the two-cell combination can reside.
- Each cell can be individually written or individually read.

00 01 ij

10 11



General Memory Fault Modeling

3. Coupling Fault Model (CF) Model

- A coupling fault, where a first cell causes a second cell to be written i
- It is possible to have a defect where a **fault is unidirectional.** **One cell can couple into another cell but the opposite does not happen.**
- **Aggressor Cell:** The cell, that does the coupling, is referred to as the aggressor cell and
- **Victim Cell:** the cell that in turn transitions due to the coupling of Aggressor Cell is called the victim cell.
- The aggressor cell appears to operate correctly but the victim cell goes to the incorrect state.

General Memory Fault Modeling

3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

i. State Coupling Fault (SCF)
ii. Inversion Coupling Fault
iii. Idempotent Coupling Fault

i. State Coupling Fault (SCF)

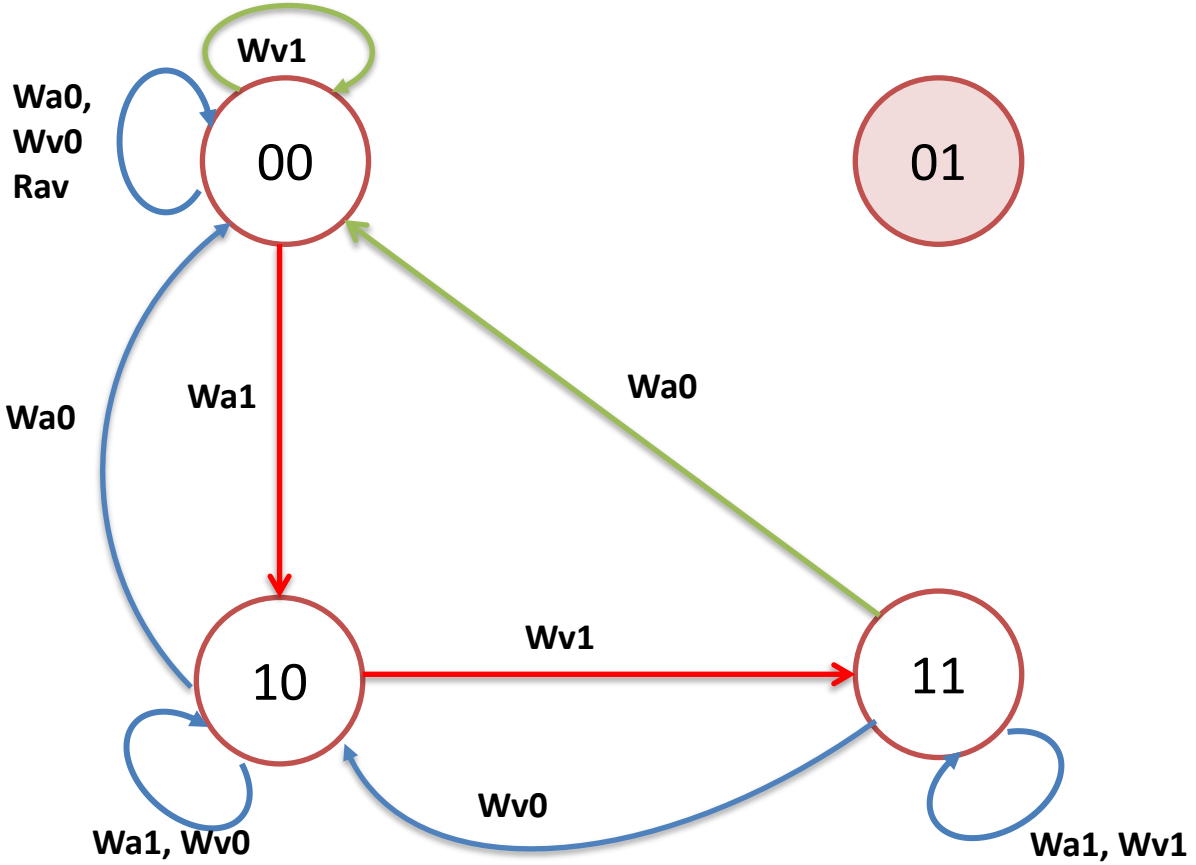
- If an **aggressor cell is in a specific state** then the **victim cell is forced to an erroneous state.**
- Does not require an operation to be performed nor a transition to occur

Example : A ‘0’ or ‘1’ state in one cell forces the content of a second cell to a certain value, 0 or 1

3. Coupling Fault Model (CF) Model

i. State Coupling Fault (SCF)

- 0 in cell *a* sets the content of the cell *v* to be 0



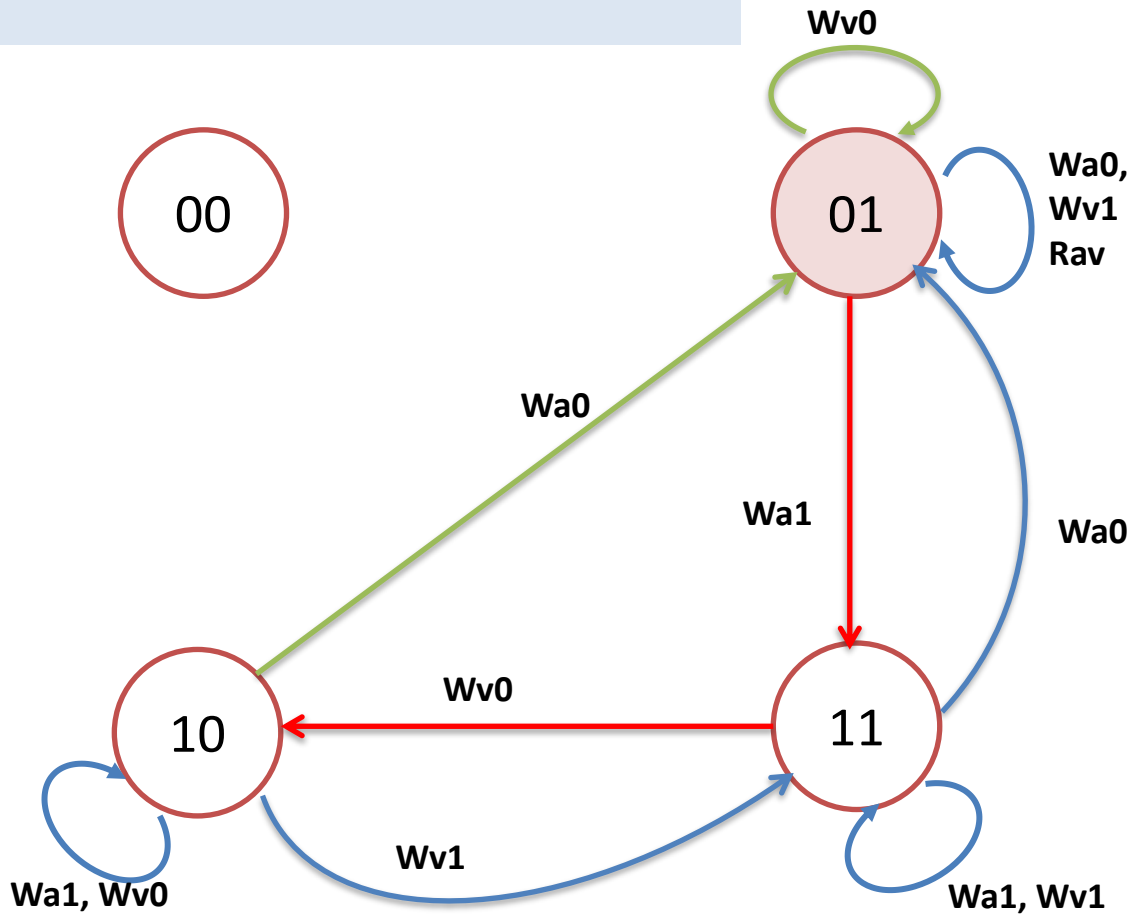
General Memory Fault Modeling

3. Coupling Fault Model (CF) Model

i. State Coupling Fault (SCF)

- 0 in cell *a* sets the content of the cell *v* to be 0
- **0 in cell *a* sets the content of the cell *v* to be 1**

Read v – Then v should have been read as 0 but the output is going to 1

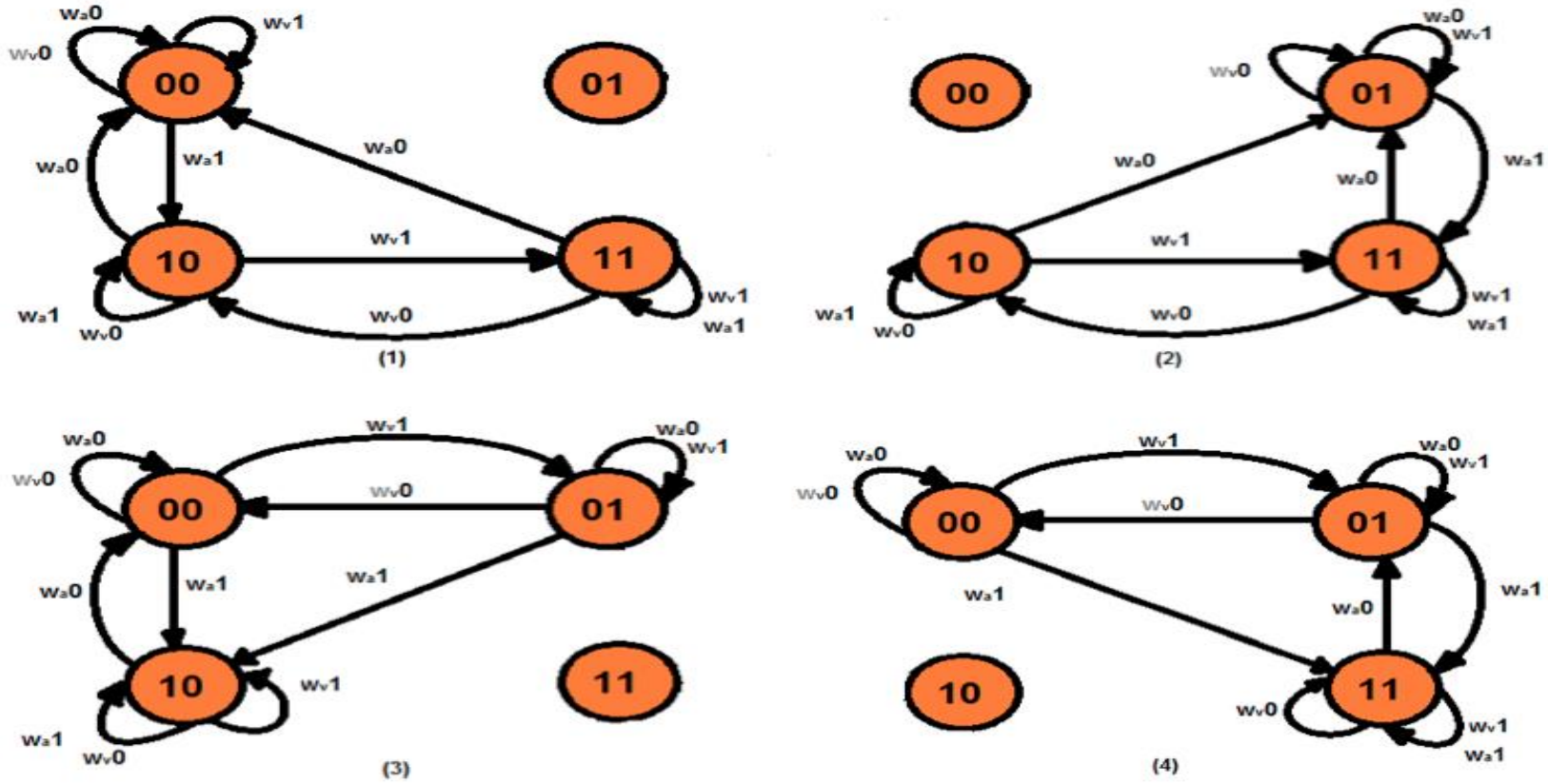


Memory Testing

General Memory Fault Modeling

3. Coupling Fault Model (CF) Model

i. State Coupling Fault (SCF)



3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

ii. Inversion Coupling Fault

- An upward (0 -> 1) or downward (1 -> 0) transition write operation in the Aggressor cell causes inversion in the victim cell (data in Victim Cell gets Inverter with .
- These faults are never being observed in a faulty memory cells and are just defined due to historical reasons [1]. Therefore, they are not included in the linked faults list.

Case a) Rising : < ↑ | ↕ > (Implying 0 to 1 change in cell *a* complements the content of cell *v*)

Case b) Falling : < ↓ | ↕ > (Implying 1 to 0 change in cell *a* complements the content of cell *v*)

Example : A '0' -> '1' transition in cell 'a' forces the content of a cell 'v' to Complement it's content i.e., If Cell 'v' is holding '0' will change to '1' or vica versa

Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

Memory Testing

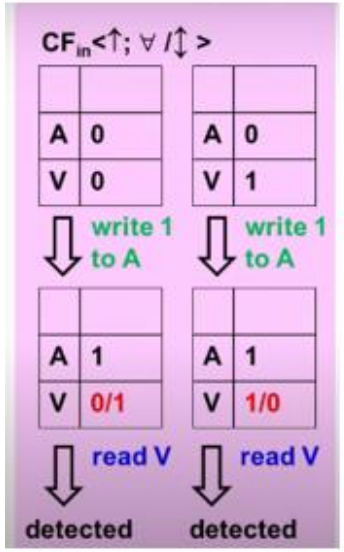
General Memory Fault Modeling

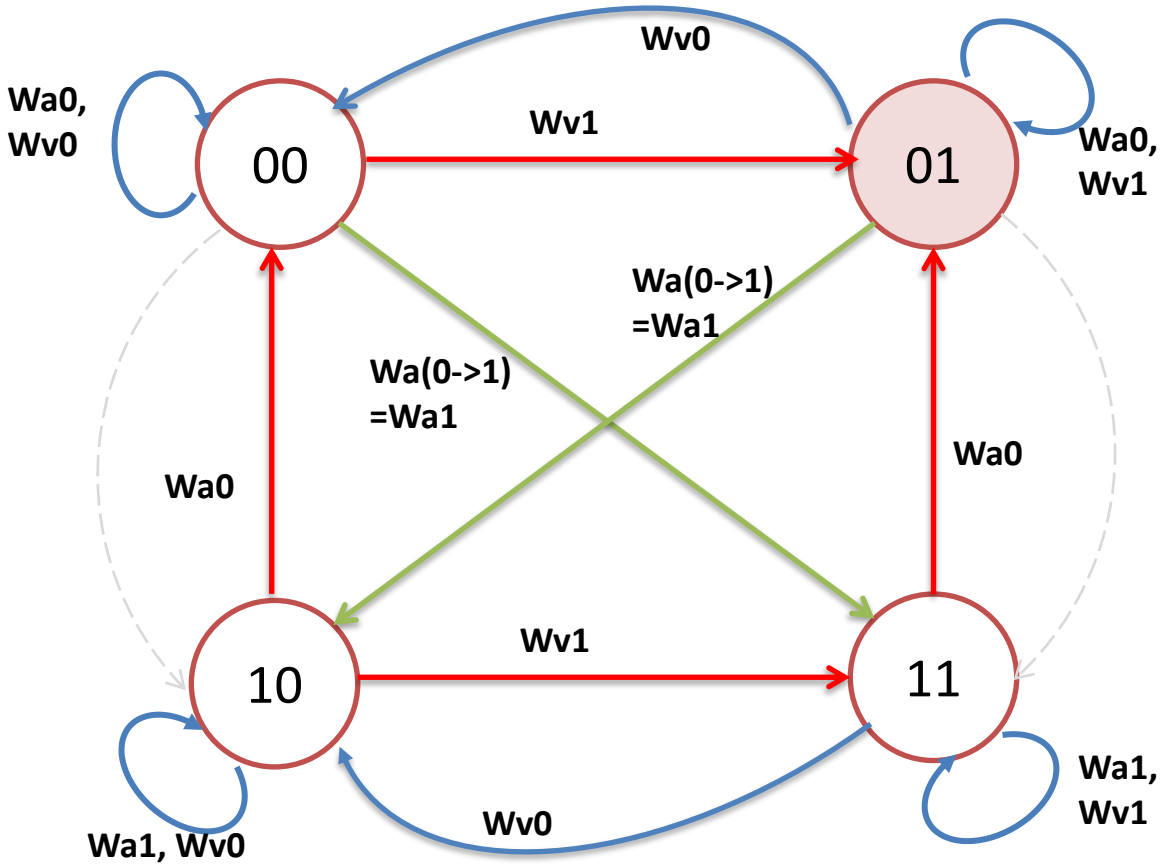
3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

ii. Inversion Coupling Fault

Case a) Rising : < ↑ | ↕ > (Implying 0 to 1 change in cell *a* complements the content of cell *v*)





Memory Testing

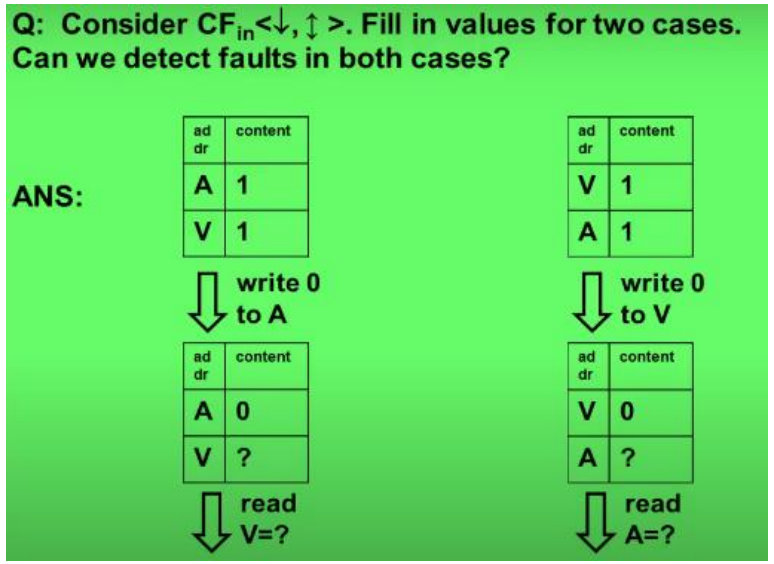
General Memory Fault Modeling

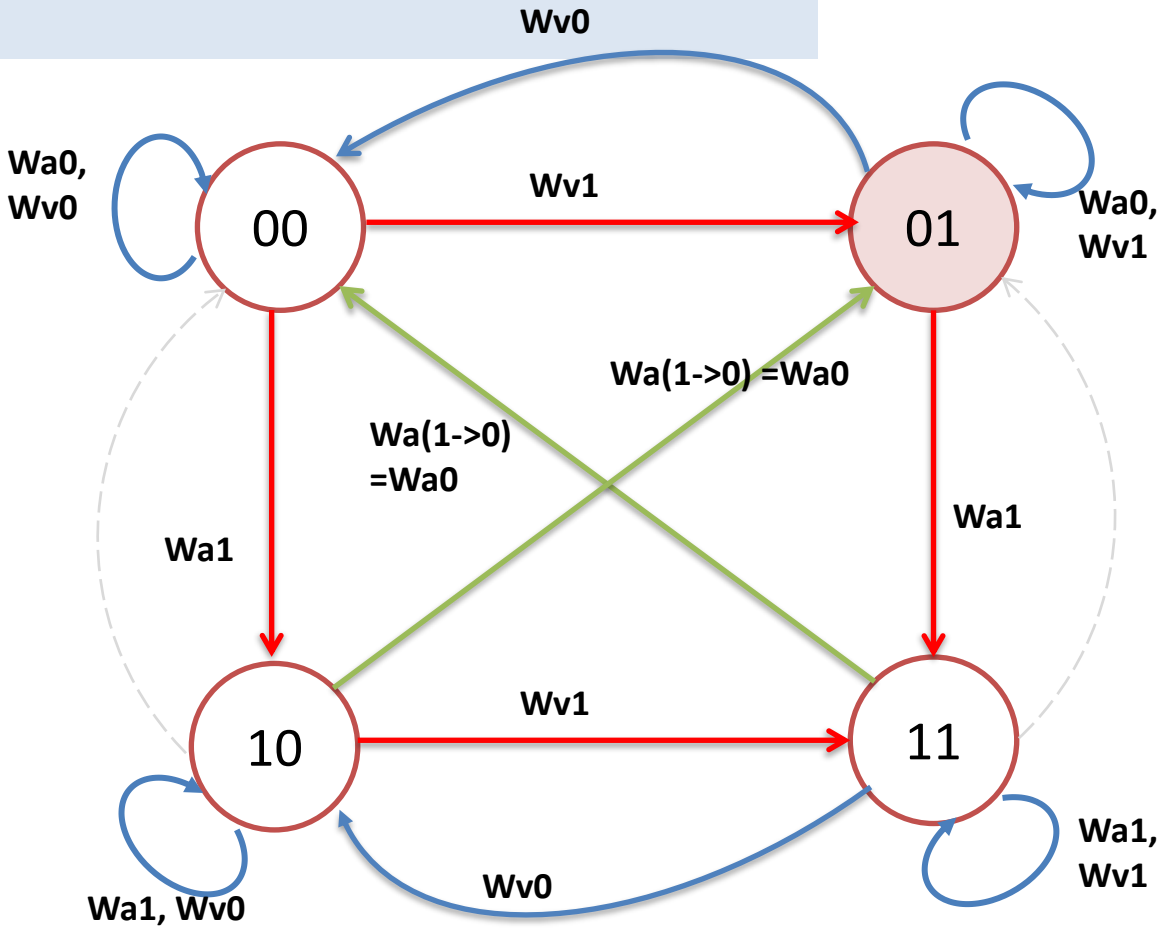
3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

ii. Inversion Coupling Fault

Case a) Falling : < ↓ | ↕ > (Implying 1 to 0 change in cell *a* complements the content of cell *v*)





3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

iii. Idempotent Coupling Fault

An upward (0->1)or downward (1->0) transition in the Aggressor cell forces the victim cell to '0' or '1'

Case a) Rising 0: < ↑ | 0 > 0 to 1 change in **cell 'a'** sets the content of **cell 'v'** to be 0.

Case b) Rising 1: < ↑ | 1 > 0 to 1 change in **cell 'a'** sets the content of **cell 'v'** to be 1.

Case c) Falling0: < ↓ | 0 > 1 to 0 change in **cell 'a'** sets the content of **cell 'v'** to be 0.

Case d) Falling1: < ↓ | 1 > 1 to 0 change in **cell 'a'** sets the content of **cell 'v'** to be 1.

General Memory Fault Modeling

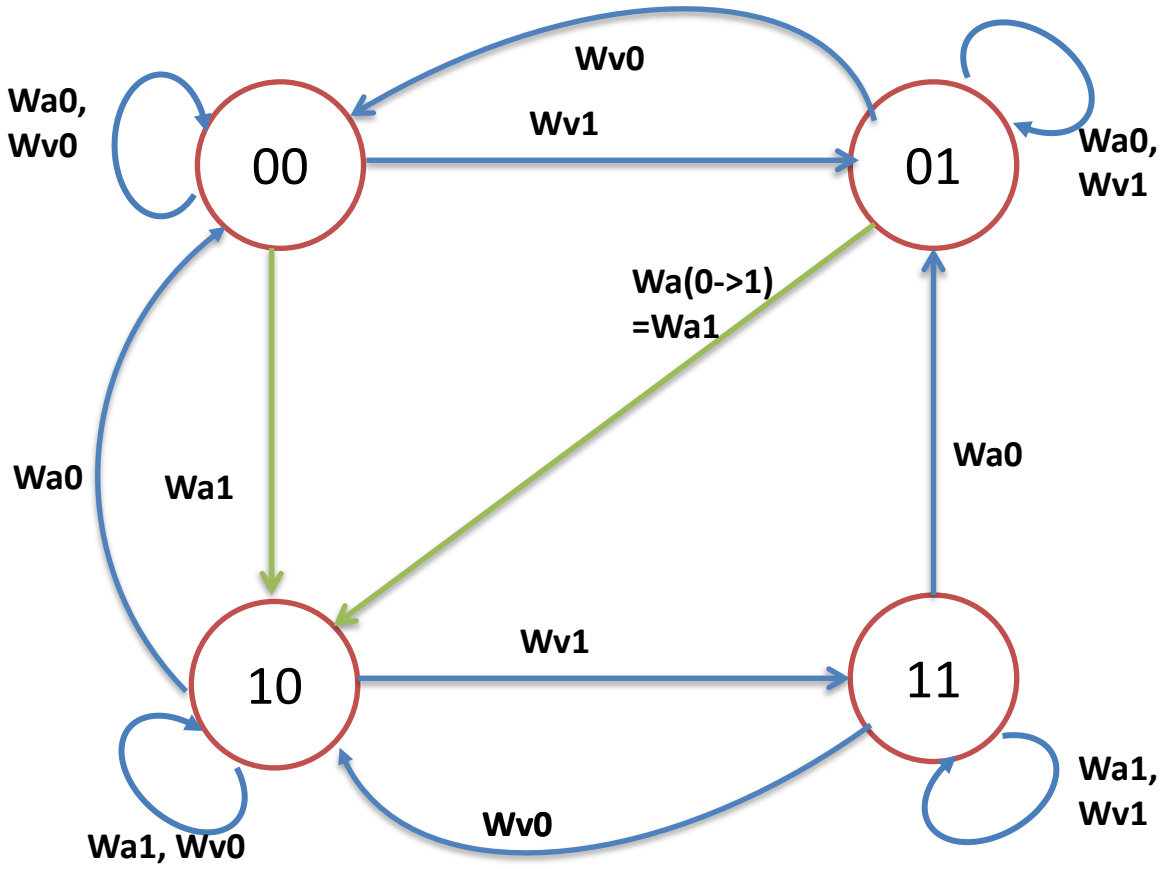
3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

iii. Idempotent Coupling Fault

Case a) Rising 0: < ↑ | 0 > 0 to 1 change in **cell 'a'** sets the content of **cell 'v'** to be 0.

An upward **(0->1) transition in the Aggressor** cell forces the **victim cell to '0'**



Memory Testing

General Memory Fault Modeling

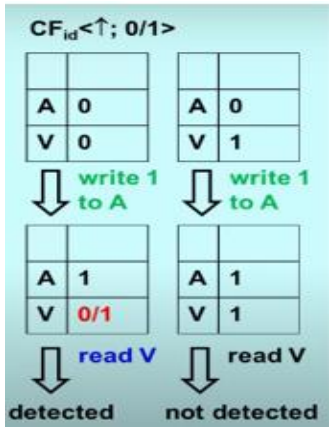
3. Coupling Fault Model (CF) Model

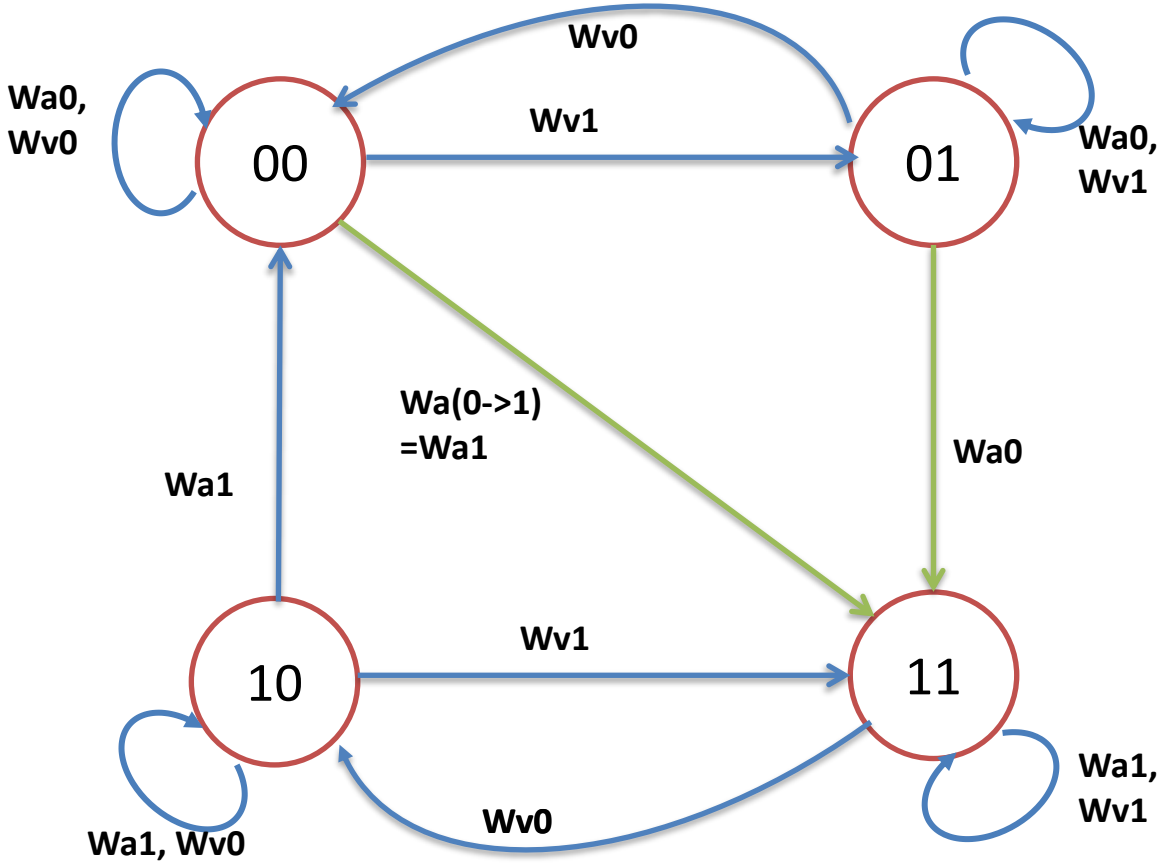
There are three types of Coupling faults

iii. Idempotent Coupling Fault

Case b) Rising 1: < ↑ | 1 > 0 to 1 change in **cell 'a'** sets the content of **cell 'v'** to be 1.

An upward **(0->1) transition in the Aggressor** cell forces the **victim cell to '1'**





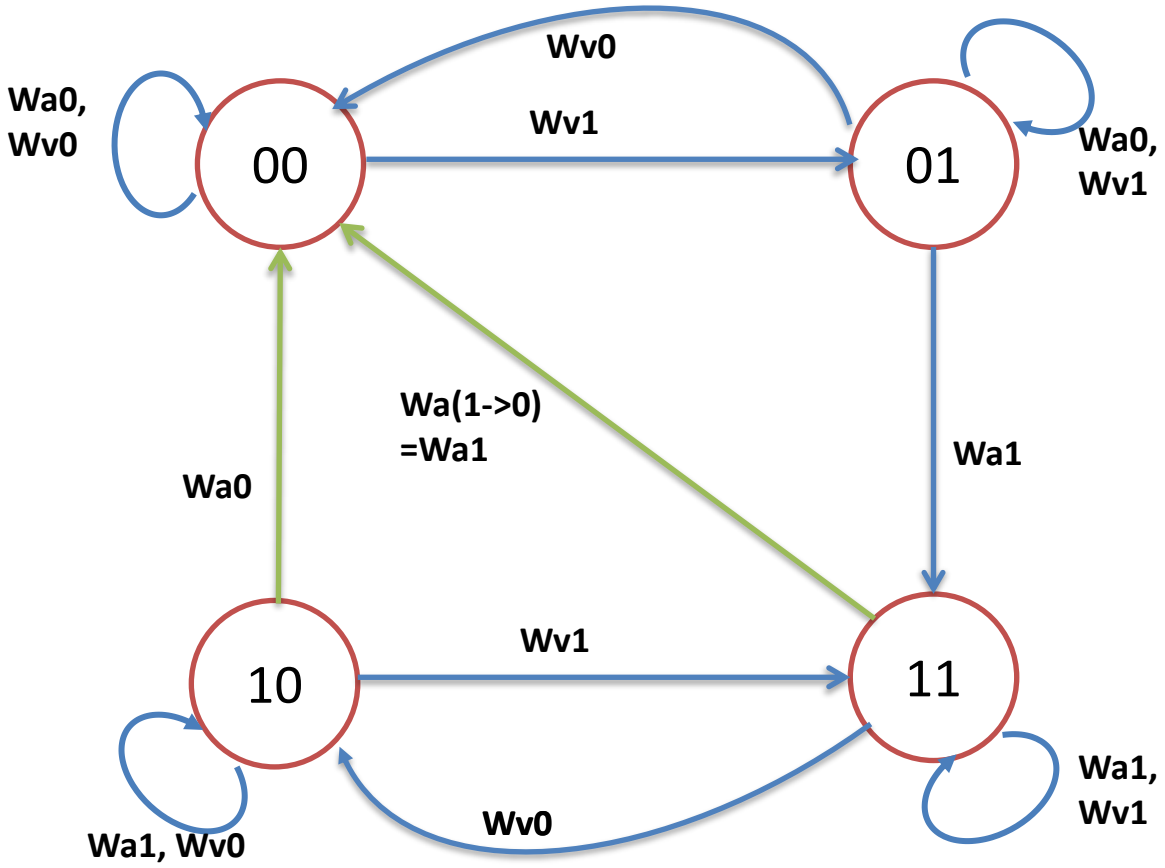
General Memory Fault Modeling

3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

iii. Idempotent Coupling Fault

Case C) Falling0: < ↓ | 0 > 1 to 0 change in **cell 'a'** sets the content of **cell 'v'** to be 0.



Memory Testing

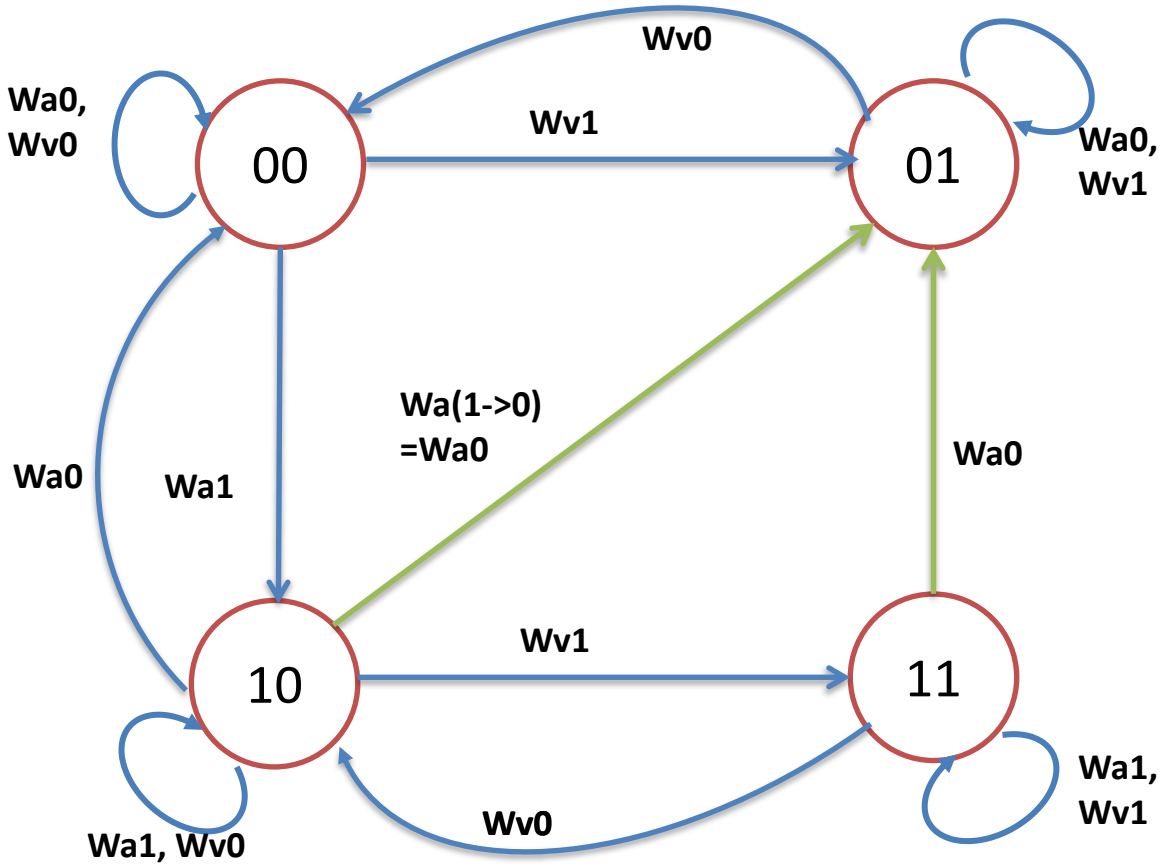
General Memory Fault Modeling

3. Coupling Fault Model (CF) Model

There are three types of Coupling faults

iii. Idempotent Coupling Fault

Case b) Falling1: < ↓ | 1 > 1 to 0 change in **cell 'a'** sets the content of **cell 'v'** to be 1.

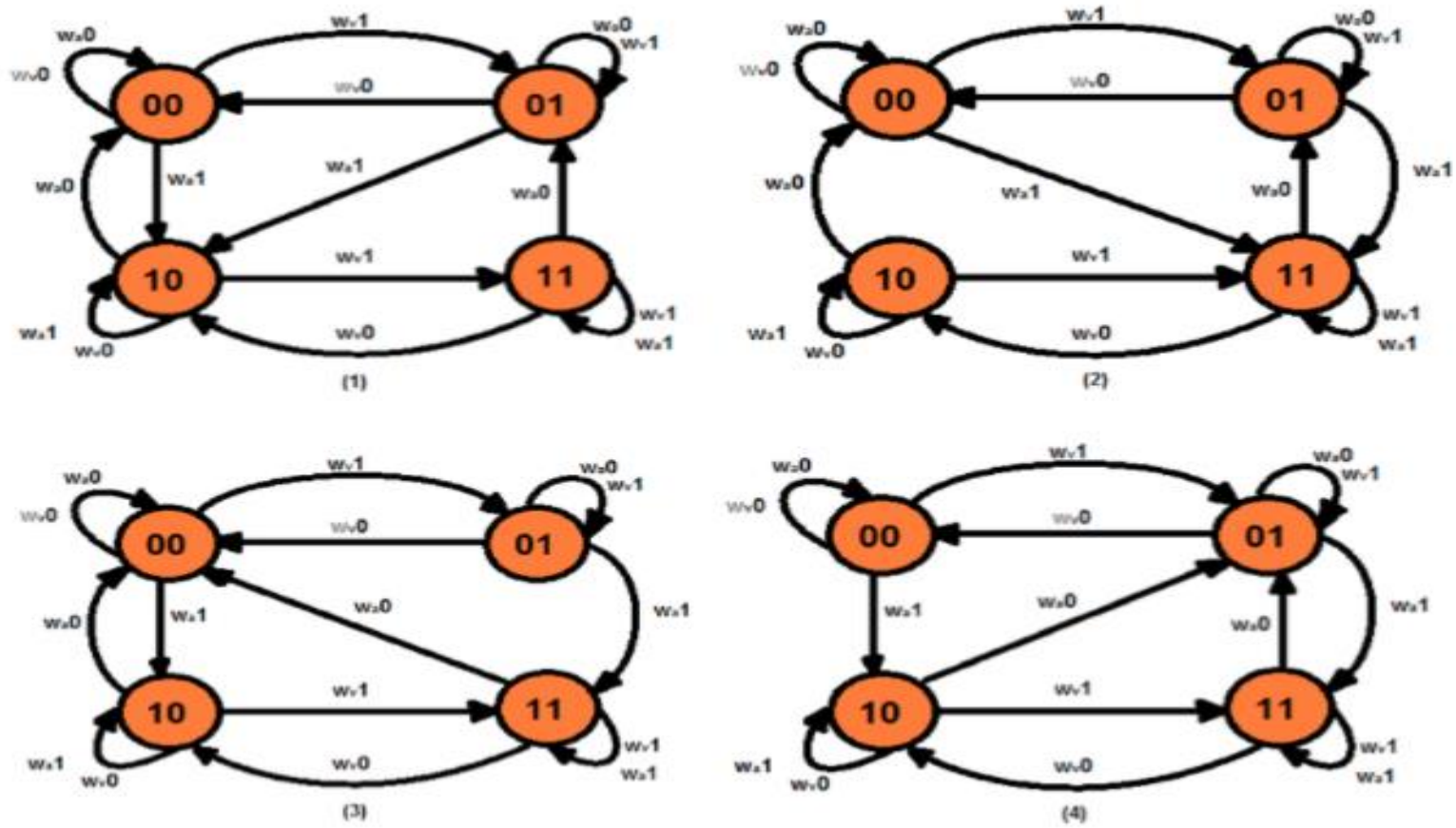


Memory Testing

General Memory Fault Modeling

3. Coupling Fault Model (CF) Model

iii. Idempotent Coupling Fault



Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

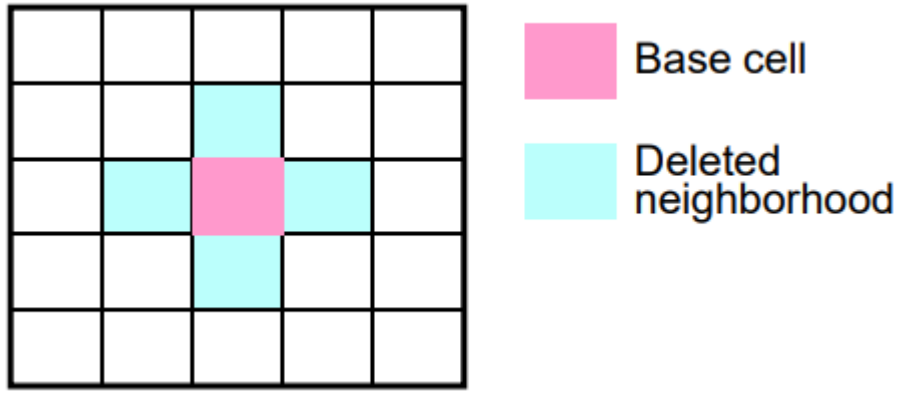
Memory Testing

General Memory Fault Modeling.

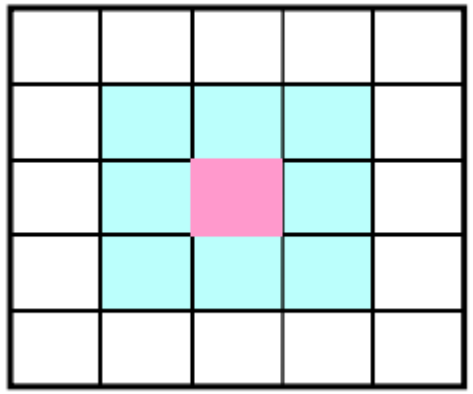
4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

- In this case a memory cell is dependent upon the cells in its neighborhood. Often times memories are described in terms of a nine cell neighborhood.
- The base cell in the center is surrounded by eight neighboring cells.
- The base cell could be dependent on all or a subset of the eight cells around it.
- Fault that occurs due to coupling of the cell under test with the pattern formed by neighborhood cells.
- Victim cell behaves incorrectly depending upon the value on adjacent cells.
- There are two types of Neighborhood
    i. Type 1 – Neighborhood
    ii. Type 2 – Neighborhood
- **The closest connections are between the base cell and those that are north, south, east, and west** but other diagonal interactions are possible.

Type 1 – Neighborhood



Type 2 – Neighborhood



Memory Testing

General Memory Fault Modeling.

4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

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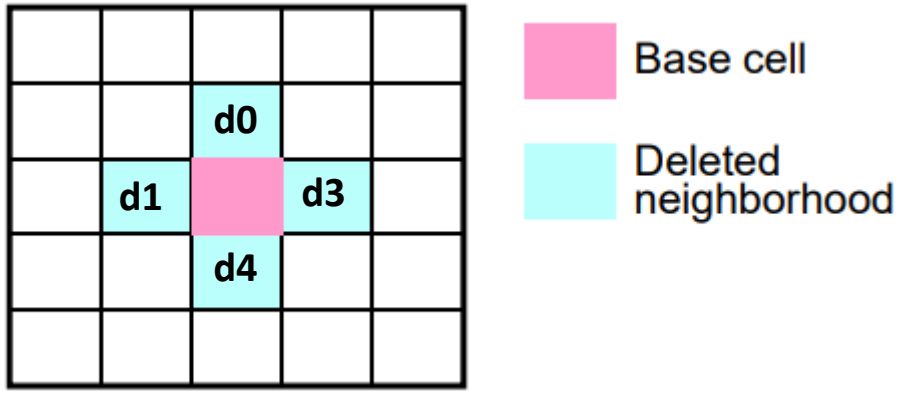
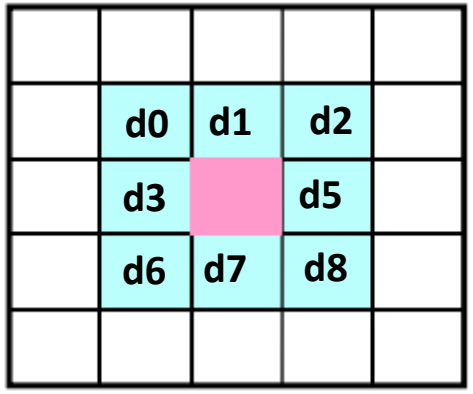


Type 1 – Neighborhood



Type 2 – Neighborhood

Memory Testing

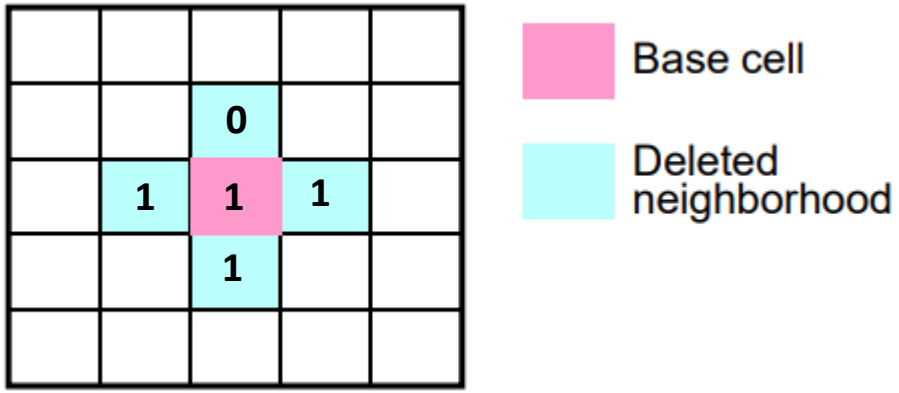
General Memory Fault Modeling.

4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

i. **Active NPSF (ANPSF):** $C_{i,j}$ <0, ↓, 1, 1; 0> and $C_{i,j}$ <0, ↓, 1, 1; ↕>

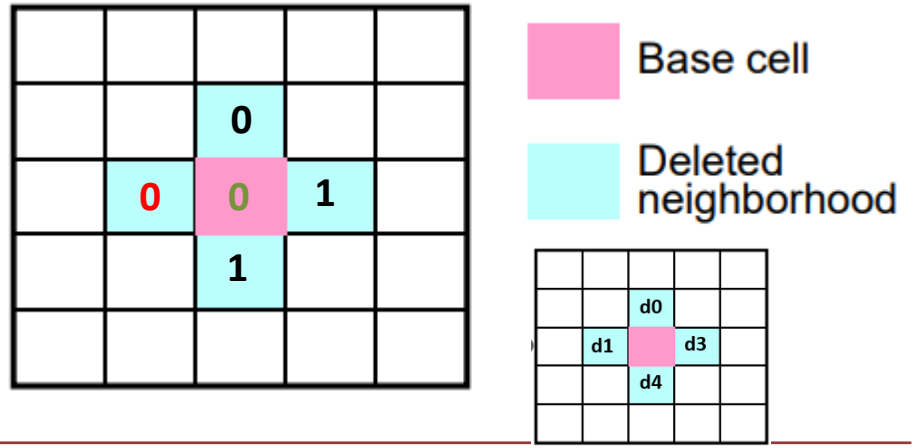
Transition in any Neighbourhood cell causes Inversion in the base cell

- ✓ Base Cell : Cell Under Test
- ✓ Deleted Neighborhood : Neighborhood without base cell
- ✓ An ANPSF is represented as Cij = (d0,d1,d3,d4 | b) where
- ✓ Cij is the value in the Cell under test
- ✓ (b0,b1,b3,b4) – Represent the values in the Neighboring cells 0,1,3,4 respectively (In one of the cell changes)
- ✓ b – Fault effect in the cell under test



Example1: 1 < 0, ↓, 1 ,1 | 0 >

It indicates that, the Cell under test has the Initial value 1 and Neighborhood cells (d0,d1,d3,d4) =(0,1,1,1) .The pattern by the Neighboring cells is (0, ↓, 1 ,1) = (0, 0, 1, 1) i.e., b1 having transition from 1-> 0 (Activity in Neighboring Cells) has a Fault effect at the cell under test i.e., Base Cell has changed from 1-> 0.



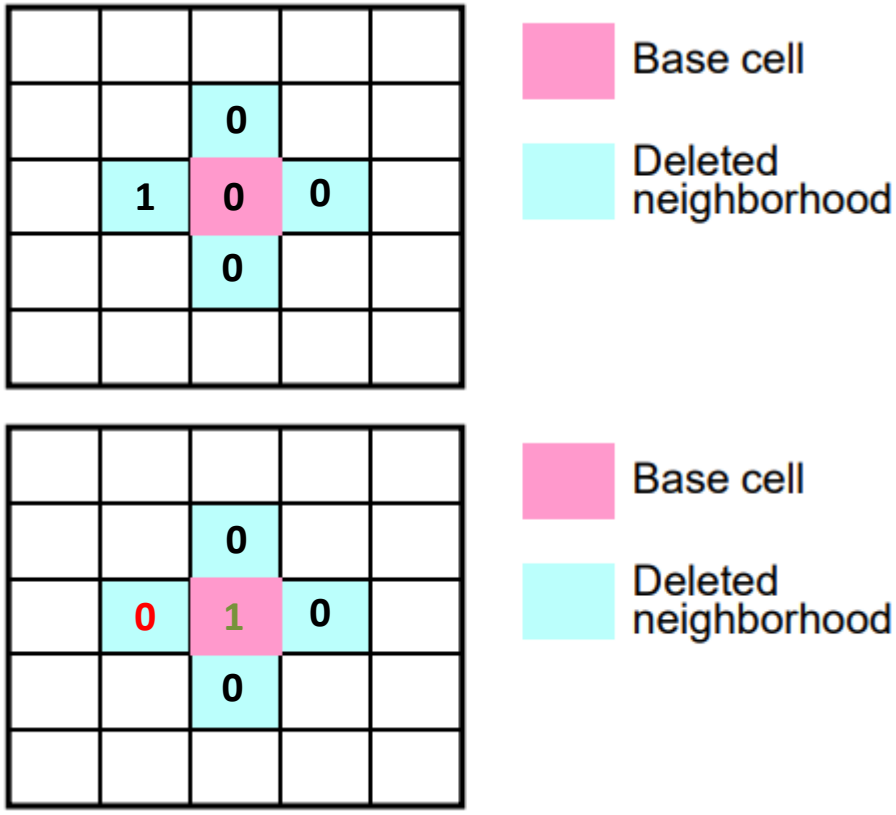
Memory Testing

General Memory Fault Modeling.

4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

i. **Active NPSF (ANPSF):** $C_{i,j}$ <0, ↓, 1, 1; 0> and $C_{i,j}$ <0, ↓, 1, 1; ↕>

- ✓ Base Cell : Cell Under Test
- ✓ Deleted Neighborhood : Neighborhood without base cell
- ✓ An ANPSF is represented as Cij = (b0,b1,b3,b4 | b) where
- ✓ Cij is the value in the Cell under test
- ✓ (b0,b1,b3,b4) – Represent the values in the Neighboring cells 0,1,3,4 respectively (In one of the cell changes)
- ✓ b – Fault effect in the cell under test



Example2: 0 < 0, 1, 0 ,0 | 0 > and 0 < 0, ↓, 0 ,0 | 1>
It indicates that, the Cell under test has the Initial value 0 and Neighborhood cells (b0,b1,b3,b4) =(0,1,0,0) .The pattern by the Neighboring cells is (0, ↓, 0 ,0) = (0, 0, 0, 0) i.e., b1 having transition from 1-> 0 (Activity in Neighboring Cells) has a Fault effect at the cell under test i.e., Base Cell has changed from 0-> 1.

Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

Memory Testing

General Memory Fault Modeling.

4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

Active NPSF (ANPSF):
Condition to detect the fault: Each base cell must be read in state '0' and state '1' for all possible deleted neighborhood pattern changes.

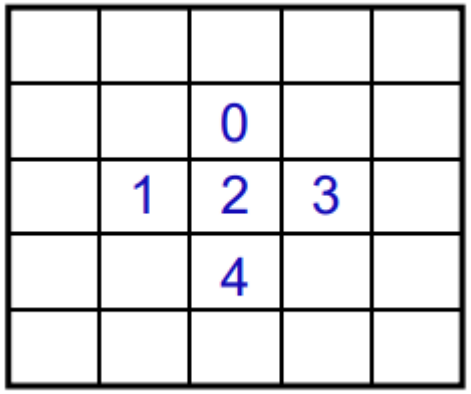
Cij (b0,b1,b3,b4 | b) – Possibility because pattern generated due to changes in b4
0 (0,0,0,1 | b) - **Pattern (0,0,0, ↓)** If Base Cell is Read as **state '0' , It means No fault else there is Fault in base cell**

0 (0,0,0,0 | b) - **Pattern (0,0,0,↑)** If Base Cell is **Read as state '0'** , It means **No fault** else there is **Fault in base cell**

1(0,0,0,1 | b) - **Pattern (0,0,0, ↓)** If Base Cell is Read as state '1' , It means No fault else there is Fault in base cell

1(0,0,0,0 | 1) - **Pattern (0,0,0,↑)** If Base Cell is Read as state '1' , It means No fault else there is Fault in base cell

Type 1 – Neighborhood



Memory Testing

General Memory Fault Modeling.

4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

2) Passive NPSF (PNPSF):

- **PNPSF implies that a certain neighborhood pattern prevents the cell under test from changing the values.**
- A PNPSF is represented by Cij (< b0,b1,b3,b4> | b) where Cij is the cell under test, < b0,b1,b3,b4> represents the values in the neighboring cells and b represents fault effect in the cell under test Cij.
- There are two types of b-PNPSF
  1. ↑ | 0; Cell under test can not be changed from 0->1 (Initial value of Cell under test is 0)
  2. ↓ | 1; Cell under test can not be changed from 1->0 (Initial value of Cell under test is 1)

Memory Testing

General Memory Fault Modeling.

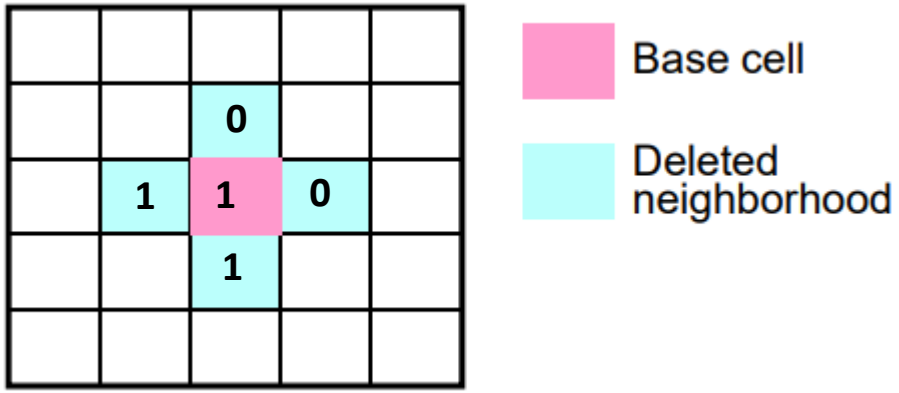
4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

2) Passive NPSF (PNPSF):

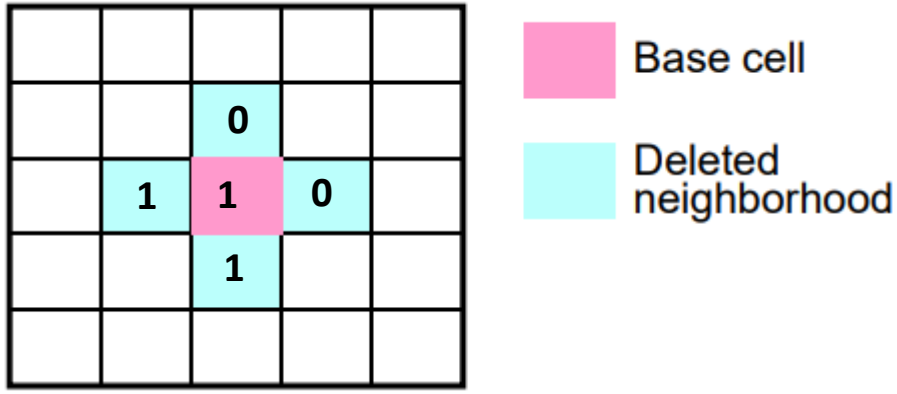
A certain neighborhood pattern prevents the victim cell from changing . It means , the

Example1: < 0, 1, 0, 1 ; ↓|1 > The victim cell is prevented from making a downward transition when the neighborhood cells have the pattern 0, 1, 0, 1

Example2: < 0, 0, 1, 1 ; ↑|0 > Condition to detect the fault: Each base cell must be written and read in state '0' and state '1' for all deleted neighborhood pattern permutations.



Writing '0' in Cell under test but, The Cell under test is Not changing ↓|1



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Memory Testing

General Memory Fault Modeling.

4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

Passive NPSF (ANPSF):
Condition to detect the fault: Each base cell **must be written and read in state '0'** and state '1' for all deleted neighborhood pattern permutations.

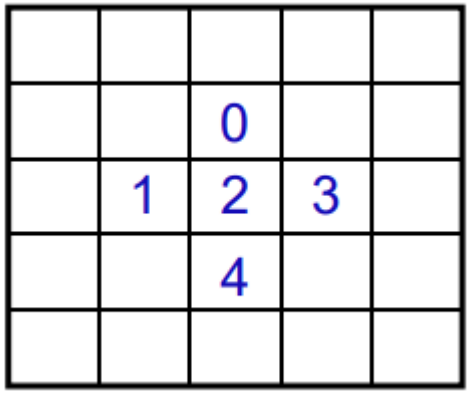
0 < 0, 0, 0, 0 ; ↑|? > ; Initially Cell is holding '0' ; Write 1 into Cell under test and then Read , If the Read Value is '1' means the Passive pattern <0,0,0,0> is NOT preventing the victim cell from changing

1 < 0, 0, 0, 0 ; ↓|? > ; Initially Cell is holding '1' ; Write 0 into Cell under test and then Read , If the Read Value is '0' means the Passive pattern <0,0,0,0> is NOT preventing the victim cell from changing

0 < 0, 0, 0, 1 ; ↑|? > ; Initially Cell is holding '0' ; Write 1 into Cell under test and then Read , If the Read Value is '1' means the Passive pattern <0,0,0,0> is NOT preventing the victim cell from changing

1 < 0, 0, 0, 1 ; ↓|? > ; Initially Cell is holding '1' ; Write 0 into Cell under test and then Read , If the Read Value is '0' means the Passive pattern <0,0,0,0> is NOT preventing the victim cell from changing

Type 1 – Neighborhood



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Memory Testing

General Memory Fault Modeling.

4. Neighborhood Pattern Sensitive Coupling Fault (NPSF) Model.

3) Static NPSF:

- ✓ The victim cell is forced into a particular state when the deleted neighborhood contains a particular pattern.
- ✓ Due to **Neighborhood pattern around the victim cell value gets stuck to either 0 or 1.**

Ex. 1: Write '1', Let Neighboring pattern set < 0, 1, 0, 1 ; - |0 >
The victim cell is forced to the value '0' when the neighborhood cells have the pattern 0, 1, 0, 1. It is stuck at '0'
Ex. 2: Write '1', Neighboring pattern < 1, 1, 1, 1 ; - |0 >
The victim cell is forced to the value '0' when the neighborhood cells have the pattern 0, 1, 0, 1. It is stuck at '0'

Condition to detect the fault: Each base cell must be read in state '0' and state '1' for all deleted neighborhood pattern permutations

Memory Testing

Address Decoder Fault

Address decoder Faults (ADFs): Row and column decoder comprises the address decoder of a memory. From the context of memory testing four types of faults are considered in address decoder.

ADF1: Disconnect Address Fault

- With certain address no word can be accessed
- Reason: Open in the path to the memory element or stuck – at – fault in the logic

ADF2: Mis–directed address fault:

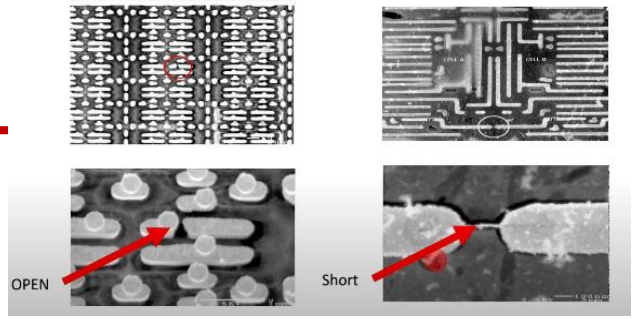
- No address from which a particular word can be accessed. i.e, Wrong location is accessed.
- Reason: Stuck – at – fault in the logic

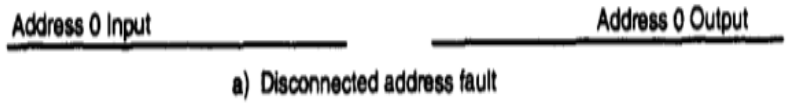
ADF3: Multiple select address fault:

- With certain address multiple words can be accessed simultaneously.
- Reason: Bridging short in the path to the memory element

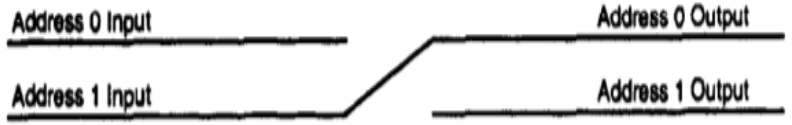
ADF4: Multiple selected cell fault:

- A certain word can be accessed with multiple addresses. i.e., Multiple addresses select a single cell.
- Reason: Bridging short in the path to the memory element

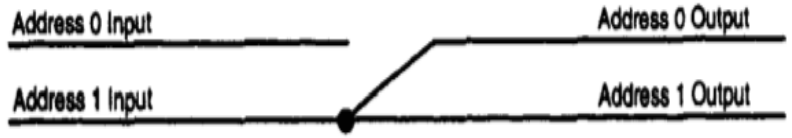




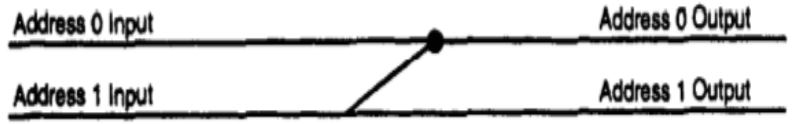
a) Disconnected address fault



b) Mis-directed address fault



c) Multiple select address fault



d) Multiple selected cell fault

Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

Memory Testing
Static decoder faults

- Static decoders have specific faults of their own.
- **A static decoder with more than 2 inputs can have an open fault which may go unnoticed**.
- A NAND gate with an open on PFET , Since PFET is defective and cannot pull the output high, one would think that this defect could then be detected.
- A NAND gate with an open on PFET shown below that can easily be missed (remain un noticed) during test.

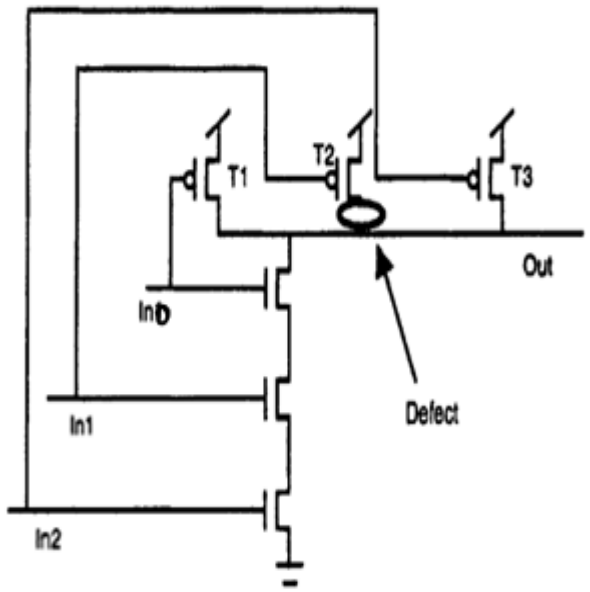


Table 8-2. Incrementing addresses with a static decoder open defect.

	In2	In1	In0	Out
1	0	0	0	1
2	0	0	1	1
3	0	1	0	1
4	0	1	1	1
5	1	0	0	1
6	1	0	1	~1
7	1	1	0	1
8	1	1	1	0

In fact the output remains high **due to capacitance on the node** thereby masking the defect from detection.

Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

Memory Testing
Static decoder faults

- To detect this type of defect the output must be set up to transition from low to high as a function of each pull-up PFET. (Every Address Generation should be followed by address input (111)
- **A NOR gate has the same susceptibility to static decoder open**s however the possible opens are in the NFET pull-down path instead of the PFET pull-up path.
- The same type of defects can **impact a dynamic decoder but they are easily detected and require** no special testing.
- **Since a dynamic decoder pre-charges in one direction and then evaluates in the other direction each cycle, an output node cannot be erroneously held at a value due to capacitive mechanisms**

Memory Testing

Circuit Dependent Fault

There are 4 different types of Circuit Dependent Faults

1. Read Disturb Fault
2. Pre-charge Faults
3. False Write Through
4. Data Retention Faults

Memory Testing

Circuit Dependent Fault

There are 4 different types of Circuit Dependent Faults

1. **Read Disturb Fault**

The Markov diagrams for different read disturb fault models

a) Good memory cell

r0(0) implies a Read 0 operation returns a 0

r1(1) implies a Read 1 operation returns a 1

The cells retain their original states after the Read

Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

Memory Testing

Circuit Dependent Fault

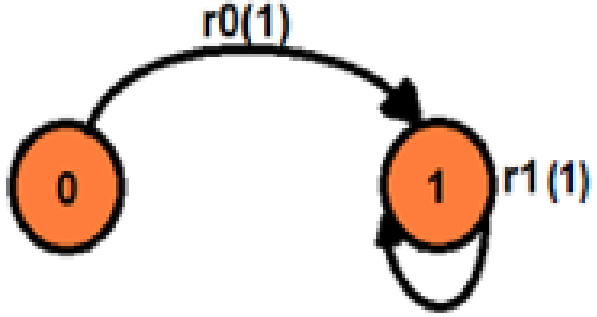
There are 4 different types of Circuit Dependent Faults

1. Read Disturb Fault

The Markov diagrams for different read disturb fault models

b) Deceptive (Misleading) Read Disturb Fault : It may disturb late in the cycle, with the Correct data is placed in the sense amplifier but incorrect data is retained in the cell.

There are two types of read destructive faults:



Memory cell in state 0, read 0 on it. Cell becomes 1 [r0(1)]

Memory cell in state 1, read 1 on it. Cell becomes 0 [r1(0)].

Memory Testing

Circuit Dependent Fault

There are 4 different types of Circuit Dependent Faults

1. Read Disturb Fault

The Markov diagrams for different read disturb fault models

c) Incorrect read Faults (IRFs): A read operation is performed to the cell returns an incorrect value, while the state of the memory cell is not changed.

There are two types of read destructive faults:

Let, Memory cell in state 0, read 0 on it.
Cell remains 0 but read operation returns 1.

Let, Memory cell in state 1, read 1 on it.
Cell remains 1 but read operation returns 0.

Memory Testing
Circuit Dependent Fault

There are 4 different types of Circuit Dependent Faults

1. **Read Disturb Fault**

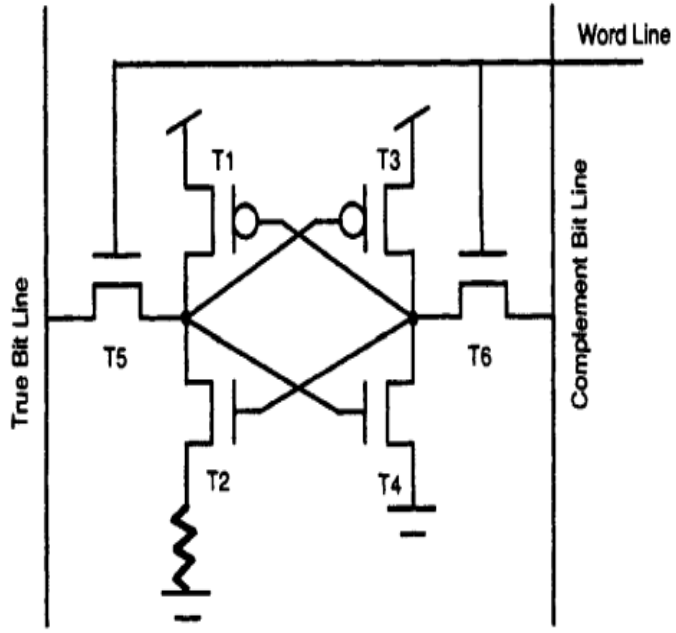
Example:

Case 2: Highly resistive contact to the ground node through the source of T2:

Depending on the defect resistance, this fault can be classified into 3 ranges.

1) **Low defect resistance:** there is a certain amount of resistance tolerable in which Normal operation can continue to occur
2) **Medium defect resistance:** It may disturb late in the cycle, with the Correct data is placed in the sense amplifier but incorrect data is retained in the cell.
    - Referred to as **'Deceptive Read disturb' or 'Deceptive destructive Read'**
    - Deceptive read disturb region where in the cell is disturbed but it is not detected until the next Read operation

3) Large defect resistance: There is a range of resistance that causes the **cell to flip immediately, which is then read as the wrong value on the first read.**



Memory Testing

Circuit Dependent Fault

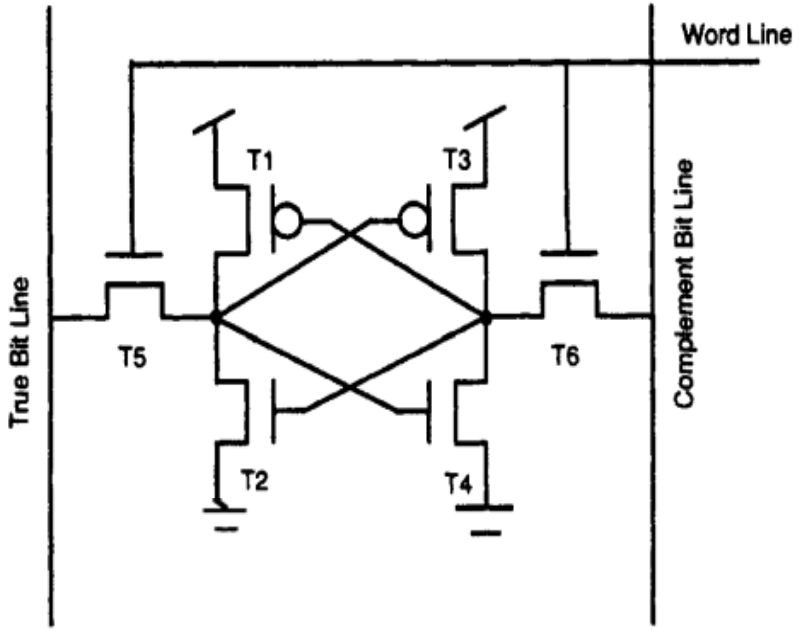
There are 4 different types of Circuit Dependent Faults

1. **Read Disturb Fault**

- ✓ An SRAM has a non-destructive read operation (Read does not destroy the Cell content.
- ✓ There are defects that cause a cell to lose its data during a read.

Example:

Conventional READ Operation: Assume Q=0, Q'=1, BLs are pre-charged to Vdd and WL is made HIGH. When a read is performed, charge is pulled off of the bit line and sunk into the cell. The bit line is pulled low through the Access NMOS and the pull-down NMOS, numbered T5 and T2 respectively.



Memory Testing

Circuit Dependent Fault

There are 4 different types of Circuit Dependent Faults

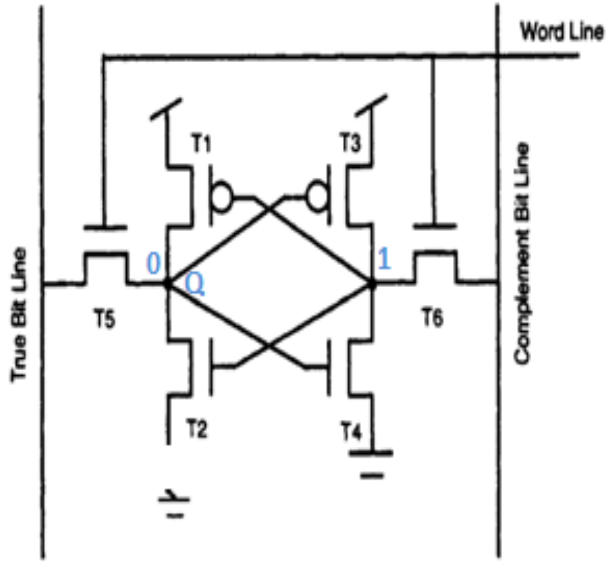
1. **Read Disturb Fault**
   - ✓ An SRAM has a non-destructive read operation (Read does not destroy the Cell content.
   - ✓ There are defects that cause a cell to lose its data during a read.

Example:

Case1: When there is no contact to the ground node through the source of T2,

the cell will flip on a read operation. A defect like this turns the memory element into a **dynamic cell**, which temporarily stores a state but which cannot be read. In other words, this defective SRAM loses its data state on a read.

A defect free DRAM loses it data state on a read, there is a write back operation at the end of a cycle to restore a cell's data after a read. No such write-back operation occurs at the end of an SRAM cycle.



Memory Testing

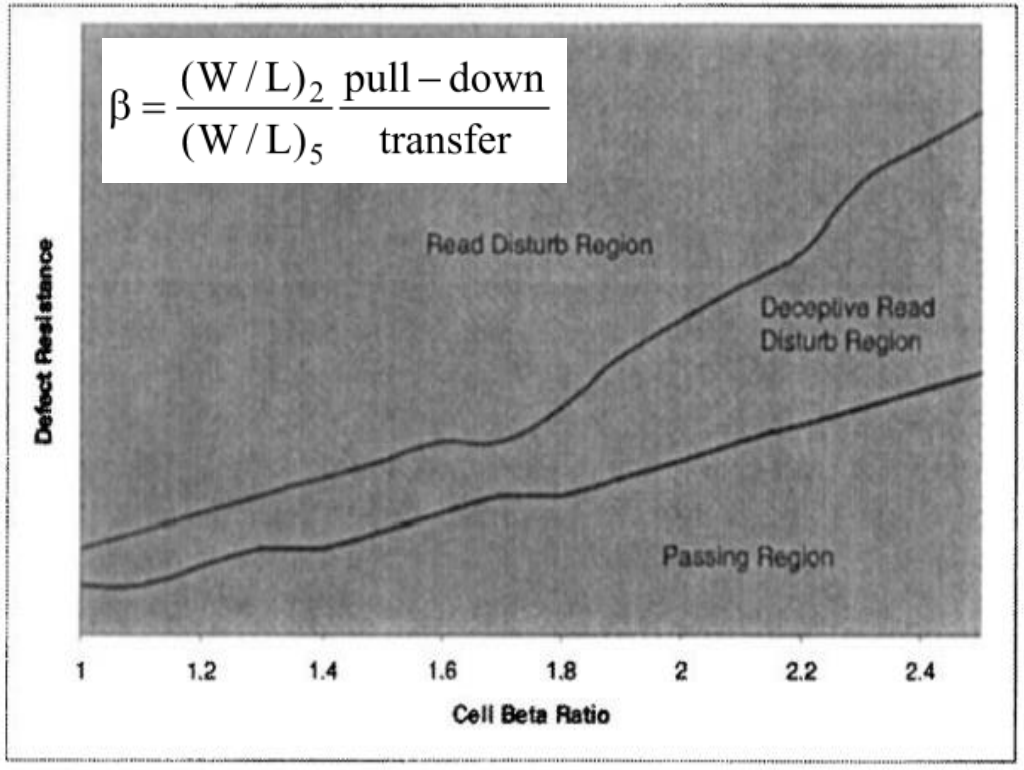
Circuit Dependent Fault

There are 4 different types of Circuit Dependent Faults

1. Read Disturb Fault

Example:

Case 2: Highly resistive contact to the ground node through the source of T2: Depending on the defect resistance, this fault can be classified into 3 ranges. These regions are illustrated by the graph



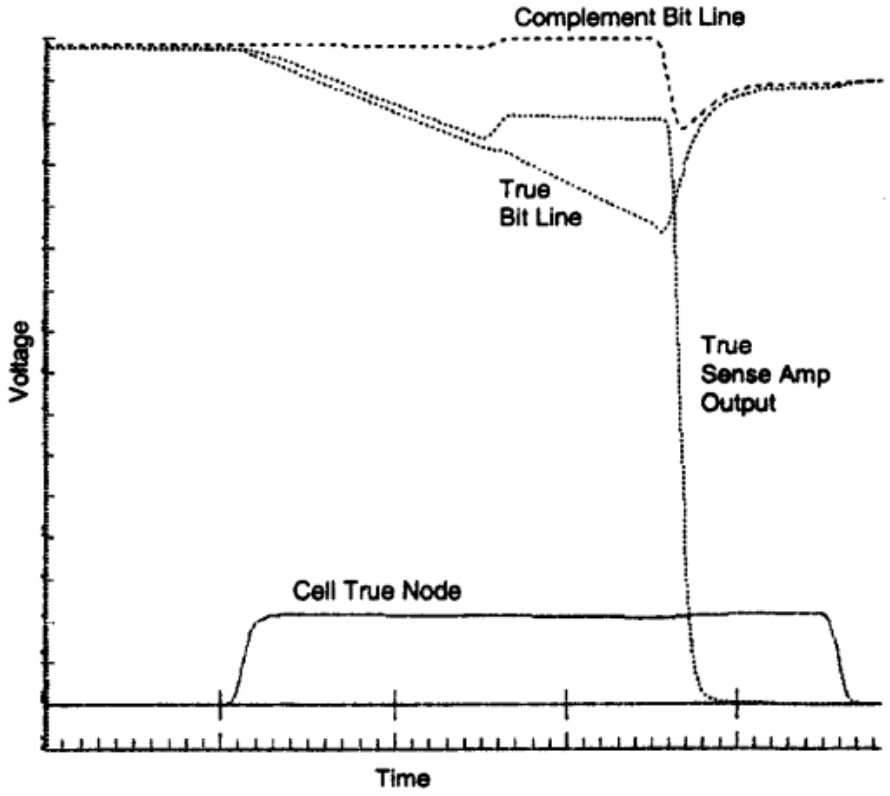
Higher the cell β ratio, that is, stronger the pull-down device, larger the tolerable resistance.

Memory Testing

Circuit Dependent Fault

2. Pre-charge Faults

- In a memory, it is possible to have a defect which causes the pre-charge circuitry not to operate.
  - ✓ One type of a **defect is a resistive pre-charge device.**
  - ✓ Another type of **defect is where the pre-charge devices do not turn on due to an open or due to a faulty control circuit** for the pre-charge devices.
- The impact of such a fault is that the bit lines do not pre-charge correctly.



Wave form of good working pre-charge circuit

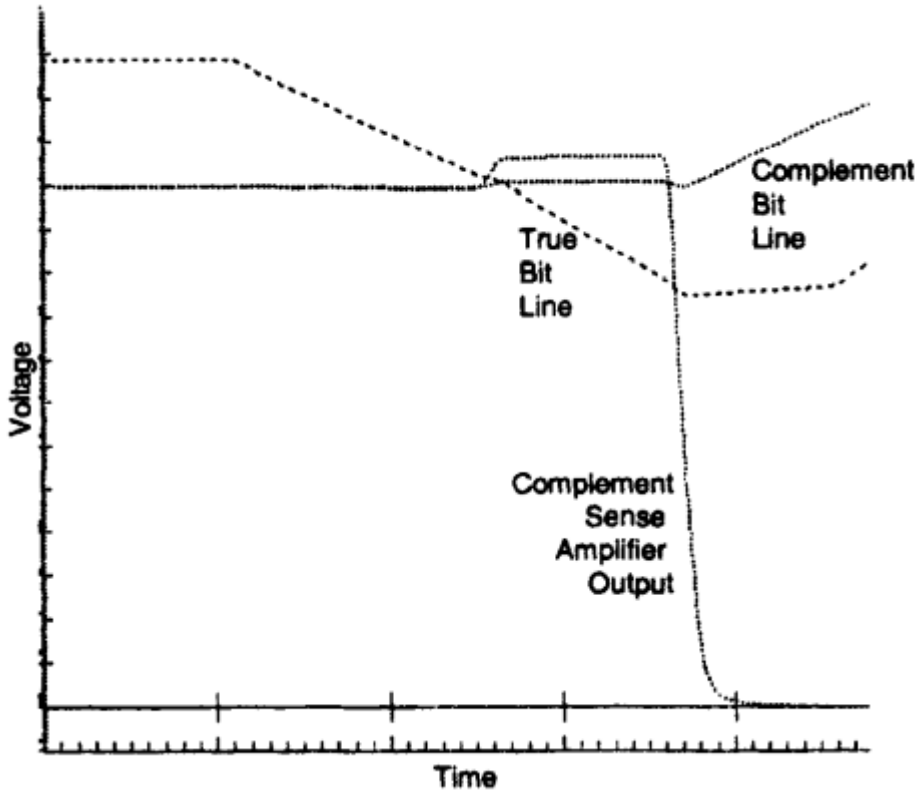
Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

Memory Testing

Circuit Dependent Fault

2. Pre-charge Faults

- The impact of such a fault is that the bit lines do not pre-charge correctly.
- A set of SRAM waveforms where the bit lines do not pre-charge correctly. As a result, one of the bit lines starts out significantly lower than the other bit line.
- **If a "0 is being read, the true bit line should be low. The complement bit line, however, starts out quite a bit lower than Vdd**. The result is that the **true bit line must discharge for a much longer period of time before it is actually lower than the complement one.** Thus, the incorrect value normally is read since the pre-charge circuit does not work correctly



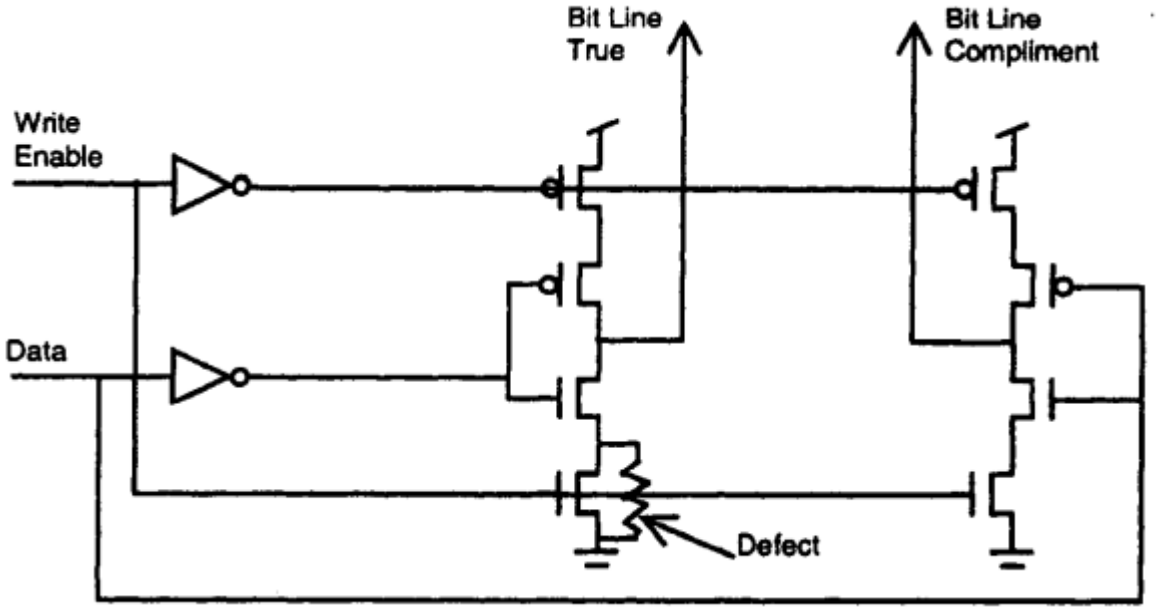
Waveforms resulting from a defective pre-chargc circuit

Memory Testing

Circuit Dependent Fault

3. False Write Through

- Defect on the Write Driver circuit.
- Causes the **data on the input of the write driver to be applied to the bit lines even when the write enable signal is low,** ie., during a Read operation.
- Depending on the **location of the defect either true or complement bit line may be pulled low causing an erroneous read**.
- The bit lines will be at an **incorrect value at the start of the Read operation**

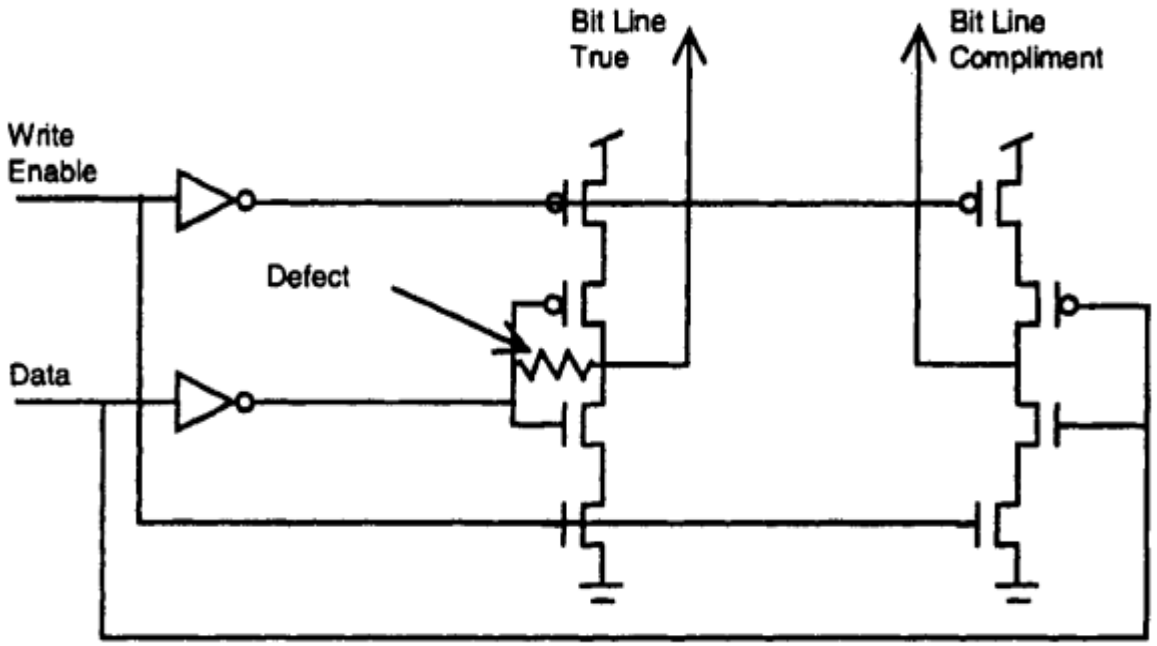


Memory Testing

Circuit Dependent Fault

3. False Write Through

- Second type of **defect on the write head which impacts the bit lines Data** on the write **head directly appears** on the bit lines.
- The possible defect sites may vary. Hence all data type combinations must be utilized in the data being read from the cells and the data input applied to the write head to detect the fault

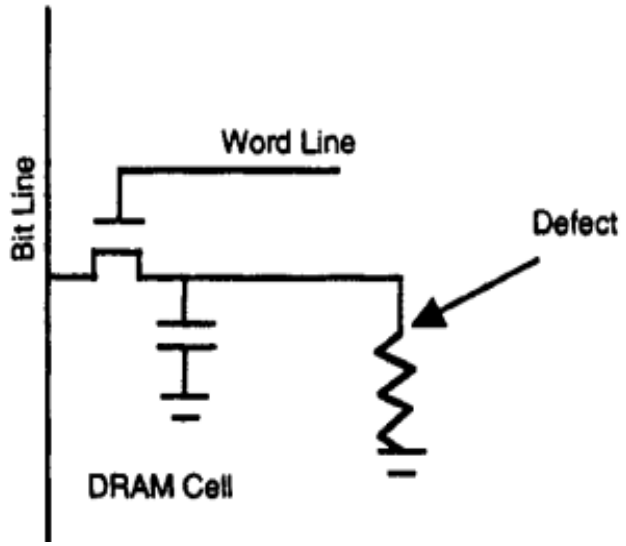


Memory Testing

Circuit Dependent Fault

4. Data Retention Faults

- The **defect resistance discharges the storage capacitor at a** faster rate than normal.
- In a DRAM cell, there is **an acceptable range of leakage within which the memory operates according to the specification.**
- Hence a pause of the order of 100ms is required to identify if the leakage is greater than normal. An SRAM cell can also have data retention fault with a variety of possible locations within the cell



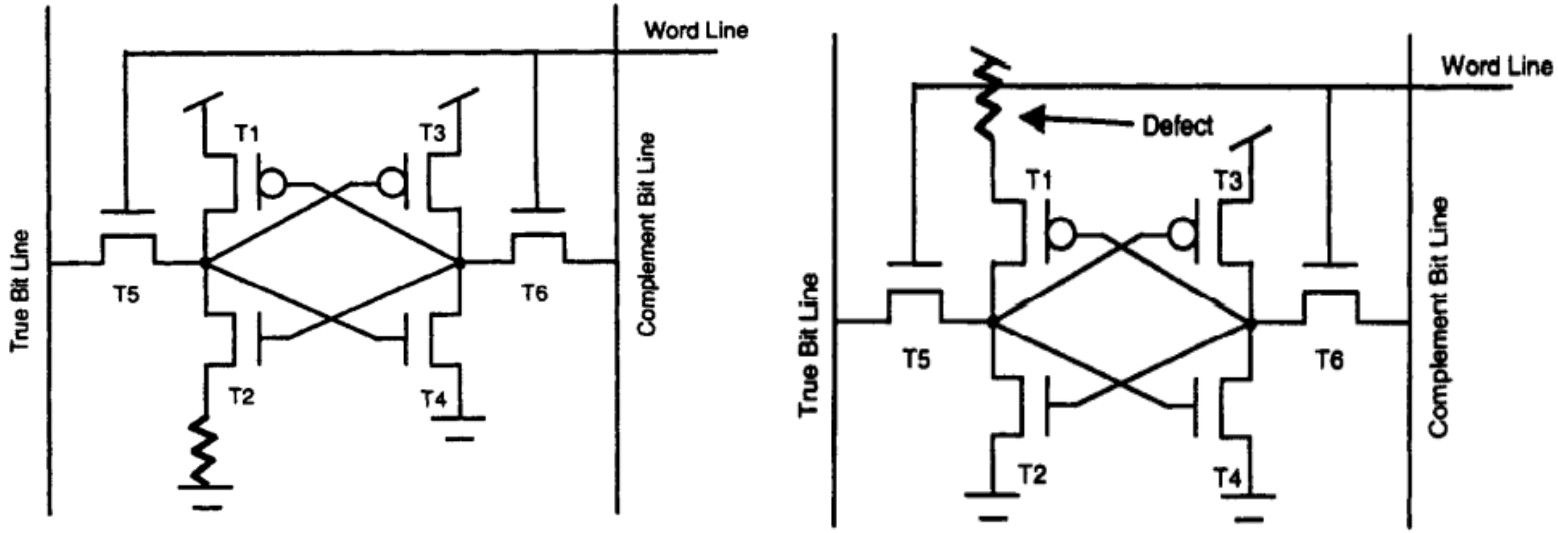
Reference :"High Performance Memory Testing: Design Principles, Fault Modeling and Self Test by R.Dean Adams, Kluwer Academic Publishers, 2003.

Memory Testing

Circuit Dependent Fault

4. Data Retention Faults

- Read disturb fault model is also a type of data retention fault occurring due to the defect in the pull-down path
- Another type of SRAM retention fault is caused by an open or highly resistive defect in the pull-up path
- Fault can be detected by performing multiple reads.



THANK YOU

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