Week 12: Assignment 12

The due date for submitting this assignment has passed.

Due on 2021-10-20, 23:59 IST.

As per our records you have not submitted this assignment.

1) State whether the statement given below is true or false. LeFLow enables flexible FPGA High-Level Synthesis of Tensor Flow Deep Neural Networks. ***1 point***

- True
- False

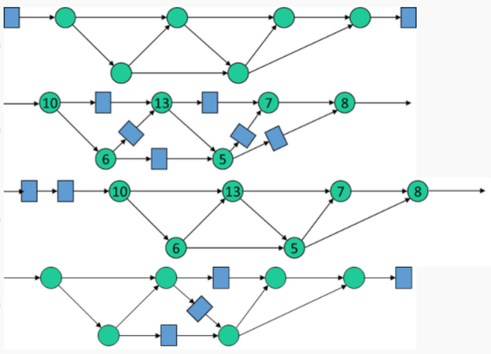
No, the answer is incorrect.
Score: 0
Accepted Answers:
True

2) State whether the statement given below is true or false. The biggest advantages of Halide are that it decouples the algorithm description of the program from the scheduling. ***1 point***

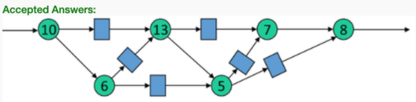
- True
- False

No, the answer is incorrect.
Score: 0
Accepted Answers:
True

3) Among four versions of a circuit, which one achieve fastest clock speed? The delay of the nodes are mentioned inside the nodes in options b and c. The delays are the same in all options. The circular nodes are combinational nodes and the rectangles are the registers. ***2 points***



No, the answer is incorrect.
Score: 0
Accepted Answers:

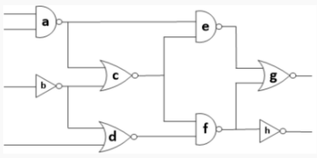


4) Which of the following statement is NOT true about folding transformation? ***1 point***

- Folding creates multiple synchronous clocks
- Folding increases register and MUX counts
- Folding of two functional units in series creates a feedback loop
- Folding of two functional units in parallel creates a feedback loop

No, the answer is incorrect.
Score: 0
Accepted Answers:
Folding of two functional units in parallel creates a feedback loop

5) Consider the following gate level design. Find the minimum 4 input LUTs required to implement it in FPGA? ***1 point***



- 1
- 2
- 3
- 4

No, the answer is incorrect.
Score: 0
Accepted Answers:
2

6) Let us assume that data path width is such that multiplier can be mapped to DSP block of FPGA. Which of the following statement is correct about DSP mapping? ***1 point***

S1: A multiplier with a pre-adder can be mapped to a single DSP.
S2: An accumulator for each multiplier cannot be mapped to a single DSP. The accumulator will be mapped to LUTs and the multiplier will be mapped to DSP block.

- S1
- S2
- S1 and S2
- None of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
S1

7) Which one of the following statements is NOT correct about Boolean functions? ***1 point***

- Boolean function can be implemented with only prime implicants.
- Essential prime implicant covers a minterm that is not covered by any other prime implicant.
- An irredundant cover is a cover that is not a proper superset of any cover.
- Don't care is an input combination that may or may not occur.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Don't care is an input combination that may or may not occur.

8) Which of the following statements are true? ***1 point***

S1: Retiming is polynomial time solvable problem
S2: Timing of a design can be improved by retiming
S3: Area of a design can be optimized by retiming

- S1, S2 and S3
- S1 and S2
- S1 and S3
- S2 and S3

No, the answer is incorrect.
Score: 0
Accepted Answers:
S1, S2 and S3

9) Which one of the following methods is Not used for two level logic minimization? ***1 point***

- Karnaugh Map
- Quine–McCluskey method
- ESPRESSO
- Algebraic Model

No, the answer is incorrect.
Score: 0
Accepted Answers:
Algebraic Model