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Week 6: Assignment 6

The due date for submitting this assignment has passed.

Due on 2025-09-03, 23:59 IST.

Assignment submitted on 2025-09-03, 21:58 IST

1) Which of the following options is correct with respect to the register binding problem in hierarchical sequence graph? ***1 point***

S1: Conflict graph is not an interval graph.

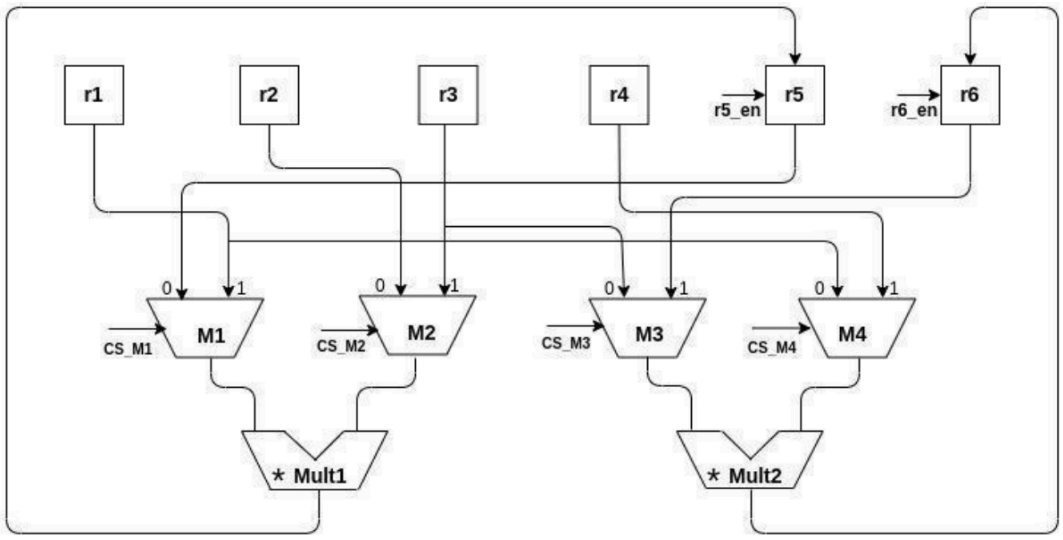
S2: The register binding problem remains NP Complete.

- Statement 1 is true; Statement 2 is false.
- Statement 1 is false; Statement 2 is true.
- Statement 1 is true; Statement 2 is true and 1 is a correct explanation for 2.
- Statement 1 is true; Statement 2 is true but 1 is not a correct explanation for 2.

Yes, the answer is correct.
Score: 1

Accepted Answers:
Statement 1 is true; Statement 2 is true and 1 is a correct explanation for 2.

2) For the data path given in the figure below: ***2 points***



The following operations are executed in the datapath in time step 1:

1. r5 = r1<Mult1>r2;
2. r6 = r6<Mult2>r4;

What would be the control assertion pattern for the operations in timestep 1 if the control assertion pattern order is: (CS_M1, CS_M2, CS_M3, CS_M4, r5_en, r6_en)

- 1, 1, 1, 1, 1, 1
- 1, 0, 1, 1, 1, 1
- 1, 0, 0, 1, 1, 1
- 1, 0, 1, 0, 1, 1

Yes, the answer is correct.
Score: 2

Accepted Answers:
1, 0, 1, 1, 1, 1

3) Considering the data path in the figure above, what would be the operations executed in the data path, if the control signal assignment is (0, 0, 1, 0, 1, 1) where the order of the control signal is CS_M1, CS_M2, CS_M3, CS_M4, r5_en, r6_en? ***1 point***

- r5 = r1 <Mult1> r2 and r6 = r3 <Mult2> r4
- r5 = r5 <Mult1> r2 and r6 = r6 <Mult2> r1
- r5 = r5 <Mult1> r3 and r6 = r6 <Mult2> r4
- r5 = r5 <Mult1> r2 and r6 = r3 <Mult2> r1

Yes, the answer is correct.
Score: 1

Accepted Answers:
r5 = r5 <Mult1> r2 and r6 = r6 <Mult2> r1

4) State whether the following statement is true/false with respect to the data path in the figure above. ***1 point***

S1: The data path interconnections are based on mux-based architecture.

- (•) True
- ( ) False

Yes, the answer is correct.
Score: 1
Accepted Answers:
True

5) Fill in the blanks with appropriate options. ***1 point***

Register allocation and binding problem can be solved using ___ in conflict graph and ___ in compatibility graph.

- (•) graph coloring; clique covering
- ( ) clique covering; graph coloring
- ( ) graph coloring; topological sort
- ( ) clique covering; topological sort

Yes, the answer is correct.
Score: 1
Accepted Answers:
graph coloring; clique covering

6) Consider the following scheduling behaviour: ***2 points***

Time - step 1: v3 = v1 + v2; v12 = v1

Time - step 2: v5 = v3 + v4; v7 = v3 * v6; v13 = v3

Time - step 3: v8 = v3 + v5; v9 = v1 + v7; v11 = v10/v5

Time - step 4: v14 = v11 & v8; v15 = v12 | v9

Consider we are binding the variables to register file/memory. Assume there is only one port available for memory binding. We want to map a subset of variables to register file/memory such that there won't be any access conflict. We should not map two variables into a single register file/memory if they are accessed at the same clock. Which of the following mapping of the variables to a register file/memory is/are correct?

M1: v2, v4, v10, v15
M2: v2, v6, v15, v13

- ( ) Only M1 is correct.
- ( ) Only M2 is correct.
- ( ) Both M1 and M2 are correct.
- (•) Both M1 and M2 are incorrect.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Only M1 is correct.

7) Consider the scheduling behaviour of the above question. ***1 point***

Consider we need to find the maximum number of variables to be stored through a fixed number of ports a. Choose the option representing the correct constraint formulation for time stamp 2 where bi is a boolean variable which takes value 1 when variable vi is mapped to a memory bank otherwise it takes value 0.

- b1 + b3 + b4 + b5 + b6 + b7 + b13 <= a
- b3 + b4 + b5 + b6 + b7 <= a
- b4 + b5 + b6 + b7 + b13 <= a
- b3 + b4 + b5 + b6 + b7 + b13 <= a

Yes, the answer is correct.
Score: 1

Accepted Answers:
b3 + b4 + b5 + b6 + b7 + b13 <= a

8) The register sharing problem is polynomial time solvable in case of hierarchical models with single function calls. The above statement is ***1 point***

- True
- False

No, the answer is incorrect.
Score: 0

Accepted Answers:
True

X

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Course outline

About NPTEL ()

How does an NPTEL online course work? ()

Prerequisite: Week 0 ()

Week1: Introduction to C-based VLSI Design ()

Week2: C-Based VLSI Design: Basic Scheduling ()

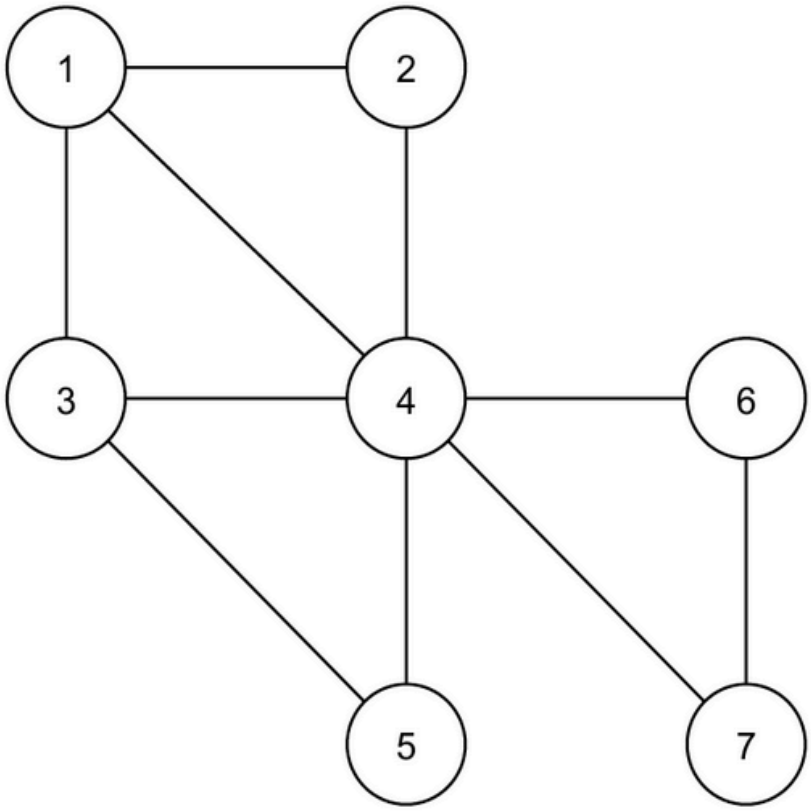
Week 5: Assignment 5

The due date for submitting this assignment has passed.

Due on 2025-08-27, 23:59 IST.

As per our records you have not submitted this assignment.

1) ***1 point***



G1

State whether the following statement is true/false with respect to graph G1.
S1: Graph G1 is not a chordal graph.

- True
- False

No, the answer is incorrect.
Score: 0

Accepted Answers:
False

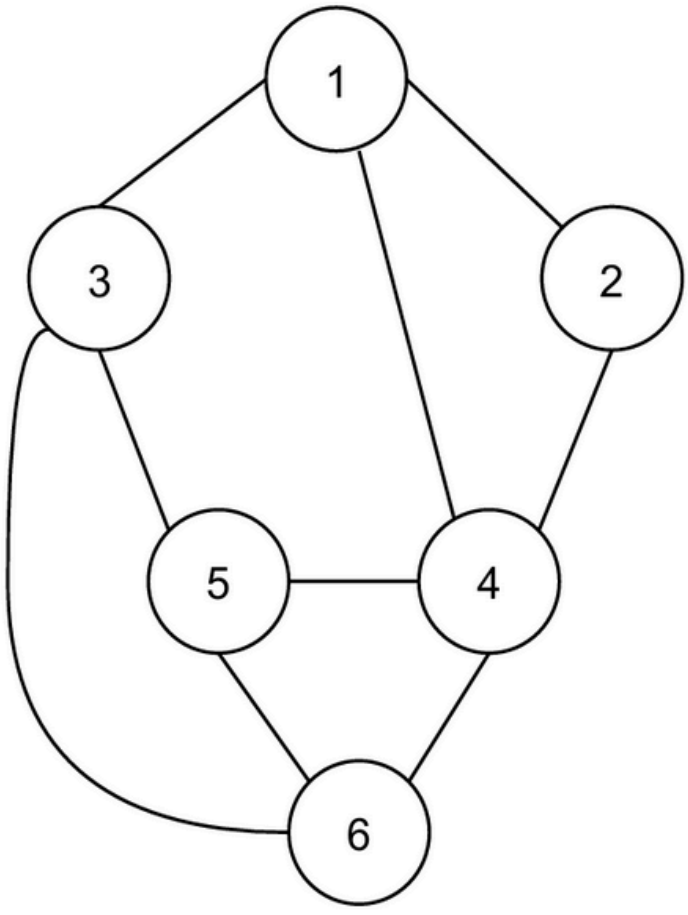
2) Identify the incorrect functional unit binding for the operations of the compatibility graph G1. ***1 point***

- **FU1:** 4, 6, 7; **FU2:** 3, 5; **FU3:** 1, 2
- **FU1:** 6, 7; **FU2:** 3, 4, 5; **FU3:** 1, 2
- **FU1:** 1, 2, 4; **FU2:** 3, 5; **FU3:** 6, 7
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
None of the above

3) ***2 points***



G2

What is the chromatic number and the clique cover number of the graph G2.

- 3, 3
- 4, 2

- 4, 3
- 3, 2

No, the answer is incorrect.
Score: 0

Accepted Answers:
3, 2

4) If the graph G2 is a conflict graph of operations 1, 2, 3, 4, 5 and 6; state whether the following statement is true/false. ***1 point***
S1: Operations 1 and 4 are scheduled in the same timestamp.

- True
- False

No, the answer is incorrect.
Score: 0

Accepted Answers:
True

5) Fill in the blanks with appropriate options. ***1 point***
An undirected graph is an interval graph if and only if it is ___ graph and its complement is a ___ graph.

- perfect; comparability
- chordal; comparability
- comparability; perfect
- comparability; chordal

No, the answer is incorrect.
Score: 0

Accepted Answers:
chordal; comparability

6) Which of the following options is correct with respect to the functional unit allocation and binding problem in hierarchical sequence graph ? ***2 points***
S1: Conflict graph may not be an interval graph.
S2: The allocation and binding problem may not be solved with the help of left edge algorithm.

- Statement 1 is true; Statement 2 is false.
- Statement 1 is false; Statement 2 is true.
- Statement 1 is true; Statement 2 is true and 1 is a correct explanation for 2.
- Statement 1 is true; Statement 2 is true but 1 is not a correct explanation for 2.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Statement 1 is true; Statement 2 is true and 1 is a correct explanation for 2.

7) ***1 point***

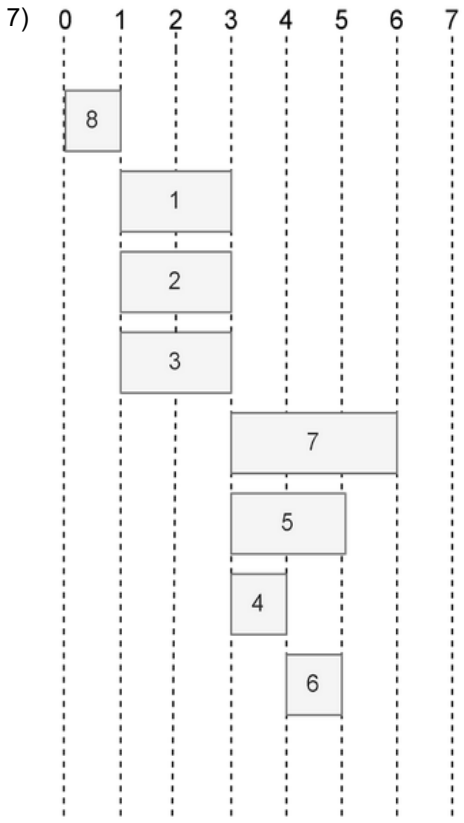


Figure 1

State whether the following statements are true/false with respect to functional unit binding for the operations of the interval graph shown in figure 1.
S1: Operations 5 and 4 can be mapped to the same functional unit.
S2: Operations 8 and 4 can be mapped to the same functional unit.

- Statement 1 is false; Statement 2 is true.
- Statement 1 is true; Statement 2 is false.
- Statement 1 is true; Statement 2 is true.
- Statement 1 is false; Statement 2 is false.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Statement 1 is false; Statement 2 is true.

8) Which of the following statements is false with respect to allocation and binding ? ***1 point***

- Chordal graphs are a subset of perfect graphs.
- Functional unit binding problem can be mapped to graph colouring problem of conflict graph.
- Functional unit binding problem can be mapped to clique cover problem of compatibility graph.
- The complexity of the left edge algorithm is O(log n) if ‘n’ is the number of nodes in the interval graph.

No, the answer is incorrect.

Score: 0

Accepted Answers:

The complexity of the left edge algorithm is O(log n) if ‘n’ is the number of nodes in the interval graph.

X

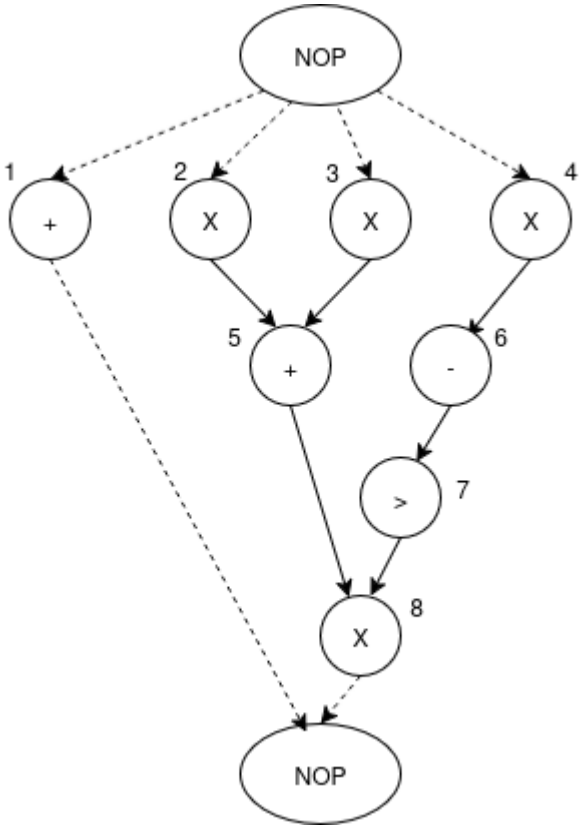
Week 4: Assignment 4

The due date for submitting this assignment has passed.

Due on 2025-08-20, 23:59 IST.

As per our records you have not submitted this assignment.

1) Consider the following DFG figure 1. For this figure assume all operations are single cycle and latency bound is ‘4’. ***1 point***



Calculate the operation probability Pi(l) for l = 1 to 4, for i = 1.

- Pi(1) = 0, Pi(2) = Pi(3) = Pi(4) = 1/3

- Pi(1) = Pi(2) = Pi(3) = 1/3, Pi(4) = 0
- Pi(1) = Pi(2) = 1/2, Pi(3) = Pi(4) = 0
- Pi(1) = Pi(2) = Pi(3) = Pi(4) = 1/4

No, the answer is incorrect.
Score: 0
Accepted Answers:
Pi(1) = Pi(2) = Pi(3) = Pi(4) = 1/4

2) For figure 1 in Question 1 and the same assumptions, what is the self force for node 3 if it is scheduled at time step 2? **1 point**

- -0.33
- -0.5
- 0.67
- -0.98

No, the answer is incorrect.
Score: 0
Accepted Answers:
-0.5

3) For figure 1 in Question 1 and the same assumptions, what is the Total force if node 3 is scheduled at time step 2? **1 point**

- -0.5
- -0.83
- 0
- 0.5

No, the answer is incorrect.
Score: 0
Accepted Answers:
-0.5

4) For figure 1 in Question 1 and the same assumptions, what is the variation of force of node 5 if node 3 is scheduled in time step 2. **1 point**

- 1.75
- 1.25
- -1
- 0

No, the answer is incorrect.
Score: 0
Accepted Answers:
0

5) Which of the following statements are correct? **1 point**

1. In the force-directed version of MLRC, operations with the least force are selected first, as this increases local concurrency.

2. In the force-directed version of MLRC, operations with the highest force are selected first, as this increases local concurrency.

3. In the force-directed version of MRLC, operations with the highest force are scheduled first to reduce the number of resources.

4. In the force-directed version of MRLC, operations with the least force are scheduled first to reduce the number of resources.

- 1 and 3 are correct
- 2 and 4 are correct
- 1 and 4 are correct
- 2 and 3 are correct

No, the answer is incorrect.
Score: 0

Accepted Answers:
2 and 4 are correct

6) Which of the following statements is/are correct? ***0 points***

1. The key difference in the Force-Directed version of MLRC is that it schedules one operation at a time instead of one iteration at a time.

2. The only difference in the Force-Directed version of MRLC is the use of a different priority function.

3. The Force-Directed version of MRLC has a time complexity of $O(n^2)$.

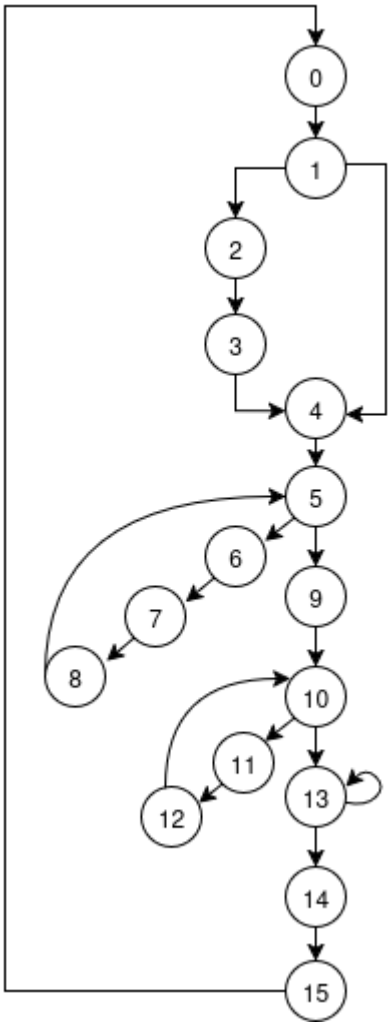
4. The only difference in the Force-Directed version of MRLC is that it schedules one operation at a time instead of one iteration at a time.

- All of the above statements are correct
- Only statements 1 and 2 are correct
- Only statement 4 is correct
- None of the statements are correct

No, the answer is incorrect.
Score: 0

Accepted Answers:
Only statement 4 is correct

7) Identify the number of longest paths from the given CDFG below. ***1 point***



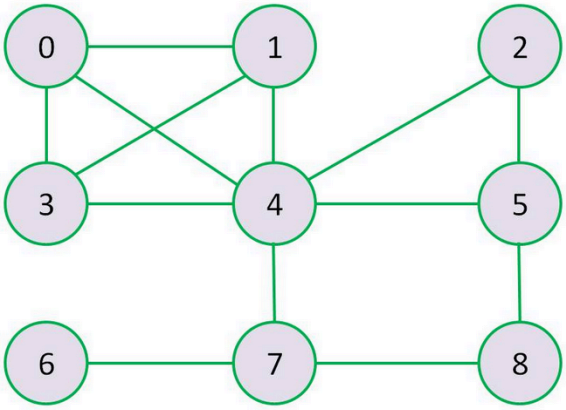
- 12
- 6
- 9
- 11

No, the answer is incorrect.
Score: 0

Accepted Answers:
12

8) Consider an interval graph given below where each node represents a constraint, and an edge exists between two nodes if their corresponding constraints ***1 point***

overlap. What is the minimum number of cuts required to satisfy all constraints?



- 2
- 3
- 4
- 5

No, the answer is incorrect.
Score: 0

Accepted Answers:
4

9) Based on the AFAP algorithm rule for construction of the state transitions: A state transition (edge) is added from state S_i to state S_j under which of the following conditions? ***1 point***

- Operation V_i is the first operation of the cut associated with S_i, and V_j is the last operation of the cut associated with S_j
- Operation V_i is any operation in S_i, and operation V_j is any operation in S_j, provided V_j is a successor of V_i.
- Operation V_i is the last operation of the cut associated with S_i, and operation V_j is the start operation of the cut associated with S_j, AND V_j is a successor of V_i.
- Only when there is a loop that connects S_i and S_j

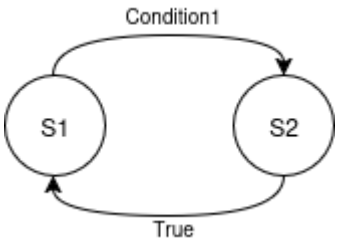
No, the answer is incorrect.
Score: 0

Accepted Answers:
Operation V_i is the last operation of the cut associated with S_i, and operation V_j is the start operation of the cut associated with S_j, AND V_j is a successor of V_i.

10) For the following figure consider S1 has operations 1, 2, 3 and 4 inside of it as follows: ***1 point***

```
1. temp = 50
2. if (temp = 50)
3.   temp = temp + 1
```

4. endif



If there exists a transition from S1 to S2, which one of the following correctly represents Condition1 of this transition?

- Always True
- temp = 50
- temp = 51
- (T v temp = 50) ^ (temp != 50)

No, the answer is incorrect.
Score: 0

Accepted Answers:
Always True

X

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Course outline

About NPTEL ()

How does an NPTEL online course work? ()

Prerequisite: Week 0 ()

Week1: Introduction to C-based VLSI Design ()

Week2: C-Based VLSI Design: Basic Scheduling ()

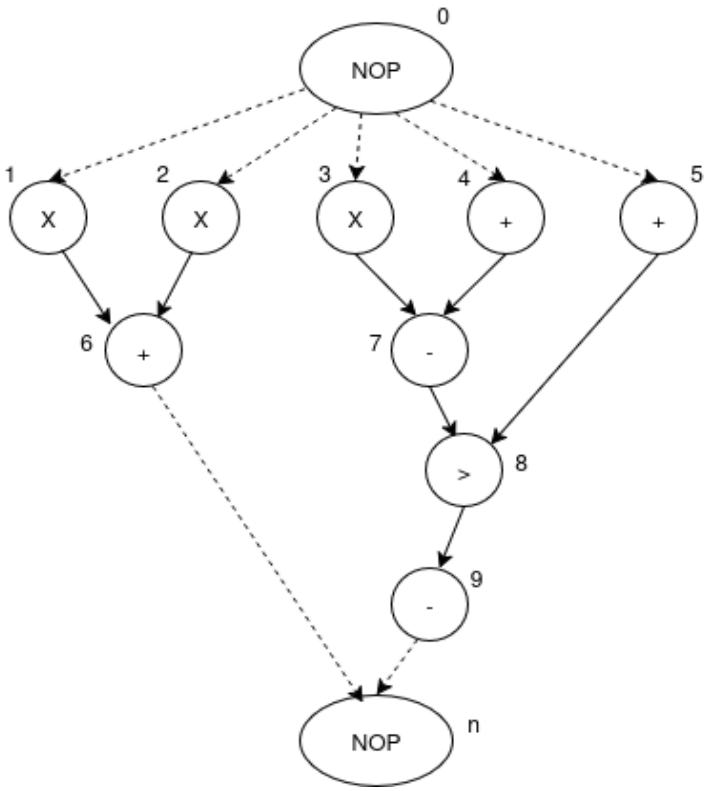
Week 3: Assignment 3

The due date for submitting this assignment has passed.

Due on 2025-08-13, 23:59 IST.

Assignment submitted on 2025-08-13, 16:46 IST

1) Given the sequencing graph shown in this figure, determine which of the following are the correct precedence constraints. Assume that all type of operations can be executed by a multiprocessor. ***1 point***



$(1) 2x_{6,2} + 3x_{6,3} + 4x_{6,4} - x_{1,1} - 2x_{1,2} - 3x_{1,3} - 1 \geq 0$
$(2) 2x_{6,2} + 3x_{6,3} + 4x_{6,4} - x_{2,1} - 2x_{2,2} - 3x_{2,3} - 1 \geq 0$
$(3) 3x_{8,3} - x_{5,1} - 2x_{5,2} - 1 \geq 0$
$(4) 5x_{n,5} - 2x_{6,2} - 3x_{6,3} - 4x_{6,4} - 1 \geq 0$

- 1,2 and 3 are correct
- 2, 3 and 4 are correct
- 1, 3 and 4 are correct
- All are correct

No, the answer is incorrect.
Score: 0

Accepted Answers:
All are correct

2) Determine the resource constraint for time step 2 for the sequence graph given in Question 1, considering the same assumptions of a multiprocessor scheduling. Let 'a' be the resource bound. ***1 point***

- $x_{1,2} + x_{2,2} + x_{5,2} + x_{6,2} + x_{7,2} + a \leq 0$
- $x_{6,2} + x_{7,2} - a \leq 0$
- $x_{1,2} + x_{2,2} + x_{5,2} + x_{6,2} + x_{7,2} - a \leq 0$
- $x_{6,2} + x_{7,2} + a \leq 0$

No, the answer is incorrect.
Score: 0

Accepted Answers:
$x_{1,2} + x_{2,2} + x_{5,2} + x_{6,2} + x_{7,2} - a \leq 0$

3) Find the value of **α** (maximum of all labels) and **p(j)** = number of vertices with label = j for the above sequence graph given in Question 1 ***1 point***

- **α** = 3, p(2) = p(3) = p(4) = 2, p(1) = 3
- **α** = 4, p(2) = p(3) = p(4) = 2, p(1) = 3
- **α** = 4, p(1) = p(2) = p(3) = 2, p(4) = 3
- **α** = 4, p(1) = p(3) = p(4) = 2, p(2) = 3

No, the answer is incorrect.
Score: 0

Accepted Answers:
***α** = 4, p(1) = p(3) = p(4) = 2, p(2) = 3*

4) Consider the sequence graph given in Question 1. Select the correct option for the statements given below for scheduling using Hu's Algorithm for the MLRC problem. Assume no. of resources available is 3. If multiple nodes have the same label, choose the one with the smallest node ID. ***1 point***

1. Node 6 will be scheduled at time step 2
2. Node 8 will be scheduled at time step 2
3. Node 6 will be scheduled at time step 3
4. Node 8 will be scheduled at time step 3

- Statements 1 and 2 are correct
- Statements 2 and 3 are correct
- Statements 3 and 4 are correct
- Statements 1 and 4 are correct

No, the answer is incorrect.
Score: 0

Accepted Answers:
Statements 3 and 4 are correct

5) Based on Theorem 1 of Hu's Algorithm, what is the lower bound on the number of processors required given the following values? ***1 point***

$\lambda = 5$, $\alpha = 5$,
$p(5) = 2$, $p(4) = 2$, $p(3) = 3$, $p(2) = 4$, $p(1) = 3$

- 2
- 2.33
- 2.8
- 3

Yes, the answer is correct.
Score: 1

Accepted Answers:
3

6) Identify the correct statement(s) regarding the candidate operations $U_{l,k}$ and unfinished operations $T_{l,k}$ in the context of MLRC (Minimum Latency under Resource Constraints) scheduling. $T(v_i) = k$ denotes node type k for node v_i for the graph G(V,E). ***1 point***

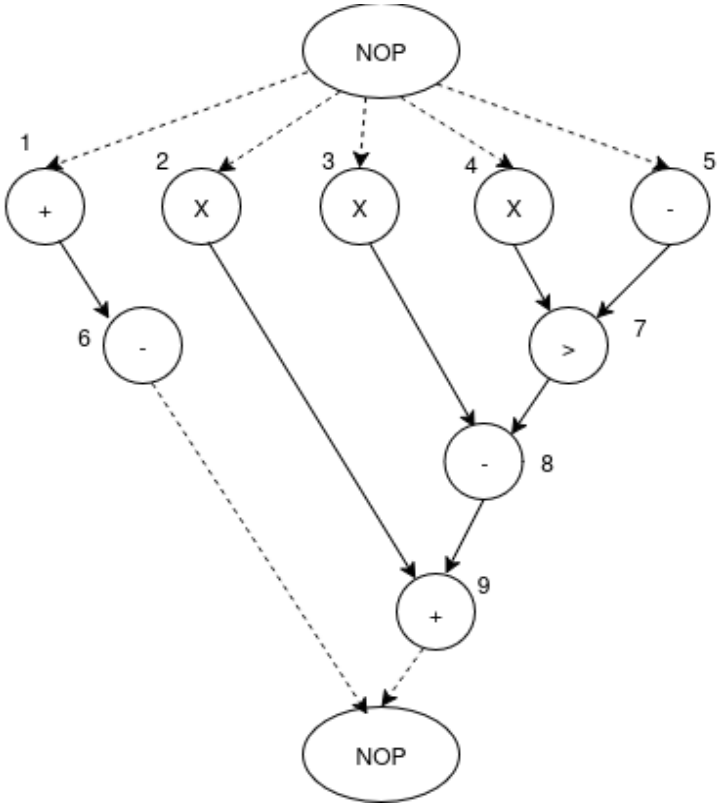
1. $U_{l,k} = \{v_i \in V \mid T(v_i) = k \ \wedge \ t_j + d_j \geq l \ \ \forall j \text{ such that } (v_j, v_i) \in E\}$
2. $T_{l,k} = \{v_i \in V \mid T(v_i) = k \ \wedge \ t_i + d_i < l\}$
3. $U_{l,k} = \{v_i \in V \mid T(v_i) = k \ \wedge \ t_j + d_j \leq l \ \ \forall j \text{ such that } (v_j, v_i) \in E\}$
4. $T_{l,k} = \{v_i \in V \mid T(v_i) = k \ \wedge \ t_i + d_i > l\}$

- Only Statement 3 is correct
- Statements 1 and 2 are correct
- Statements 3 and 4 are correct
- All statements are correct

No, the answer is incorrect.
Score: 0

Accepted Answers:
Statements 3 and 4 are correct

7) Consider the following sequence graph. ***1 point***



Assume resource constraint of 2 multipliers and 1 alu and single cycle operations. Schedule it using list scheduling for the MLRC problem given the priority function equal to the distance of longest path from the sink node. If multiple nodes have equal priority, further prioritize the ones with the smaller node ID.

Statements
1. Node 1 is scheduled at time step 3
2. Node 8 is scheduled at time step 4
3. Node 6 is scheduled at time step 5
4. Node 9 is scheduled at time step 6

Which is/are the correct Statements?

- Only statements 1 and 2 are correct
- Only Statement 4 is correct
- All Statements are correct
- None of the Statements are correct

No, the answer is incorrect.
Score: 0

Accepted Answers:
All Statements are correct

8) Consider the sequence graph of Question 7. Assume multipliers are pipelined with delay of 2 and alu 1, and resource constraint of 1 multiplier and 2 alus. Schedule it using list based scheduling for the MLRC problem given that the priority function equals distance of longest path from sink node. Which node is scheduled in time step 5? ***1 point***

- Node 6
- Node 7

- Node 8
- Node 9

No, the answer is incorrect.
Score: 0

Accepted Answers:
Node 9

9) Consider the sequence graph of Question 7. Given latency bound $\lambda = 4$, use list based scheduling for this MRLC problem to find the minimum resource required. Consider all operations are single cycle operations. **1 point**

- 1 multiplier, 1 adder
- 1 multiplier, 2 adders
- 2 multipliers, 1 adder
- 2 multipliers, 2 adders

No, the answer is incorrect.
Score: 0

Accepted Answers:
1 multiplier, 2 adders

10) At which time step is Node 1 scheduled in the solution to Question 9? **1 point**

- 1
- 2
- 3
- 4

No, the answer is incorrect.
Score: 0

Accepted Answers:
3

X

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Course outline

About NPTEL ()

How does an NPTEL online course work? ()

Prerequisite: Week 0 ()

Week1: Introduction to C-based VLSI Design ()

Week2: C-Based VLSI Design: Basic Scheduling ()

Week 2: Assignment 1

The due date for submitting this assignment has passed.

Due on 2025-08-06, 23:59 IST.

Assignment submitted on 2025-08-04, 21:15 IST

1) An Integer Linear Program always gives: ***1 point***

- Heuristic Solution
- Optimal Solution
- Near-optimal Solution.
- Approximate Solution

Yes, the answer is correct.
Score: 1

Accepted Answers:
Optimal Solution

2) What is the full form of MLRC and MRLC Scheduling? ***1 point***

- MLRC: Maximum Latency Resource Constraint
  MRLC: Minimum Resource Latency Constraint
- MLRC: Minimum Latency Resource Constraint
  MRLC: Minimum Resource Latency Constraint
- MLRC: Minimum Latency Resource Constraint
  MRLC: Maximum Resource Latency Constraint
- MLRC: Maximum Latency Resource Constraint
  MRLC: Maximum Resource Latency Constraint

No, the answer is incorrect.

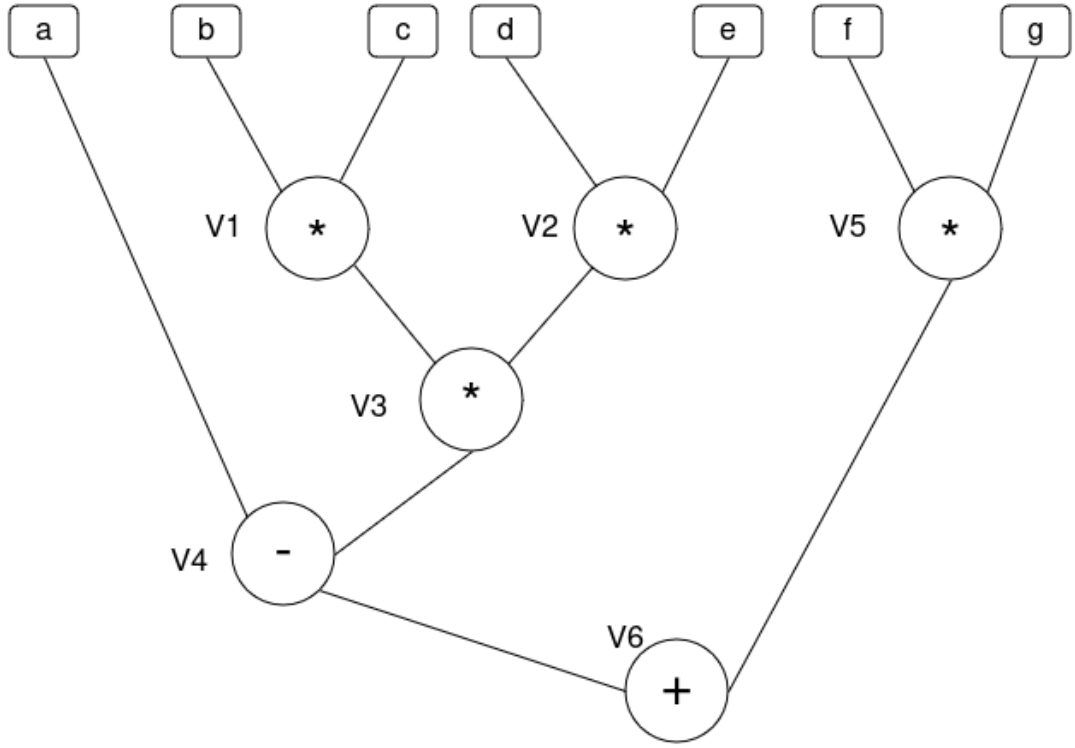
Score: 0

Accepted Answers:

MLRC: Minimum Latency Resource Constraint

MRLC: Minimum Resource Latency Constraint

3) Consider the following Data Dependency Graph. Each node represents an operation, and each edge represents a data dependency. If the Multiplication operation takes 3 cycles, while the addition takes 2 cycles, then perform the ASAP and ALAP schedules on the graph. For ALAP, take the latency bound as 10 cycles. Also, the schedule begins from time step 1. ***1 point***



The ASAP and ALAP start time of operation V5 is

- ASAP = 4, ALAP = 5
- ASAP = 4, ALAP = 4
- ASAP = 1, ALAP = 6
- ASAP = 1, ALAP = 5

No, the answer is incorrect.
Score: 0

Accepted Answers:

ASAP = 1, ALAP = 6

4) Consider the information in Q3. The ASAP and ALAP start time of operation V3 is ***1 point***

- ASAP = 4, ALAP = 5
- ASAP = 4, ALAP = 4
- ASAP = 1, ALAP = 6
- ASAP = 1, ALAP = 5

Yes, the answer is correct.

Score: 1

Accepted Answers:

ASAP = 4, ALAP = 4

5) Consider the Data Dependency Graph of Q3. What is the mobility value of operations V4 and V5? ***1 point***

- V4 = 1, V5 = 2
- V4 = 0, V5 = 3
- V4 = 1, V5 = 4
- V4 = 0, V5 = 5

Yes, the answer is correct.
Score: 1

Accepted Answers:

V4 = 0, V5 = 5

6) Consider the Data Dependency Graph of Q3. What is the mobility value of operations V3 and V6? ***1 point***

- V3 = 1, V6 = 1
- V3 = 0, V6 = 0
- V3 = 1, V6 = 0
- V3 = 0, V6 = 1

Yes, the answer is correct.
Score: 1

Accepted Answers:

V3 = 0, V6 = 0

7) Consider Q3. What is the number of cycles required to schedule all the operations when the ASAP algorithm is applied? ***1 point***

- 8
- 9
- 10
- 11

Yes, the answer is correct.
Score: 1

Accepted Answers:

10

8) What are the constraints that are involved with MLRC? ***1 point***

C1) Unique Start time.
C2) Data dependency constraint.
C3) Resource Constraint.
C4) Latency Constraint.

Choose the correct option:

- C2 and C3.
- C1, C2 and C3

- C1, C2 and C4
- C2 and C4

Yes, the answer is correct.
Score: 1

Accepted Answers:
C1, C2 and C3

9) Consider the information in Q3. The unique start time constraint equation for operation V5 is: ***1 point***

- $x_{5,1} + x_{5,2} + x_{5,3} + x_{5,4} + x_{5,5} + x_{5,6} = 1$
- $x_{5,1} + x_{5,2} + x_{5,3} + x_{5,4} + x_{5,5} = 1$
- $x_{5,2} + x_{5,3} + x_{5,4} + x_{5,5} + x_{5,6} = 1$
- $x_{5,2} + x_{5,3} + x_{5,4} + x_{5,5} + x_{5,6} + x_{5,7} = 1$

No, the answer is incorrect.
Score: 0

Accepted Answers:
$x_{5,1} + x_{5,2} + x_{5,3} + x_{5,4} + x_{5,5} + x_{5,6} = 1$

10) Consider the information in Q3. If we consider two multipliers are given, the equation for resource constraints at time step t4 for multiplication type will be (Time step starts from t1): ***1 point***

- $x_{5,4} + x_{1,4} + x_{2,4} <= 2$
- $x_{3,4} + x_{5,4} + x_{2,4} <= 2$
- $x_{3,4} + x_{5,4} <= 2$
- $x_{3,4} + x_{1,4} + x_{2,4} <= 2$

Yes, the answer is correct.
Score: 1

Accepted Answers:
$x_{3,4} + x_{5,4} <= 2$

X

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Course outline

About NPTEL ()

How does an NPTEL online course work? ()

Prerequisite: Week 0 ()

Week1: Introduction to C-based VLSI Design ()

Lec 1: Introduction to C-Based VLSI Design (unit?unit=17&lesson=18)

Lecture Notes for Lec1 (unit?

Week 1: Assignment 1

The due date for submitting this assignment has passed.

Due on 2025-08-06, 23:59 IST.

Assignment submitted on 2025-08-04, 21:03 IST

1) The correct sequence of the VLSI Design flow is: ***1 point***

- System Specification → Architectural Design → High Level Synthesis → Physical Synthesis → Logic Synthesis → Fabrication → Packaging & Testing
- System Specification → Architectural Design → High Level Synthesis → Logic Synthesis → Physical Synthesis → Fabrication → Packaging & Testing
- Architectural Design → System Specification → High Level Synthesis → Logic Synthesis → Physical Synthesis → Fabrication → Packaging & Testing
- System Specification → Architectural Design → High Level Synthesis → Physical Synthesis → Logic Synthesis → Packaging & Testing → Fabrication

Yes, the answer is correct.
Score: 1

Accepted Answers:
System Specification → Architectural Design → High Level Synthesis → Logic Synthesis → Physical Synthesis → Fabrication → Packaging & Testing

2) Consider the statements: ***1 point***

S1) Moore's law states that the number of transistors in a chip doubles every five years.
S2) According to Dennard's law, as the transistors are getting smaller, we can actually put more transistors in the same area. Hence, the power density also increases.
Then,

- Only S1 is correct.
- Only S2 is correct

Both S1 and S2 are correct

Both S1 and S2 are wrong.

Yes, the answer is correct.
Score: 1

Accepted Answers:
Both S1 and S2 are wrong.

3) The correct sequence of the HLS flow is: ***1 point***

Scheduling→Allocation&Binding→Preprocessing→Datapath & Controller Generation

Preprocessing→Allocation & Binding → Scheduling → Datapath & Controller Generation

Preprocessing→ Scheduling→ Allocation & Binding → Datapath & Controller Generation

Preprocessing→Datapath & Controller Generation → Scheduling→Allocation & Binding

Yes, the answer is correct.
Score: 1

Accepted Answers:
Preprocessing→ Scheduling→ Allocation & Binding → Datapath & Controller Generation

4) Often, we use the term “nanometer (nm)” while discussing transistors in VLSI. What exactly does this nanometer value represent in terms of transistor structure or distance? ***1 point***

Physical length of the transistor.

Distance between two adjacent transistors.

Distance between source and drain.

None of the above.

Yes, the answer is correct.
Score: 1

Accepted Answers:
Distance between source and drain.

5) Consider the statements: ***1 point***

S1) Scheduling involves assigning timestamps to each operation.
S2) Scheduling of operations can be done randomly without any constraints.
S3) The input graph to scheduling is the Control & Data Flow Graph.

Choose the correct option:

S1 and S3 is correct.

S2 and S3 is correct.

Only S1 is correct

Only S3 is correct.

No, the answer is incorrect.

Score: 0

Accepted Answers:

Only S1 is correct

6) Match the following between C/C++ Constructs and RTL Constructs. ***1 point***

C Constructs	**RTL Constructs**
A) Functions	i) RAM/ROM
B) Variables	ii) Modules
C) Operators	iii) Input/Output ports
D) Arguments	iv) Functional Units
E) Arrays	v) Registers

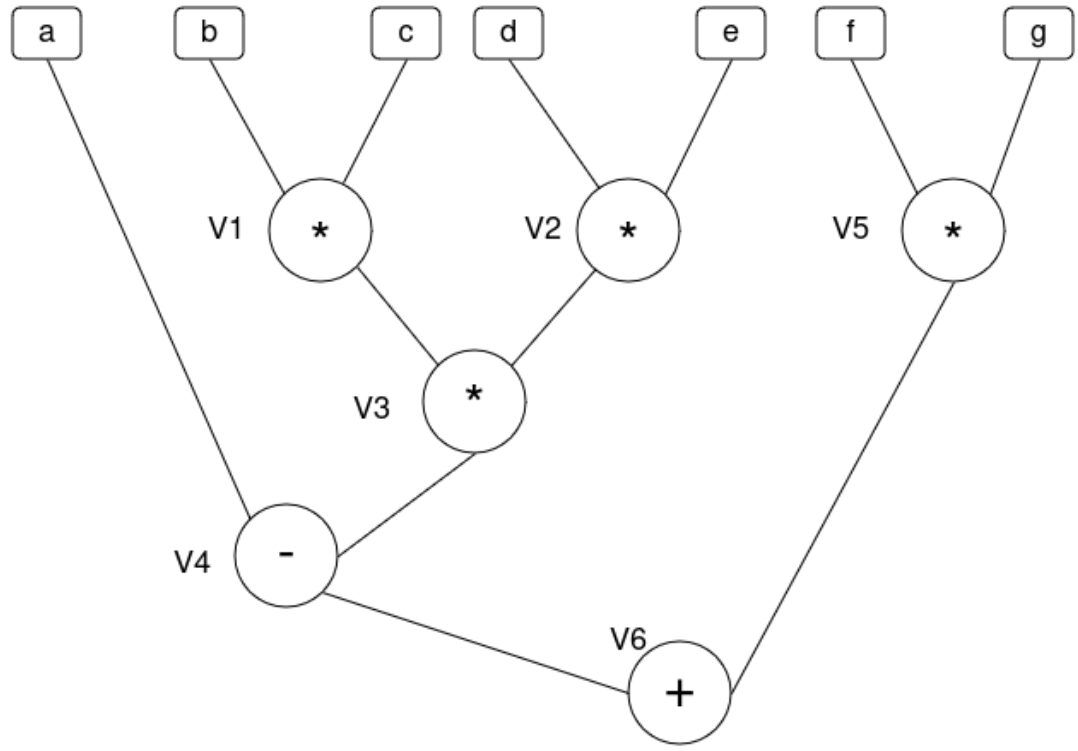
- A-(ii), B-(i), C-(iii), D-(iv), E-(v)
- A-(iv), B-(i), C-(iii), D-(v), E-(ii)
- A-(iii), B-(ii), C-(iv), D-(v), E-(i)
- A-(ii), B-(v), C-(iv), D-(iii), E-(i)

Yes, the answer is correct.
Score: 1

Accepted Answers:

A-(ii), B-(v), C-(iv), D-(iii), E-(i)

7) Consider the following Data Dependency Graph. Each node represents an operation, and each edge represents data dependency. Let each operation take one unit of time to execute. ***1 point***



If one multiplier and one arithmetic operator (which can perform addition and subtraction) are available, and t represents the time step, then consider the statements showing the flow of execution of the operations.

S1) V1 schedules at t1, V5 schedules at t2, V3 schedules at t3, V4, V2 schedules at t4 and V6 schedules at t5
S2) V1 schedules at t1, V2 schedules at t2, V3 schedules at t3, V4,V5 schedules at t4 and V6 schedules at t5
S3) V5 schedules at t1, V1 schedules at t2, V2 schedules at t3, V3 schedules at t4, V4 schedules at t5 and V6 schedules at t6
Then,

- Both S1 and S2 are correct
- Both S2 and S3 are correct
- Both S3 and S1 are correct
- Only S2 is correct

No, the answer is incorrect.
Score: 0

Accepted Answers:
Both S2 and S3 are correct

8) Consider the statements: ***1 point***

S1) The functional arguments in a function are implemented as ports in the RTL.
S2) HLS generates an RTL in which both the datapath and controller FSM are present.

Then,

- Only S1 is correct.
- Only S2 is correct.
- Both S1 and S2 are correct.
- Both S1 and S2 are wrong.

Yes, the answer is correct.
Score: 1

Accepted Answers:
Both S1 and S2 are correct.

9) Consider the statements ***1 point***

S1) If the lifetimes of two variables are overlapping, we can put them into the same register.
S2) Allocation and Binding involve maximizing resource sharing, hence minimizing the number of resources.

Then,

- Only S1 is correct.
- Only S2 is correct
- Both S1 and S2 are correct
- Both S1 and S2 are wrong.

Yes, the answer is correct.

Score: 1

Accepted Answers:

Only S2 is correct

10) The full form of HLS and VLSI is: ***1 point***

- Hardware Level Synthesis and Very Long Scope Integration
- High-Level Synthesis and Very Large Scale Integration
- Hardware Logic Simulation and Very Long Scale Integration
- High-Level Simulation and Very Large Scale Integration

Yes, the answer is correct.
Score: 1

Accepted Answers:

High-Level Synthesis and Very Large Scale Integration