# Shrikrishna Pandit

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**Profile:** Final-year ECE student interested in VLSI, digital design, hardware architecture & reconfigurable computing. Open to research and internship opportunities.

## Education

**PES University, Bengaluru** **August 2022 – Present**

*B. Tech in Electronics and Communication Engineering (First Class)* *Expected Completion Aug, 2026*

## Experience

**Ovii** **Oct, 2023 – Present**

*Founding Engineer, Founding Marketer* *Bengaluru, India*

- Developed Java-based REST APIs for AI-integrated testing and HR platforms, contributing 20% of backend development.
- Transitioned into marketing to lead outreach and community growth, representing Ovii at tech meetups.
- Contributed to both product stability and brand development during the startup's formative phase.

## Projects

**6T SRAM Design and Simulation** | *Cadence Virtuoso (Layout, DRC, LVS in progress)* **April 2025**

- Designed and simulated a 6-transistor SRAM cell with focus on read/write operation stability.
- Currently progressing through layout validation using DRC and LVS in Cadence Virtuoso.

**RISC-V Processor** | *Vivado* **November 2024**

- Developed a single-cycle, 5-stage RISC-V (RV32I) processor in Vivado using Verilog HDL.
- Implemented instruction fetch, decode, execute, memory, and write-back stages.

**Layered Testbench for 4-bit Gray-Code Counter** | *SystemVerilog* **October 2024**

- Built a modular SystemVerilog testbench including driver, monitor, scoreboard, and generator.
- Verified correctness and robustness of a 4-bit Gray-Code counter under different test scenarios.

**6D Sorter and Euclidean Distance Calculator on FPGA** | *SystemVerilog* **August 2024**

- Implemented a parallel 6D sorter and Euclidean distance calculator using SystemVerilog on FPGA.
- Optimized for speed to accelerate k-nearest neighbors (KNN) classification tasks.

**Conductivity & Shielding Properties of ZINC Doped Polyaniline** | *Chemistry Research Paper* **December 2023**

- Conducted material synthesis with Ag and Zn doping of polyaniline to enhance shielding behavior.
- Evaluated conductivity and EMI shielding effectiveness of pressed pellets in a lab environment.

## Technical Skills

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| **Languages** | System Verilog, Verilog, C, C++, Java, Python, Embedded C, SQL, Assembly. |
| **Tools** | Vivado, Vitis, Cadence (Virtuoso, Spectre, Genus), Quartus Prime, RIPES, LT-Spice, GNS3, Wireshark, MATLAB. |

## Leadership & Extracurricular

**Silicon Club (Discrete Electronics Club)** **Till Aug 2025**

*Head of Club* *PES University, Bengaluru*

Conducted workshops on soldering and hands-on electronics; Mentored juniors on circuit design and project development.

**Entrepreneurship Club** **Till April 2025**

*Head of Events* *PES University, Bengaluru*

Organized "Wolf of Wall Street", a stock market simulation for 450+ participants.

**CodeChef Club** **Till Jan 2025**

*Member of Events and Operations team* *PES University, Bengaluru*

**QQC (Quotient Quiz Club)** **Till Feb 2025**

*Member of Events and Operations team* *PES University, Bengaluru*

## Certificates

- IEEE CAS Seasonal School 2025
- DIRv Symposium Participation
- Volunteering For VLSId Conference
- ISWDP Cohort-2 Level-1