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## Section 7. Reset

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## 7.1 INTRODUCTION

The Reset module combines all Reset sources and controls the device Master Reset signal,  $\overline{\text{SYSRST}}$ . The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Pin Reset
- SWR: `RESET` Instruction
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode/Uninitialized W Register Reset

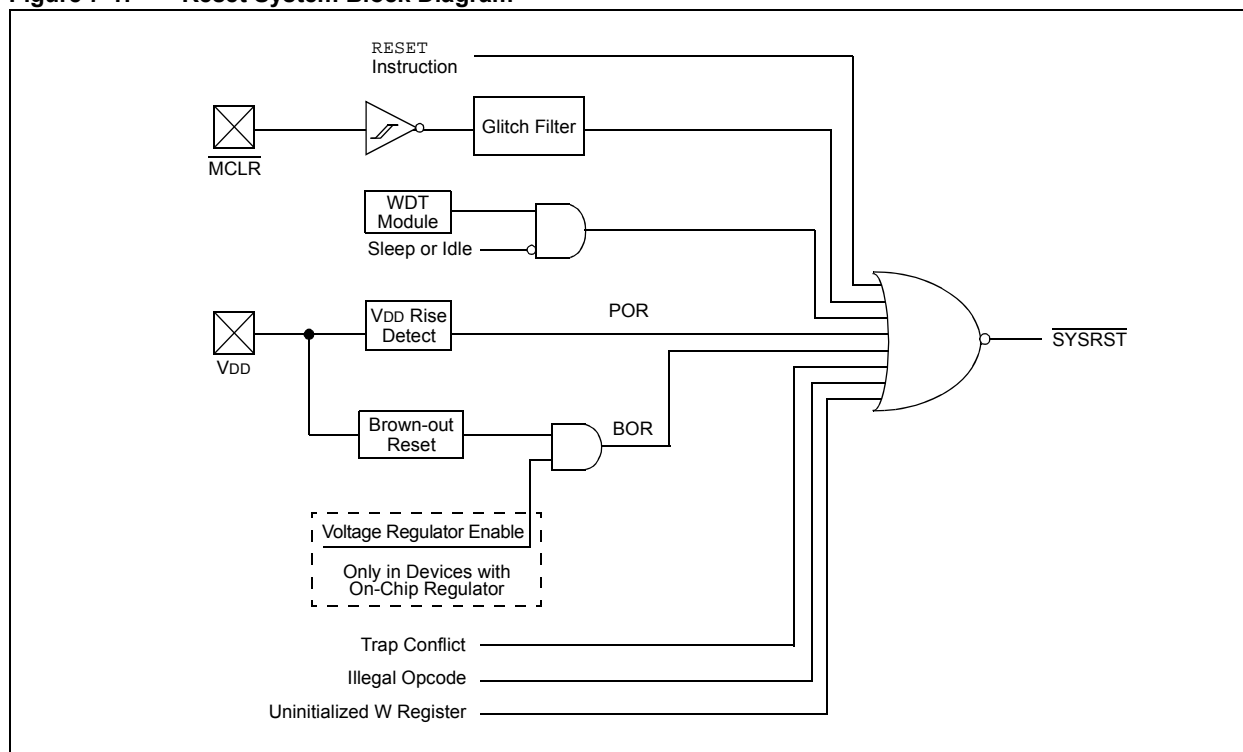
Figure 7-1 displays a simplified block diagram of the Reset module. Any active source of Reset will make the  $\overline{\text{SYSRST}}$  signal active. Many registers associated with the CPU and peripherals are forced to a known "Reset state". Most registers are unaffected by a Reset; their status is unknown on Power-on Reset (POR) and unchanged by all other Resets.

**Note:** Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Resets will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A POR will clear all bits, except for the BOR and POR bits ( $\text{RCON}\langle 1:0 \rangle$ ) which are set. Users may set or clear any of the bits at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. For more information on the function of these bits, refer to **Section 7.12.1 "Using the RCON Status Bits"**.

**Figure 7-1: Reset System Block Diagram**



**Register 7-1: RCON: Reset Control Register<sup>(1)</sup>**

R/W-0	R/W-0	U-0	U-0	U-0	R/C-0	U-0	U-0
TRAPR	IOPUWR	—	—	—	DPSLP <sup>(2)</sup>	CM	PMSLP <sup>(2,3)</sup>
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN <sup>(4)</sup>	WDTO	SLEEP	IDLE	BOR	POR
bit 7						bit 0	

<b>Legend:</b>	C = Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit  
1 = A Trap Conflict Reset has occurred  
0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit  
1 = An illegal opcode detection, an illegal address mode or an uninitialized W register used as an Address Pointer caused a Reset  
0 = An illegal opcode or uninitialized W Reset has not occurred
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **DPSLP:** Program Memory Power During Sleep bit<sup>(2)</sup>  
1 = Deep Sleep has occurred  
0 = Deep Sleep has not occurred
- bit 9 **CM:** Configuration Mismatch Flag bit  
1 = A Configuration Mismatch Reset has occurred  
0 = A Configuration Mismatch Reset has not occurred
- bit 8 **PMSLP:** Program Memory Power During Sleep Control bit<sup>(2,3)</sup>  
1 = Program memory bias voltage remains powered during Sleep  
0 = Program memory bias voltage is powered down during Sleep; voltage regulator enters Standby mode
- bit 7 **EXTR:** External Reset ( $\overline{\text{MCLR}}$ ) Pin bit  
1 = A Master Clear (pin) Reset has occurred  
0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software Reset (Instruction) Flag bit  
1 = A RESET instruction has been executed  
0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software WDT Enable/Disable bit<sup>(4)</sup>  
1 = WDT is enabled  
0 = WDT is disabled
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit  
1 = WDT time-out has occurred  
0 = WDT time-out has not occurred

**Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** Implemented on select PIC24F devices only; otherwise unimplemented, read as '0'.

**3:** This bit is named VREGS in some earlier PIC24F devices, with a different description of the bit's functionality. Regardless of the name or description, its function in power reduction is identical in all devices.

**4:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

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## Register 7-1: RCON: Reset Control Register<sup>(1)</sup> (Continued)

bit 3	<b>SLEEP:</b> Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	<b>IDLE:</b> Wake-up from Idle Flag bit 1 = Device has been in Idle mode 0 = Device has not been in Idle mode
bit 1	<b>BOR:</b> Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred; the BOR is also set after a Power-on Reset 0 = A Brown-out Reset has not occurred
bit 0	<b>POR:</b> Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

- 2:** Implemented on select PIC24F devices only; otherwise unimplemented, read as '0'.
- 3:** This bit is named VREGS in some earlier PIC24F devices, with a different description of the bit's functionality. Regardless of the name or description, its function in power reduction is identical in all devices.
- 4:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

## 7.2 CLOCK SOURCE SELECTION AT RESET

If clock switching is enabled (OSWEN), the system clock source at device Reset is chosen, as displayed in Table 7-1. If clock switching is disabled, the system clock source is always selected according to the oscillator Configuration bits. Refer to **Section 6. “Oscillator”** for further details.

**Table 7-1: Oscillator Selection vs. Type of Reset (Clock Switching Enabled)**

Reset Type	Clock Source Selected Based on
POR	Oscillator Configuration Bits FNOSC<2:0>
BOR	
MCLR	COSC Control bits OSCCON<14:12>
WDTR	
SWR	
TRAPR	
IOPUWR	

## 7.3 POWER-ON RESET (POR)

The POR monitors the core power supply for adequate voltage levels to ensure proper chip operation. There are two threshold voltages associated with a POR. The first voltage is the device threshold voltage, VPOR. The device threshold voltage is the voltage at which the POR module becomes operable. The second voltage associated with a POR event is the POR circuit threshold voltage. Once the correct threshold voltage is detected, a power-on event occurs and the POR module hibernates to minimize current consumption.

A power-on event generates an internal POR pulse when a VDD rise is detected. The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR pulse. In particular, VDD must fall below VPOR before a new POR is initiated. For more information on the VPOR and VDD rise rate specifications, refer to the **“Electrical Characteristics”** section of the specific device data sheet.

The POR pulse resets the POR timer and places the device in the Reset state. The POR also selects the device clock source identified by the oscillator Configuration bits. After the POR pulse is generated, the POR circuit inserts a small delay, TPOR, which is nominally 5 µs and ensures that internal device bias circuits are stable.

After the expiration of TPOR, a delay, TSTARTUP, is always inserted. TSTARTUP is applied every time the device resumes operation after any power-down. In the devices with an on-chip regulator, the TSTARTUP parameter depends on whether the on-chip voltage regulator is enabled or disabled. When the on-chip voltage regulator is enabled, there is a delay until the regulator can generate a proper voltage level, referred to as TVREG. During this time, code execution is disabled.

**Note:** Some device data sheets use the term, TPM (Program Memory Available Delay), in place of TVREG. The terms can be considered to be interchangeable.

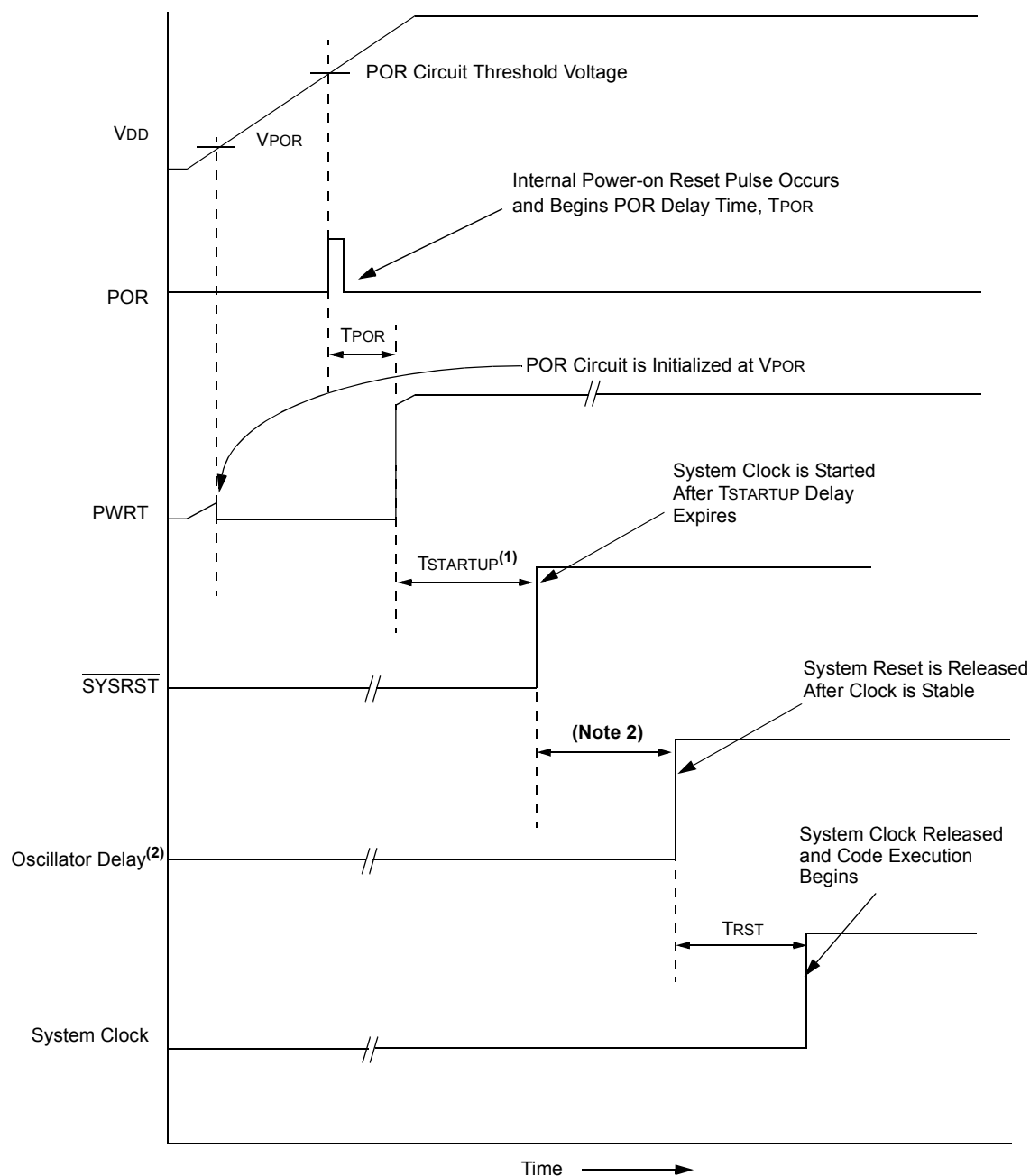
If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed 64 ms nominal delay at device start-up. The PWRT is used to extend the duration of a power-up sequence when the on-chip voltage regulator is disabled and the core is supplied from an external power supply. Hence, the TSTARTUP delay can either be TVREG (for devices using an on-chip voltage regulator), or the Power-up Timer delay TPWRT (for devices not using a regulator). The power-on event sets the BOR and POR status bits (RCON<1:0>). In some devices, the PWRT can be disabled by using the device Configuration bit. After TSTARTUP expires, an additional start-up time for the system clock (either TOST, TFRC or TLPRC, depending on the source) occurs while the clock source becomes stable.

Code execution is delayed further by a small delay, designated as TRST. The TRST delay is required to transfer the configuration values from Flash Configuration Words (FCW) in the program memory into the Configuration registers, and occurs after any device Reset. SYSRST is released and the device is no longer held in Reset, but the device clocks are prevented from running during TRST, as depicted in Figure 7-2. Once all of the delays have expired, the system clock is released and code execution can begin.

Refer to **Section 7.15 “Electrical Specifications”** for more information on the values of the delay parameters.

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**Figure 7-2: POR Module Timing Sequence for Rising VDD**



**NOTE 1:**  $T_{\text{VREG}}$  if the on-chip regulator is enabled or  $T_{\text{PWRT}}$  if the on-chip regulator is disabled.

**2:** Timer and interval are determined by the initial start-up oscillator configuration;  $T_{\text{OSC}}$  is for external oscillator modes,  $T_{\text{FRC}}$  is for the FRC oscillator or  $T_{\text{LPRC}}$  for the internal 31 kHz RC oscillator.

**Note:** When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device will not function correctly. The user must ensure that the delay between the time power is first applied and the time  $\overline{\text{SYSRST}}$  becomes inactive is long enough to get all operating parameters within the specification.

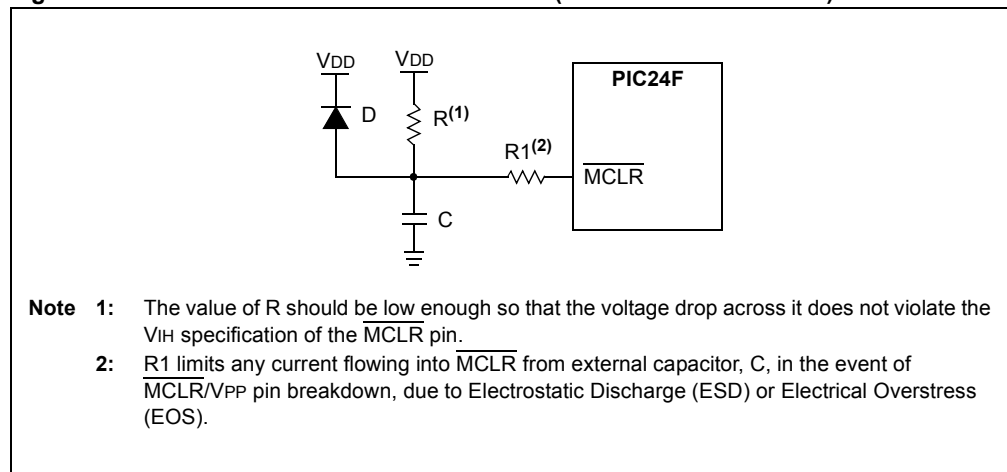
## 7.3.1 Using the POR Circuit

To take advantage of the POR circuit, just tie the  $\overline{\text{MCLR}}$  pin directly to  $\text{VDD}$ . This will eliminate external RC components usually needed to create a POR delay. A minimum rise time for  $\text{VDD}$  is required. Refer to the “**Electrical Characteristics**” section of the specific device data sheet for more information.

Depending on the application, a resistor may be required between the  $\overline{\text{MCLR}}$  pin and  $\text{VDD}$ . This resistor can be used to decouple the  $\overline{\text{MCLR}}$  pin from a noisy power supply rail.

Figure 7-3 displays a possible POR circuit for a slow power supply ramp up. The external POR circuit is only required if the device would exit Reset before the device  $\text{VDD}$  is in the valid operating range. The diode, D, helps discharge the capacitor quickly when  $\text{VDD}$  powers down.

**Figure 7-3: External Power-on Reset Circuit (for Slow  $\text{VDD}$  Rise Time)**



## 7.4 $\overline{\text{MCLR}}$ RESET

Whenever the  $\overline{\text{MCLR}}$  pin is driven low, the device asynchronously asserts  $\overline{\text{SYSRST}}$ , provided the input pulse on  $\overline{\text{MCLR}}$  is longer than a certain minimum width,  $\text{SY10}$  (see **Section 7.15 “Electrical Specifications”**). When the  $\overline{\text{MCLR}}$  pin is released,  $\overline{\text{SYSRST}}$  is also released. The Reset vector fetch starts after the expiration of the  $\text{TRST}$  delay, starting from the  $\overline{\text{SYSRST}}$  release. The processor continues to use the existing clock source that was in use before the  $\overline{\text{MCLR}}$  Reset occurred. The  $\text{EXTR}$  status bit ( $\text{RCON}<7>$ ) is set to indicate the  $\overline{\text{MCLR}}$  Reset.

## 7.5 SOFTWARE RESET INSTRUCTION (SWR)

Whenever the  $\text{RESET}$  instruction is executed, the device asserts  $\overline{\text{SYSRST}}$ . This Reset state does not re-initialize the clock. The clock source that is in effect prior to the  $\text{RESET}$  instruction remains in effect.  $\overline{\text{SYSRST}}$  is released at the next instruction cycle, but the Reset vector fetch starts only after the  $\text{TRST}$  delay.

## 7.6 WATCHDOG TIMER RESET (WDTR)

Whenever a Watchdog Timer time-out occurs, the device asynchronously asserts  $\overline{\text{SYSRST}}$ . The clock source remains unchanged. Note that a  $\text{WDT}$  time-out during Sleep or Idle mode will wake-up the processor, but NOT reset the processor. For more information, refer to **Section 9. “Watchdog Timer (WDT)”**.

## 7.7 BROWN-OUT RESET (BOR)

When the on-chip regulator is enabled, PIC24F family devices have a simple brown-out capability. BOR is applicable only when the regulator is enabled. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<0>).

Refer to **Section 7.15 “Electrical Specifications”** for further details.

### 7.7.1 Detecting BOR

When the BOR is enabled, the BOR bit (RCON<1>) is always reset to ‘1’ on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR bit is reset to ‘0’ in the software immediately after any POR event. If the BOR bit is ‘0’ while POR is ‘1’, it can be reliably assumed that a BOR event has occurred.

### 7.7.2 Deep Sleep BOR (DSBOR) (Select Devices Only)

For devices with Deep Sleep capability, an independent Deep Sleep BOR (DSBOR) circuit provides simple BOR/POR protection during Deep Sleep operation. Rather than trigger a Reset in its own right, the DSBOR re-arms the regular POR circuit to ensure a device Reset if VDD drops below the POR threshold during Deep Sleep operation.

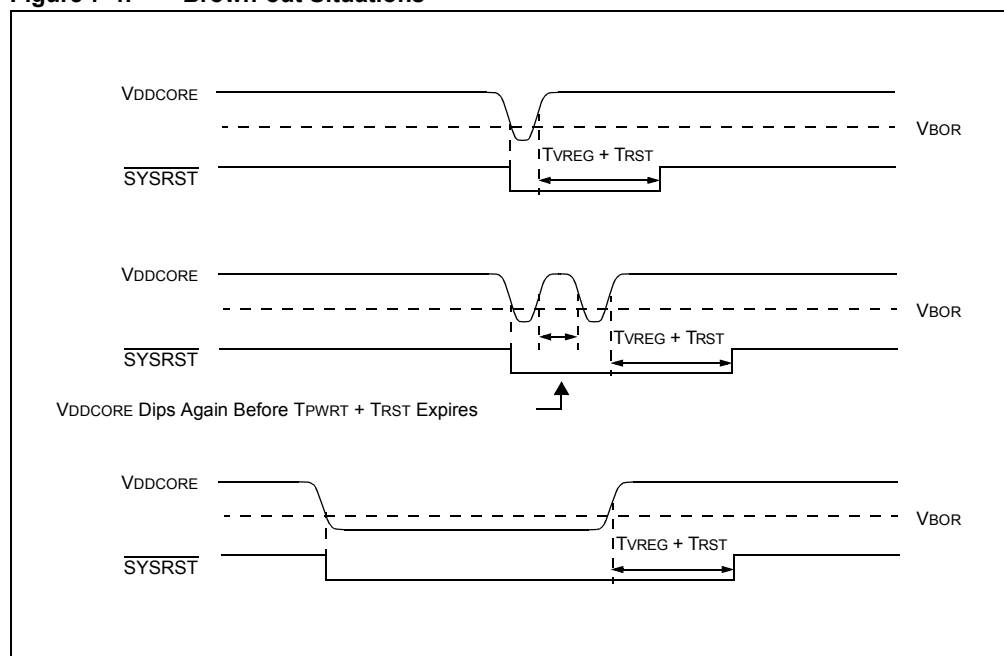
The DSBOR operates on a single trip point of 2.0V nominal. Because it is designed for very low-current consumption, its accuracy may vary.

DSBOR events (BOR and POR) are monitored through the DSCON and DSWAKE registers, respectively. Refer to **Section 39. “Power-Saving Features with Deep Sleep”** for a more detailed discussion.

The DSBOR circuit can be selectively enabled or disabled using the DSBOREN Configuration bit. By default, the circuit is enabled.

**Note:** As with other BOR events in other power-saving modes, both the POR and the BOR are set when the device exits from the Deep Sleep mode.

**Figure 7-4: Brown-out Situations**





## 7.8 CONFIGURATION MISMATCH RESET

To maintain the integrity of the stored configuration values, all device Configuration bits are implemented as a complementary set of register bits. For each bit, as the actual value of the register is written as '1', a complementary value, '0', is stored in its corresponding background register and vice versa. The bit pairs are compared every time, including Sleep mode. During this comparison, if the Configuration bit values are not found opposite to each other, a Configuration Mismatch event is generated which causes a device Reset.

If a device Reset occurs as a result of a Configuration Mismatch, the CM status bit (RCON<9>) is set.

## 7.9 TRAP CONFLICT RESET (TCR)

A Trap Conflict Reset (TCR) occurs when a hard and a soft trap occur at the same time. The TRAPR status bit (RCON<15>) is set on this event. Refer to **Section 8. "Interrupts"** for more information on traps.

## 7.10 ILLEGAL OPCODE RESET (IOPUWR)

A device Reset is generated if the device attempts to execute an illegal opcode value that was fetched from program memory. If a device Reset occurs as a result of an illegal opcode value, the IOPUWR status bit (RCON<14>) is set.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

## 7.11 UNINITIALIZED W REGISTER RESET

The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to. An attempt to use an uninitialized register as an Address Pointer causes a device Reset and sets the IOPUWR status bit (RCON<14>).

## 7.12 REGISTERS AND STATUS BIT VALUES

Status bits from the RCON register are set or cleared differently in different Reset situations, as indicated in Table 7-2.

**Table 7-2: Status Bits, Their Significance and the Initialization Condition for the RCON Register**

Condition	Program Counter	TRAPR	IOPUWR	DPSLP	EXTR	SWR	WDTO <sup>(1)</sup>	SLEEP <sup>(2)</sup>	IDLE <sup>(2)</sup>	CM	BOR	POR
Power-on Reset	000000h	0	0	0	0	0	0	0	0	0	1	1
RESET Instruction	000000h	u	u	u	u	1	u	u	u	u	u	u
Brown-out Reset	000000h	0	0	u	u	0	0	0	0	0	1	u
MCLR during Run Mode	000000h	u	u	u	1	u	u	u	u	u	u	u
MCLR during Idle Mode	000000h	u	u	u	1	u	0 <sup>(1)</sup>	u	1 <sup>(2)</sup>	u	u	u
MCLR during Sleep Mode	000000h	u	u	u	1	u	0 <sup>(1)</sup>	1 <sup>(2)</sup>	u	u	u	u
MCLR during Deep Sleep Mode <sup>(3)</sup>	000000h	0	0	1	1	0	0	0	0	0	1	1
WDT Time-out Reset during Run Mode	000000h	u	u	u	u	u	1	u	u	u	u	u
WDT Time-out Reset during Idle Mode	PC + 2	u	u	u	u	u	1	u	1 <sup>(2)</sup>	u	u	u
WDT Time-out Wake-up during Sleep Mode	PC + 2	u	u	u	u	u	1	1 <sup>(2)</sup>	u	u	u	u
Trap Event Reset	000000h	1	u	u	u	u	u	u	u	u	u	u
Illegal Opcode/Uninitialized WREG	000000h	u	1	u	u	u	u	u	u	u	u	u
Configuration Word Mismatch Reset	000000h	u	u	u	u	u	u	u	u	1	u	u
Interrupt Exit from Idle Mode <sup>(4)</sup>	PC + 2 <sup>(5)</sup>	u	u	u	u	u	u	u	1 <sup>(2)</sup>	u	u	u
Interrupt Exit from Sleep Mode <sup>(4)</sup>	PC + 2 <sup>(5)</sup>	u	u	u	u	u	0 <sup>(2)</sup>	1 <sup>(2)</sup>	u	u	u	u
Idle Mode (execute PWRSAV 1)	PC + 2	u	u	u	u	u	u	u	1	u	u	u
Sleep Mode (execute PWRSAV 0)	PC + 2	u	u	u	u	u	u	1	u	u	u	u
Deep Sleep Mode (set DSEN and execute PWRSAV 0) <sup>(3)</sup>	000000h	0	0	1	0	0	0	0	0	0	1	1

**Legend:** u = unchanged

**Note 1:** The PWRSAV instruction also clears the WDTO bit

**2:** The state of the SLEEP and IDLE bits is defined by the previously executed PWRSAV instruction.

**3:** Select PIC24F devices only.

**4:** An interrupt's priority should not be changed while the interrupt is enabled. If a priority change is needed, clear the associated interrupt enable bit, select the new priority and set the interrupt to enable it.

**5:** The Program Counter (PC) is loaded with PC + 2 if the interrupt priority is less than, or equal to, the CPU interrupt priority level. The PC is loaded with the hardware vector address if the interrupt priority is greater than the CPU interrupt priority level.

### 7.12.1 Using the RCON Status Bits

The user can read the RCON register after any device Reset to determine the cause of the Reset. Table 7-3 provides a summary of the Reset flag bit operation.

**Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

**Table 7-3: Reset Flag Bit Operation**

Flag Bit <sup>(1)</sup>	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
DPSLP (RCON<10>) <sup>(2)</sup>	Deep Sleep Sequence (set DSEN, then execute PWRSAV #SLEEP instruction)	POR
EXTR (RCON<7>)	MCLR Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON<3>) <sup>(1)</sup>	PWRSAV #SLEEP Instruction	POR, CLRWDI instruction
IDLE (RCON<2>) <sup>(1)</sup>	PWRSAV #IDLE Instruction	POR, CLRWDI instruction
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

**Note 1:** All Reset flag bits may be set or cleared by the user software. Setting a Reset flag does not trigger the associated Reset state.

**2:** Select PIC24F devices only.

## 7.13 DEVICE RESET TO CODE EXECUTION START TIME

The delay between the end of a Reset event and when the device actually begins to execute code is determined by two main factors: the type of Reset and the system clock source coming out of the Reset. The code execution start time for various types of device Resets is summarized in Table 7-4. Individual delays are characterized in **Section 7.15 “Electrical Specifications”**.

For POR, the system Reset signal,  $\overline{\text{SYSRST}}$ , is released after the POR delay time ( $\text{TPOR}$ ) and the  $\text{TSTARTUP}$  delay time expires. For BOR,  $\overline{\text{SYSRST}}$  is released after the  $\text{TSTARTUP}$  delay time expires. For all other Resets, the system Reset signal,  $\overline{\text{SYSRST}}$ , is released immediately after the Reset condition is removed. For all Resets, the  $\text{TRST}$  delay starts after the  $\overline{\text{SYSRST}}$  is released. The system clock starts at the expiration of  $\text{TRST}$ ; code execution starts after the clock source is stable.

The time that the device actually begins to execute code also depends on the system oscillator delays, which include the Oscillator Start-up Timer delay ( $\text{TOST}$ ) and the PLL lock time ( $\text{TLOCK}$ ). The PLL lock is additive to (i.e., occurs after) the OST.

**Table 7-4: Reset Delay Times for Various Device Resets**

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR <sup>(6)</sup>	EC	$\text{TPOR} + \text{TRST} + \text{TSTARTUP}$	—	1, 2, 3
	FRC, FRCDIV	$\text{TPOR} + \text{TRST} + \text{TSTARTUP}$	$\text{TFRC}$	1, 2, 3, 4
	LPRC	$\text{TPOR} + \text{TRST} + \text{TSTARTUP}$	$\text{TLPRC}$	1, 2, 3, 4
	ECPLL	$\text{TPOR} + \text{TRST} + \text{TSTARTUP}$	$\text{TLOCK}$	1, 2, 3, 5
	FRCPLL	$\text{TPOR} + \text{TRST} + \text{TSTARTUP}$	$\text{TFRC} + \text{TLOCK}$	1, 2, 3, 4, 5
	XT, HS, SOSC	$\text{TPOR} + \text{TRST} + \text{TSTARTUP}$	$\text{TOST}$	1, 2, 3, 6
	XTPLL, HSPLL	$\text{TPOR} + \text{TRST} + \text{TSTARTUP}$	$\text{TOST} + \text{TLOCK}$	1, 2, 3, 5, 6
BOR	EC	$\text{TRST} + \text{TSTARTUP}$	—	2, 3
	FRC, FRCDIV	$\text{TRST} + \text{TSTARTUP}$	$\text{TFRC}$	2, 3, 4
	LPRC	$\text{TRST} + \text{TSTARTUP}$	$\text{TLPRC}$	2, 3, 4
	ECPLL	$\text{TRST} + \text{TSTARTUP}$	$\text{TLOCK}$	2, 3, 5
	FRCPLL	$\text{TRST} + \text{TSTARTUP}$	$\text{TFRC} + \text{TLOCK}$	2, 3, 4, 5
	XT, HS, SOSC	$\text{TRST} + \text{TSTARTUP}$	$\text{TOST} + \text{TLOCK}$	2, 3, 6
	XTPLL, HSPLL	$\text{TRST} + \text{TSTARTUP}$	$\text{TFRC} + \text{TLOCK}$	2, 3, 4, 5
All Others	Any Clock	$\text{TRST}$	—	2

**Note 1:**  $\text{TPOR}$  = Power-on Reset delay.

**Note 2:**  $\text{TRST}$  = Internal State Reset time.

**Note 3:**  $\text{TSTARTUP}$  =  $\text{TVREG}$  if regulator is enabled or  $\text{TPWRT}$  (64 ms nominal) if regulator is disabled.

**Note 4:**  $\text{TFRC}$  and  $\text{TLPRC}$  = RC oscillator start-up times.

**Note 5:**  $\text{TLOCK}$  = PLL lock time.

**Note 6:**  $\text{TOST}$  = Oscillator Start-up Timer (OST). A 10-bit counter waits 1024 oscillator periods before releasing the oscillator clock to the system.

**Note 7:** If Two-Speed Start-up is enabled, regardless of the primary oscillator selected, the device starts with FRC, and in such cases, FRC start-up time is valid.

**Note:** For nominal operating frequency and timing specifications, see **Section 7.15 “Electrical Specifications”**. For a particular device’s specifications, refer to the “**Electrical Specifications**” section of the appropriate data sheet.

### 7.13.1 POR and Long Oscillator Start-up Times

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after SYSRST is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has NOT expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

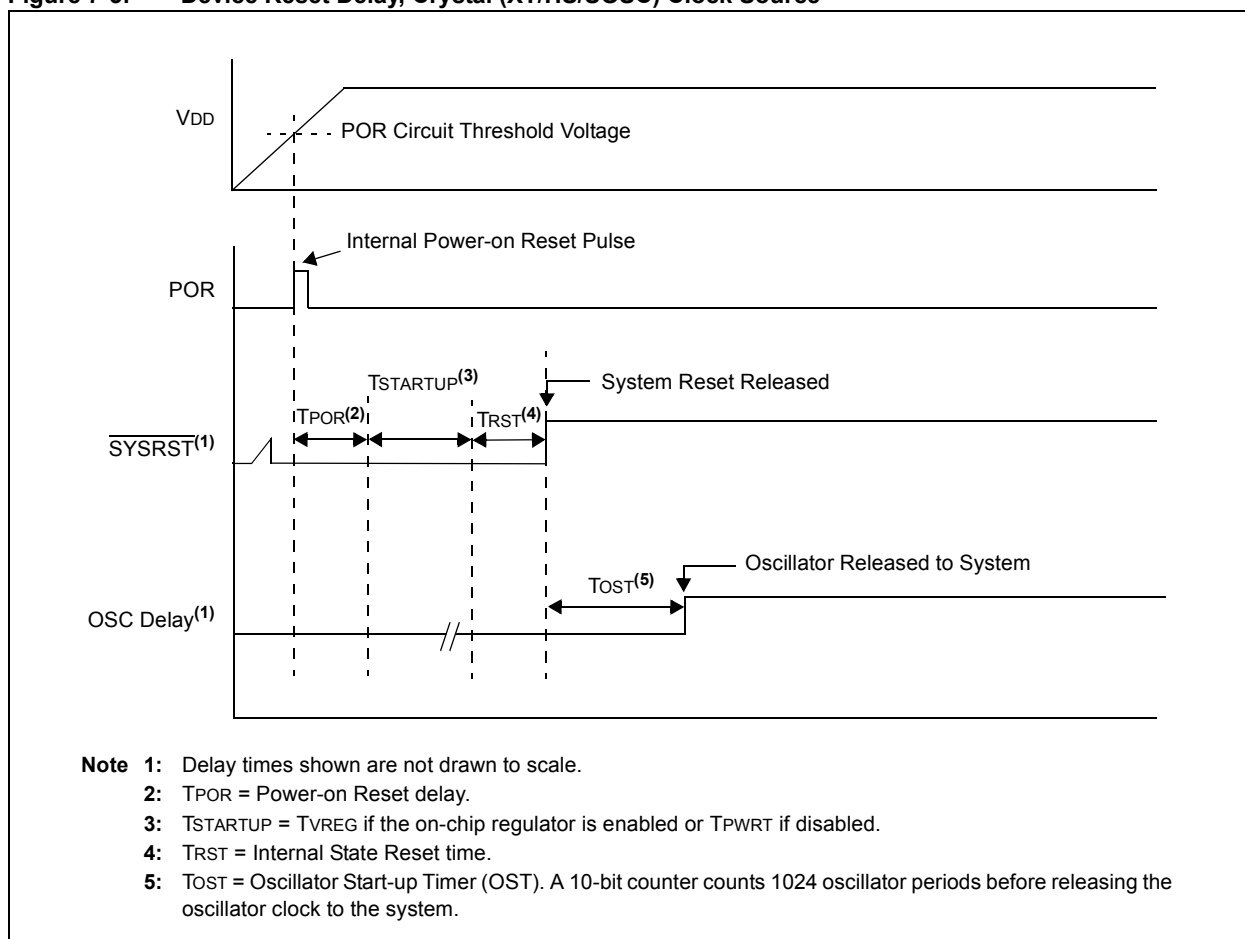
The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

### 7.13.2 Examples of Device Start-up Sequences

Figure 7-5 through Figure 7-8 depict graphical sequences for the delays associated with device Reset for several operating scenarios. The individual delays are characterized in **Section 7.15 “Electrical Specifications”**.

Figure 7-5 displays the delay time line when a crystal oscillator is used as the system clock. The internal POR pulse occurs at the VPOR threshold. TPOR, TSTARTUP and TRST delays occur after the internal POR pulse.

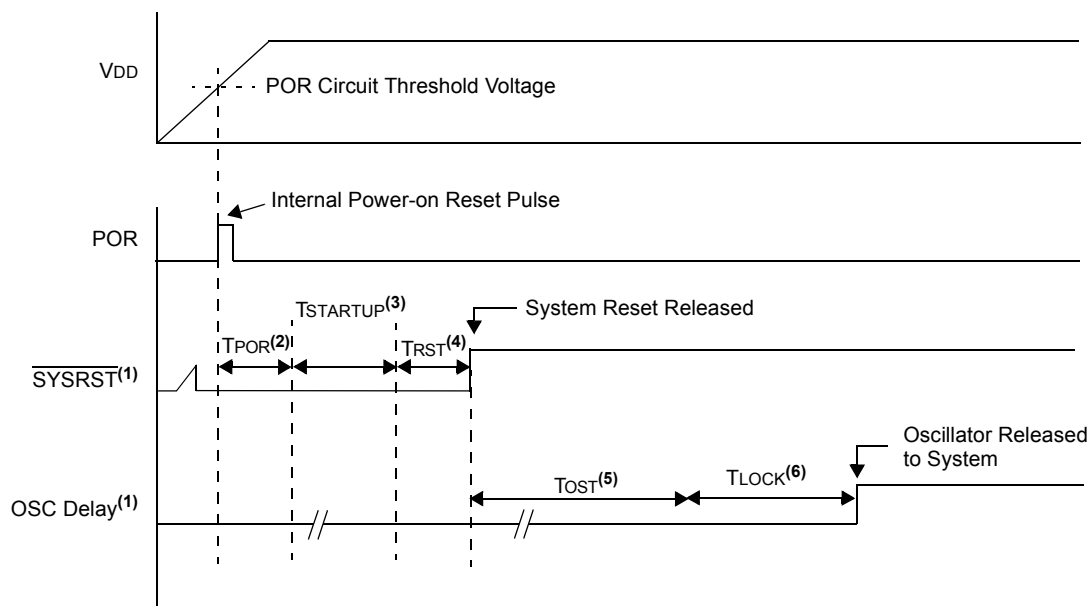
**Figure 7-5: Device Reset Delay, Crystal (XT/HS/SOSC) Clock Source**



The Reset time line displayed in Figure 7-6 is similar to that displayed in Figure 7-5, except that the PLL has been enabled, which increases the oscillator stabilization time.

The FSCM, if enabled, will begin to monitor the system clock after  $T_{FSCM}$  expires. Figure 7-6 displays that the oscillator and PLL delays expire before the FSCM is enabled. However, it is possible that these delays may not expire until after FSCM is enabled. If a valid clock source is not available at this time, the device will automatically switch to the FRC oscillator and a clock failure trap will be generated. The user can switch to the desired crystal oscillator in the TSR.

**Figure 7-6: Device Reset Delay, Crystal (XT/HS/SOSC) + PLL Clock Source**



**Note 1:** Delay times shown are not drawn to scale.

**2:**  $T_{POR}$  = Power-on Reset delay.

**3:**  $T_{STARTUP}$  =  $T_{VREG}$  if the on-chip regulator is enabled or  $T_{PWRT}$ .

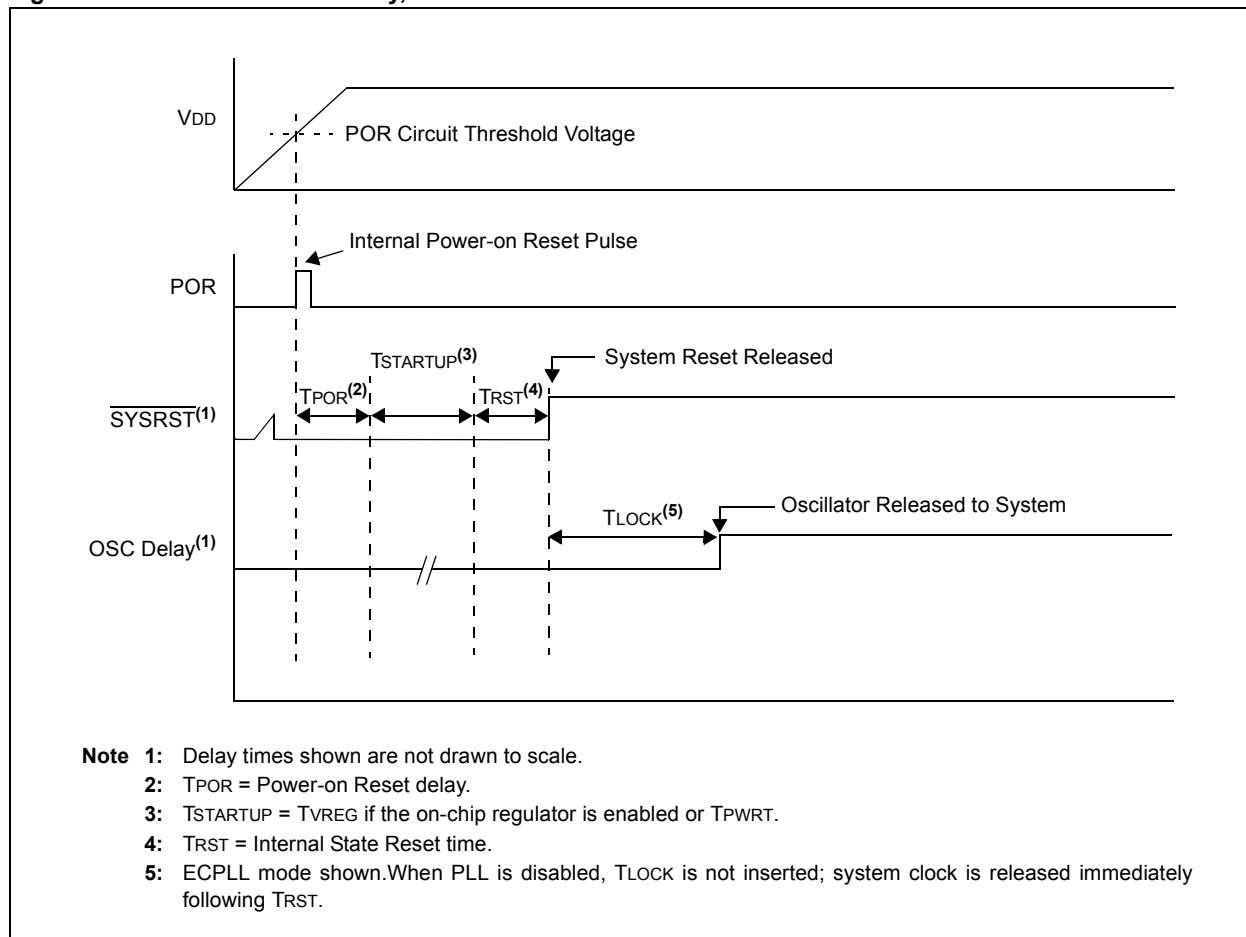
**4:**  $T_{RST}$  = Internal State Reset time.

**5:**  $T_{OST}$  = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

**6:**  $T_{LOCK}$  is not inserted when PLL is disabled.

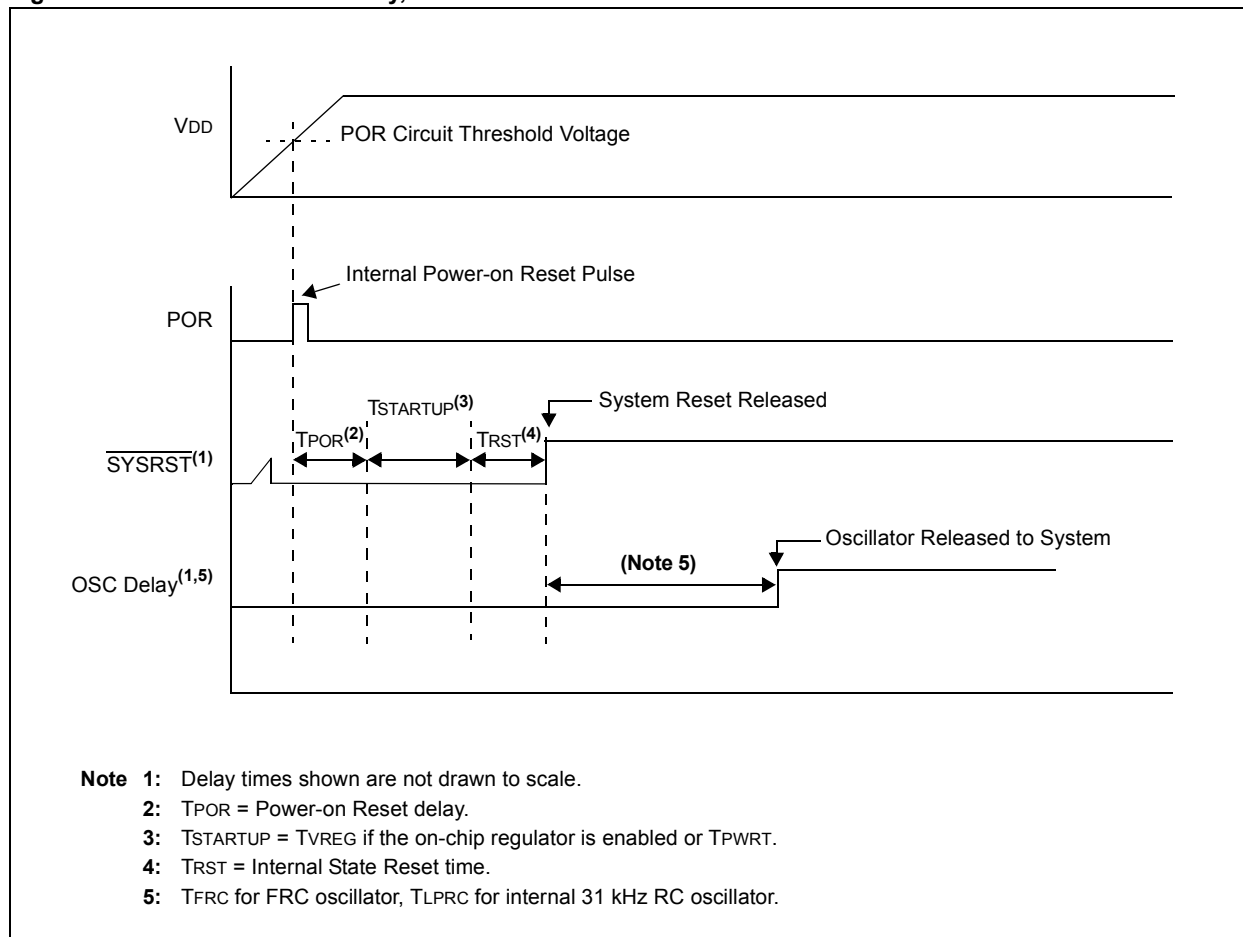
The Reset time line in Figure 7-7 displays an example of when the EC clock source is used as the system clock. This example is similar to the one provided in Figure 7-6, except that the Oscillator Start-up Timer delay,  $T_{OST}$ , does not occur.

**Figure 7-7: Device Reset Delay, EC and ECPLL Clocks**



The Reset time line displayed in Figure 7-8 provides an example of where the FRC or LPRC system clock source is selected. This sequence also applies if an external clock source is used with two-speed start-up enabled.

**Figure 7-8: Device Reset Delay, FRC or LPRC Clocks**



## 7.14 SPECIAL FUNCTION REGISTER (SFR) RESET STATES

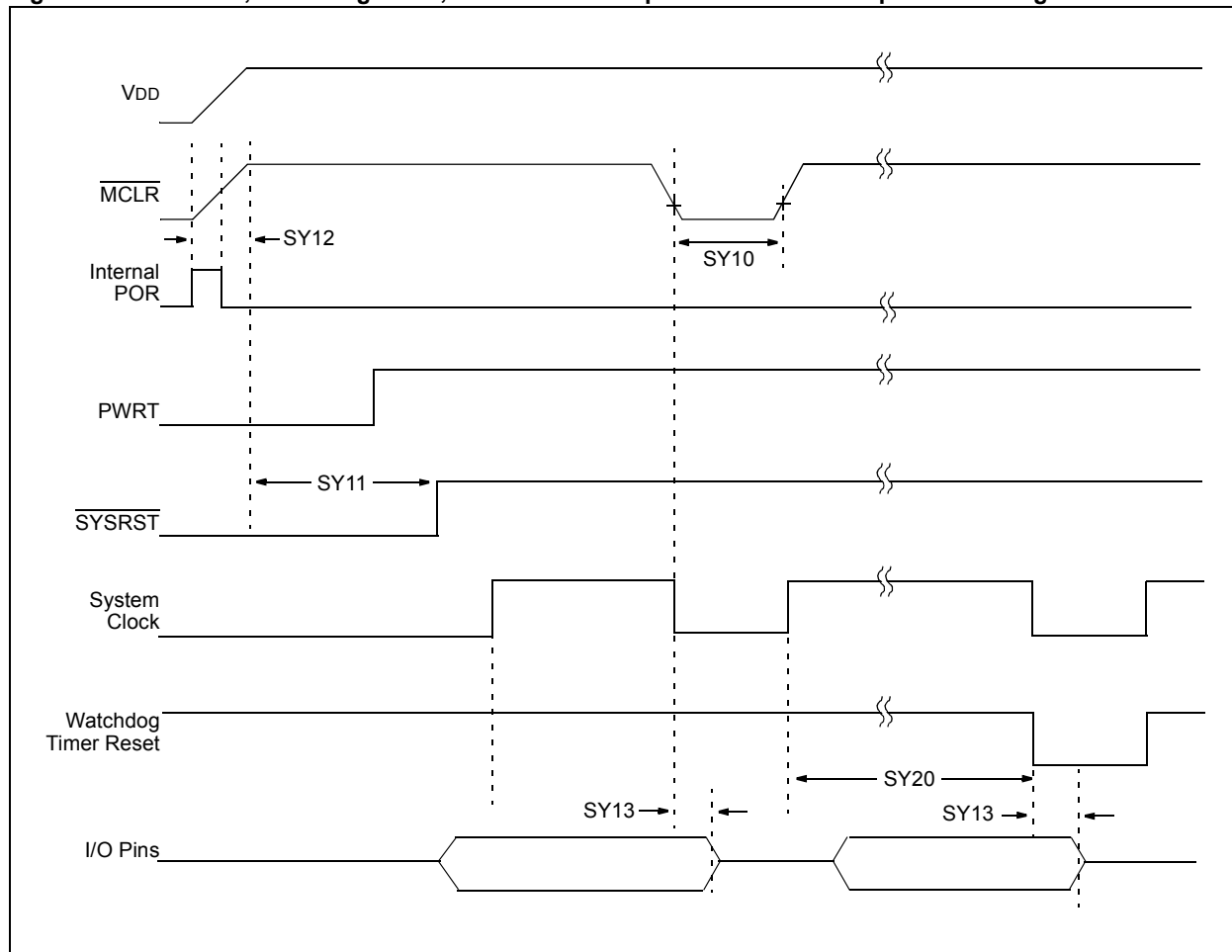
Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in the corresponding section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of two registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the oscillator Configuration bits in the FOSC Device Configuration register (see Table 7-1).



## 7.15 ELECTRICAL SPECIFICATIONS

**Figure 7-9: Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing Characteristics**



**Table 7-5: Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer and Brown-out Reset Timing Requirements**

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Param No.	Symbol	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
SY10	Tmcl	MCLR Pulse Width (low)	2	—	—	$\mu\text{s}$	
SY11	TPWRT	Power-up Timer Period	—	64	—	ms	
SY12	TPOR	Power-on Reset Delay	1	5	10	$\mu\text{s}$	
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	—	100	ns	
SY20	TWDT	Watchdog Timer Time-out Period	0.85 3.4	1.0 4.0	1.15 4.6	ms ms	1:32 prescaler 1:128 prescaler
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	$\mu\text{s}$	$V_{DD} \leq V_{BOR}$ , voltage regulator disabled

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

## 7.16 DESIGN TIPS

**Question 1:** *How do I use the RCON register?*

**Answer:** The initialization code after a Reset should examine RCON and confirm the source of the Reset. In some applications, this information can be used to take appropriate action to correct the problem that caused the Reset to occur. All Reset status bits in the RCON register should be cleared after reading them to ensure the RCON value provides meaningful results after the next device Reset.

**Question 2:** *I initialized a W register with a 16-bit address; why does the device appear to reset when I attempt to use the register as an address?*

**Answer:** Because all data addresses are 16-bit values, the uninitialized W register logic only recognizes that a register has been initialized correctly if it was subjected to a word load. Two-byte moves to a W register, even if successive, will not work, resulting in a device Reset if the W register is used as an Address Pointer in an operation.

## 7.17 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Reset for PIC24F 'K' Devices are:

Title	Application Note #
Power-up Trouble Shooting	AN607
Power-up Considerations	AN522

**Note:** Please visit the Microchip web site ([www.microchip.com](http://www.microchip.com)) for additional application notes and code examples for the PIC24F family of devices.

## 7.18 REVISION HISTORY

### Revision A (September 2006)

This is the initial released revision of this document.

### Revision B (October 2008, not released)

Added Configurable BOR section.

Adds material on Deep Sleep functionality and device Resets.

### Revision C (March 2010)

Removes material on configurable BOR; this material has been incorporated into **Section 40, “Reset with Programmable BOR”** of the *“PIC24F Family Reference Manual”* (DS39728).

Removes all references to the Fail-Safe Clock Monitor and its role in device Resets.

Updates **Section 7.3 “Power-on Reset (POR)”** with a corrected description of the POR start-up sequence.

Replaces Figures 7-2, 7-5, 7-6, 7-7 and 7-8 with new start-up sequence diagrams.

Updates Tables 7-2 and 7-4 with new versions.

Other minor typographic corrections throughout the chapter.