UNIT 1:

1. List any four features of 8086 microprocessor.
    - 16 bit architecture.
    - Segmented memory address.
    - Pipelining.
    - Assembly language support.

2. Explain the function of the following pins.

    a. MN/MX’
        - This pin is used to switch the 8086 processor between minimum (MN) and maximum (MX) modes.
    b. Ready
        - This pin is used to indicate whether a memory or I/O operation has been completed.
    c. ALE
        - The Address Latch Enable (ALE) pin is used to latch the address from the address bus onto the external latch for the peripherals.
    d. DT/R’
        i. This pin is used to indicate whether the data bus is being used for data transfer or instruction fetch. When the DT/R' pin is low, the processor is performing a data transfer operation, and when it is high, the processor is performing an instruction fetch operation..

3. State function of following pins of 8086.

    a. WR’
        - This pin is used to indicate that the processor is writing data to a memory or an I/O device. When the WR' pin goes low, the data on the data bus is written to the device.
    b. M/IO’
        - This pin is used to differentiate between memory and I/O operations. When the M/IO' pin is low, the processor is performing an I/O operation, and when it is high, the processor is performing a memory operation.

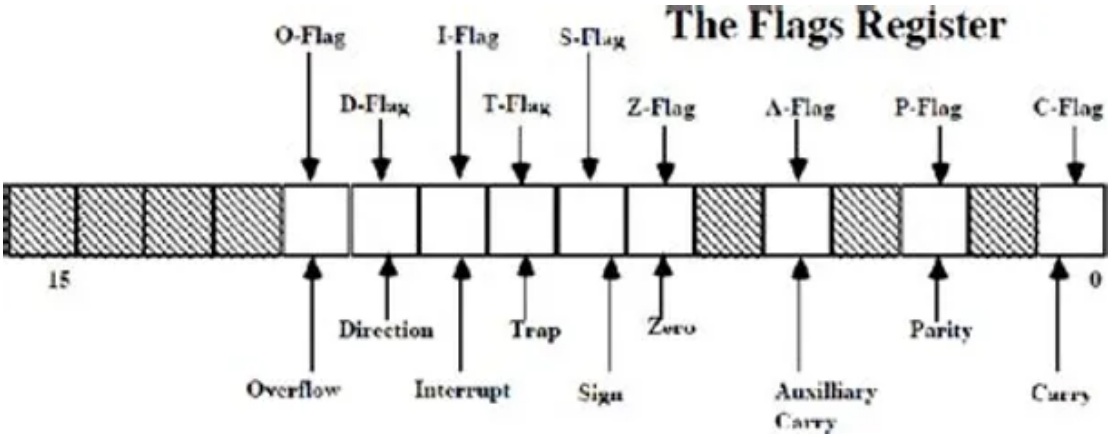
4. Draw the architecture of 8086 microprocessor and state function of BIU.

    - [DIAGRAM]

    - **BIU:**
        - The BIU (Bus Interface Unit) of the 8086 processor is responsible for interfacing with the system bus and for controlling the execution of instructions.

- The registers in the BIU are used for various purposes, such as holding the address of the next instruction to be executed, storing the base address of the current segment, and managing the instruction queue.
- Registers in the Bus Interface Unit (BIU)
    a. Instruction Pointer (IP)
    b. Code Segment (CS)
    c. Data Segment (DS)
    d. Stack Segment (SS)
    e. Extra Segment (ES)

5. Draw the diagram of flag registers.



6. State the use of below flag registers in 8086.
    a. OF
        - The OF flag is set when a signed arithmetic operation results in a value that is too large or too small to be represented in the destination operand. This flag is used to detect signed arithmetic overflow.

    b. TF
        - The TF flag is used for debugging purposes. When the TF flag is set, the processor enters single-step mode, where it executes one instruction at a time and pauses after each instruction.
    c. AF
        - The AF flag is set when an arithmetic operation results in a carry from bit 3 to bit 4 of a byte. This flag is used in binary-coded decimal (BCD) arithmetic operations.
    d. PF
        - The PF flag is set if the result of an operation has an even number of set bits in the least significant byte. This flag is used for parity checking.

7. Explain the concept of the segmentation in 8086.

    - [DIAGRAM]

    - Complete physical memory is divided into the number of login segments.
    - The Side of each segment is 64KB.
    - There are a total of 4 memory segments in 8086.
    - The available memory space is 1MB.
    - The memory can be addressed with the segment registers.

8. With the help of a diagram describe the physical memory address generation of 8086. Calculate the physical address for given
   DS = 7342H AND SI = 3216H.

    - [DIAGRAM]

    - All registers in 8086 are of 16 bit and it generated the physical address of 20bit.
    - Logical address is specified as the segment : offset
    - Physical address is obtained by shifting the segment address 4 bit to the left and adding the offset address.
    - Example: DS = 7342H AND SI = 3216H.
        - DS = 7 3 4 2 0 H
          SI = 3 2 1 6 H
        - ANS = 7 6 6 3 6 H

9. Describe the concept of pipelining.

    - [DIAGRAM]

    - The process of fetching the next instruction when present instruction is been executed is called the pipelining
    - Pipelining had become possible due to the use of instruction queue.
    - The instructions executes more quick with the help of pipelining architecture.

10. Difference between min mode and max mode:

	MIN MODE	MAX MODE
1	It is a **uniprocessor mode.** 8086 is the only processor in the circuit.	It is a **multiprocessor mode.** Along with 8086, there can be other processors like 8087 and 8089 in the circuit.
2	Here **MN/ $\overline{\text{MX}}$** is connected to **Vcc.**	Here **MN/ $\overline{\text{MX}}$** is connected to **Ground.**
3	**ALE** for the latch is **given by 8086** itself.	As there are multiple processors, **ALE** for the latch is **given by 8288 bus controller.**
4	**$\overline{\text{DEN}}$** and **DT/ $\overline{\text{R}}$** for the transreceivers **are given by 8086 itself.**	As there are multiple processors, **DEN** and **DT/ $\overline{\text{R}}$** for the transreceivers is **given by 8288 bus controller.**
5	Direct control signals like **M/ $\overline{\text{IO}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are produced by 8086 itself.**	Instead of control signals, all processors produce status signals **$\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$**
6	Control signals **M/ $\overline{\text{IO}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are decocded by a 3:8 decoder IC 74138.**	Status signals **$\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$ require special decoding** are decoded by **8288 bus controller.**
7	**$\overline{\text{INTA}}$** for interrupt acknowledgement **is produced by 8086.**	**$\overline{\text{INTA}}$** for interrupt acknowledgement **is produced by 8288 Bus Controller.**
8	**Bus request are grant** is handled using **HOLD and HLDA** signals.	**Bus request are grant** is handled using **$\overline{\text{RQ}}$ / $\overline{\text{GT}}$** signals.
9	Since **74138** does not independently generate any signals, it **does not need a CLK.**	Since **8288** independently generates control signals, it **needs a CLK from 8284** clock generator.
10	The circuit is **simpler but does not support multiprocessing.**	The circuit is **more complex but supports multiprocessing.**

UNIT 2:

1. Describe the function of following directives.

    a. DD
        - DD is a data definition directive.
        - It is use to define the double word data i.e 16 + 16 = 32 bit data
        - EX - a DD 12345H

    b. DB
        - DB is a data definition directive.
        - It is used to define the word i.e 16 bit data.
        - EX - a DB 1234H

    c. DUP
        - DUP is a data definition directive.
        - It is used to duplicate a specified number of data items or blocks of memory.
        - EX - array DUP (10)
        -

    d. EQU
        - EQU is a data definition directive.
        - It is used to define a symbolic constant with a specified value
        - EX - SIZE EQU 10

2. State the function of the following.

    a. Editor
        - Used to create and modify the Assembly language source code files.

    b. Assembler
        - Used to convert the assembly language code to the machine code.

    c. Linker
        - Used to combine the objects files into executable files that can run on the target system.

    d. Debugger
        - Used to find and fix the errors (bugs) in the program by executing the program line by line.

3. State the function of

    a. ASSUME
        - Assume directive is used to group the code segments
        - Ex: assume cs: code, ds: data
    b. SEGMENT
        - Segment directive is used to define the memory segments
        - Ex:

```
Code segment
        ; statements
Code Ends
```

UNIT 3:

1. List any two addressing modes of 8086 with examples.
    a. Register Addressing Mode:
        - In this mode, the operand is contained in one of the CPU's registers. The register can be specified explicitly in the instruction
        - Ex: ADD AX, BX

    b. Direct Addressing Mode:
        - In this mode, the operand is contained in a memory location that is directly specified in the instruction.
        - Ex: ADD AL, [1000H]

2. Identify the addressing modes of following instructions.
    a. MOV AX, 2034H
        - Immediate addressing mode
    b. MOV AL, [60000H]
        - Direct addressing
    c. ADD AL, CL
        - Register addressing mode
    d. MOV AX, 50H[BX] [SI]
        - Based Indexed addressing mode,