

**Theory:-**

A **Field Programmable Gate Array (FPGA)** is a **reconfigurable digital logic device** that can be programmed by the user to implement custom hardware functions after manufacturing. It bridges the gap between **custom ASICs** and **general-purpose processors**, offering both **hardware-level speed** and **design flexibility**.

An FPGA consists of three main components:

1. **Configurable Logic Blocks (CLBs):** Implement logic functions using Look-Up Tables (LUTs), flip-flops, and multiplexers.
2. **Programmable Interconnects:** Provide routing paths between logic blocks, allowing complex circuit connectivity.
3. **Input/Output Blocks (IOBs):** Interface the FPGA with external devices or systems.

Designs for FPGAs are created using **Hardware Description Languages (HDL)** such as **Verilog** or **VHDL**. The design flow involves **simulation**, **synthesis**, **implementation (placement and routing)**, and **bitstream generation**, which is then downloaded onto the FPGA chip.

FPGAs are widely used in **digital signal processing (DSP)**, **communication systems**, **embedded systems**, and **prototyping of ASIC designs**. Their key advantages include **high performance**, **parallel processing capability**, **reconfigurability**, and **short development cycles**.

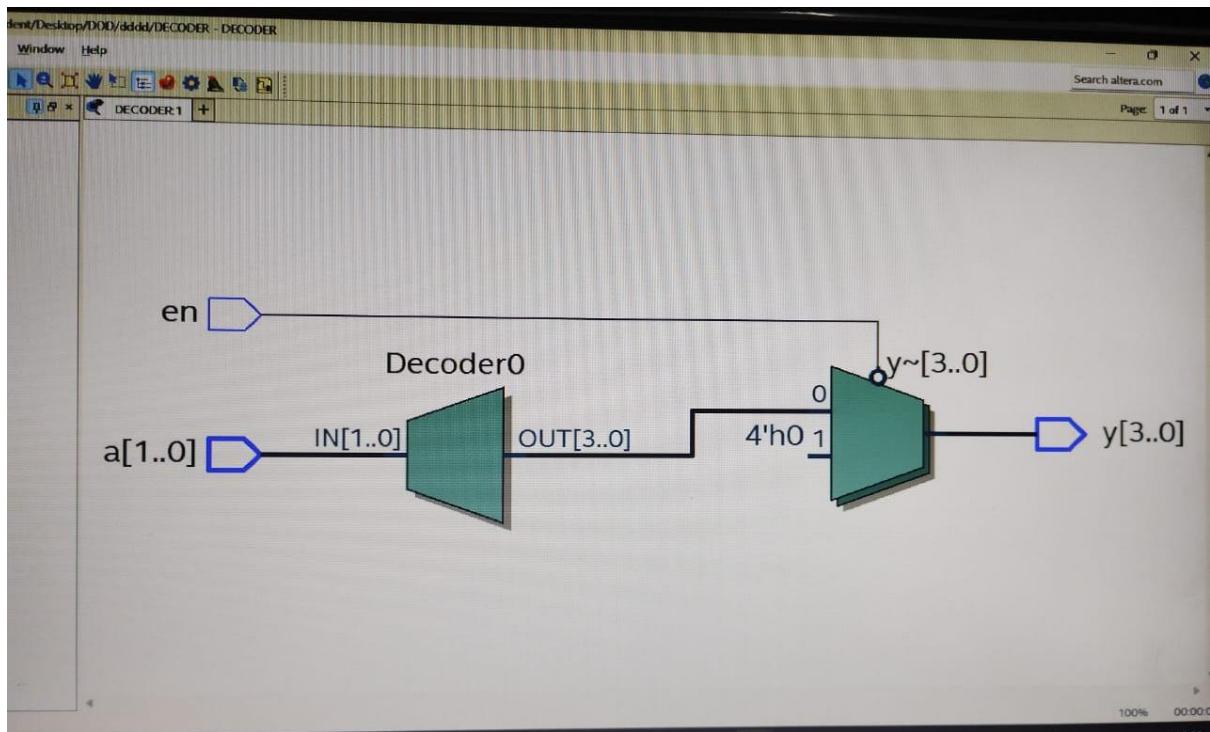
## Code (2:4 decoder)

The screenshot shows a Verilog code editor window titled "DECODER.v". The code defines a module named "DECODER" with three ports: output [3:0]y, input [1:0]a, and input en. It includes a default case for when en is 0, setting y to 1'b0. For other values of en (1'b1), it uses a case statement to map 2-bit inputs a to 4-bit outputs y. The case statement covers all possible combinations of a (00, 01, 10, 11) and sets y to 4'b0001, 4'b0010, 4'b0100, and 4'b1000 respectively. A default case handles all other values of a by setting y to 1'bX. The code editor interface includes tabs for "Compilation Report - DECODER" and "Assignment Editor". At the bottom, there are buttons for "End..." and "Find Next". Below the code editor, a status bar displays the message "Compilation was successful. 0 errors, 79 warnings".

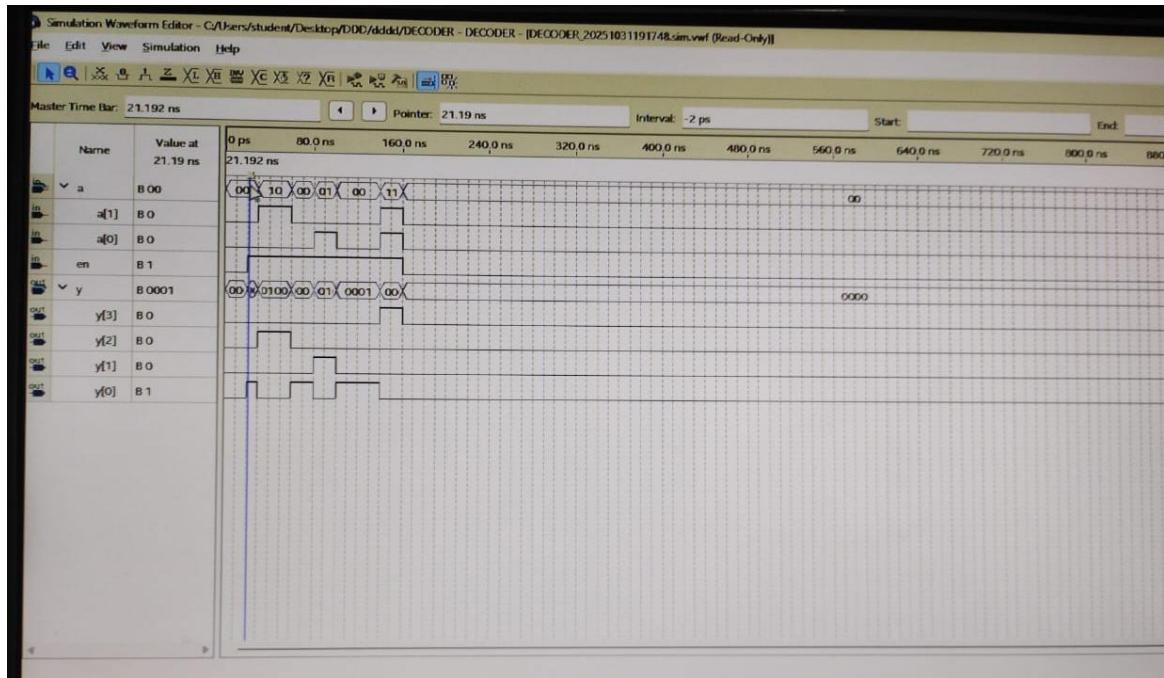
```
1 module DECODER(y,a,en);
2   output [3:0]y;
3   input [1:0]a;
4   input en;
5   reg [3:0]y;
6   always @ (a,en)
7     if (en==0)
8       y=1'b0;
9     else
10      case(a)
11        2'b00:y=4'b0001;
12        2'b01:y=4'b0010;
13        2'b10:y=4'b0100;
14        2'b11:y=4'b1000;
15      endcase
16    endmodule
17
18
19
```

Compilation was successful. 0 errors, 79 warnings

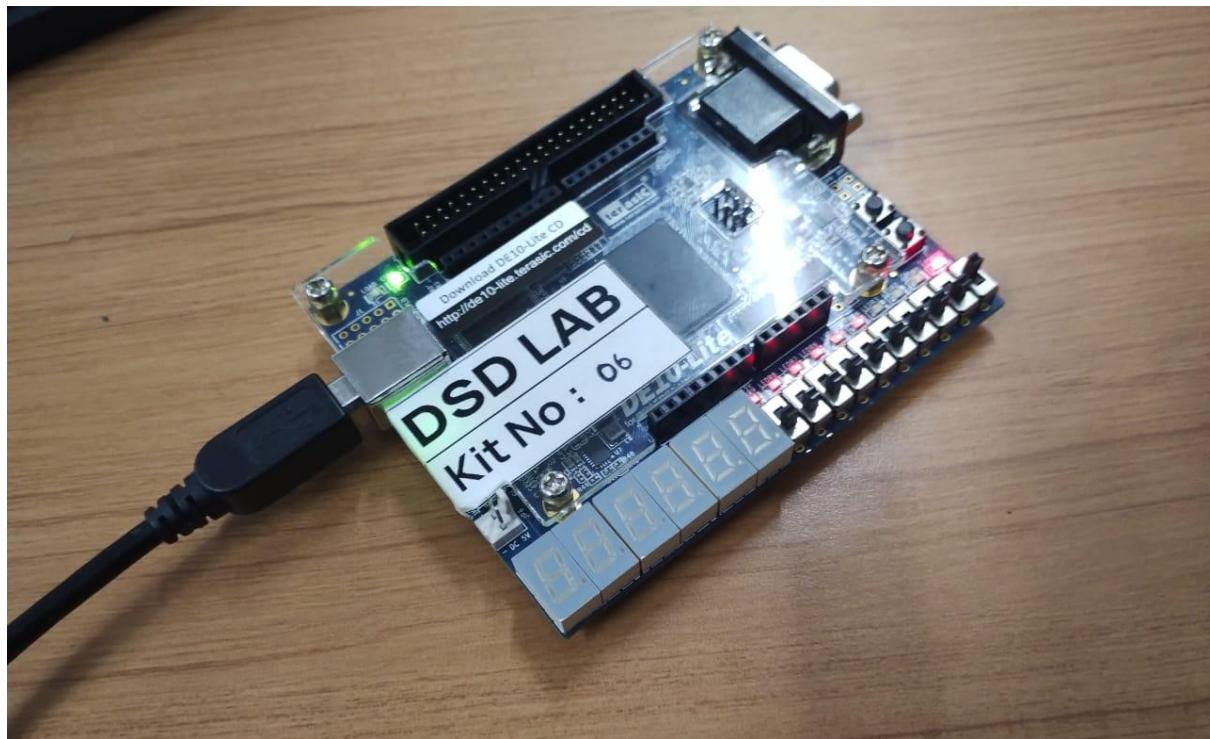
RTL View:-

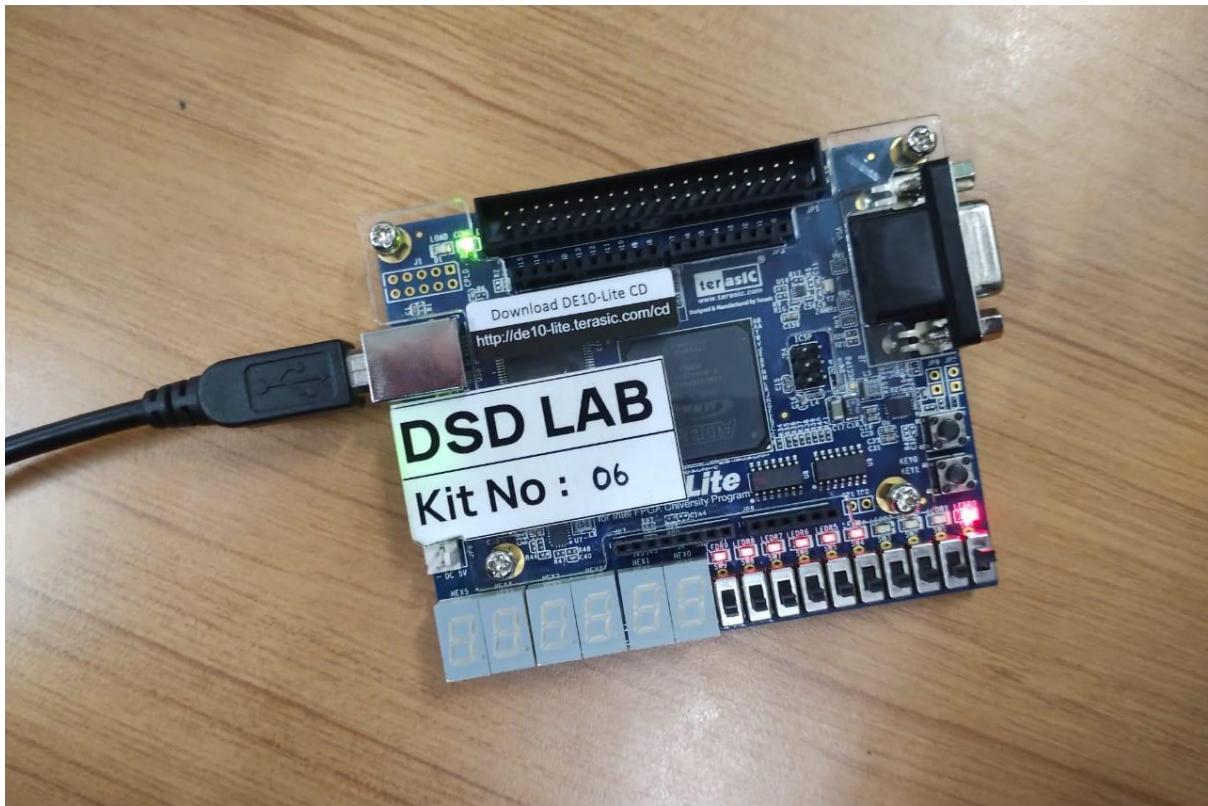


Wave Form:-



FPGA and pictures of its working :-





Lab Signatures: -

classmate

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31/10/25

Req → FPCNF

→ 2:4 decoder code

module Decoder(y, q, en);

output [3:0] y;

input [1:0] q;

input en;

begin

Always @ (q, en)

if (en == 0)

y = 11b0;

else

case (q)

2'b00: y = 4'b0001;

2'b01: y = 4'b0010;

2'b10: y = 4'b0100;

2'b11: y = 4'b1000;

default: y = 4'b1111;

endcase

endmodule

MJ