DSD TASK 6- FPGA 31st Oct 2025

Theory:-

A **Field Programmable Gate Array (FPGA)** is a **reconfigurable digital logic device** that can be programmed by the user to implement custom hardware functions after manufacturing. It bridges the gap between **custom ASICs** and **general-purpose processors**, offering both **hardware-level speed** and **design flexibility**.

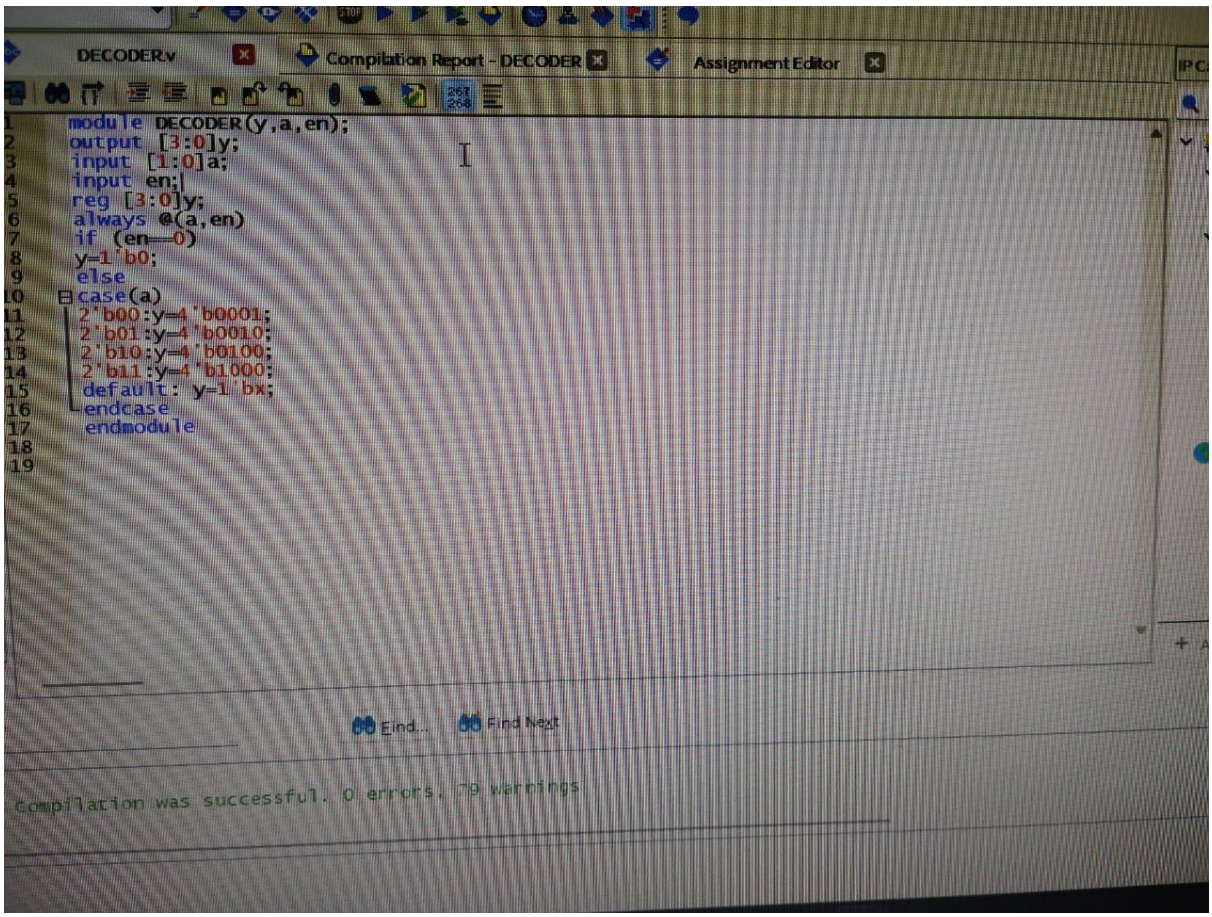
An FPGA consists of three main components:

1. **Configurable Logic Blocks (CLBs):** Implement logic functions using Look-Up Tables (LUTs), flip-flops, and multiplexers.
2. **Programmable Interconnects:** Provide routing paths between logic blocks, allowing complex circuit connectivity.
3. **Input/Output Blocks (IOBs):** Interface the FPGA with external devices or systems.

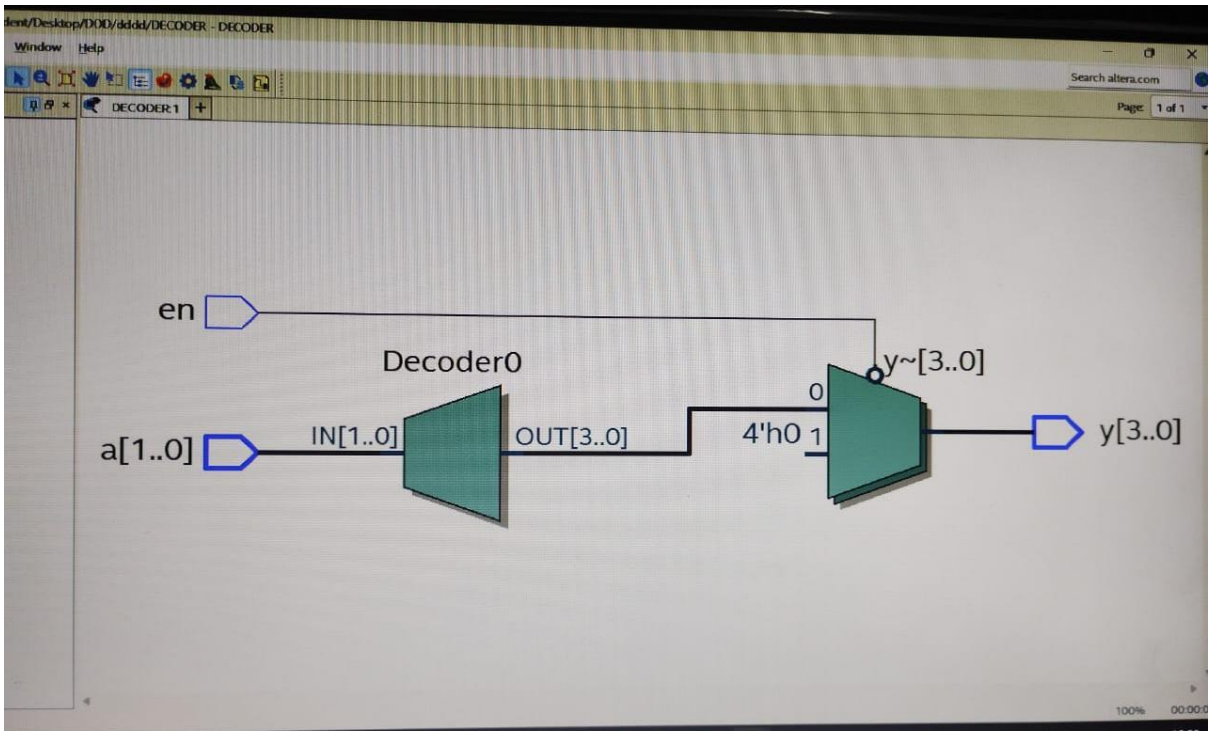
Designs for FPGAs are created using **Hardware Description Languages (HDL)** such as **Verilog** or **VHDL**. The design flow involves **simulation**, **synthesis**, **implementation (placement and routing)**, and **bitstream generation**, which is then downloaded onto the FPGA chip.

FPGAs are widely used in **digital signal processing (DSP)**, **communication systems**, **embedded systems**, and **prototyping of ASIC designs**. Their key advantages include **high performance**, **parallel processing capability**, **reconfigurability**, and **short development cycles**.

Code (2:4 decoder)



RTL View:-


Window
Help
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DECODER:1
Page: 1 of 1
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0
a[1..0]
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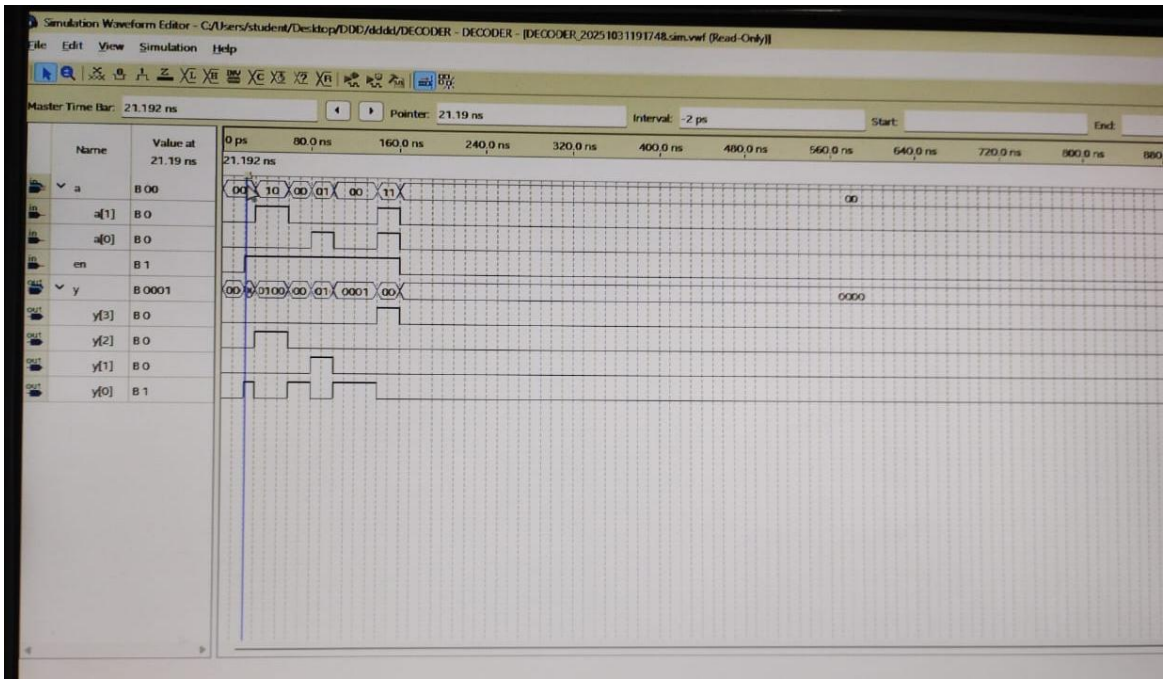
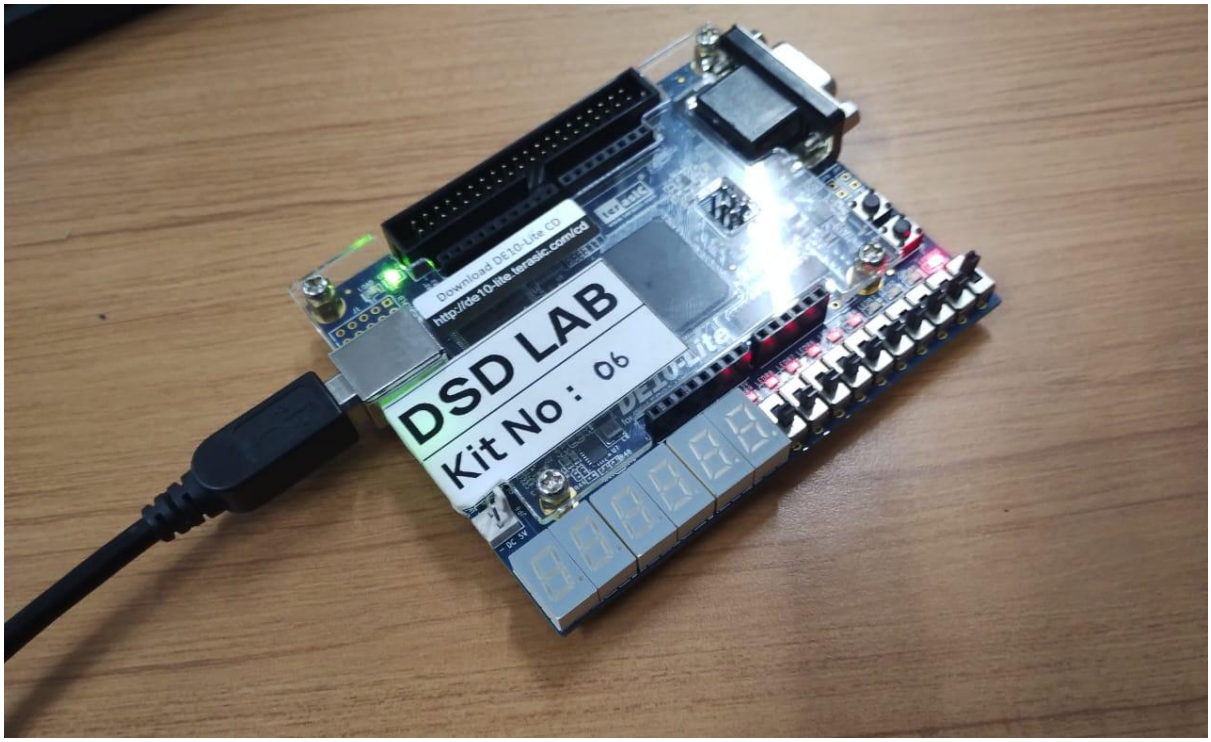
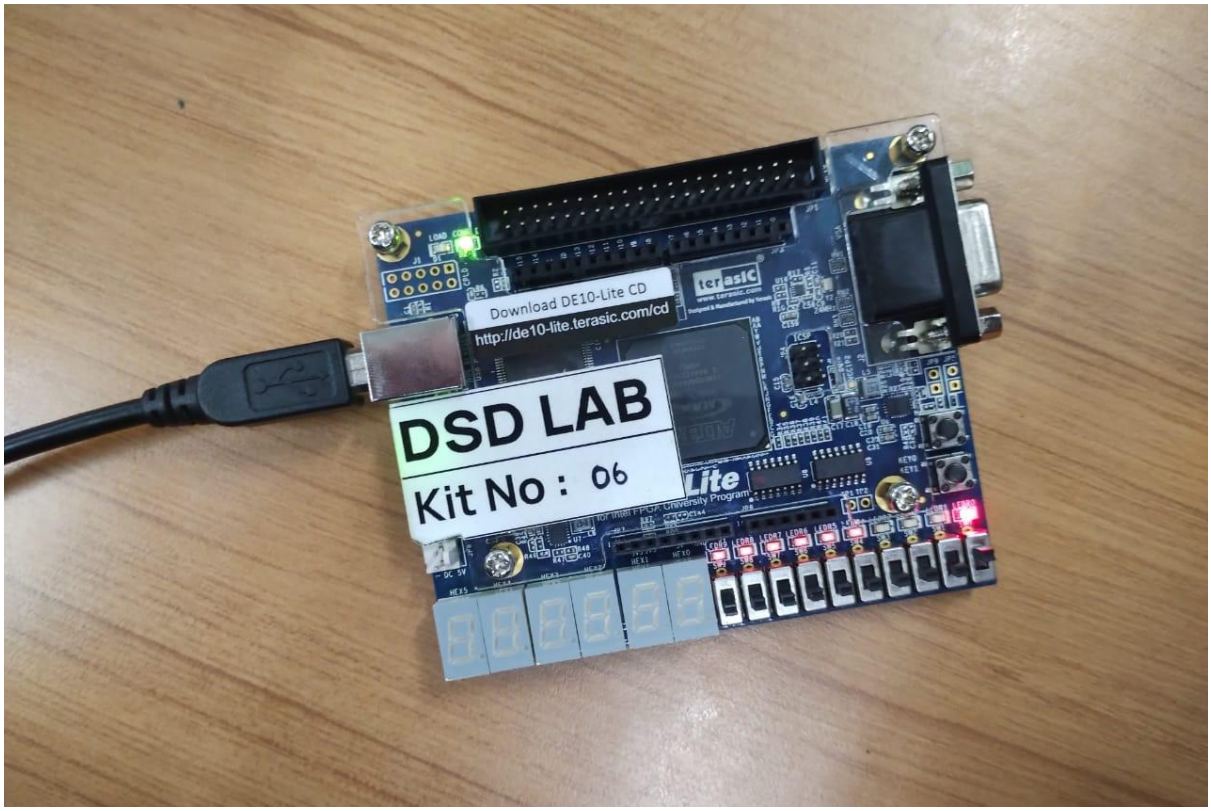
Wave Form:-



FPGA and pictures of its working :-




Download DE10-Lite CD
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DSD LAB
Kit No : 06

Lab Signatures: -

Exp → FPGA

31/10/25

→ 2:4 decoder code

```
module Dec2x4(y,a,en);
output [3:0]y;
input [1:0] a;
input en;
reg [3:0]y;
always @(a, en)
if (en==0)
y= 4'b0;
else
case (a)
2'b00 : y= 4'b0001;
2'b01 : y= 4'b0010;
2'b10 : y= 4'b0100;
2'b11 : y= 4'b1000;
default : y= 4'bx;
endcase
endmodule
```